TẬP ĐOÀN CÔNG NGHIÊP
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DESIGN SPECIFICATION

MODEL

DUMMY SLAVE

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CATALOG

FIGURE

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1. OVERVIEW

The documents illustrates design specification of dummy slave model. It is a part of SoC platform developing by SystemC. The dummy slave model supports for ports monitoring and testing process.
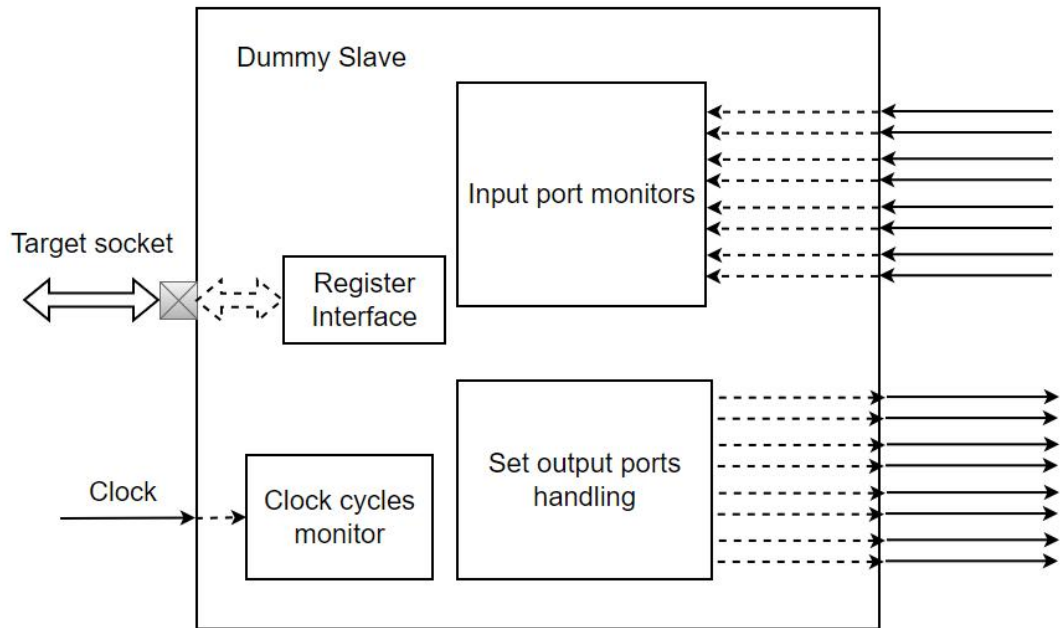
2. DUMMY SLAVE ARCHITECTURE

Figure 1: Dummy slave architecture

Dummy slave mainly use for monitor ports, which are bond directly by API function supporting from dummy salve model. In particular, It allows user to control any output ports with high or low level, supporting for testing process. On the other hand, the dummy slave offers a register call DUMMYRESULT, it is used to exit program. When user write 0x01 or 0x00 to this register, the dummy salve will print out a "TM is Pass" or "TM is FAIL" statement.
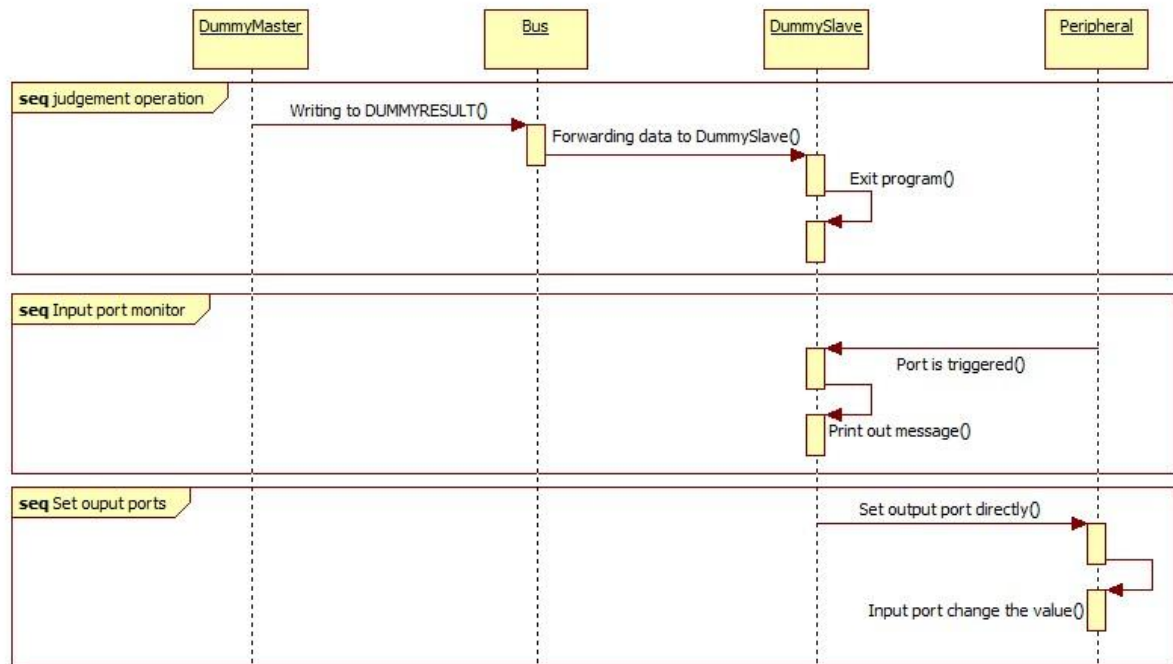
3. SEQUENCE DIAGRAM

Figure 2: Sequence diagram for operation

The dummy slave supports for input port monitor and output port handling directly for user. In case of judgement operation, user will write 0x01 or 0x00 value into DUMMYRESULT register, the program will be terminated, printing result out to monitor.

4. FLOW DIAGRAM

In this section, the document shows flow diagram of functions that mainly contributes to the dummy slave operation.
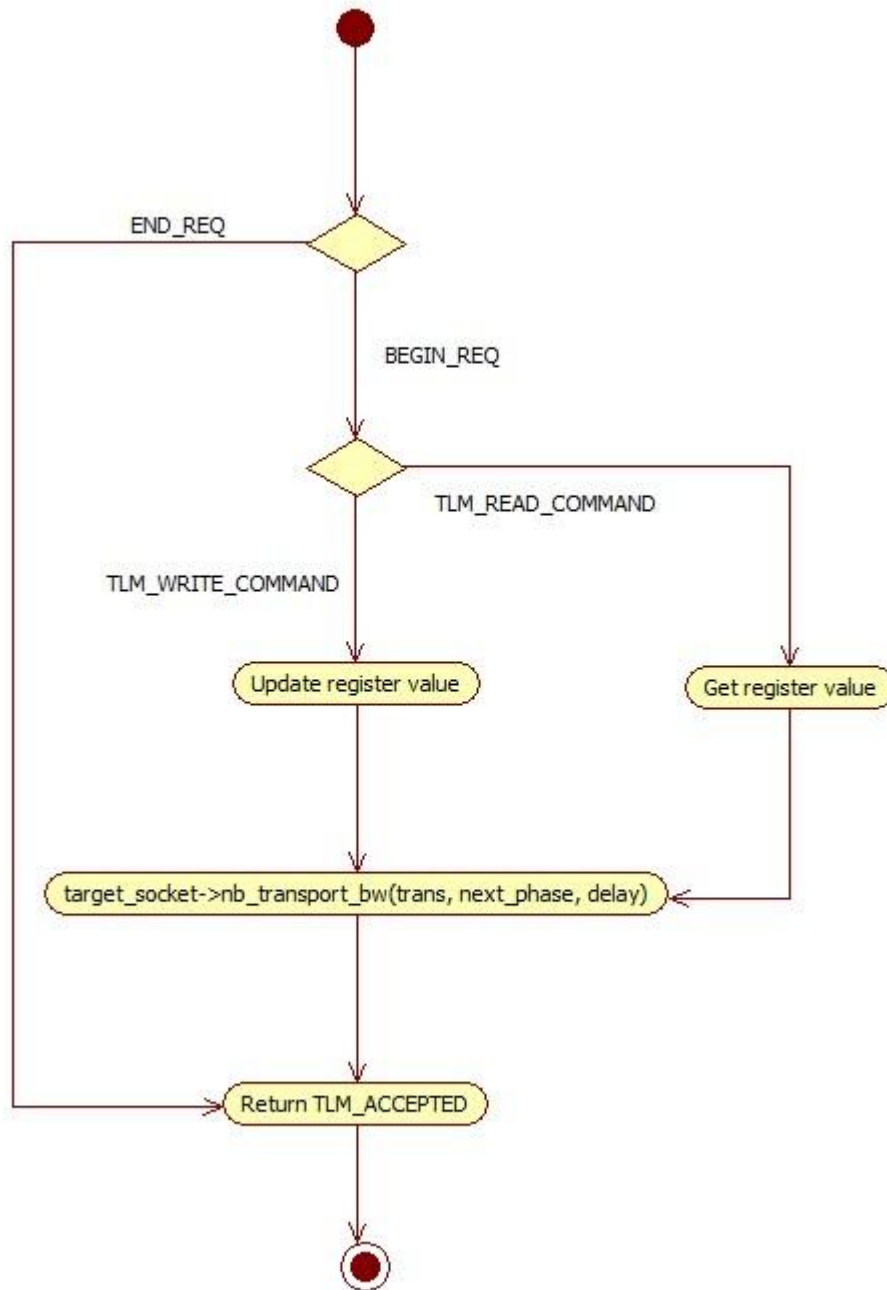
4.1. Nb_transport_fw

Figure 3: nb_transport_fw flow diagram

The nb_transport_fw function is called by target socket as callback function. It copies data from TLM write transaction into internal register or from internal register to TLM read transaction.
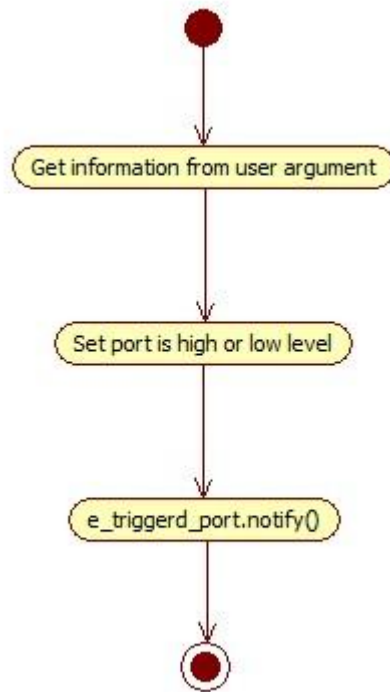
4.2. Trigger_output_ports

Figure 4: Trigger_output_ports flow diagram

This function is used to control output port of peripherals, it will triggered the specific output port to low or high level in a clock cycle.
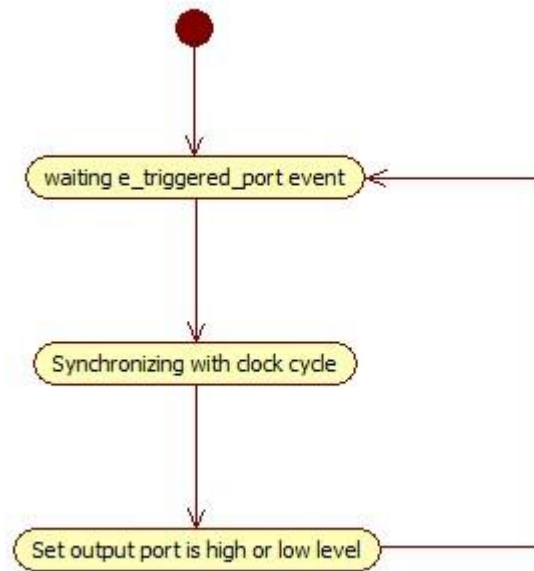
4.3. Thr_trigger_port_porcess

Figure 5: thr_trigger_port_process flow diagram

This process is used to synchronize with the clock cycle. In the next clock cycle, the specific port will be returned to old value.