PERFORMANCE ENHANCED ROUTER DESIGN FOR NETWORK ON CHIP

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***Abstract*— Network on chip is a new paradigm for on chip design that is able to sustain the communication provisions for the SoC with the desired performance. NOC applies networking methodology concepts to system on chip data transfer and it gives noticeable elevation over conventional bus based communication. NOC router is the backbone of on chip communication which directs the flow of data. In NOC router the arbiter is used during number of inputs request for the similar out port. Arbiter generates the grant based on the priority and previous granted input. For NOC router we have design the efficient round robin arbiter and analyse the power and area. In this paper on chip router is designed with a buffering technique of FWFT based asynchronous FIFO which improves timing and reduce power consumption. The proposed design of router is simulated and synthesized in Xilinx ISE 13.2 and the source code is written in Verilog. Cadence soc encounter of technology ami035 is used to generate layout of router and RTL compiler is used to compute area, power and timing.**

Keyword- NOC, router, masked round robin arbiter, FWFT

I. Introduction

As per Moore's law the density of chip doubles every 18 months, so the parameters of a single chip get affected due to increase of processing elements on a chip. NOC is a packet switched on-chip data transfer network that solves challenges faced by SOC of bus based communication. The basic ingredients of NOC are topology which defines the communication architecture, routing technique which decides how the data is routed from sender to receiver, routers and switching technique which determines when the data flow through the routers.

NOC used only point to point wires for all network sizes and it increases the utilization of wires. Large value of parallelism can attain, due to all associate links in the NOC can able to function simultaneously on different data packets. NOC offers improved performance such as throughput and scalability in comparison with previous communication architectures.

The focus of paper is design of Network on chip five port router. The effective on chip communication is achieved by router's routing functionality and efficient arbitration [1]. The main goal of this paper is the design of power and area efficient on chip router.

II.DESIGN OF FIVE PORT ROUTER

The on chip router has three main blocks; they are first in first out (FIFO), arbiter and crossbar. FIG 1 reveals the block diagram of proposed five port router. FIFO acts as a buffer which stores the packet from the neighbour router and from the processing element. Arbiter generates grant signal according to the priority of input ports and it is used to trap the destination address of the requested input [2]. According to the grant from arbiter the crossbar switch transfer the data from source to the destination port. In this router design store and forward switching technique is used, it is simple thereby reducing both area and power [1]. Network on chip routes the messages in segmented packets of three parts. Three parts in packets are data flits, source address and destination address. Proposed design use packet size of 16 bits which has first part is source address, second part is destination address and third one is data. Here the source and destination address are three bits.

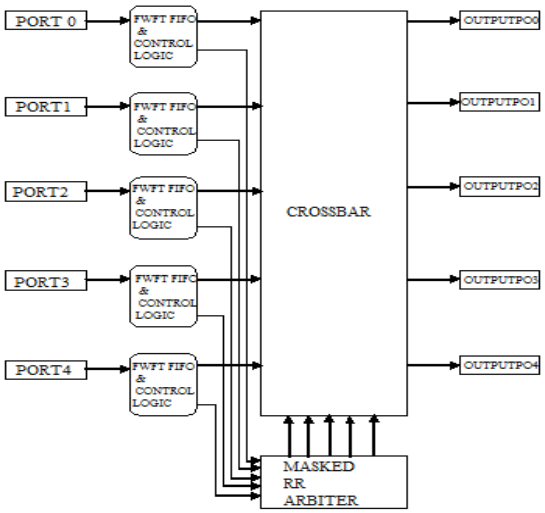

FIG 1: Router block diagram

A. First in First out:

For a NOC router buffering is needed to store the data temporarily which are going to transmit. Each port has one FIFO which has control logic to decides the read and write operation. In the proposed design, FIFO has depth of 5 and width of 16 with a control signal of full and empty.

Control logic check FIFO empty when read port is high. If FIFO empty is high then operation is terminated otherwise read counter is incremented by one. Control logic check FIFO full when write port is high. If FIFO full is high, it indicates there is no memory to store the packet and operation is stop otherwise packet is stored in the memory by increment the write counter. Comparison of read counter and write counter are performed, if both are equal then FIFO full =0 and FIFO empty=1.

In the proposed router design an asynchronous FIFO is designed based on first word fall through (FWFT) technique. In an asynchronous FIFO two separate clock signals are used for read and write operation where the two clock domains are asynchronous to each other. In the FIFO design read and write pointer are used to indicate the next word to be read and write respectively. These pointers are designed with gray code counter, which reduce the power consumption when compare to the binary counter. In gray code counter only one bit value is change when incremented but not in binary counter. More power consumption takes place in flip flops when there is a value change, so gray code counter saves power compare to binary counter. This asynchronous FIFO design uses FWFT technique which improves the timing.

B.ARBITER:

Arbiter resolves the contention problem occurred during which additional number of input ports request for the similar output port. Arbiter denotes which ports are unused and which ports are in function, it keeps the updated status of every port. Arbiter holds the out port which is communicated to crossbar, until the previous packet gets transmitted. After that other incoming packets can utilize the output port through arbiter.

Arbiter generates the grant signal, select lines and read signal. According to the grant signal the arbiter trap the destination address and generate the three bit select lines. The select lines are given to the crossbar and it find out the output port. In proposed design mask based round robin arbiter is used during the arbitration.

III. ROUND ROBIN SCHEDULER

The arbiter used in the design is RR arbiter which used the round robin algorithm. The concept behind the round robin algorithm is the request which was presently allotted which gets lowest priority value on the next cycle of operation. Ports which are sending request for the same output port is processed with the round robin arbiter.

A. GENERIC ROUND ROBIN ARBITER

In generic round robin arbiter there are two blocks as shown in FIG 2, the input selector and round robin pointer. Input selector generates a grant for the input port based on the request and round robin pointer. Round robin pointer is used to achieve fairness among inputs by update pointer value to the input port next to the winner input in a circular manner. The time intense process of generic RR Arbiter is due to input selector. Complications with the input selector are it needs to consider all possible priority settings during which if there

are no request from inputs greater than pointer value but there are request from inputs lesser than pointer value. This lead to acquire two conditions for grant generation: grant decision for request below the pointer and grant decision for request above the pointer. These issues are lead to RRA size gets larger especially at increase of inputs.

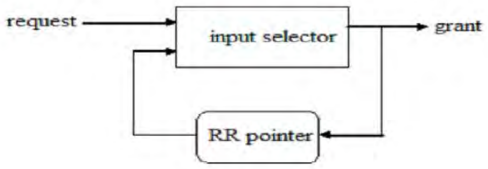

FIG 2: Generic RR arbiter

B.MASKED ROUND ROBIN ARBITER

In the proposed design mask based round robin arbiter is used which gives good results for both area and timing [5]. In this proposed arbiter design two priority arbiters are used and mask is generated with the help of round robin pointer. Here the round robin pointer is update according to the result from two priority arbiter. Mask-based round robin arbitration enforces the priority scheduling while maintaining fairness to all Participants. Among the two priority arbiter, the entire request is given to the one of the arbiter and masked request is given to the other arbiter. The mask based round robin arbiter is shown in FIG 3.

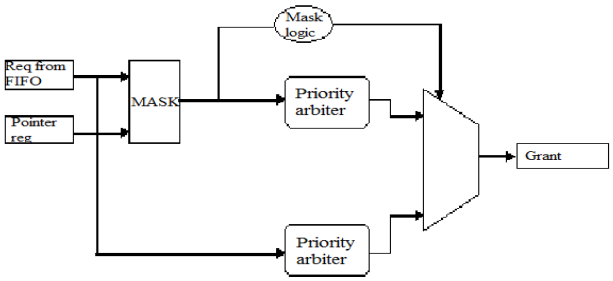

FIG 3: Masked round robin arbiter

IV. SIMULATION RESULT

Simulation is used for design's function verification. It is a process of forcing vectors to the design and verifies its response. The tool used to simulate the design is ISIM simulator of Xilinx ISE 13.2.

In FIG 4 router's functional verification is performed with no contention i.e. no input port ask for the same output port. This simulation is performed in ISIM simulator.

In FIG 5 the input ports of port0, port1 and port3 request for the output port4 and also port2 and port4 request for the output port 3. Here round robin scheduling is performed to avoid the contention problem in resource allocation.

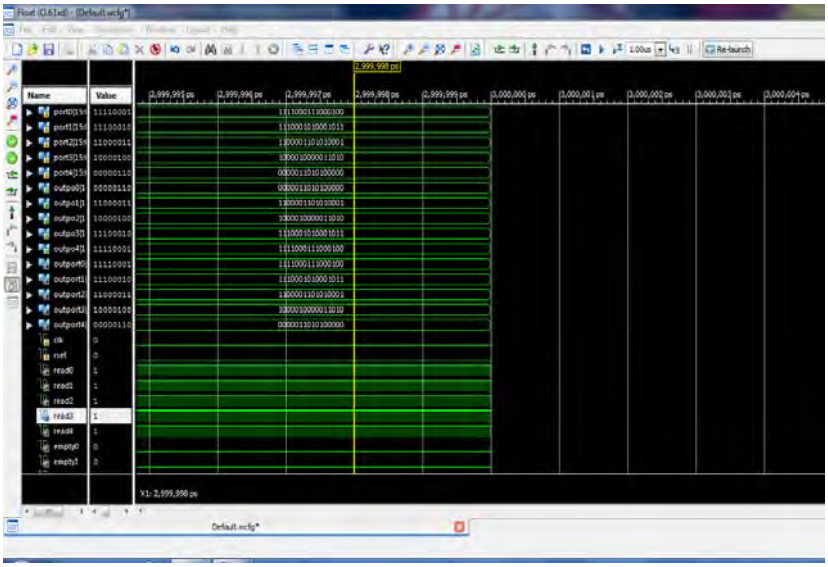

FIG 4: Simulated result of five port router when there is no contention.

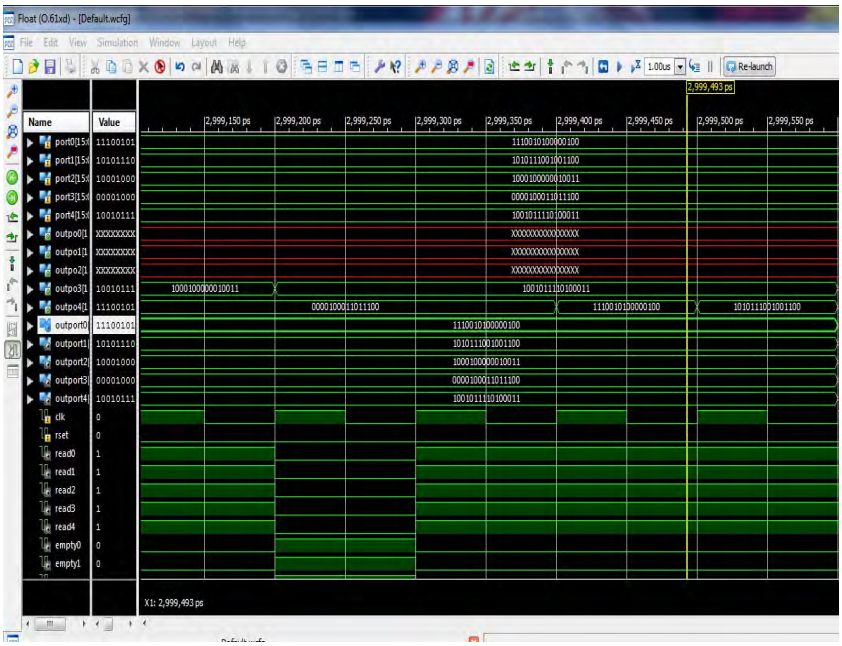

FIG 5: simulation result of five port router when there is contention.

V. EXPERIMENTAL RESULTS

The proposed router is designed and synthesized in Xilinx 13.2 software. The area and power is analysed in cadence tool. By using cadence SoC encounter the layout view of proposed router is generated which is shown in FIG 7. Area and power consumption of the proposed router is generated from the cadence RTL compiler. The area and power report is shown in Table 1, the switching power get reduced by means of proposed buffering method. The critical path of the design is reduced compare to non FWFT based router design, which is shown in FIG 6.

Table 1
Power and area report of router

Instance	CELLS	AREA	POWER
Proposed router	3183	489008	6.07mW
Router with non FWFT and generic arbiter	3406	549576	7.33mW

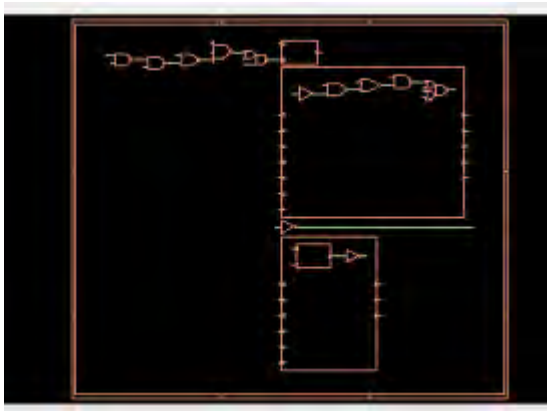

FIG 6: Worst path of the design

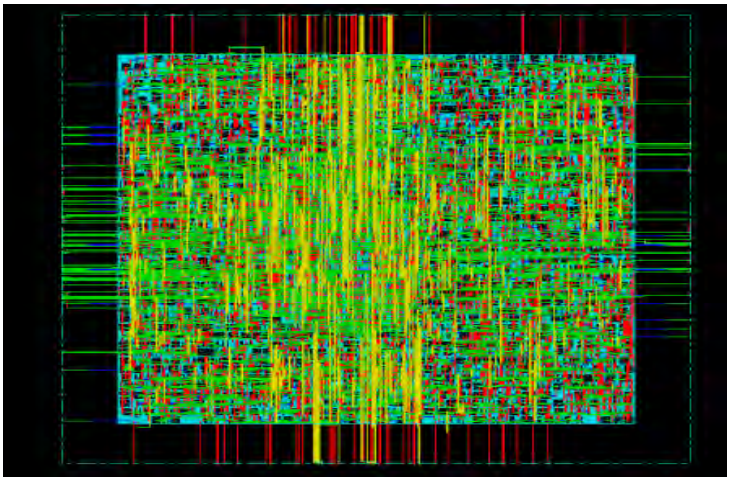

FIG 7: Layout of the router

VI. CONCLUSION

An area and power efficient five port router is designed for NOC. In this paper the router is designed with masked round robin arbiter along with enhanced buffering technique. The router is designed with masked RRA assure that all input requests are treated fairly and occupy less area, especially when the design scales up.

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