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Design and Simulation Five Port Router using Verilog HDL

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Abstract: Multiprocessor system on chip is emerging as a new trend for System on chip design but the wire and power design constraints are forcing adoption of new design methodologies. Researchers pursued a scalable solution to this problem i.e. Network on Chip (NOC). Network on chip architecture better supports the integration of SOC consists of on chip packet switched network. Thus the idea is borrowed from large scale multiprocessors and wide area network domain and envisions on chip routers based network. Cores access the network by means of proper interfaces and have their packets forwarded to destination through multichip routing path. In order to implement a competitive NOC architecture, the router should be efficiently design as it is the central component of NOC architecture .Design and simulation of 5 Port Router was designed and its simulation was done with ModelSim6.5e and synthesis using Xilinx ISE.

Keywords: 5-Port Route, Network on Chip (NOC), Xilinx ISE.

I. INTRODUCTION

The challenge of the verifying a large design is growing exponentially. There is a need to define new methods that makes functional verification easy. Several strategies in the recent years have been proposed to achieve good functional verification with less effort. Recent advancement towards this goal is methodologies. The methodology defines a skeleton over which one can add flesh and skin to their requirements to achieve functional verification. OVM (open verification methodology) is one such efficient methodology and best thing about it is, it is free. This ovm is built on system Verilog and used effectively to achieve maintainability, reusability, speed of verification etc. This project is aimed at building a reusable test bench for verifying 8 Port Router Protocol Bridge by using system Verilog and ovm. In this document the use of vmm and system Verilog to verify a design and to develop a reusable test bench is explained in step by step as defined by verification principles and methodology. The test bench contains different components and each component is again composed of subcomponents, these components and subcomponents can be reused for the future projects as long as the interface is same.

II. ROUTER

System on chip is a complex interconnection of various functional elements. It creates communication bottleneck in the gigabit communication due to its bus based architecture. Thus there was need of system that explicit modularity and parallelism, network on chip possess many such attractive properties and solve the problem of communication bottleneck. It basically works on the idea of interconnection of cores using on chip network. The communication on network on chip is carried out by means of router, so for implementing better NOC, the router should be efficiently design. This router supports four parallel connections at the same time. It uses store and forward type of flow control and Fsm Controller deterministic routing which improves the performance of router. The switching mechanism used here is packet switching which is generally used on network on chip. In packet switching the data the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions on the Internet. A router is a microprocessor-controlled device that is connected to two or more data lines from different networks. When a data packet comes in on one of the lines. The router reads the address information in the packet to determine its ultimate destination. Then, using information in its routing table, it directs the packet to the next network on its journey. The router is a " Five Port Network Router" has a one input port from which the packet enters. It has seven output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 bytes to 64 bytes. Packet header contains three fields DAand length. Destination address(DA) of the packet is of 8 bits. The

switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data.

Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet. The router has a one input port from which the packet enters. It has three output ports where the packet is driven out. The router has an active low synchronous input resetn which resets the router. Data packet moves in to the input channel of one port of router by which it is forwarded to the output channel of other port. Each input channel and output channel has its own decoding logic which increases the performance of the router. Buffers are present at all ports to store the data temporarily. The buffering method used here is store and forward. Control logic is present to make arbitration decisions. Thus communication is established between input and output ports. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called switching mechanism The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 0 bits to 8 bits. A detailed explanation of Design is as bellow Fig.1.

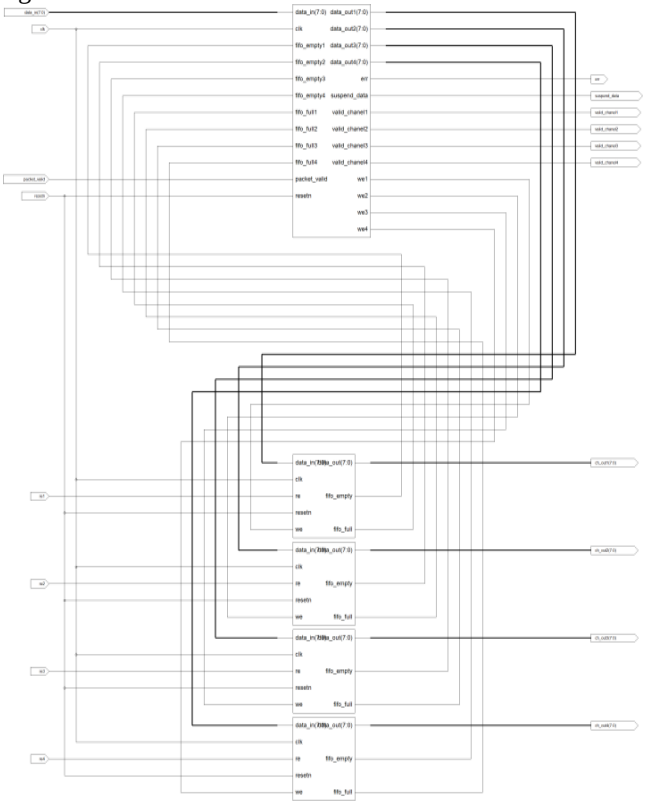

Fig.1. Block Diagram of Five Port Router.

A. Data Packet Format

- Packet contains 3 parts.
- They are Header, payload and parity.
- Packet width is 8 bits and the length of the packet can be between 1 bytes to 63 bytes as shown in Fig.2.

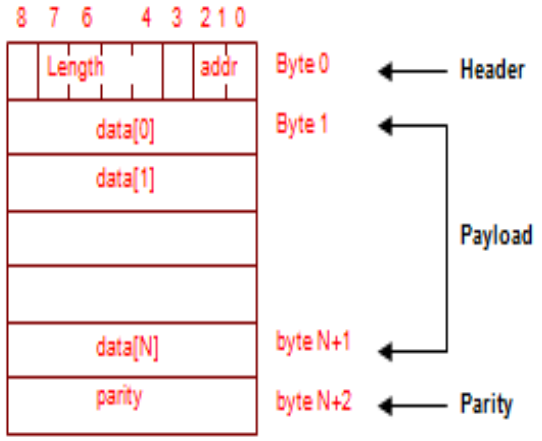

Fig.2. Data Packet Format.

B. Router Input Protocol

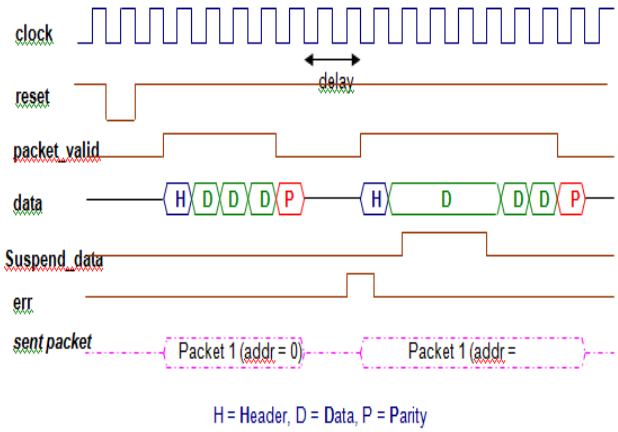

Fig.3. Router Input Protocol.

- All input signals are active high and are synchronized to the falling edge of the clock as shown in Fig.3. This is because the router is sensitive to the rising edge of clock. Therefore, driving input signals on the falling edge ensures adequate setup and hold time, but the signals can also be driven on the rising edge of the clock.
- The packet_valid signal has to be asserted on the same clock as when the first byte of a packet (the header byte), is driven onto the data bus.
- Since the header byte contains the address, this tells the router to which output channel the packet should be routed (data_out_0, data_out_1, or data_out_2).
- Each subsequent byte of data should be driven on the data bus with each new rising/falling clock.

- After the last payload byte has been driven, on the next rising/falling clock, the packet_valid signal must be deserted, and the packet parity byte should be driven. This signals packet completion.
- The input data bus value cannot change while the suspend_data signal is active (indicating a FIFO overflow). The packet driver should not send any more bytes and should hold the value on the data bus. The width of suspend_data signal assertion should not exceed 100 cycles.
- The err signal asserts when a packet with bad parity is detected in the router, within 1 to 10 cycles of packet completion.

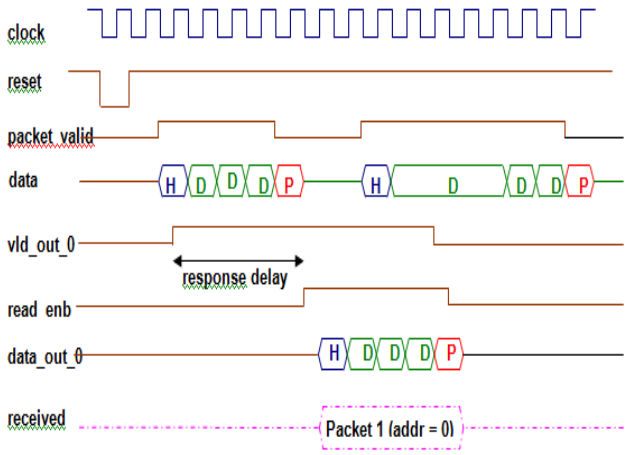

Fig.4. Router output Protocol.

The characteristics of the output protocol are as follows:

- All output signals are active high and can be synchronized to the rising/falling edge of the clock. Thus, the packet receiver will drive sample data at the rising/falling edge of the clock. The router will drive and sample data at the rising edge of clock as shown in Fig.4.
- Each output port data_out_X (data_out_0, data_out_1, data_out_2) is internally buffered by a FIFO of 1 byte width and 16 location depth.
- The router asserts the vld_out_X (vlld_out_0, vld_out_1 or vld_out_2) signal when valid data appears on the vld_out_X (data_out_0, data_out_1 or data_out_2) output bus. This is a signal to the packet receiver that valid data is available on a particular router.
- The packet receiver will then wait until it has enough space to hold the bytes of the packet and then respond with the assertion of the read_enb_X (read_enb_0, read_enb1 or read_enb_2) signal that is an input to the router.
- The read_enb_X (read_enb0, read_enb_1 or read_enb_2) input signal can be asserted on the rising/falling clock edge in which data are read from the data_out_X (data_out_0, data_out_1 or data_out_2) bus.
- As long as the read_enb_X (read_enb_0, read_enb_1 or read_enb_2) signal remains active, the data_out_X (data_out_0, data_out_1 or data_out_2) bus drives a valid packet byte on each rising clock edge.
- The packet receiver cannot request the router to suspend data transmission in the middle of the packet. Therefore, the packet receiver must assert the read_enb_X (read_enb_0, read_enb_1 or read_enb_2) signal only after it ensures that there is adequate space to hold the entire packet.
- The read_enb_X (read_enb_0, read_enb_1 or read_enb_2) must be asserted within 30 clock cycles of the vld_out_X (vld_out_0, vld_out_1 or vld_out_2) being asserted. Otherwise, there is too much congestion in the packet receiver.
- The DUV data_out_X (data_out_0, data_out_1 or data_out_2) bus must not be tri-stated (high Z) when the DUV signal vld_out_X (vld_out_0, vld_out_1or vld_out_2) is asserted (high) and the input signal read_enb_X (read_enb_0, read_enb_1 or read_enb_2) is also asserted high.

III. REGISTER BLOCK

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock. Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the fifo for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity as shown in Fig.5.

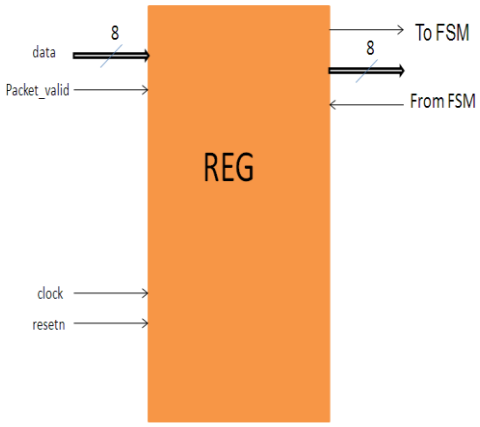

Fig.5. Router Output Block.

IV. ROUTER CONTROLLER (FSM)

This module generates all the control signals when new packet is sent to router as shown in Fig.6. These control signals are used by other modules to send data at output, writing data into the fifo. There are 3 fifos used in the router design. Each fifo is of 8 bit width and 16 bit depth. The fifo works on system clock. It has synchronous input signal reset. If resetn is low then full =0, empty = 1 and data_out = 0.

The FIFO has doing 3 deferent operations

- Write Operation
- Read operation
- Read and Write Operation

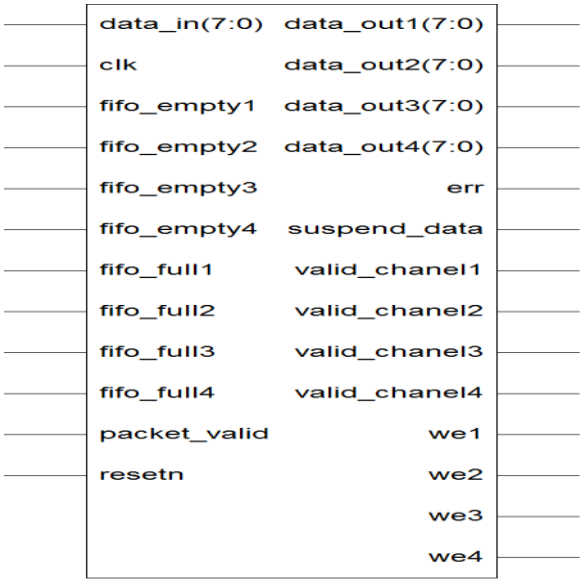

Fig.6. Block Diagram of FSM.

The functionality of FIFO explains Below Fig.7.

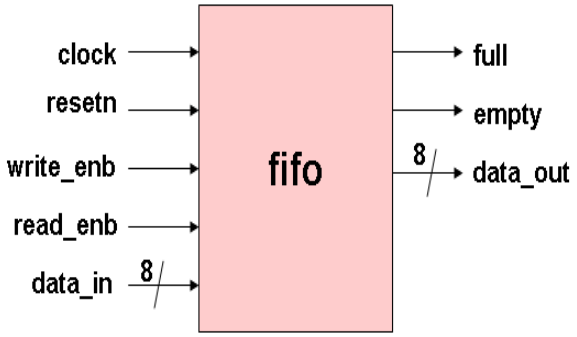

Fig.7. Five port Router FIFO.

Write operation: The FIFO write operation is done by when the data from input data_in is sampled at rising edge of the clock when input write_enb is high and fifo is not full. in this condition onaly FIFO Write operation is done.

Read Operation: The FIFO Read Operation is The data is read from output data_out at rising edge of the clock, when read_enb is high and fifo is not empty.

Read and Write operation can be done simultaneously.
Full: it indicates that all the locations inside fifo has been written.
Empty: it indicates that all the locations of fifo are empty.

V. SIMULATION RESULTS

The router was designed using verilog and it was synthesized using XILINX ISE and Simulated using Model SIM6.5e as shown in Figs.8 and 9.

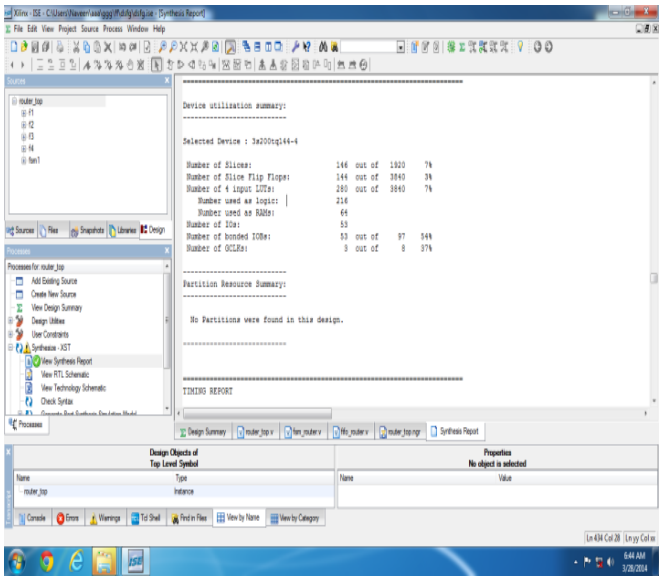

Fig.8. Synthesis report of 5 Port Router.

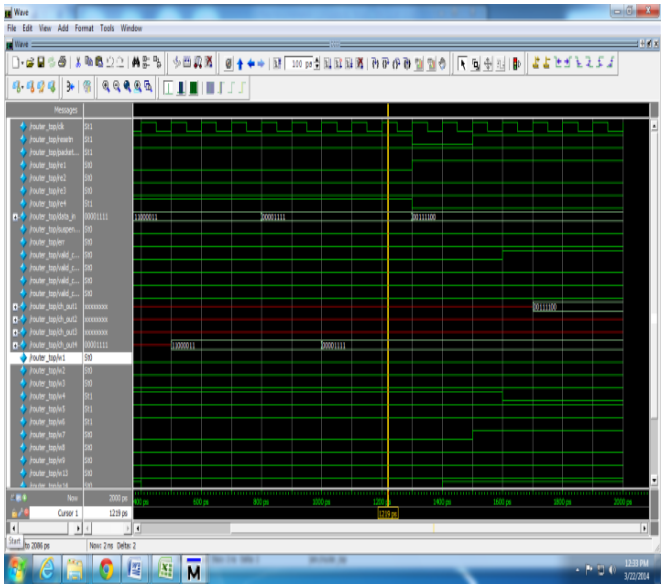

Fig.9. Port Router Output.

VI. CONCLUSION

Here we have proposed the router which supports five connections at the same time without any communication bottleneck. We have used simplest decoding logic, store and forward flow mechanism, packet switching, XY deterministic routing, input and output buffering which increases the performance of router. In this paper awe proposed a 5 Port router design for effective data transfer its simulation and synthesis was done using the verilog coding.

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