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SC-HEAP_E3 : Bus I/F TLM timing specification

Renesas Electronics Corporation
MCU Software Division

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RENESAS Group CONFIDENTIAL

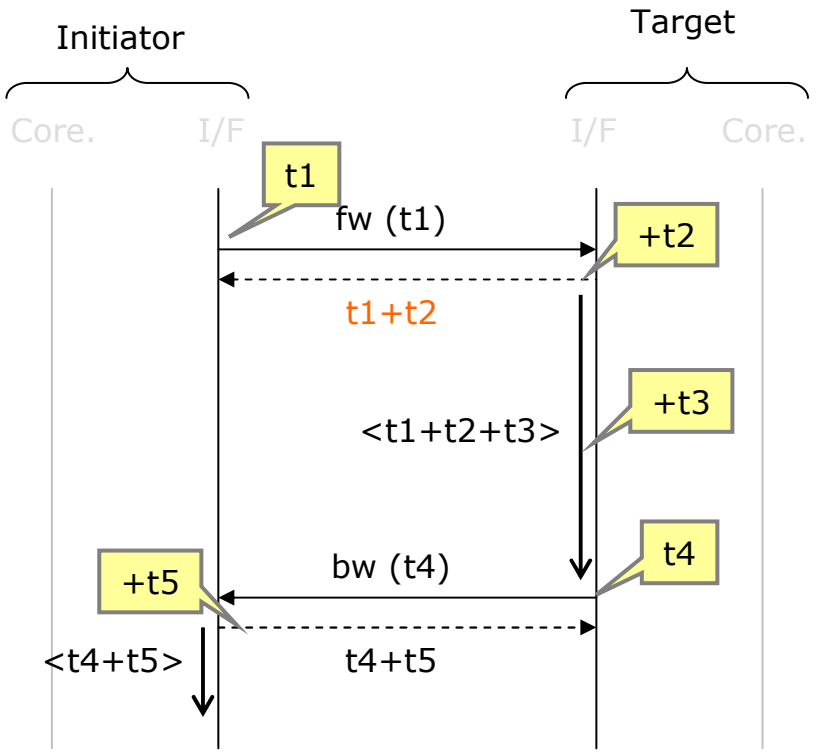
Purpose of the document

The document describes the communication timing of bus I/F applied to SC-HEAP_E3.
The document is for the developer of the bus master IP or bus slave IP.

The bus modeling outline in OSCI TLM2.0

Time which can be set in AT 2phase of OSCI TLM 2.0 and IP to set the time

- It's possible to set time to spend with argument of nb_transport_fw and nb_transport_bw in AT 2phase. It's also possible to add time to spend between bw from fw.

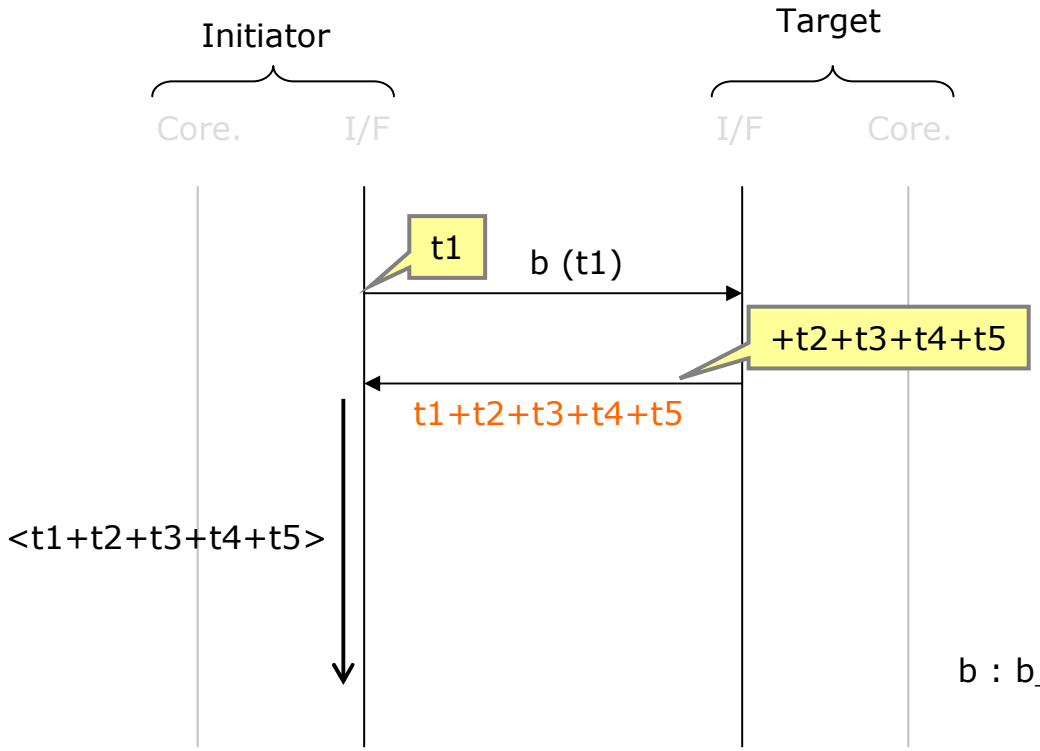


Time	IP to set	meaning
t1	Initiator	Time until the transaction starting
t2	Target	Time until the request completion
t3	Target	The internal processing time
t4	Target	Time until the response starting
t5	Initiator	Time until the response completion

fw : nb_transport_fw
bw : nb_transport_bw

Time which can be set in LT of OSCI TLM 2.0 and IP to set the time

- It is possible to set time to spend with argument of b_transport in LT. Initiator can set time to spend at b_transport calling. Target adds time to spend for transmission and returns it to initiator.

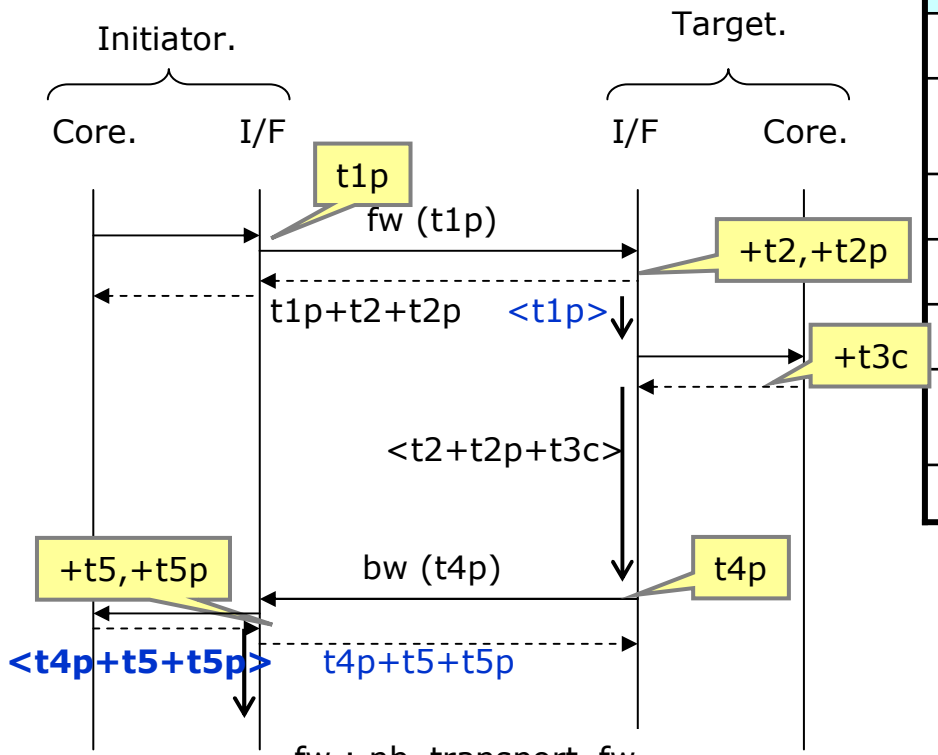


Time	IP to set	The meaning
t1	Initiator	Time until the transaction starting
t2	Target	Time until the request completion
t3	Target	The internal processing time
t4	Target	Time until the response starting
t5	Target	Time until the response completion

b : b_transport

Bus modeling policy using AT 2phase of OSCI TLM 2.0

- Model consists of I/F and core, and time is sent at I/F or core.
- Initiator set time until a request is acquired (t1p). It is set by initiator core.
- t2 is set by target I/F and consists of time for transmission(t2) and latency(t2p). t2p is a parameter of I/F, and variable.
- Target core set inner spending time(t3c).
- Target set time until the response acquisition(t4p). It's a parameter of I/F, and variable.
- t5 is set by initiator, and consists of time for transmission(t5p) and latency(t5). t5p is variable by a parameter of I/F.



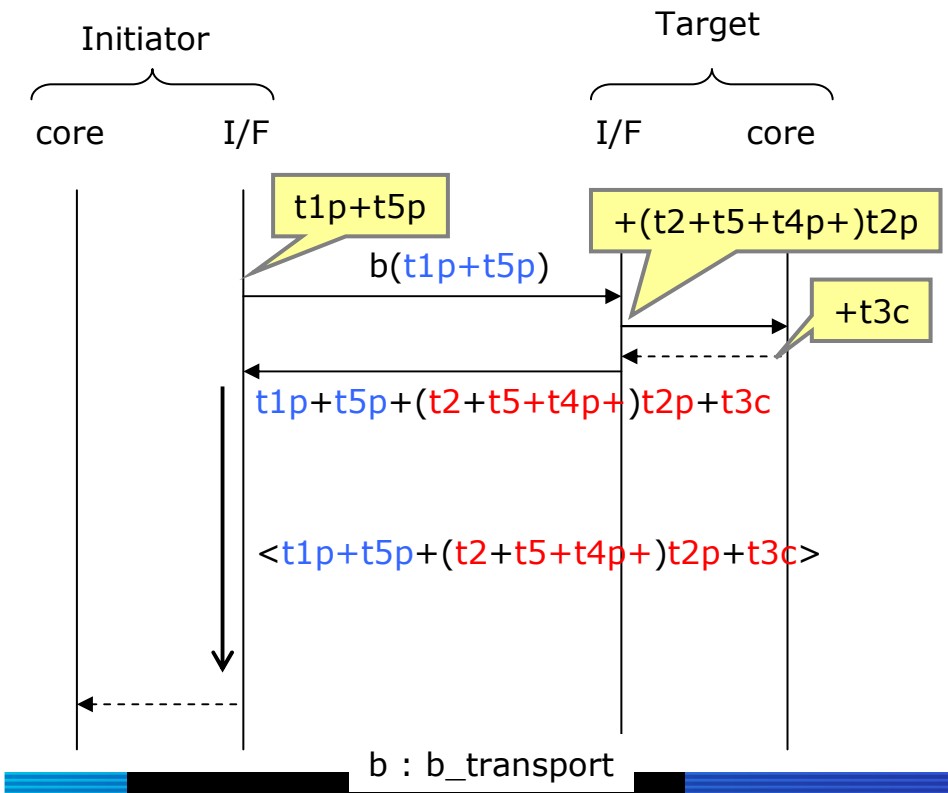
Time	IP to set	meaning	value
t1p	Ini IF	Time before request acquisition*1	Depend on core
t2	Tgt IF	Transfer time for request phase	Depend on transmission
t2p	Tgt IF	Request phase latency	Parameter
t3c	Tgt core	Response Readiness time	Depend on core
t4p	Tgt IF	Time before response acquisition	Parameter
t5	Ini IF	Transfer time for Response phase	Depend on transmission
t5p	Ini IF	Response phase latency *1	Parameter

*1: not supported by this I/F

explanation of subscript of t	
no subscript	Time to consume in IF (time to spend for bus protocol)
p	Time to spend in IF (time to set by parameter)
c	Time to spend in core

Modeling policy of a bus using a letter telegram of OSCI/TLM 2.0

- Model consists of I/F and core, and time is sent at I/F or core.
- Initiator sets time to spend in in initiator at b calling. (t1p+t5p)
- t2p is set by target IF as a parameter. t3c is time to spend in target core.
- T40 is set by target. But t4p is included in tp2 because there is no phase which can set t4p in LT.



Time	IP to set	meaning	value
t1p	Ini IF	Time before request acquisition*1	Depend on core
t2	Tgt IF	Transfer time for request phase	Depend on transmission
t2p	Tgt IF	Request phase latency	Parameter
t3c	Tgt core	Response Readiness time	Depend on core
t4p	Tgt IF	Time before response acquisition	Parameter
t5	Tgt IF *2	Transfer time for Response phase	Depend on transmission
t5p	Ini IF	Response phase latency *1	Parameter

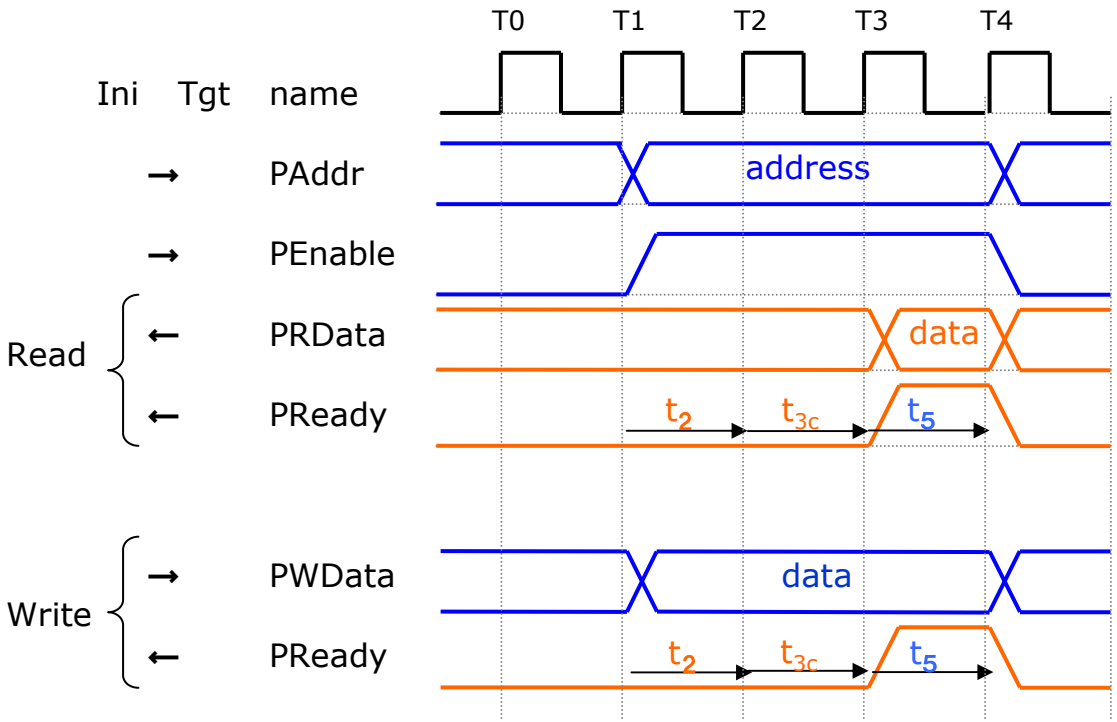
*1: not supported by this I/F

*2: notice that IP which set it is different from AT

explanation of subscript of t	
no subscript	Time to consume in IF (time to spend for bus protocol)
p	Time to spend in IF (time to set by parameter)
c	Time to spend in core

APB

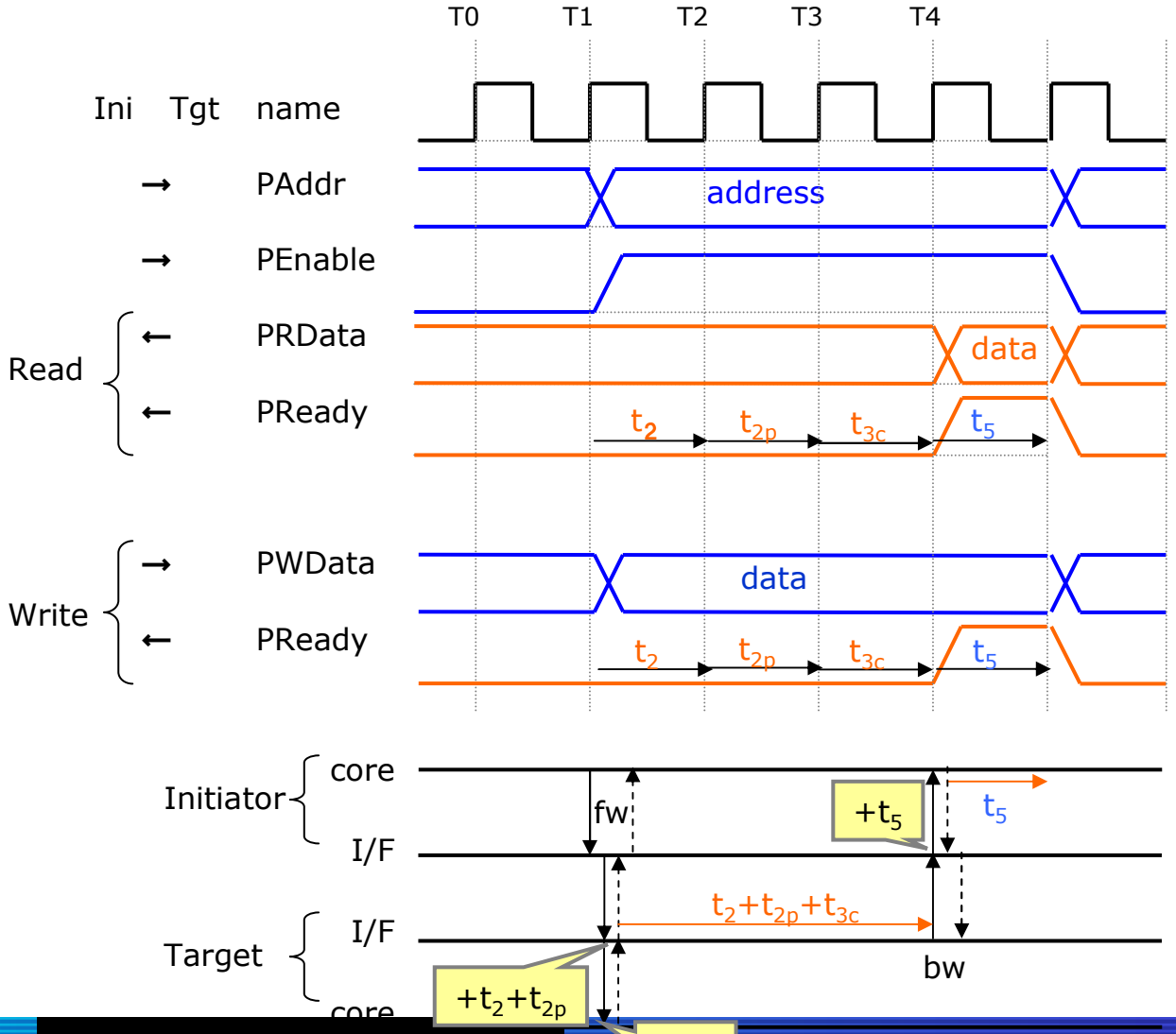
Time to spend in APB



time	meaning	IP to set	number of cycles
t2	Target acquires the address.	-	fixed to 1
t3c	Preparation time for data acquisition or data output for target.	Tgt	>= 0
t5	Time for data acquisition or data output for target.	-	fixed to 1

Mapping to OSCI/TLM2.0 AT 2phase

- Timing specification details

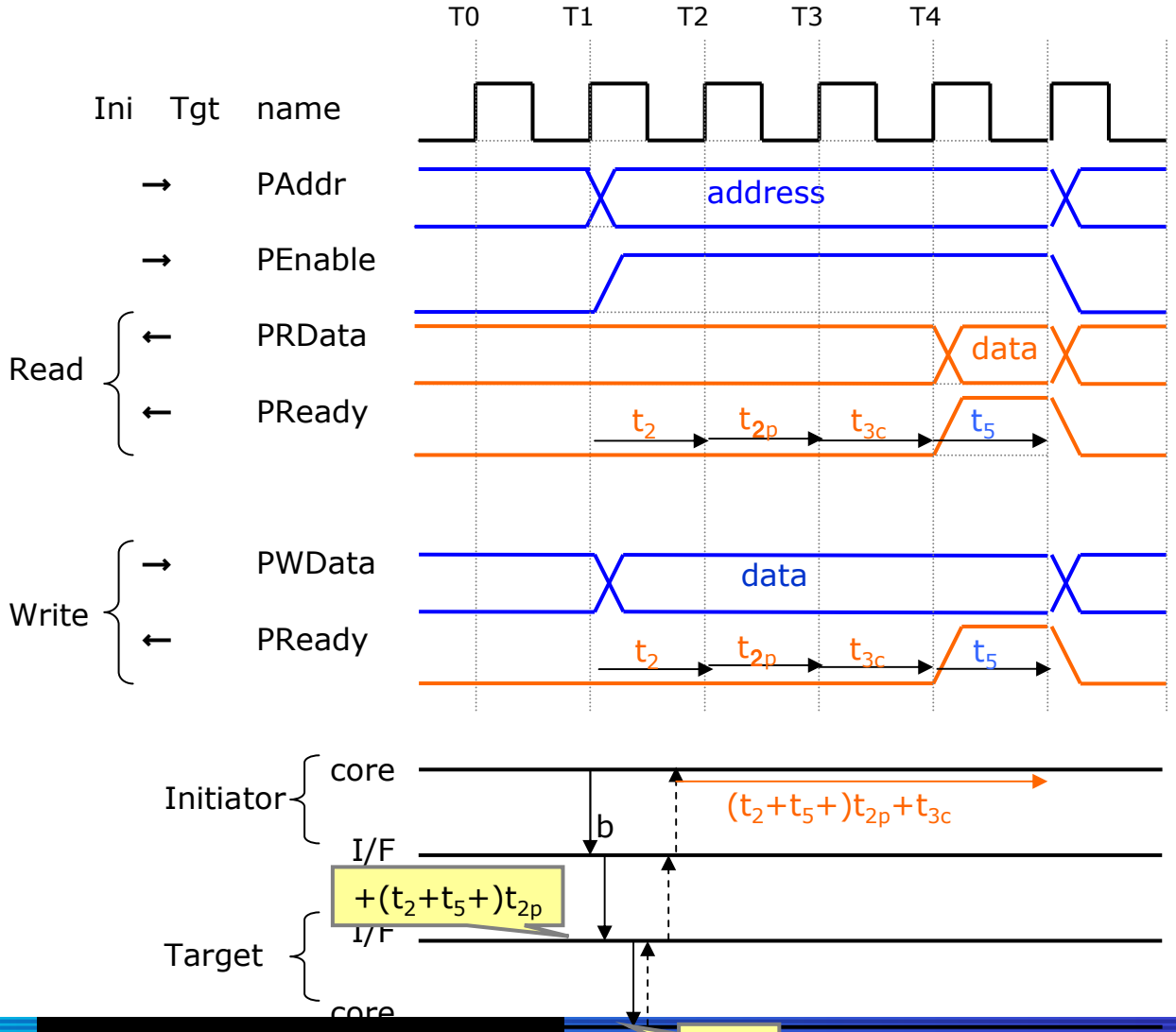


There is no time to express at t1p and t4p in APB/AT, so t1p and t4p are fixed to 0.

1. Initiator core calls API in initiator I/F.
2. Initiator I/F calls fw(0), and target I/F returns the value (t2+t2p) to initiator I/F. Target I/F calls API in target core with time (t2+t2p).
3. Target core returns t2+t2p+t3c to target I/F, and target I/F spends the time.
4. After target I/F spends the time, bw (0) is called.
5. Initiator I/F returns the value(t5) to target I/F and spend the time.

Mapping to OSCI/TLM2.0 LT

- Timing specification details



There is no time to express in t1p by APB/LT, so t1p is fixed to 0.

1. Initiator core calls API in initiator I/F.
2. Initiator I/F calls b(0), and target I/F calls API in target core with (t2+t5+)t2p. t2p is set with a parameter of target IF. Default value of t2p is 0.
3. Target core returns (t2+t5+)t2p+t3c to target I/F, and target I/F returns to initiator I/F with the return value(t2+t5+t2p+t3c).
4. Initiator I/F spend the time(t2+t5+t2p+t3c).
5. After the time spending Initiator I/F return API of initiator core.

Mapping to OSCI/TLM2.0

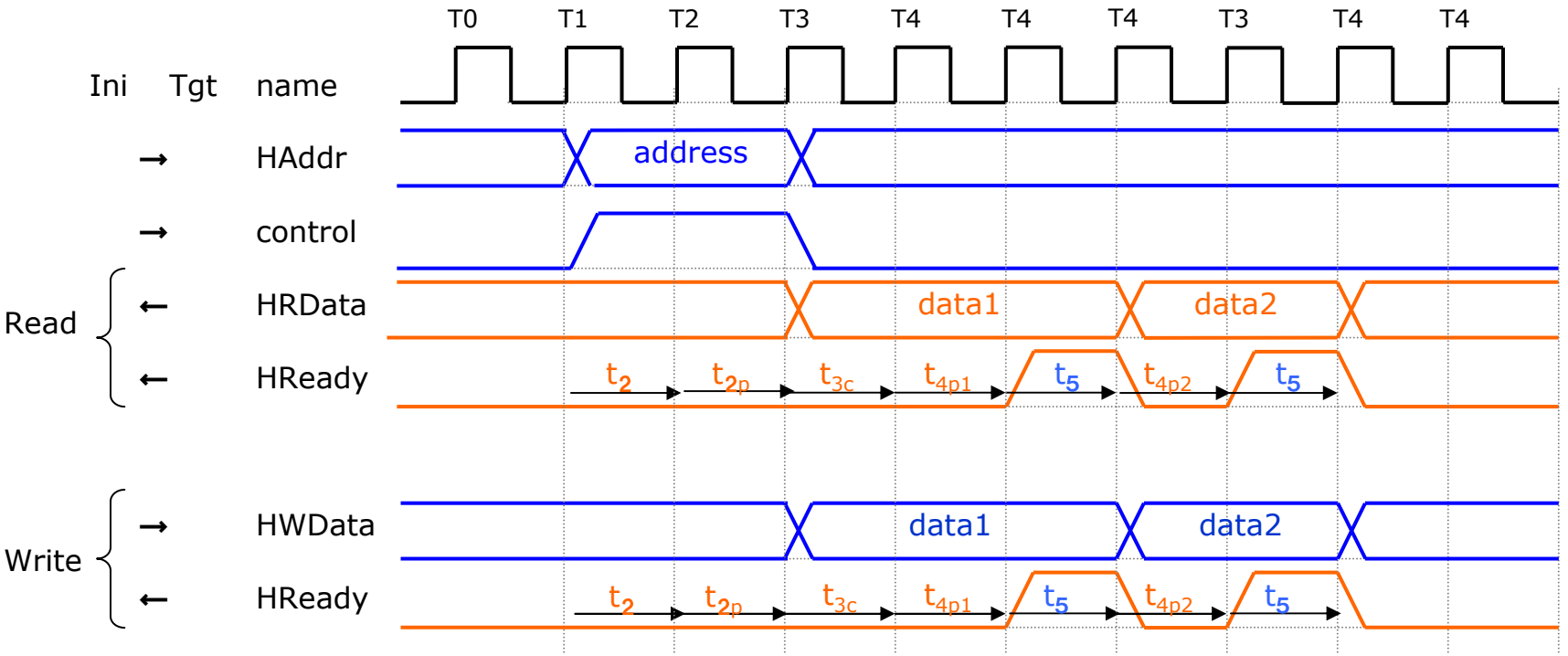
- The timing specification which is not supported
  - AT

    none
  - LT

    none

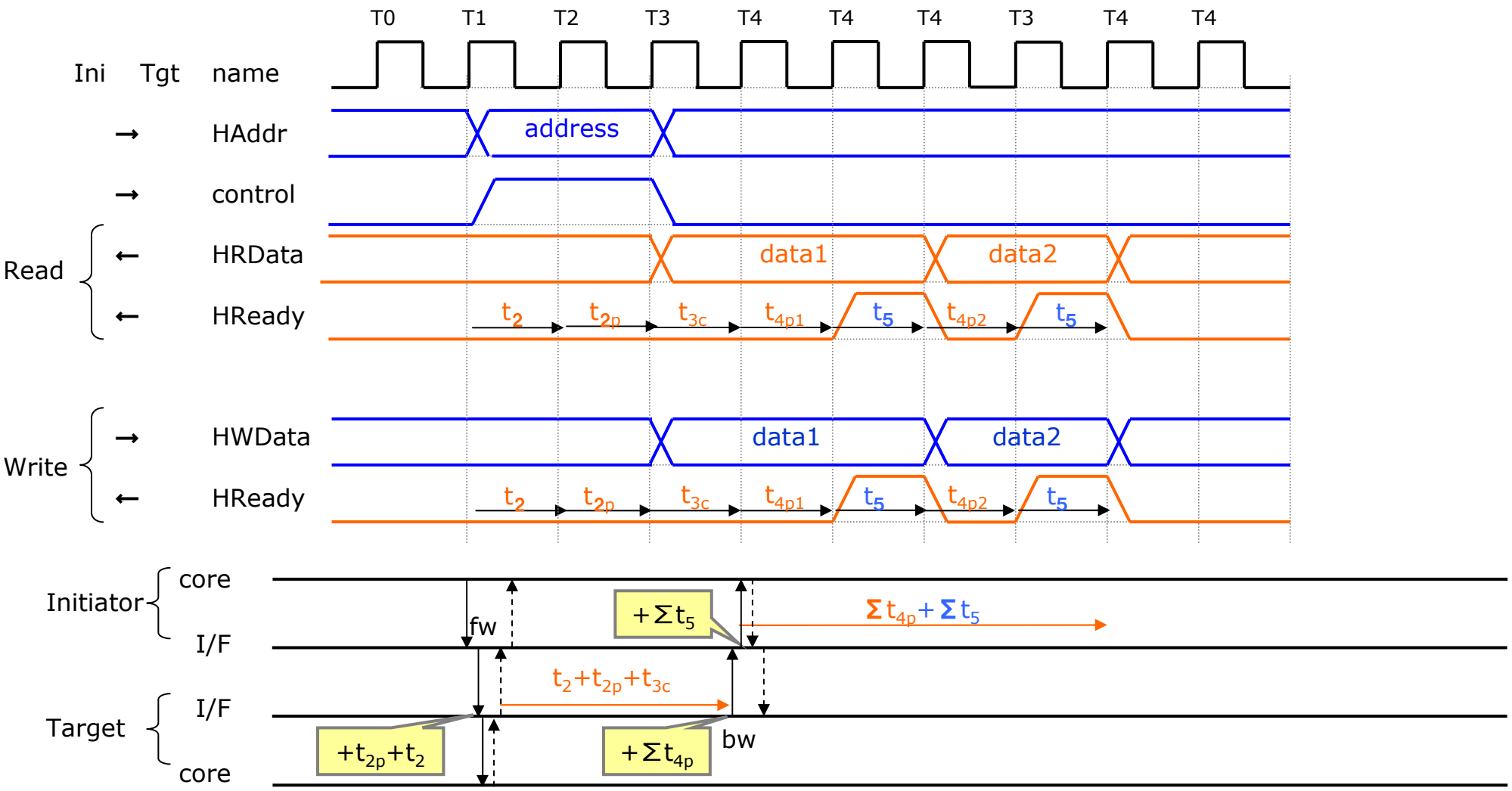
AHB

Time to spend in AHB

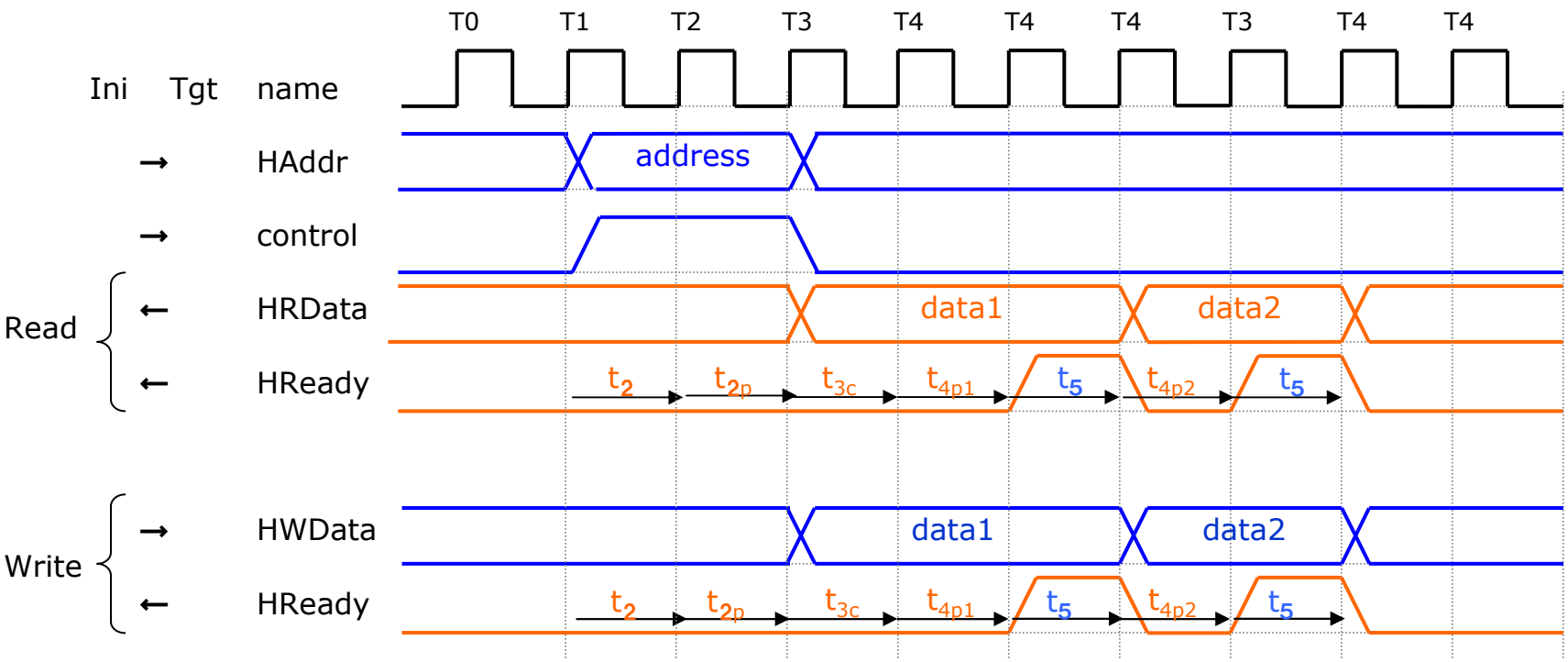


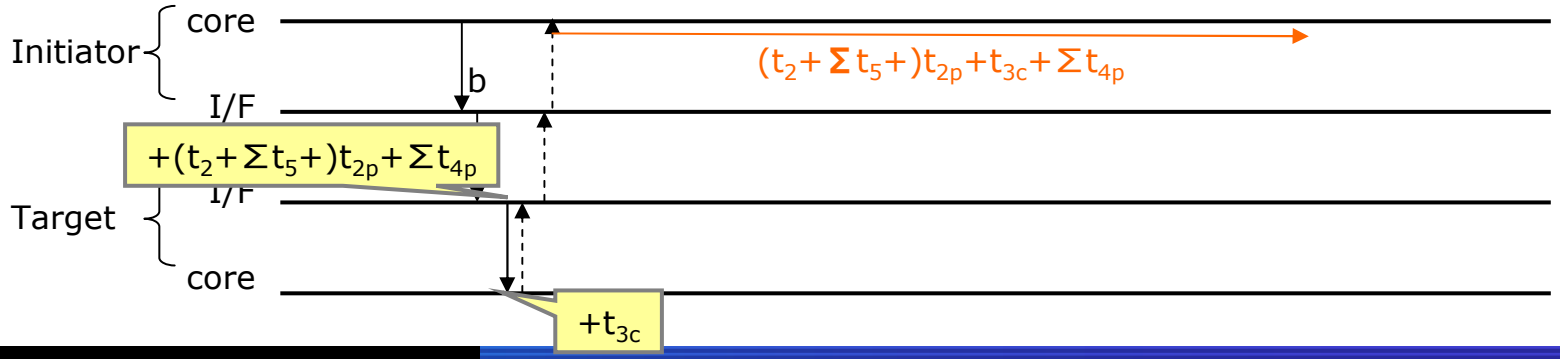
time	meaning	IP to set	number of cycles
t2	A target acquires the address.	-	fixed to 1
t3c	Preparation time for data acquisition or data output for target.	Tgt	>= 0
t4p	Preparation time for next data output for target.	Tgt	>= 0
t5	Time for data acquisition or data output for target.	-	fixed to 1

Mapping to OSCI/TLM2.0 AT 2phase



Mapping to OSCI/TLM2.0 LT





Mapping to OSCI/TLM2.0

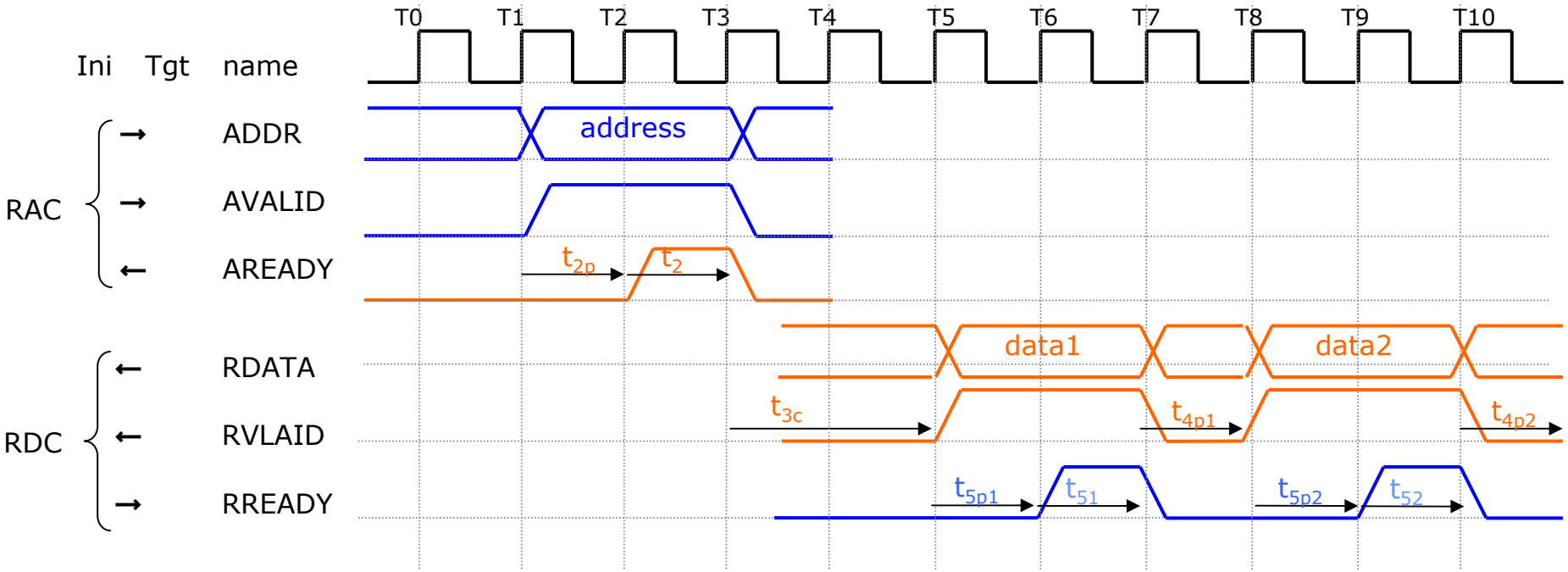
- The timing specification which is not supported
  - AT

    Split transaction (SPLIT transmission and RETRY transmission)
  - LT

    Split transaction (SPLIT transmission and RETRY transmission)

AXI

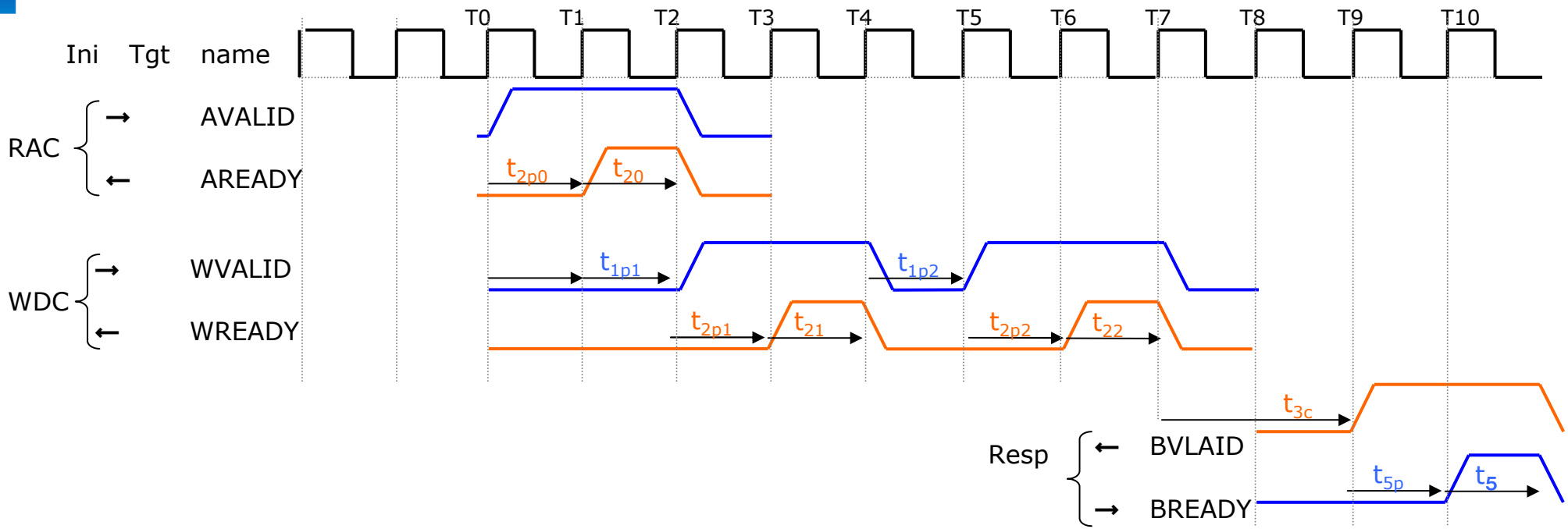
Time to spend at read in AXI



time	meaning	IP to set	number of cycles
t2p	Preparation time for data acquisition for target.	Tgt	>= 0
t2	Time for address acquisition for target.	-	fixed to 1
t3c	Preparation time for data output for target.	Tgt	>= 0
t4p*i*	Preparation time for next data output for target.	Tgt	>= 0
t5p*i*	Preparation time for data acquisition for initiator.	Ini	fixed to 0*
t5*i*	Time for data acquisition for initiator.	-	1 fixing

※ It means that it isn't supported by I/F. The addition is possible by core part.

Time to spend at write in AXI

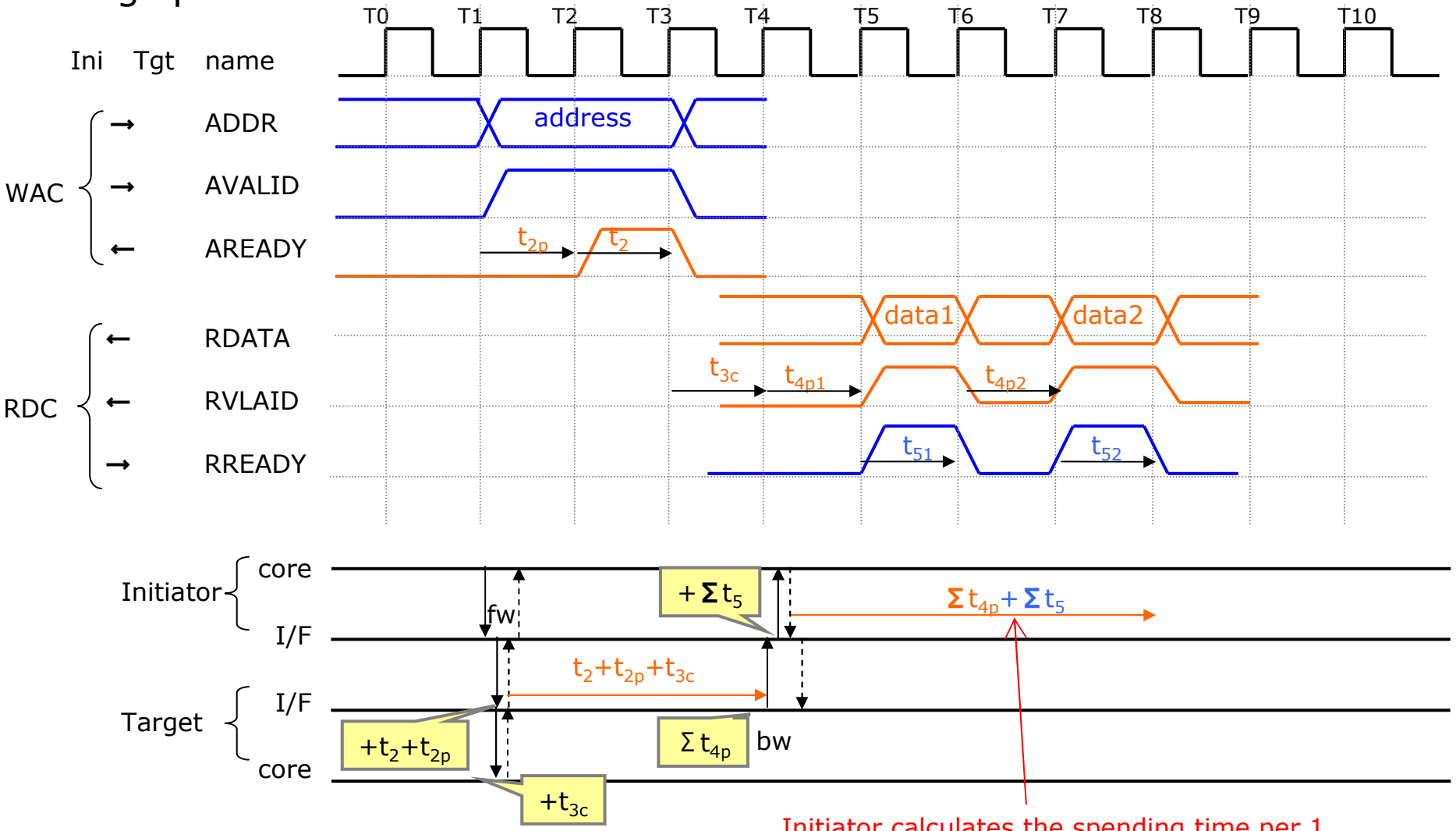


time	meaning	IP to set	number of cycles
t2p*i*	Preparation time for address and data acquisition for target.	Tgt	>= 0
t2*i*	Time for address and data acquisition for target.	-	fixed to 1
t1p*i*	Preparation time for next data output for initiator.	Ini	fixed to 0
t3c	Preparation time for response output for target.	Tgt	>= 0
t5p	Preparation time for response acquisition for initiator.	Ini	fixed to 0*
t5	Time for response acquisition for initiator.	-	fixed to 1

※ It means that it isn't supported by I/F. The addition is possible by core part.

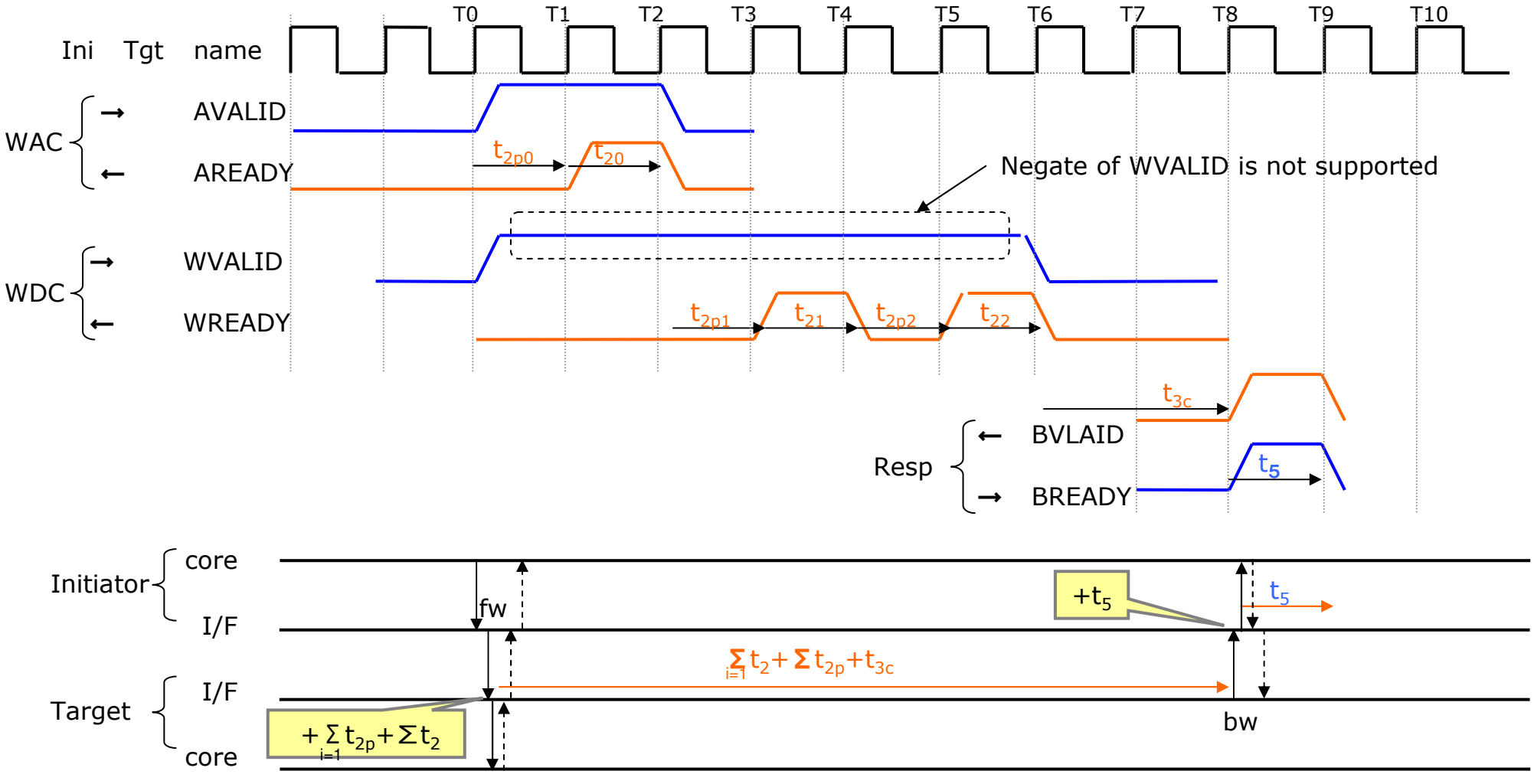
Mapping /Read to OSCI/TLM2.0 AT 2phase

- Timing specification details



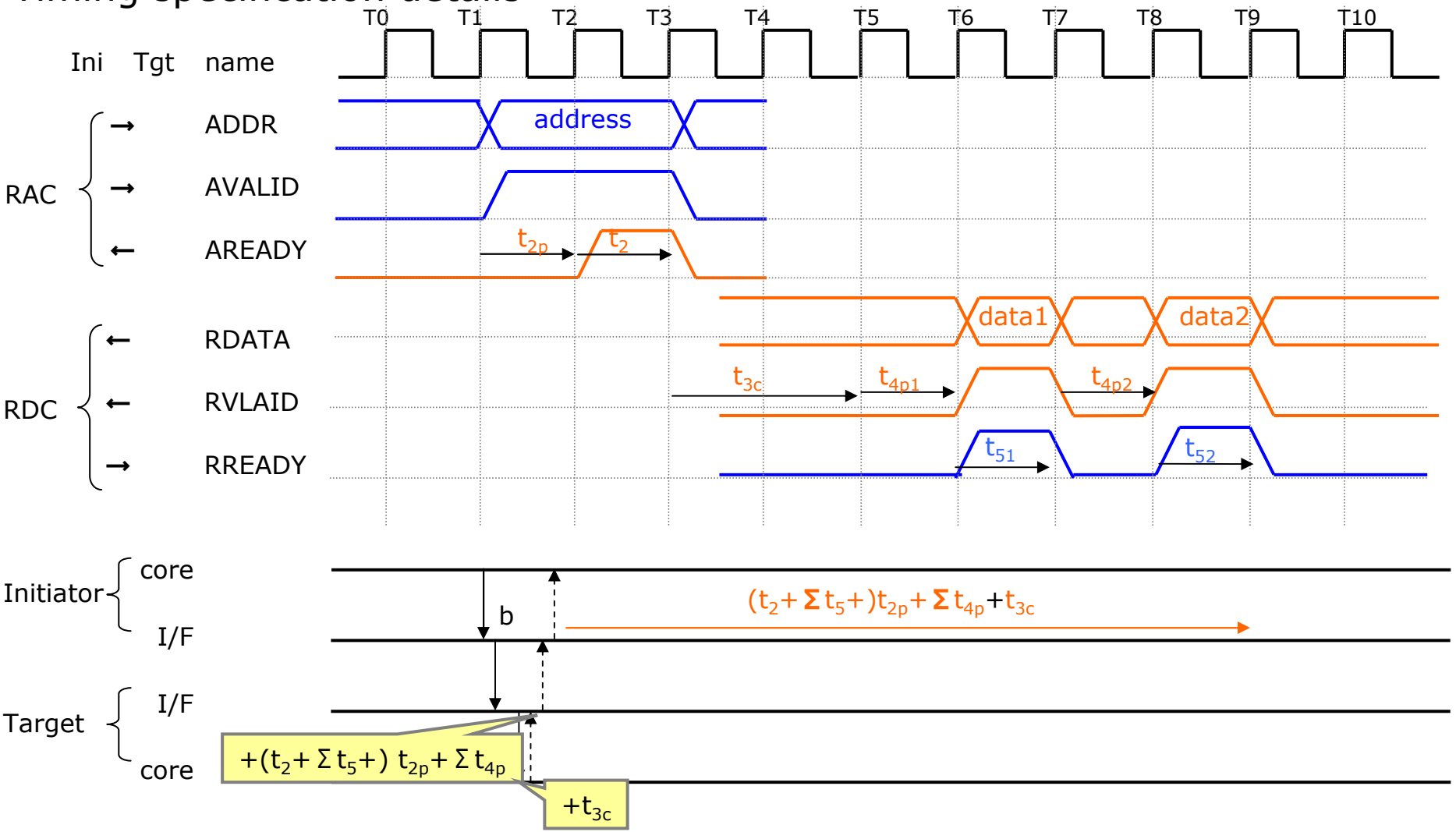
Mapping /Write to OSCI/TLM2.0 AT 2phase

- Timing specification details



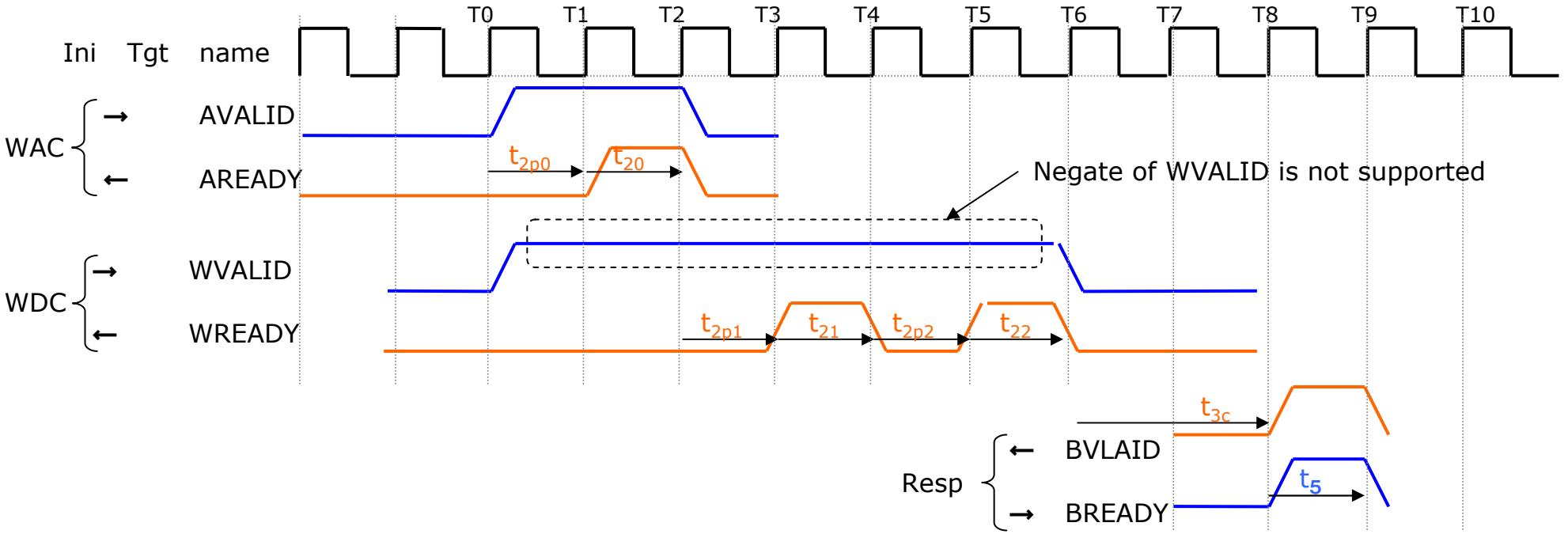
Mapping /Read to OSCI/TLM2.0 LT

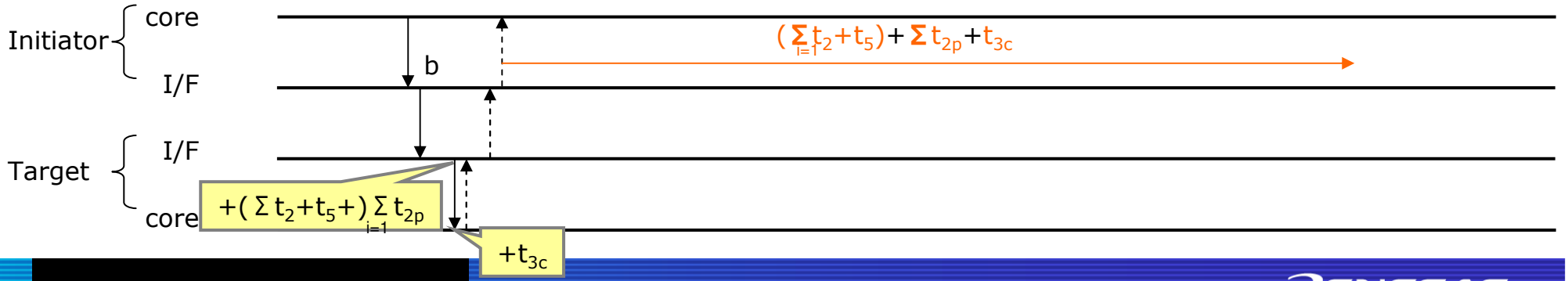
- Timing specification details



Mapping /Write to OSCI/TLM2.0 LT

- Timing specification details





Mapping to OSCI/TLM2.0

- The timing specification which is not supported
  - AT
    - Pipeline treatment of WAC WDC
      (The output order that WDC is output behind t2p after WAC, is fixed.)
  - LT
    - Pipeline treatment of RAC RDC.
    - Pipeline treatment of WAC WDC WRC.

Parameterization of latency

Parameterization of latency

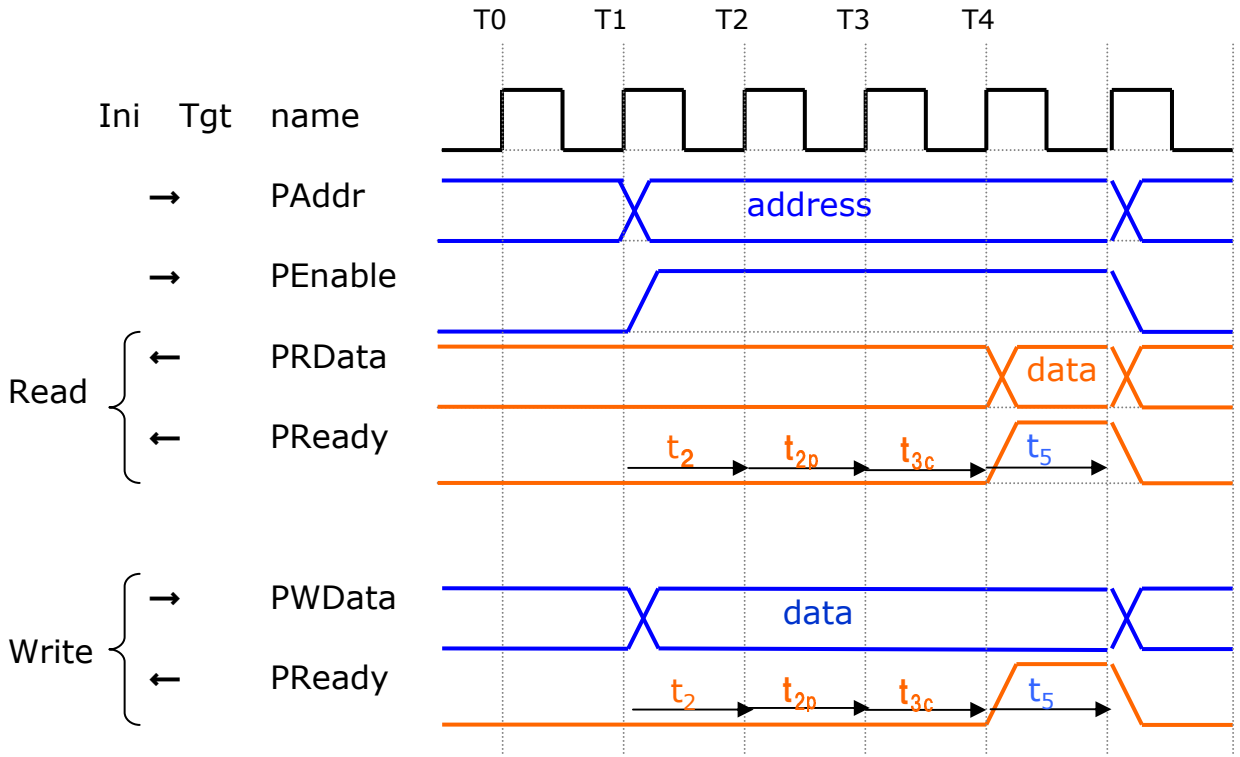
- Each of read/write has 1 parameter in APB.
- Each of read/write has 3 parameters in AHB and AXI.

latency setting API	APB	AHB	AXI
SetReadLatency	t_{2p}	-	-
SetWriteLatency	t_{2p}	-	-
SetReadInitialLatency	-	t_{2p}	t_{2p0} of read address channel
SetWriteInitialLatency	-	t_{2p}	t_{2p0} of write address channel
SetReadFirstDataLatency	-	t_{4p1}*	t_{2p} of first read data channel
SetWriteFirstDataLatency	-	t_{4p1}*	t_{2p1} of first write data channel
SetReadNextDataLatency	-	t_{4pn} (n>=2)*	t_{4pn} of next read data channel (n>=1)
SetWriteNextDataLatency	-	t_{4pn} (n>=2) *	t_{2pn} of write data channel (n>=2)

*: Latency of FirstData and NextData is usually same value in AHB.

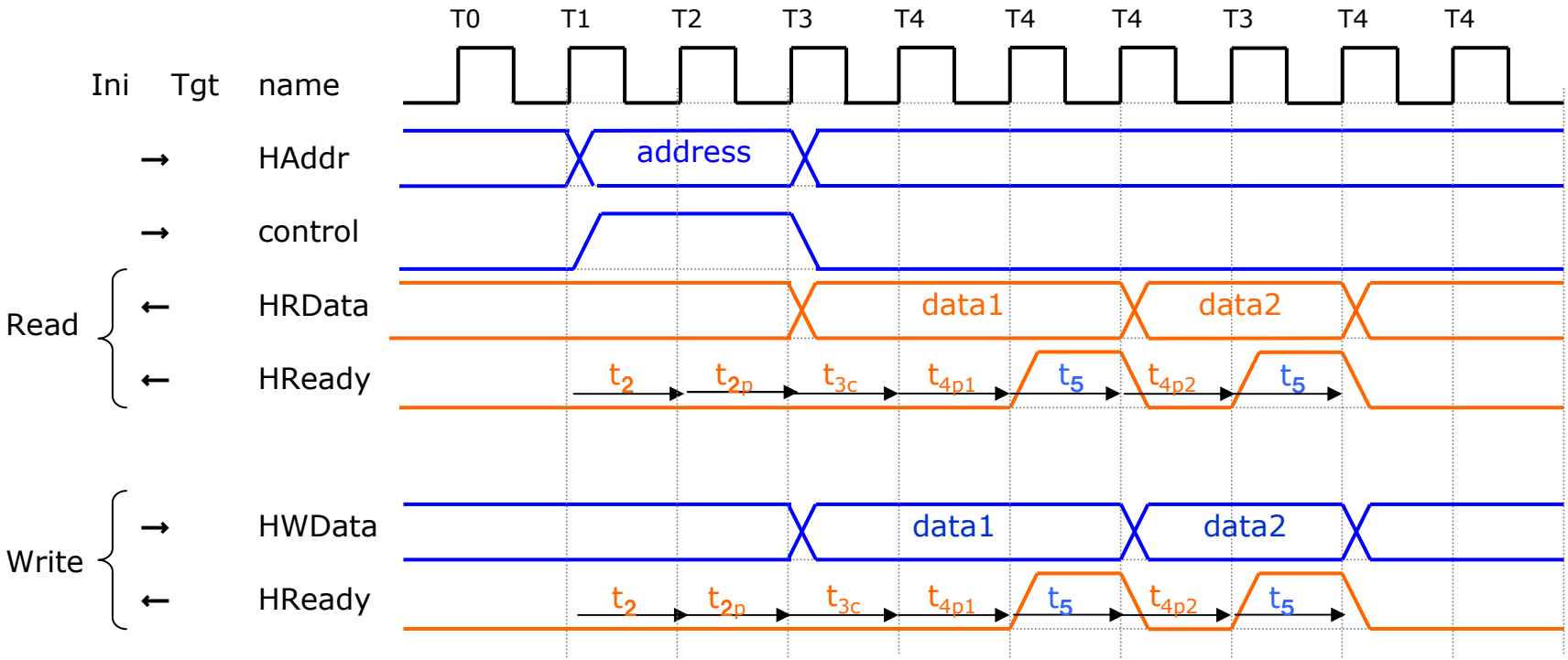
APB (read/write)

- t_{2p} is parameterized in APB.
- One of read is set with setReadLatency function, one of write is set with setWriteLatency function.



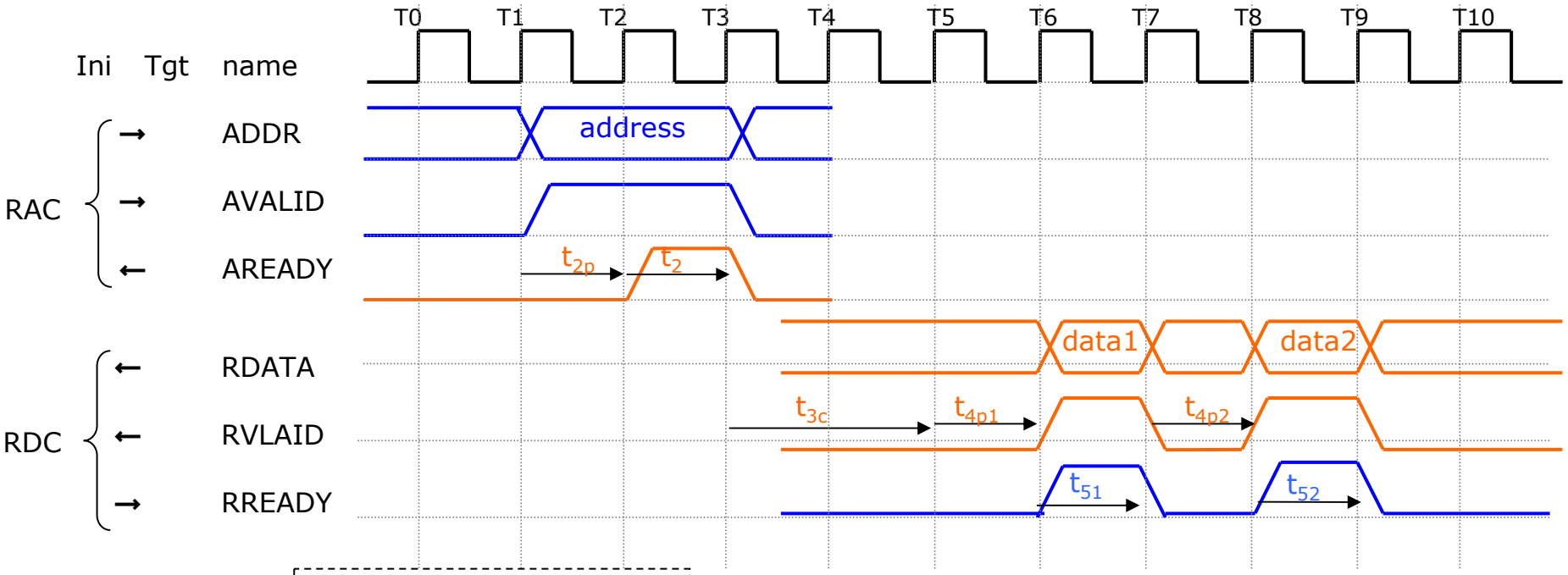
AHB (read/write commonness)

- t_{2p}, t_{4p1} and t_{4pn} (n>=2) are parameterized.
- t_{4p0} is set with setReadInitialLatency/setWriteInitialLatency function.
- t_{4p1} is set with setReadFirstDataLatency/setWriteFirstDataLatency function.
- t_{4pn} (n>=2) is set with setReadNextDataLatency/setWriteNextDataLatency function.



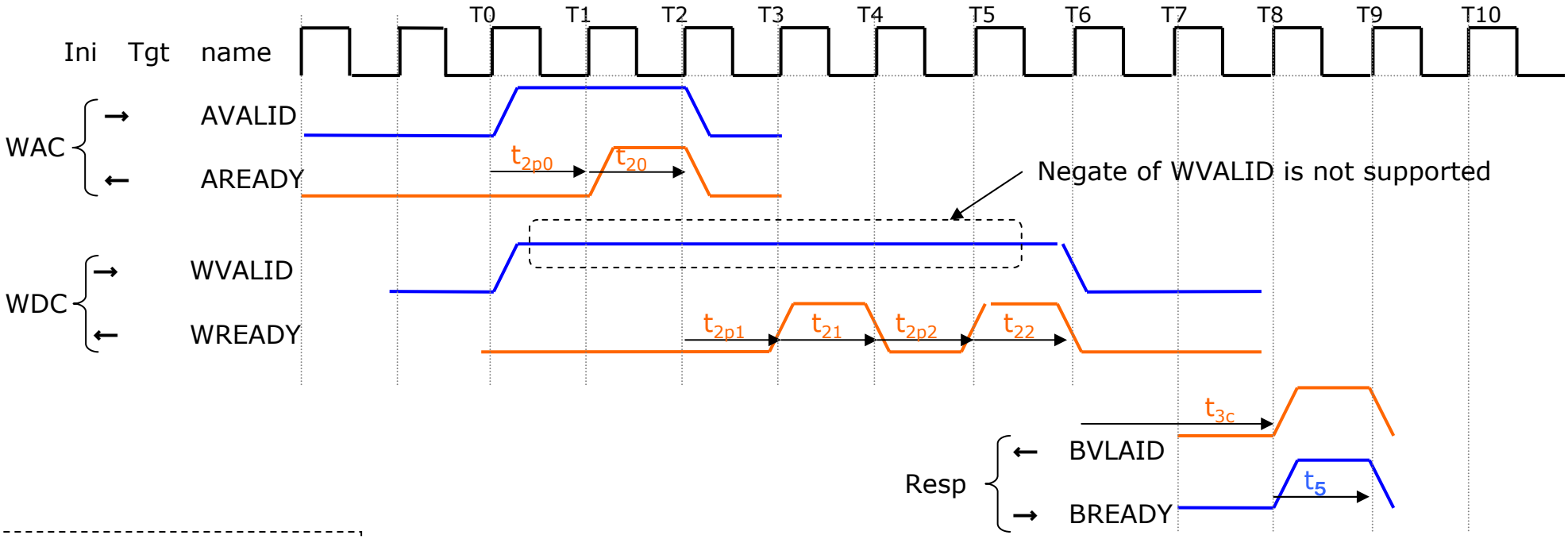
AXI (Read)

- t_{2p} of read address channel and t_{4p1}, t_{4pn}(n>=2) of read data channel are parameterized.
- t_{2p} of read address channel is set with setReadInitialLatency function.
- t_{4p1} of read data channel is set with setReadFirstDataLatency function.
- t_{4pn} of read data channel (n>=2) is set with setReadNextDataLatency function.



AXI (Write)

- t_{2p0} of write address channel and t2p1, t2pn(n>=2) of write data channel are parameterized.
- t_{2p0} of write address channel is set with setWriteInitialLatency function.
- t_{2p1} of write data channel is set with setWriteFirstDataLatency function.
- t_{2pn} of write data channel (n>=2) is set with setWriteNextDataLatency function.



WAC:write address channel

WDC:write data channel

Restriction

- AHB.
  - Split transaction (SPLIT transmission and RETRY transmission)
- AXI.
  - Pipeline treatment of WAC WDC at AT
    (The output order that WDC is output behind t2p after WAC, is fixed.)
  - Pipeline treatment of RAC RDC at LT
  - Pipeline treatment of WAC WDC WRC at LT