Exploring SC-HEAP

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10/06/11 Rev. 1.0

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1. Introduction

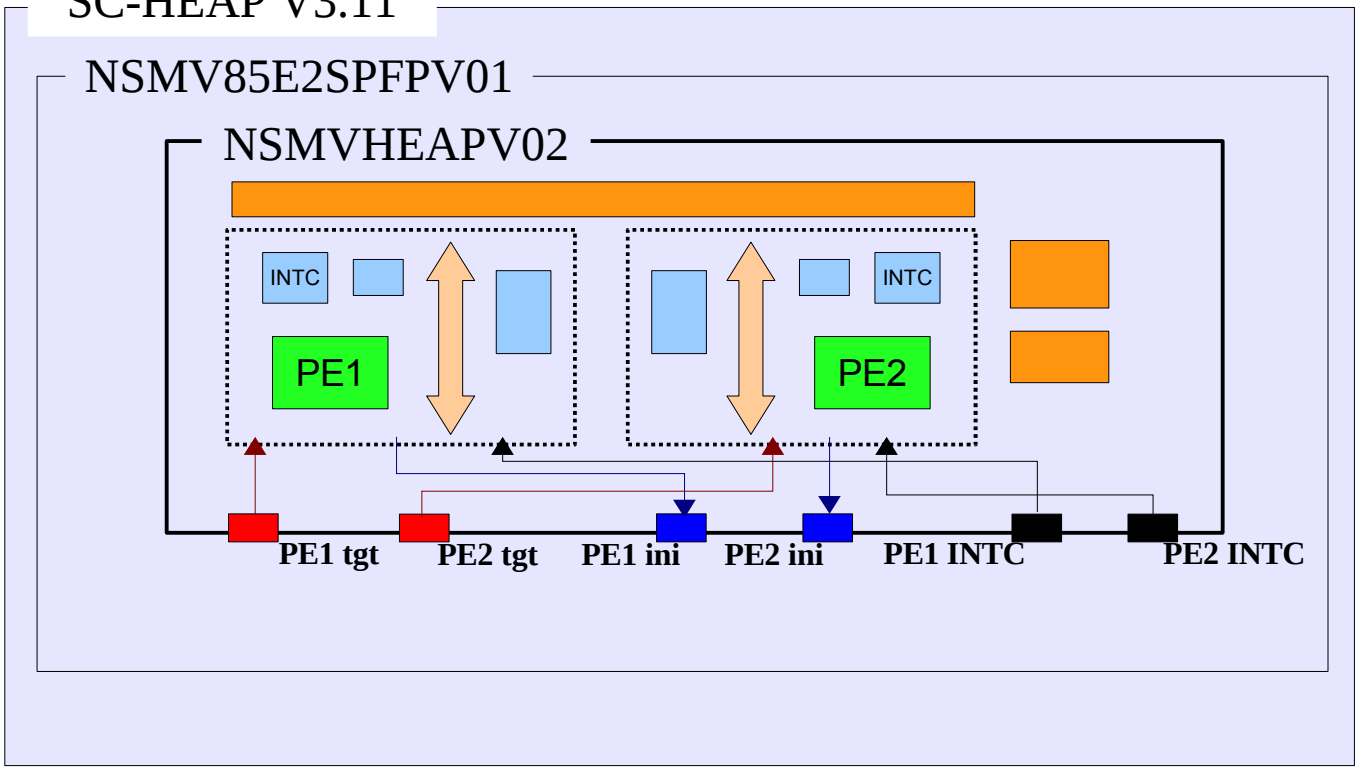
Introduction

Front-End Design Technology Development Department (FE) are working with MCU Software Division (S-tool team) to develop a V850-based SystemC verification platform for automotive customer (part of M40 project). It will be used for performance estimation and software development.

The new platform is customized from existing SC-HEAP platform. Therefore, investigating existing SC-HEAP is a good preparation for the development of the new platform.

2. Platform overview

Hierarchy of SC-HEAP platform (1/3)



Platform

E2SPF

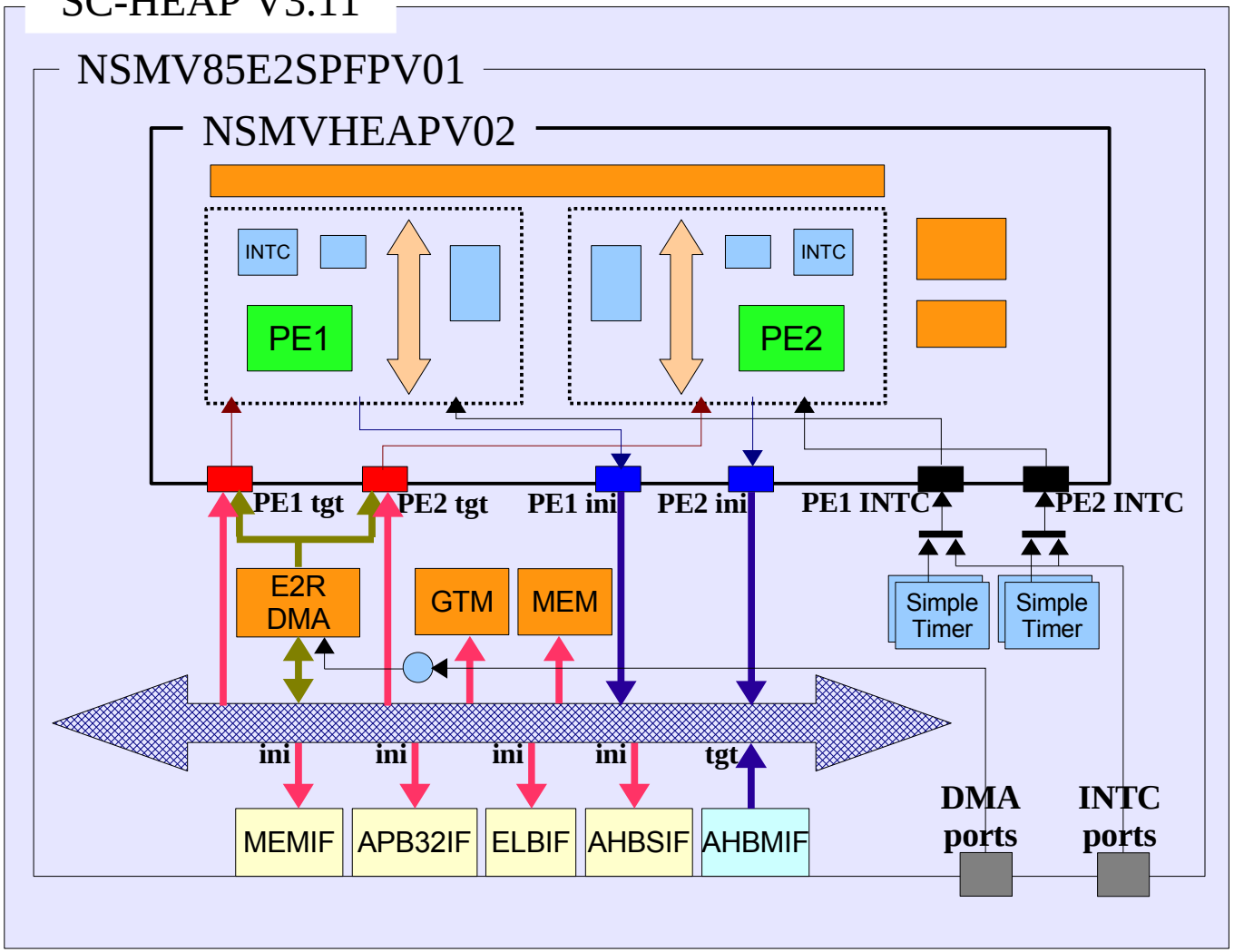
HEAP (1/2 CPU)

V850E2 *cpu*
(E2R/E2M/E2H)

E2R INTC

PPU
Local Bus
Cache ...

Hierarchy of SC-HEAP platform (2/3)



Platform

E2SPF

HEAP (1/2 CPU)

V850E2 *cpu*
(E2R/E2M/E2H)

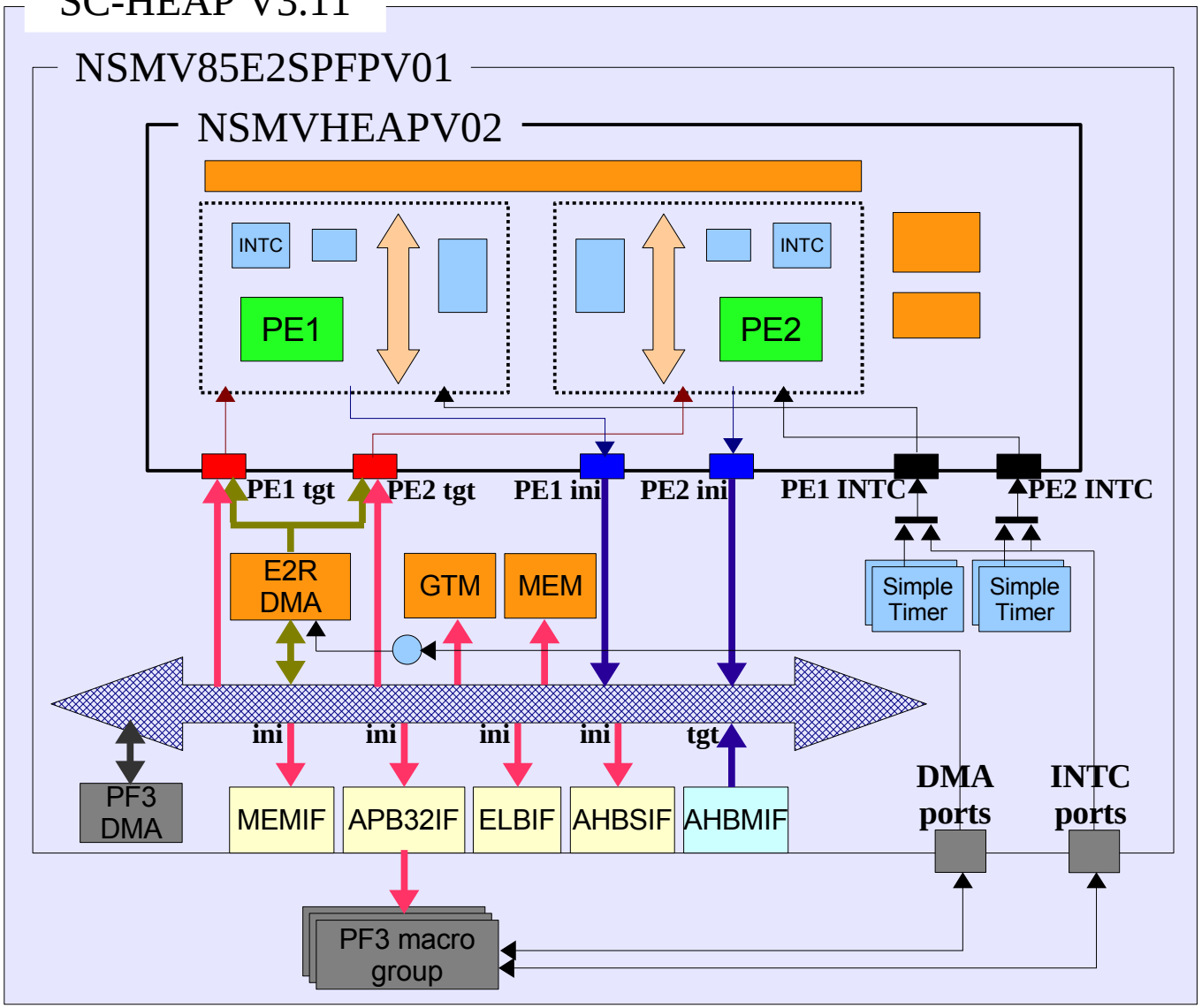
E2R INTC

PPU
Local Bus
Cache ...

E2R DMA
GTM
MEM
Local Bus ...

BUS IF
(AHB/APB/...)

Hierarchy of SC-HEAP platform (3/3)

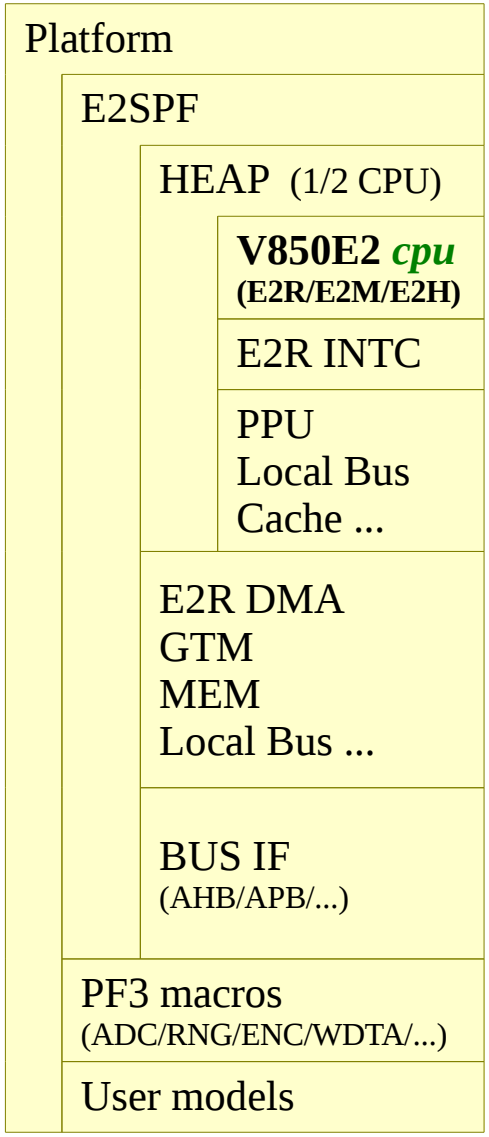


Platform

- E2SPF
  - HEAP (1/2 CPU)
    - **V850E2** ***cpu*** **(E2R/E2M/E2H)**
    - E2R INTC
    - PPU
      Local Bus
      Cache ...
  - E2R DMA
    GTM
    MEM
    Local Bus ...
  - BUS IF
    (AHB/APB/...)
- PF3 macros *unofficial*
  (ADC/RNG/ENC/WDTA/...)
- User models

Directory structure

```
pltfrmCompile
    |-- build
    |   `-- ITintv1m
    |       |-- pltfrm.h, pltfrm.cpp    --->  platform construction
    |       |-- Makefile, *.mk          --->  'make' files
    |       |-- sim.x                   --->  executable file
    |       |-- heap.cfg                --->  configuration files
    |       |-- *.map                   --->  address map files
    |       `-- run*.csh                --->  execution script
    |-- include                         --->  Header files
    |   |-- HEAPPlatform.h
    |   |-- NSMV85E2SPFPV01.h
    |   |-- PF3.h
    |   `-- ....
    |-- lib
    |   `-- SCHEAP-G4.a                 --->  Archive of SC-HEAP
    |-- lib-modelsO3                    --->  Objective (*.o) files
    |-- models                          --->  User models
    |   |-- ATSLAVE
    |   |-- TIMER
    |   `-- tlm
    `-- soft                            --->  Software programs
        `-- intv1m_v4_heap
```



2. The simulation

Simulation

How to start the simulation?

> Execute **run_core.csh**

run_core.csh

```
setenv SC_SIGNAL_WRITE_CHECK DISABLE
set SIMX          = "./sim.x"
set RESULT_LOG    = "result.txt"
set CONFIG_BASE   = "heap.cfg"
set CYCLE         = "1600"

# invoke command
${SIMX} -n ${CYCLE} -config ${CONFIG_BASE} >>& ${RESULT_LOG}
```

Configuration file should be prepared to set parameter to the model. (sample on next slide)

Configuration file

heap.cfg

```
// For SystemC clock
[CLOCK]                              = (10, SC_NS);

// For HEAP(2CPU) or 1CPU platform
[PLATFORM]                           = HEAP

// For INTC module
[INTC_11]                            = (1, 1)
[INTC_21]                            = (1, 1)

// For V850E2R module
[V850E2R_MASK_12]                    = 0x1fffffff
[V850E2R_PROFILE_MEMORY_12]          = ITintv_memory_12.log
[V850E2R_PROGRAM_12]                 = ../../soft/intv1m_v4_heap/core1/core1.hex
....

// For iLB module
[ILB_MAPFILE_13]                     = top.iLB_13.map
[ILB_MAPFILE_23]                     = top.iLB_23.map
```

Parameter

Output log files

Address map files

Model number

Address map file

The address range of the slave connected with the bus should be set.

top.dLB_14.map

```
; [ Format ]
; slave_target_port_name  StartAddress  Size
;
; slave_target_port_name is the target_port name of the bus slave.
; It is with hierarchy path like "top.slave.target_port".
;
; for FlashCache_15
E2SPFP.NSMVHEAPV02.CACHE_15.target_port          0x00000000      0x00040000
; for EXctrlMEM_18(TLM2IF_3A1)
E2SPFP.NSMVHEAPV02.BRIDGE_17.target_port         0x00300000      0x00100000
; for EXctrlMEM_28(TLM2IF_3A1)
E2SPFP.NSMVHEAPV02.BRIDGE_17.target_port         0x00400000      0x00100000
; for INTC_11
E2SPFP.NSMVHEAPV02.INTC_11.target_port           0x1fff6000      0x00000460
; for Slave_34 via bridge_17
E2SPFP.NSMVHEAPV02.BRIDGE_17.target_port         0x00600000      0x00008000
; for GTM24_35 via bridge_17
E2SPFP.NSMVHEAPV02.BRIDGE_17.target_port         0x1ffffb00      0x00000100
; for PEG_1H
E2SPFP.NSMVHEAPV02.PEG_1H.target_port            0x1fff69a0      0x00000020
```

(Sample of address map file)

Output log files

Various kinds of report files can be created: memory access, cache access, register access, CPU operation,...

ITintv_register_12.log

Time	PC	OpeCode	Mnemonic	RegisterNo	Data
170	0x00002000	0xffff5640	movhi	r10	0xffff0000
170	0x00002004	0x64905f2a	ld.h	r11	0x00000001
190	0x00002008	0x00005a61	cmp	0x5(PSW)	0x00000021
		dfecff80	jarl	r31	0x00002018
		00d0062a	mov	r10	0x000100d0
		0020a7ea	ldsr	0x14	0x000100d0
		340c0623	mov	r3	0x0030340c
		a0080624	mov	r4	0x0030a008
			mov	r5	0x000182cc
			mov	r1	0x0030340c
			cmp	0x5(PSW)	0x00000020
			cmov	r30	0x0030340c
			jarl	r31	0x0001002c
			ori	0x5(PSW)	0x00000021
			ori	r6	0x00000000
			mov	r1	0xffff6400
			ld.h	r8	0x00000000
			movhi	r17	0x00300000
			mov	r30	0x00300000

ITintv_memory_12.log

Time	PC	Address	Size	Event	Data
620	0x00010048	0x00302000	4	W	0x00000000
870	0x00030004	0x00303408	4	W	0xffff6400
920	0x0003000c	0x003033e0	4	W	0x00000000

ITintv_fcache_25.log

Cache Configuration I-Cache=8KB 2Way D-Cache=0KB 0Way

Time	PC	Address	Size	Event	Result	Way-No.	Level
20	0x00000000	0x00000000	16	I	Miss	--	0
25	0x00000000	0x00000000	16	I	Miss	--	1
80	0x00000000	0x00000010	16	I	Hit	0	0
100	0x00000000	0x00002000	16	I	Miss	--	0
105	0x00000000	0x00002000	16	I	Miss	--	1
160	0x00000000	0x00002010	16	I	Hit	0	0
180	0x00000000	0x00002020	16	I	Hit		
200	0x00000000	0x00002030	16	I	Hit		
220	0x00000000	0x00002010	16	I	Hit		
240	0x00000000	0x00002020	16	I			
260	0x00000000	0x00020000	16				
265	0x00000000	0x00020000	1				
320	0x00000000	0x00020010	1				

ITintv_execution_summary_core1.log

```
Execution Summary
==========
                                    ions: 481
                                        : 16000 nsec
                                        : 1600
```

ITintv_heap_cache_summary_core1.log

```
Cache Summary
==========
Fetch access
 Total number of Cache miss hit:          9
 Total number of Executed Instructions: 481
 Cache miss hit ratio:                  0.018711
```


3. Upcoming plan

M40PF platform

The new platform is planned to be released in 2012/12 with below customized features from current platform:

- CPU architecture will be changed from V850E2R to RH850 G3x.
- Number of CPU will be increased to four.
- Main bus will be replaced by AXI.
- New IP models (mainly APB peripherals) will be developed.
- A wrapper class similar to TLM common class will be provided for IP modeling.

Reference

[1] SC-HEAP V3.11 Users Manual (OSCI version V850E2 HEAP)

[2] SC-HEAP user modeling environment users manual.

[3] SC-HEAP Trial.

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