Cadence Op-Amp Schematic Design Tutorial for TSMC CMOSP35

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Contents

Preface

The purpose of this document is to familiarize the reader with the Cadence set of tools in order to do analog micro-electronic circuits. The design process will use TSMC's CMOSP35 technology and as a result requires access to the restricted technology files.

Chapter 1

Introduction

This tutorial assumes that the user is working in the CMC supplied environment for CMOSP35 design.

1.1 Review of CMOS FET's

The Complimentary Metal Oxide Semi-Conductor Field Effect Transistor is a four terminal device: Base, Emitter, Collector and Substrate. Unlike the Bipolar Transistor the MOSFET is a symmetrical device: the source and drain can be interchanged.

The models which SPICE uses for the CMOSP35 technology are very accurate, however, are too complex to be used by humans. A quick overview of the device operation follows, for a more complete discussion please refer to an appropriate text book. The gate of the device is insulated from the rest of the device, meaning that no current will flow into the gate of a MOSFET. The substrate connection, for an N-channel transistor, is always connected to V_{SS} (which usually means ground). When the voltage on the gate of the device is large enough an inversion layer forms under the gate, between the drain and source. This means that a channel of charge carriers exists between the two N-type regions. For an N-channel transistor these charge carriers will be electrons. This allows current to flow from the source terminal to the drain terminal. Some generalized relationships are stated below.

$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left[\left(V_g - V_{fb} - 2\psi_B - \frac{V_{ds}}{2} \right) V_{ds} \right] - \mu_{eff} C_{ox} \frac{W}{L} \left[\frac{2}{\sqrt{3} C_{ox}} \sqrt{2\varepsilon^{si} q N^a} \left[(2\psi_B + V_{ds})^{\frac{3}{2}} - (2\psi_B)^{\frac{3}{2}} \right] \right] \quad (1.1)$$

1.2 Creating a New Library in Cadence

Once Cadence has been started the *icfb* window is shown. This is the main window for Cadence; all messages, including error and warning messages, will be displayed in this window.

Figure 1.1: Cadence *icfb* Window with CMOSP35 technology

In order to create a new library select the following menu options:

Tools → Library Manager

From the *Library Manager* window it is possible to access all available libraries and to create new libraries. In order to create a new library:

File → New → Library

This will pop-up a new window where the library name can be specified. In this example we will use the name *mylib*.

Once you have entered the name of the library which is to be created, press *OK*. The next dialog will ask information about the technology file which is to be associated with the new library. For this tutorial we will be using CMOSP35, therefore, select *Attach to existing techfile*: this will bring another dialog window which lets us select which technology file we will use. Select *cmosp35*.

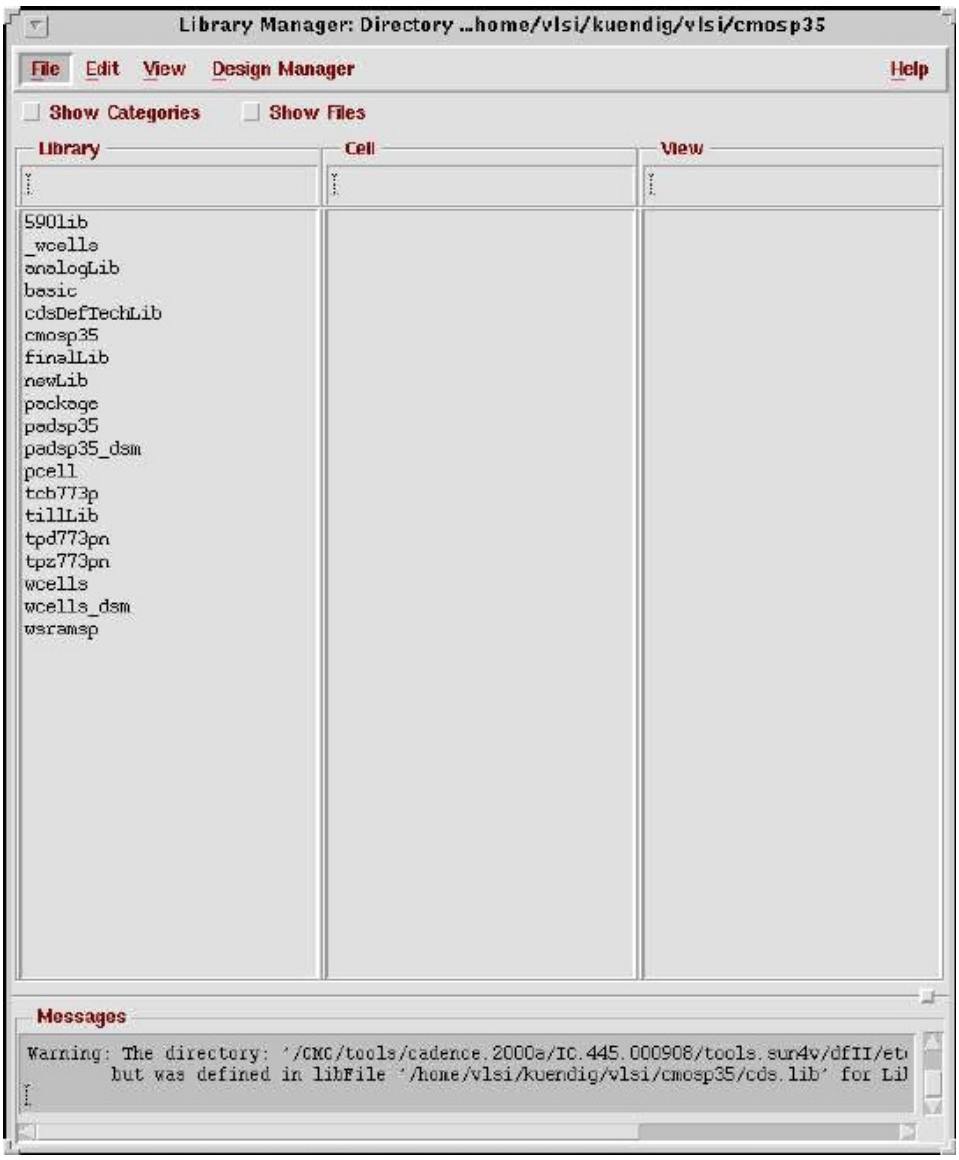


Figure 1.2: Cadence *Library Manager*

Figure 1.3: *New Library* Dialog Window

Figure 1.4: Technology File For New Library Window

Figure 1.5: *Attach Design Library Window*

1.3 Schematic Capture

In this section we will be showing step by step how to enter a circuit schematic into Cadence's *Virtuoso Schematic Editor* and how to create a symbol view for the schematic using the *Virtuoso Symbol Editor*. This section will not give a circuit directly, but rather leave the reader to use some of the schematics presented later in the document (Section 1.4 is a good starting circuit for a novice user).

In order to create a new *Cell View*, open the *Library Manager* and click on the new library which has been created, followed by:

File → New → Cell View

A dialog window will appear asking for the name of the new *Cell View*: enter *OpAmp*. This will automatically open the schematic capture session.

1.3.1 Virtuoso Schematic Editor

Figure 1.6) is the main window from which all of the schematic capture is performed. Along the left boarder of the window are icon-buttons which allow for easy access to the more common commands. Moving the mouse cursor over these windows will show a *tool-tip* which explains which command is executed with each button. All commands are also available via the menus at the top of the window. Most commands will also have a short-cut key associated with them.

When a schematic is entered the *Insert Instance* but is used (alternatively *Add → Instance* may be used) is used in order to place components into the schematic. We will mostly be using transistors, resistors and capacitors (which are found in the library *cmosp35*) and power supplies and grounds (which are found in the library *analogLib*). If the exact name of the desired cell is not known the *Browse* button may be used to open the *Library Manager* and graphically select the component. Components are connected with *narrow wires* which may also be added via the icon-buttons or the menus.

When an instance of a component is added to a schematic all of the available parameters to the model may be set. These parameters may be changed later using the *Properties* option. Some parameters are mandatory to be entered (e.g. power supply voltage) whereas some parameters will default to certain values if they are not entered. Values may also be set to variables, by entering a string instead of a numeric value, which can be set

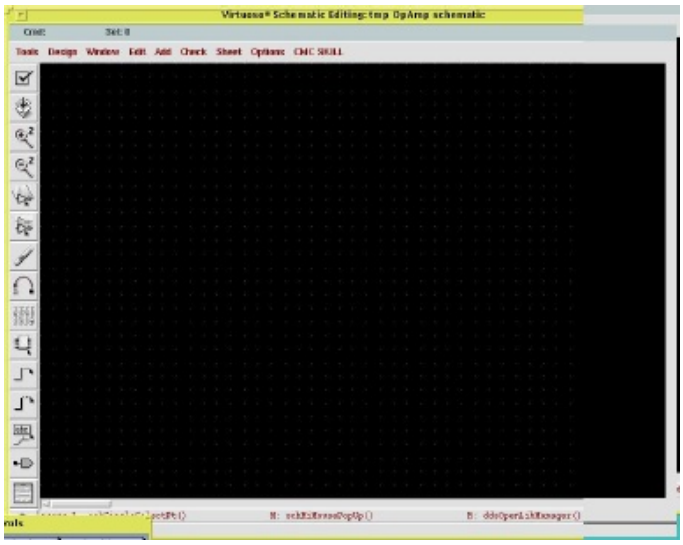


Figure 1.6: Cadence *Virtuoso Schematic Editor*

in the simulation stage.

Once a design has been entered, it can be saved with a *Check and Save* icon-button. This will do a general check of the circuit in order to make sure that all circuits have and ground and that all device terminals are connected to something.

An example of schematics for generating the characteristic curves is shown in Section 1.4. We will not discuss all of the options available for this window since they are very numerous and are mostly self-explanatory.

1.3.2 Virtuoso Symbol Editor

Once the schematic for the circuit is done, a symbol view must be created. This is the view which is used when an instance of the circuit is put into another schematic (e.g. a test bench circuit). Create a "default symbol" by clicking:

Design → Create Cell View → From Cell View

Simply except the defaults and this opens the Symbol Editor. On start-up the symbol editor will have a plain looking rectangle with terminal pins for each I/O pin inserted in the schematic. Once again we will simply accept the defaults and

In order to use the circuit which has been created is it necessary to create a test bench circuit. This test bench circuit is created similarly to the original circuit, except that no symbol is generally required. The symbol of the newly created circuit may be inserted as any other sub-circuit.

1.3.3 Affirma Analog Circuit Design Environment

Once a test bench circuit has been created and saved it is possible to start the simulation environment:

Tools → Analog Environment

The *Affirma* window, figure 1.7, is the window from which all simulations are configured and executed.

Figure 1.7: *Affirma Analog Environment Simulation Window*

In order to run a simulation there are several things which must be defined:

- Selecting a simulator. The Avant Star-HSPICE simulator is the best simulator available; in order to select the simulator: *Setup → Simulator*. In the dialog window which appears change the simulator selection to *hspiceS*; click OK. It is also important to define the environment for the simulator so that all of the correct models files are used by the simulator: *Setup → Environment*. The dialog box which appears contains a field entitled *Include File*. Set this field to */CMC/kits/cmosp35/models/hspice/icdhspice.init*,click OK.

- Setting variables from the schematic. If there are any parameter settings which are set to variables, these variables must be copied from the cell view to the analog environment: *Variables → Copy From Cell view*. All variables which appear in the cell view will now be listed in the bottom left of the *Affirma* window. By double-clicking the variables it is possible to change the value of the variable for the next simulation run. All variables must be assigned values before a simulation may be performed.

- Selecting and configuring the simulations. There are several types of simulations which may be performed at the same time. In order to choose the simulation settings: *Simulation* → *Choose*. Most of the parameters available in the simulation settings are relatively straight forward and are left to the reader to lookup.
- Selecting which variables are saved/plotted from the simulation. The last step required to run a simulation is to set which variables should be plotted and saved. By default not all variables are saved since this could lead to vary large amounts a data being generated by the simulation, this becomes more important for larger designs. In order to plot/save a set of values: *Outputs* → *To Be Plotted* → *Select on Schematic*. This allows the user to click on all nodes (voltages) and device terminals (currents entering/leaving) in the schematic. The schematic should reflect which nodes/terminals have been selected. Once the selection is done press *ESC*.

Simulation may now be started by using the menu system or with the icon-buttons located on the right side of the *Affirma* window.

1.3.4 The Waveform Window

Once the simulation is complete all outputs which were selected to be plotted, will be in *Waveform Window*, Figure 1.8.

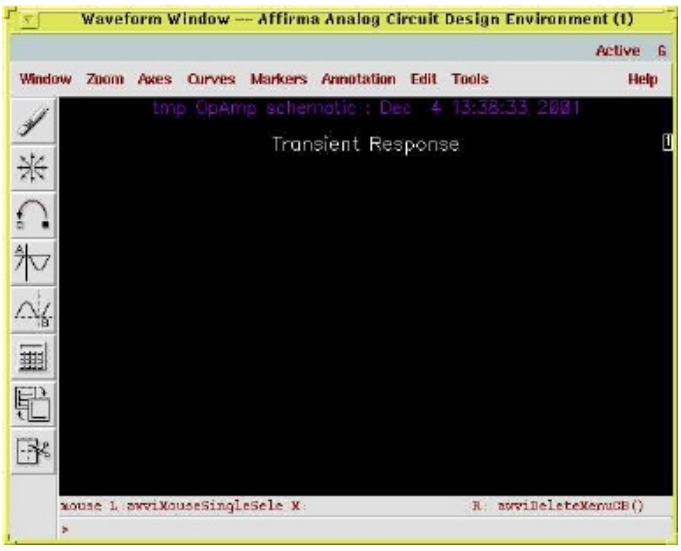


Figure 1.8: *Waveform Window*

The *Waveform Window* allows may customizations in order to generate desired plots; it is possible to add annotations, titles, modify plot ranges & axis and add additional plots. Most of these options are fairly straight

forward and will not be discussed in detail, the reader is encouraged to experiment with the various display options.

One of the more advanced features available from the window is the calculator which is discussed in the next section.

1.3.5 The Cadence Calculator

The Cadence *Calculator* is an extremely powerful tool for analyzing data generated by the simulation. Some of the many features of the *Calculator* are: basic arithmetic operations on waveforms, Discrete Fourier Transforms, Total Harmonic Distortion analysis, and many more.

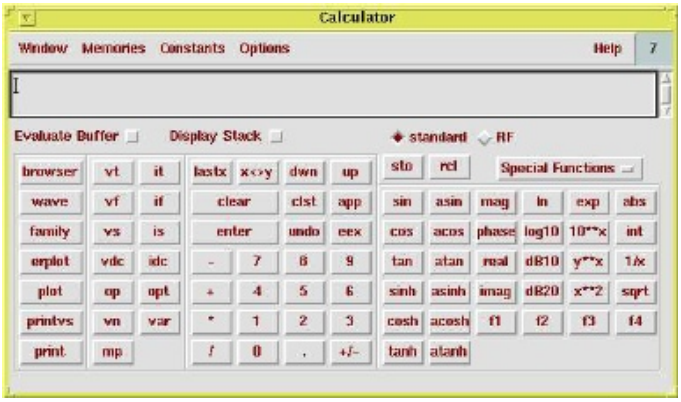


Figure 1.9: Cadence *Calculator*

The calculator allows entry of waveform information by a variety of ways. One way of easily accessing the data is to use the *wave* button and followed by selecting one of the waveform's displayed in the *waveform window*. If the simulation contains a larger number of simulated values than the *browser* button may be employed to browse through all of the information stored from the simulation.

The order in which operations are entered into the calculator may be counter intuitive to new users: The calculator uses a Postfix notation. The table below shows some examples of the default order of operations:

$a + b$	$a,\ b,\ +$
$a * b + c$	$a,\ b,\ *, c, +$
$\sin a + \cos b$	$b,\ cos,\ a,\ sin,\ +$

In the above table each letter represents one expression/waveform from the simulation. The *display stack* options is useful for evaluating large expressions. In order to learn more about the many functions available in the calculator the reader should refer to the Cadence documentation.

1.4 Generating the Characteristic MOSFET Curves

The enhancement-type MOSFET (Metal-Oxide Semiconductor Field-Effect Transistor) is the most widely used field-effect transistor in the FET family, which significance is on par with that of the bipolar junction transistor, with each having its own areas of application. The current-control mechanism is based on an electric field established by the voltage applied to the control terminal. And the current is conducted by only type of carrier(electrons or holes) depending on the type of FET (N channel or P channel).

1.4.1 N-channel Enhancement-Type MOSFET

The transistor is fabricated on a P-type substrate, which is a single-crystal silicon wafer that provides physical support for the device. Two heavily doped n-type regions, the source and the drain regions, are created in the substrate. A thin (about 0.1um) layer of silicon dioxide(SiO2) is grown on the surface of the substrate, covering the area between the source the drain regions. Metal is deposited on top of the oxide layer to form the gate electrode of the device. Metal contacts are also made to the source region, the drain region,and the substrate, also known as the body. Thus, four terminals are brought out: the Gate(G), the Source(S), the Drain(D), and the Body(B).

Observe that the substrate forms PN junctions with the source and drain regions. In normal operation these PN junctions are kept reverse-biased at all time. Since the drain will be at a positive voltage relative to the source, the two PN junctions can be effectively cut off by simply connecting the substrate terminal to the source terminal.Here, the substrate will be considered as having no effect on device operation, and the MOSFET will be treated as a 3-terminal device, with the terminals being the gate(G), the source(S), and the drain(D). We applied a voltage to the gate controls current flow between source and drain. This current will flow in the longitudinal direction from drain to source in the region called "channel region". Note that this region has a length L and a width W, two important parameters of the MOSFET. Typically, L is in the range 1 to 10 μm, and W is in the range 2 to 500 μm.

The operation with V_{ds}

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source. They prevent current conduction from drain to source when a voltage V_{ds} is applied. In fact, the path between drain and source has a very high resistance (of the order of 10^{12} Ω)

With a positive voltage, which exceed the threshold voltage V_t, applied to the gate, the transistor induced a n-channel. When applying a positive voltage V_{ds} between drain and source, as shown in the figure below,

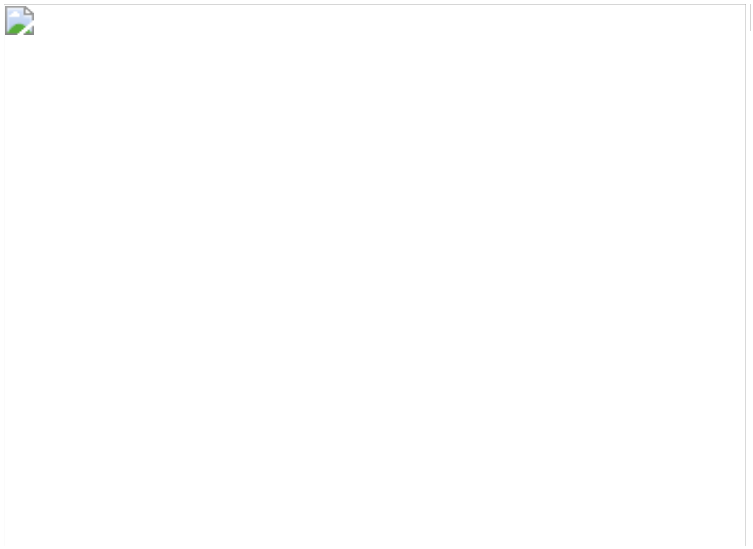


Figure 1.10: N-Channel Test Circuit

The voltage V_{ds} cause a current i_D to flow through the induced N channel. Current is carried by free electrons travelling from source to drain. The magnitude of i_D depends on the density of electrons in the channel, which in turn depends on the magnitude of V_{GS}. As V_{GS} exceeds V_t, more electrons are attracted into the channel. We may visualize the increase in charge carriers in the channel as an increase in the channel depth. The result is a channel of increased conductance or equivalently reduced resistance.

Let V_{GS} be held constant at a value greater than V_t (for example 2V), and increase the V_{DS} from 0 to 3.3V. As V_{DS} is increased, the $I_D - V_{DS}$ curve is shown in

Eventually, when V_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t, that is :

$$V_{GS} - V_{DS} = V_t$$

or

$$V_{DS} = V_{GS} - V_t$$

the channel depth at the drain end decreases to almost zero, and the channel is said to be pinched off. Increase V_{DS} beyond this value has little effect (theoretically, no effect) on the channel shape, and the current through the channel remain constant at the value reached for $V_{DS} = V_{GS} - V_t$. The drain current thus saturates at this value, and the MOSFET is said to

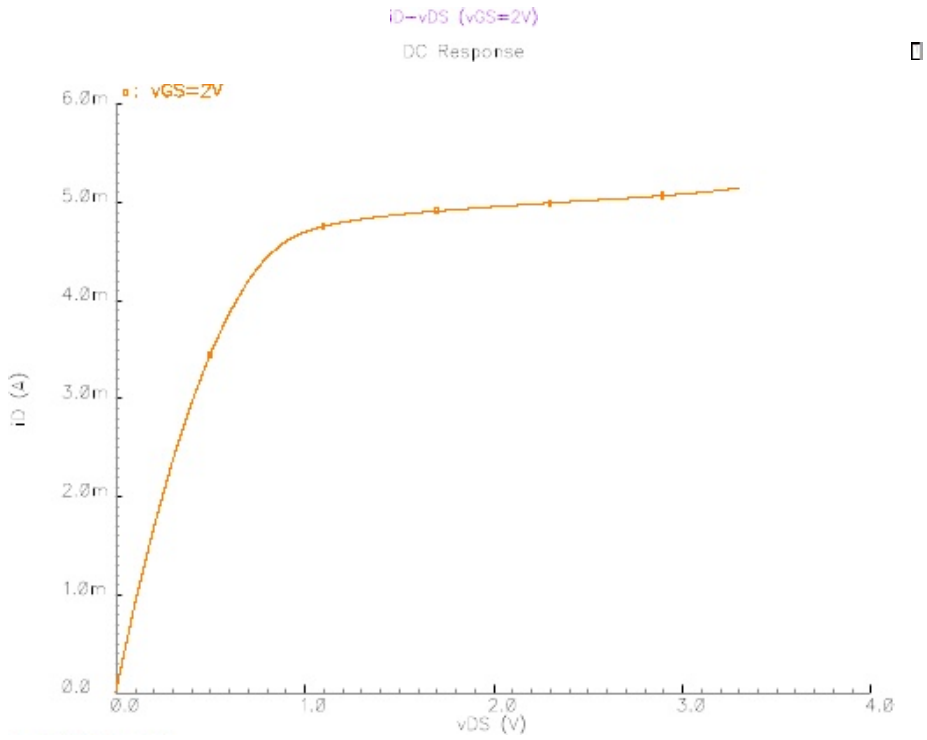


Figure 1.11: $I_D - V_{DS}$ Curve

have entered the saturation region of operation. The voltage V_{DS} at which saturation occurs is named $V^{DS,sat}$

$$V_{DS,sat} = V_{GS} - V_t$$

Obviously, for every value of $V_{GS} \geq V_t$, there is a corresponding value of $V_{DS,sat}$. The device operates in the saturation region if $V_{DS} \geq V_{DS,sat}$. The region of the $I_D - V_{DS}$ characteristic obtained for $V_{DS} < V_{DS}$,sat is called the triode region.

The $I^D - V^{DS}$ Characteristics

The Figure above shows a typical set of $I_D - V_{DS}$ characteristics, which are a family of curves, each measured at a constant V_{GS}. We can see that there are three distinct regions of operation: the cutoff region, the triode region, and the saturation region. The saturation region is used if the FET is to operate as a amplifier. For operation as a switch, the cutoff and triode regions are utilized.

1. Triode

   If $V_{GS} > V_t$ and $V_{DS} \leq V_{GS} - V_t$, then the n-channel is continuous all the way from S to D. The S and D are connected by a conductor (or a resistor) of a given resistance. The drain current increases if the voltage drop between S and D increases. The channel resistance

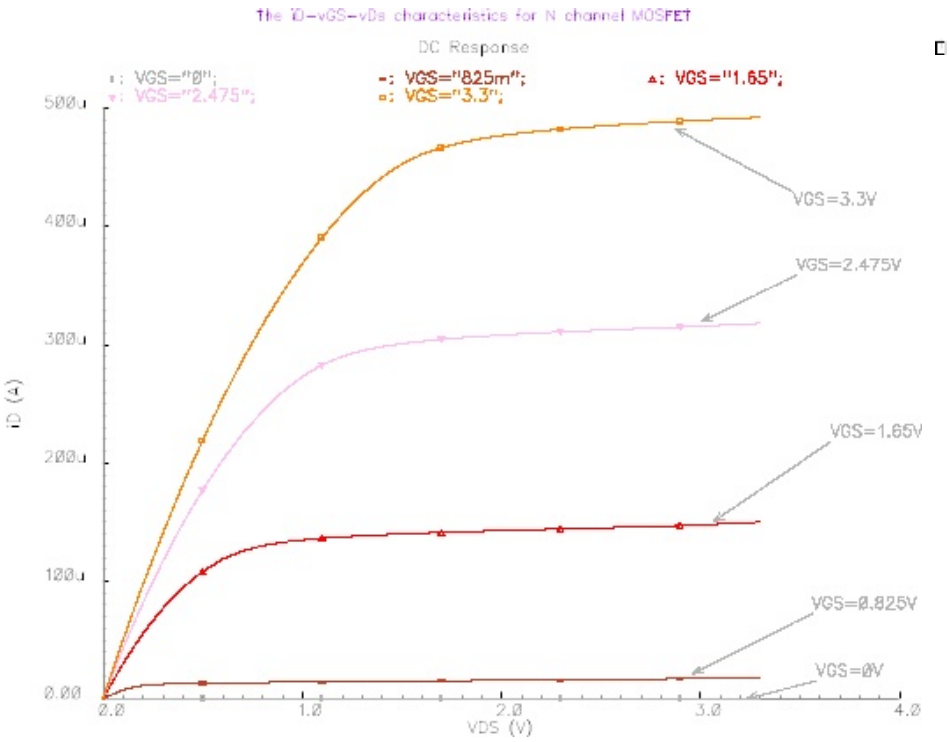


Figure 1.12: $I_D - V_{DS}$ Curve

depends on how much charge is injected at the S-end, which in turn is controlled by v_{GS}. The Drain current I_d depends on both v_{GS} and V_{GD} (or V_{DS}). The $I_D - V_{DS}$ characteristics can be approximately described by the relationship

$$I_D = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS} \cdot V_{DS}\right] \tag{1.2}$$

in which K is a device parameter given by

$$K = 0.5U_n \quad C_{ox} \quad \frac{W}{L} \quad \frac{A}{V^2} \tag{1.3}$$

U_n physical constant known as the electron mobility(its value in this case applies for the electrons in the induced n channel)

C_{ox} oxide capacitance, the capacitance per unit area of the gate-to-body capacitor for which the oxide layer serves as dielectric.

L,W the length and the width of the channel.

Since for a given fabrication process the quantity ($0.5U_n$*C_{ox}) is a constant, approximately $10\mu A/V^2$ for the standard NMOS process with a $0.1\mu m$ oxide thickness. So the aspect ratio of $\frac{W}{L}$ determines its conductivity parameter K.

If V_{DS} is sufficiently small so that we can neglect the $V_{DS} \cdot V_{DS}$ in equation 1.2, then the $I_D - V_{DS}$ characteristics near the origin the relationship

$$I_D \cong 2K(V_{GS} - V_t)V_{DS} \tag{1.4}$$

This linear relationship represents the operation of the MOS transistor as a linear resistance R_{DS}

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{2K(V_{GS} - V_t)} \tag{1.5}$$

2. Saturation

If $V_{GS} \geq V_t$ and $V_{DS} \geq V_{GS} - V_t$, then N-channel is induced at the S-end, but the channel is depleted at the D-end. That is, the N-channel is pinched off at the Drain-end. Increasing V_{ds} beyond $V_{ds-(sat)}$, or equivalently decreasing V_{GD} below V_t, creates a fully depleted region between the inversion n-channel and the drain region. An electric field is set up in this region, pointing from the Drain region toward the inversion channel. Carrier electrons in the N-channel that reach the depletion boundary are swept across the depletion region into the Drain. This is similar to PN junction diode where the minority carrier electrons of the P-side are swept to the n-side by the built-in field whenever they reach the depletion boundary. Once the drain-end of channel is pinched off, the current no longer depends on the voltage apply between S and D.

The boundary between the triode region and the saturation region is characterized by

$$V_{DS} = V_{GS} \quad V_t \tag{1.6}$$

Substituting it into Equation 1.2 gives the saturation value of the current I_D is

$$I_D = K(V_{GS} - V_t) \cdot (V_{GS} - V_t) \tag{1.7}$$

Thus in saturation the MOSFET provides a drain current whose value is independent of the drain voltage V_{DS} and is determined by the gate voltage V_{GS} according to the square-law relationship.

The complete independence of I^D on V^{DS} in saturation and the corresponding infinite output resistance at the drain is an idealization based on the premise that once the channel is pinched off at the drain end, further increases in V_{DS} have no effect on the channel's shape. In practice, increasing V_{DS} beyond v_{DS},sat does affect the channel somewhat.

Specifically, as V_{DS} is increased, the channel pinch-off point is moved slightly away from the drain toward the source. Thus the effective channel is reduced, a phenomenon called channel-length modulation. Since the channel resistance is proportional to the channel length, the channel resistance is decreased. This results in the slight increase of the drain current beyond the saturation level. Now since K is inversely proportional to the channel length (Equation 1.3), so, K and, correspondingly, I_D, increases with V_{DS}. Mathematically, the channel length modulation introduces a V_{DS}-dependent term in I_D:

$$I_D = K(V_{GS} - V_t)(V_{GS} - V_t)(1 + \lambda \cdot V_{DS}) \tag{1.8}$$

λ the channel-length modulation parameter:$0.005 < \lambda < 0.03$
From Fig.nid.ps we extrapolated the straight-line $I_D - V_{DS}$ characteristics in saturation, intercept the V_{DS}-axis at the point $V_{DS} = \frac{-1}{\lambda} = -V_A$. So v_A is in the range 200 to 30 volts. It should be obvious that channel-length modulation makes the output resistance in saturation finite. Let the output resistance Rout as

$$R_{out} = \frac{1}{\lambda \cdot K(V^{GS} - V^t) \cdot (V^{GS} - V^t)} \qquad V_{GS} = constant \tag{1.9}$$

approximated by

$$R_{out} \cong \frac{1}{\lambda \cdot I_D} \tag{1.10}$$

substituted by $\lambda = \frac{1}{V_A}$

$$R_{out} \cong \frac{V_A}{I_D} \tag{1.11}$$

Thus the output resistance is inversely proportional to the DC bias current I_D.

3. Cutoff

   If $V_{GS} < V_t$ (and of course, $V_{GD} < V_t$), then the no n-channel is present and no current flows.

1.4.2 P-channel Enhancement-Type MOSFET

A P-channel enhancement-type MOSFET (PMOS transistor) is fabricated on an N-type substrate with p+ regions for the drain and the source, and holes as charge carriers. The device operates in the same manner as the N-channel device except the V_{GS} and V_{DS} are negative and the threshold

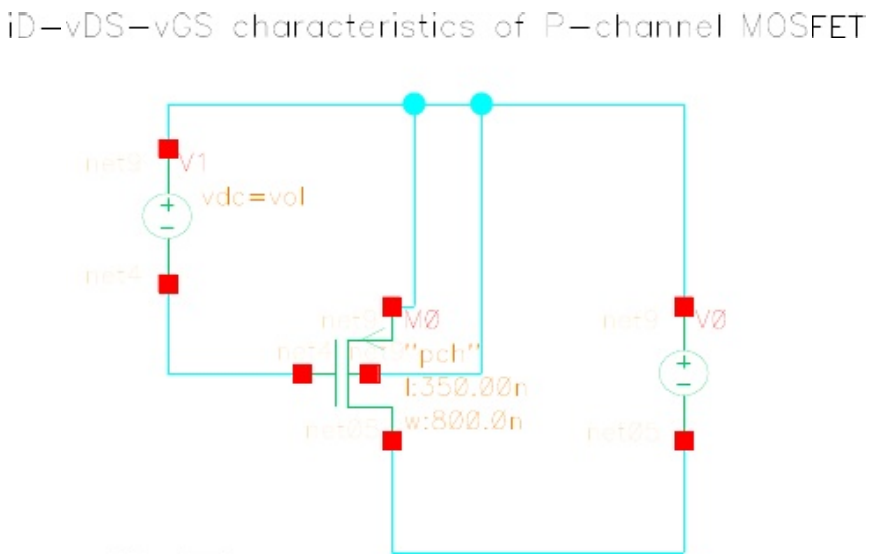


Figure 1.13: P-Channel Test Circuit

voltage V_t is negative. Also the current i_D enters the source terminal and leaves through the drain terminal.

To induce a channel we apply a gate voltage that is more negative than V_t, and apply a drain voltage that is more negative than the source voltage (i.e. V_{DS} is negative or, equivalently, v_{SD} is positive). The current i_D is given by the same equation as for NMOS, and the K is given by

$$K = 0.5 \cdot U_p \cdot C_{ox} \left(\frac{W}{L} \right) \tag{1.12}$$

where Up is the mobility of holes in the induced p channel. Typically, $Up \simeq 0.5U_n$, with the result that for the same W/L ratio a PMOS transistor has half the value of K as the NMOS device.

The $I_D - V_{DS}$ characteristics is shown above. The current I_D is given by the same equation used for NMOS.

$$I_D = K(V_{GS} - V_t)(V_{GS} - V_t)(1 + \lambda \cdot V_{DS})$$

where V^{GS}, V^t, λ, and V^{DS} are all negative.

PMOS technology was originally the dominant one. However, because NMOS devices can be made smaller and thus operate faster, and because NMOS requires lower supply voltages than PMOS, NMOS technology has virtually replaced PMOS. Nevertheless, it is important to develop the PMOS

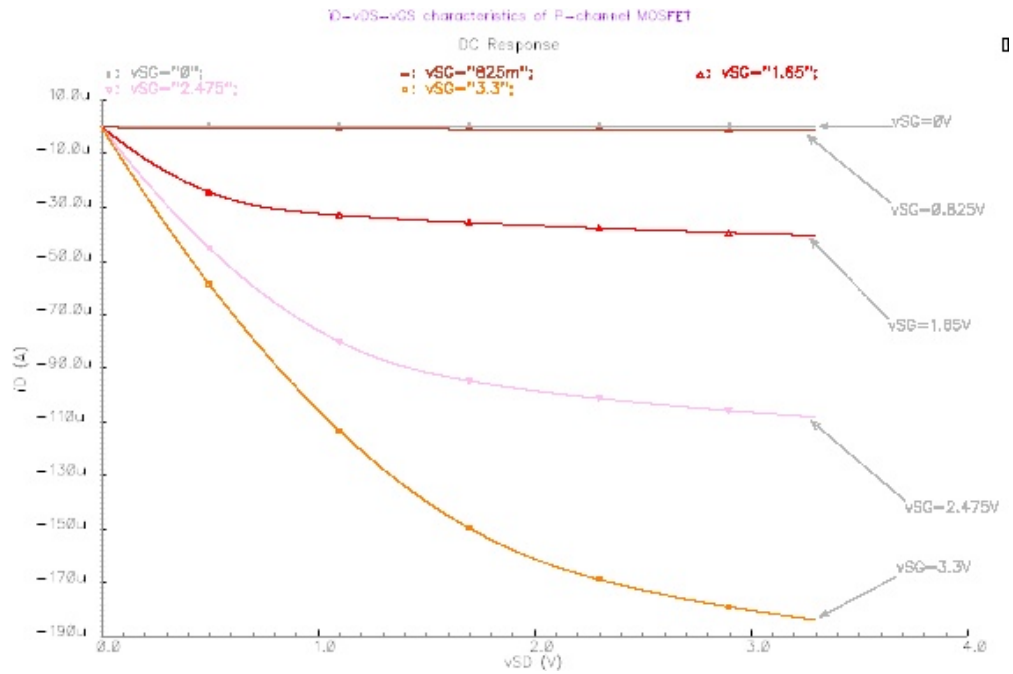


Figure 1.14: $I_D - V_{DS}$ Curve

transistor for two reasons: PMOS devices are still available for discrete-circuit design, and more importantly, both PMOS and NMOS transistors are utilized in CMOS circuits!

Chapter 2

An Introduction to Op-Amps

2.1 Parameters of an Op-Amp

This section will discuss Op-Amp parameters. The designer of an Op-Amp must have a clear understanding of what Op-Amp parameters mean and their impact on circuit design. The selection of any Op-Amp must be based on an understanding of what particular parameters are most important to the application. In the next section, we will discuss the method of measurement of these different parameters.

2.1.1 Offset Voltage

All Op-Amps require a small voltage between their inverting and noninverting inputs to balance mismatches due to unavoidable process variations. The required voltage is known as the input offset voltage and is abbreviated V_{os}. V_{os} is normally modelled as a voltage source driving the noninverting input. Generally, Bipolar input Op-Amps typically offer better offset parameters than JFET or CMOS input Op-Amps. There are two other parameters related to and affect V_{os}: the average temperature coefficient of input offset voltage, and the input offset voltage long-term drift. The average temperature coefficient of input offset voltage, a V_{os}, specifies the expected input offset drift over temperature. Its units is $\left[\frac{mV}{^oC}\right]$. V_{os} is measured at the temperature extremes of the part, and a V_{os} is computed as $\frac{V_{os}}{^oC}$. Normal aging in semiconductors causes changes in the characteristics of devices. The input offset voltage long-term drift specifies how V_{os} is expected to change with time. Its units are $\frac{mV}{month}$. Input offset voltage is of concern anytime that DC accuracy is required of the circuit. One way to null the offset is to use external null inputs on a single Op-Amp package (2.1). A potentiometer is

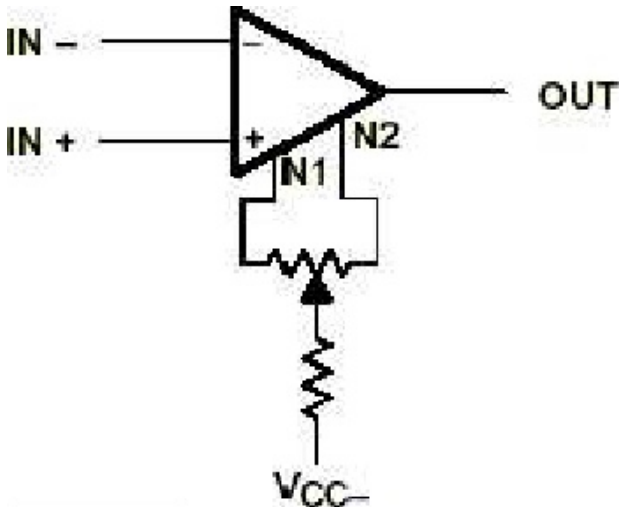


Figure 2.1: Offset Voltage Adjust

connected between the null inputs with the adjustable terminal connected to the negative supply through a series resistor. The input offset voltage is nulled by shorting the inputs and adjusting the potentiometer until the output is zero. However, even if the V_{os} is nulled at the beginning, it will change with temperature and some other conditions.

2.1.2 Input Current

The input circuitry of all Op-Amps requires a certain amount of bias current for proper operation. The input bias current, I_{IB}, is computed as the average of the two inputs:

$$I_{IB} = \frac{(I_N + I_P)}{2} \tag{2.1}$$

CMOS and JFET inputs offer much lower input current than standard bipolar inputs. The difference between the bias currents at the inverting and noninverting inputs is called the input offset current, $I_{os} = I_N + I_P$. Offset current is typically an order of magnitude less than bias current.

Input bias current is of concern when the source impedance is high. If the Op-Amp has high input bias current, it will load the source and a lower than expected voltage is seen. The best solution is to use an Op-Amp with either CMOS or JFET input. The source impedance can also be lowered by using a buffer stage to drive the Op-Amp that has high input bias current.

In the case of bipolar inputs, offset current can be nullified by matching the impedance seen at the inputs. In the case of CMOS or JFET inputs, the offset current is usually not an issue and matching the impedance is not necessary. The average temperature coefficient of input offset current,

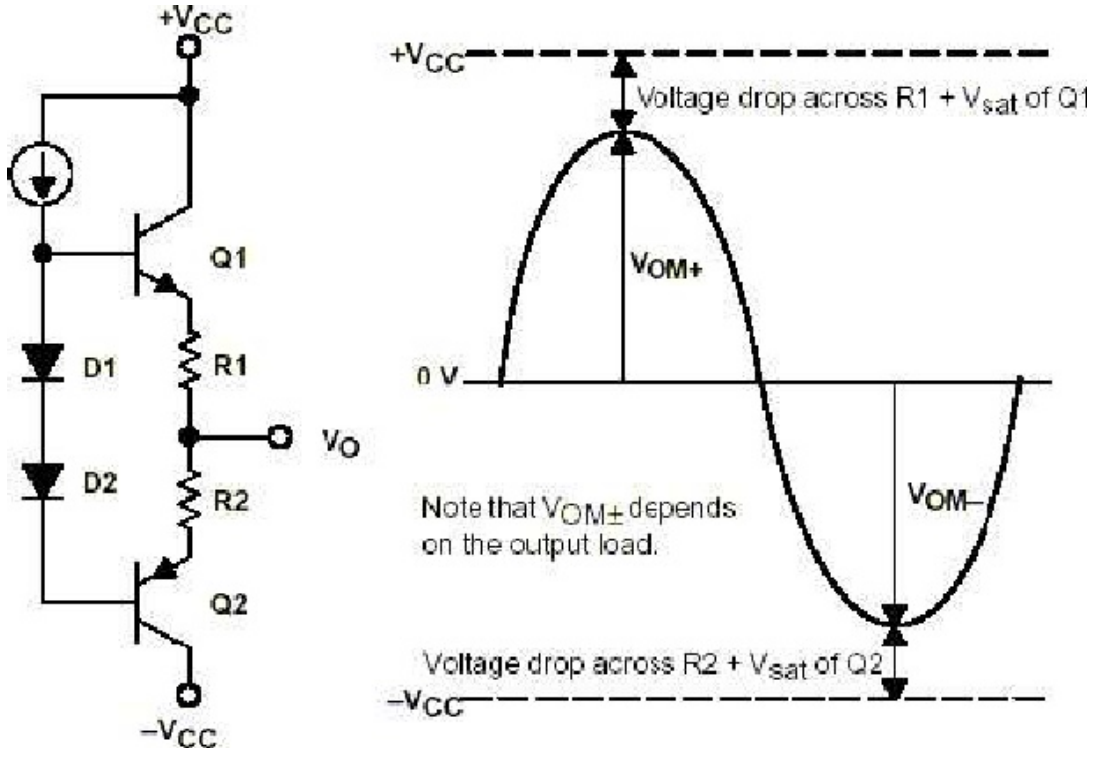


Figure 2.2: Output Voltage Swing

I_{os}, specifies the expected input offset drift over temperature. Its units are $\frac{mA}{^oC}$.

[ ]

2.1.3 Input Common Mode Voltage Range

The input common voltage is defined as the average voltage at the inverting and noninverting input pins. If the common mode voltage gets too high or too low, the inputs will shut down and proper operation ceases. The common mode input voltage range, VICR, specifies the range over which normal operation is guaranteed. For instance, Rail to rail input Op-Amps use complementary N and P channel devices in the differential inputs. When the common-mode input voltage nears either rail, at least one of the differential inputs is still active, and the common-mode input voltage range includes both power rails.

2.1.4 Maximum Output Voltage Swing

The maximum output voltage, V_{OM}, is defined as the maximum positive or negative peak output voltage that can be obtained without waveform clipping, when quiescent DC output voltage is zero. V_{OM} is limited by the output impedance of the amplifier, the saturation voltage of the output transistors, and the power supply voltages. This is shown pictorially in 2.2.

This emitter follower structure cannot drive the output voltage to either rail. Rail-to-rail output Op-Amps use a common emitter (bipolar) or common source (CMOS) output stage. With these structures, the output voltage swing is only limited by the saturation voltage (bipolar) or the on resistance (CMOS) of the output transistors, and the load being driven.

2.1.5 Output Impedance

Different data sheets list the output impedance under two different conditions. Some data sheets list closed-loop output impedance while others list open-loop output impedance, both designated by Z_o. Z_o is defined as the small signal impedance between the output terminal and ground. Generally, values run from 50 to 200Ω .

Common emitter (bipolar) and common source (CMOS) output stages used in rail-to-rail output Op-Amps have higher output impedance than emitter follower output stages. Output impedance is a design issue when using rail-to-rail output Op-Amps to drive small resistive or large capacitive loads. If the load is mainly resistive, the output impedance will limit how close to the rails the output can go. If the load is capacitive, the extra phase shift will erode phase margin. 2.3 shows how output impedance affects the output signal assuming Z^o is mostly resistive.

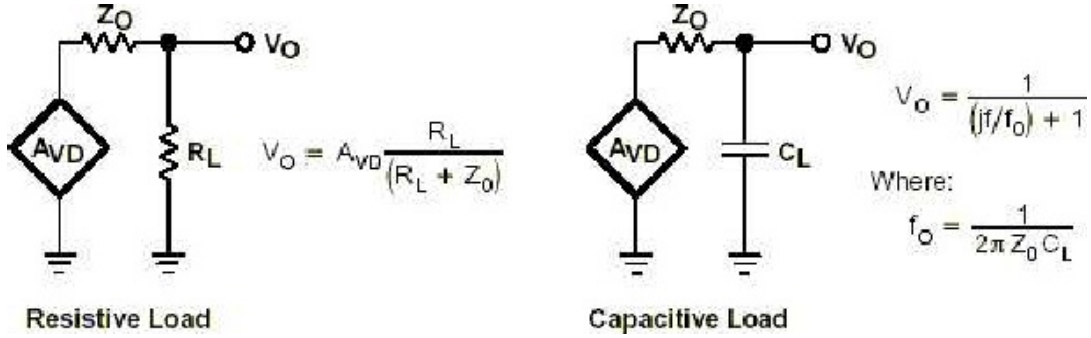


Figure 2.3: Effect of Output Impedance

2.1.6 Common-Mode Rejection Ratio

Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, $\frac{A^{dif}}{A_{com}}$. Ideally this ratio would be infinite with common mode voltages being totally rejected.

The common-mode input voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry,

changing the bias point changes the offset voltage, which, in turn, changes the output voltage.

2.1.7 Supply Voltage Rejection Ratio

Supply voltage rejection ratio, kSVR (AKA power supply rejection ratio, PSRR), is the ratio of power supply voltage change to output voltage change.

The power voltage affects the bias point of the input differential pair. Because of the inherent mismatches in the input circuitry, changing the bias point changes the offset voltage, which, in turn, changes the output voltage.

For a dual supply Op-Amp, $KSVR = \frac{VCC}{VOS}$ or $KSVR = \frac{V_{DD}}{VOS}$. The term V_{CC} means that the plus and minus power supplies are changed symmetrically. For a single supply Op-Amp, $KSVR = \frac{VCC}{VOS}$ or $KSVR = \frac{V_{DD}}{VOS}$. Also note that the mechanism that produces kSVR is the same as for CMRR. Therefore kSVR as published in the data sheet is a DC parameter like CMRR. When kSVR is graphed vs. frequency, it falls off as the frequency increases.

2.1.8 Slew Rate

Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/ms or V/ms. 2.4 shows slew rate graphically.

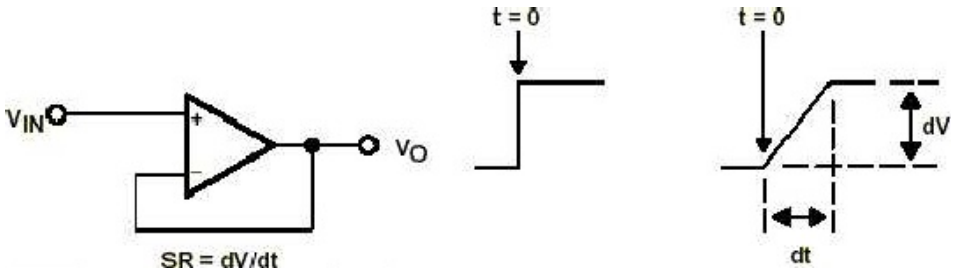


Figure 2.4: Slew Rate

The primary factor controlling slew rate in most amps is an internal compensation capacitor CC, which is added to make the Op-Amp unity gain stable. Referring to 2.5, voltage change in the second stage is limited by the charging and discharging of the compensation capacitor CC. The maximum rate of change is when either side of the differential pair is conducting 2IE. Essentially $SR = \frac{2IE}{CC}$. However, that not all Op-Amps have compensation capacitors. In Op-Amps without internal compensation capacitors, the slew rate is determined by internal Op-Amp parasitic capacitances. Uncompensated Op-Amps have greater bandwidth and slew rate, but the designer must ensure the stability of the circuit.

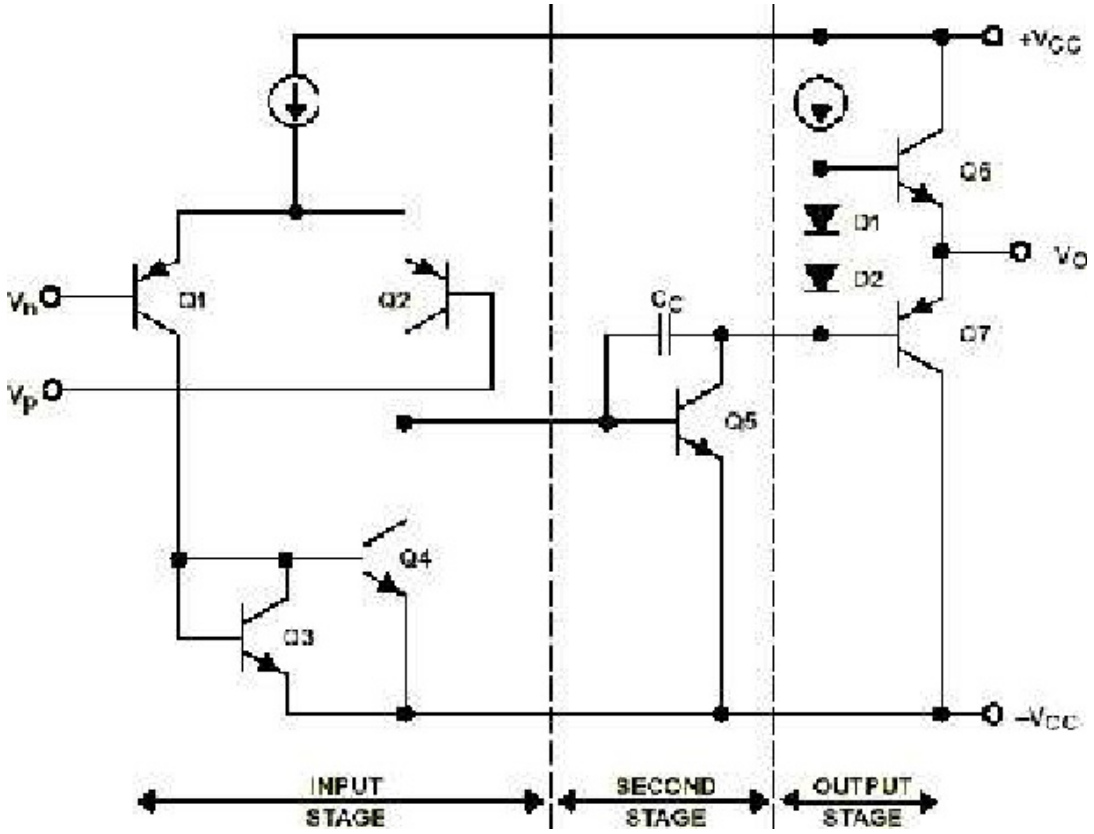


Figure 2.5: Op amp schematic simplified

In Op-Amps, power consumption is traded for noise and speed. In order to increase slew rate, the bias currents within the Op-Amp are increased.

2.1.9 Unity Gain Bandwidth and Phase Margin

Unity-gain bandwidth (B1) and gain bandwidth product (GBW) are very similar. B1 specifies the frequency at which A_{VD} of the Op-Amp is 1. GBW specifies the gain-bandwidth product of the Op-Amp in an open loop

configuration and the output loaded:

$$GBW = AVD \cdot f \tag{2.2}$$

Phase margin at unity gain (fm) is the difference between the amount of phase shift a signal experiences through the Op-Amp at unity gain and 180^o:

$$fm = 180^o - f@B1 \tag{2.3}$$

Gain margin is the difference between unity gain and the gain at 180^o phase shift:

$$Gain\ margin = 1 - Gain@180^o\ phase\ shift \tag{2.4}$$

In order to make the Op-Amp stable, a capacitor, C_C, is purposely fabricated on chip in the second stage (2.5). This type of frequency compensation is

termed dominant pole compensation. The idea is to cause the open-loop gain of the Op-Amp to roll off to unity before the output phase shifts by 180^o. 2.5 is very simplified, and there are other frequency shaping elements within a real Op-Amp. 2.6 shows a typical gain vs. frequency plot for an internally compensated Op-Amp.

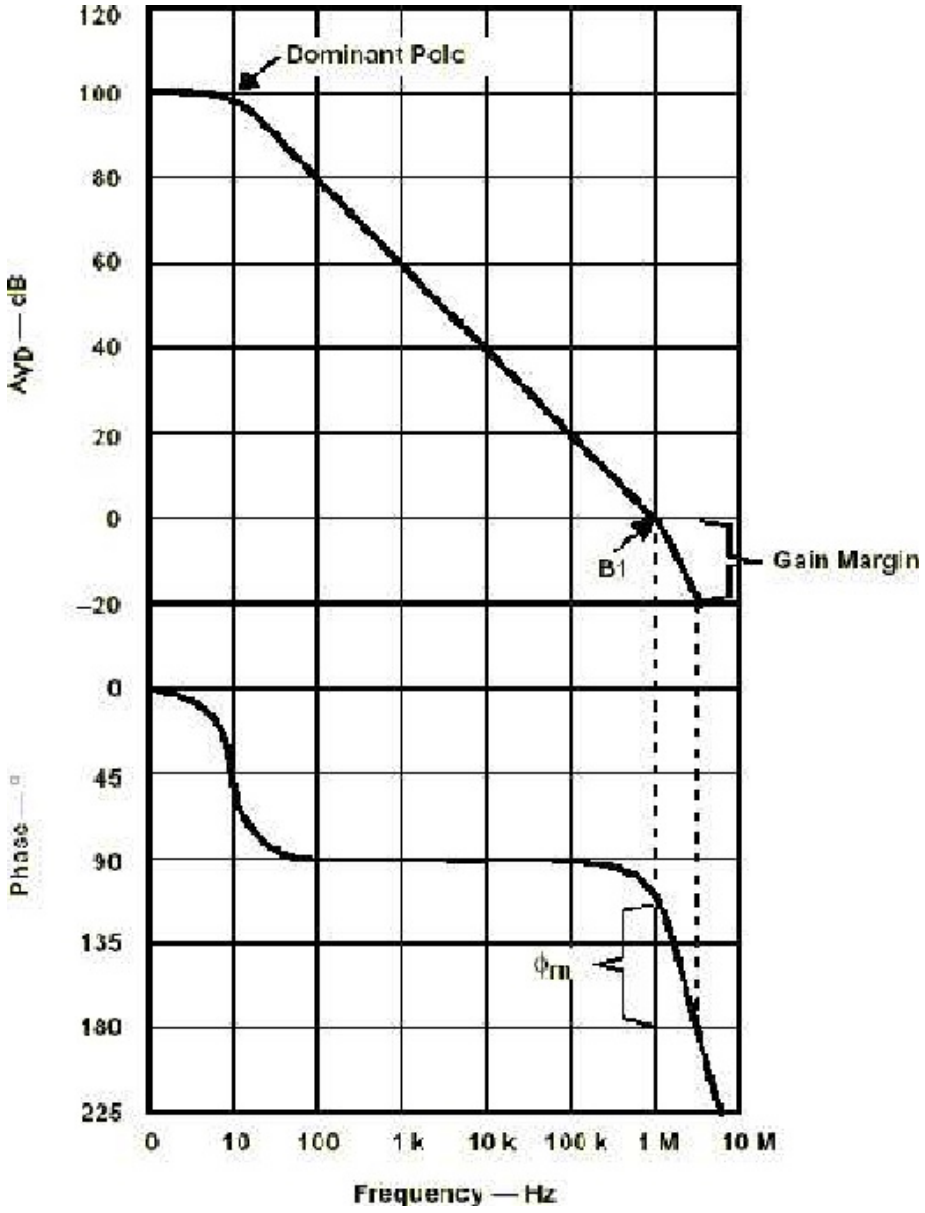


Figure 2.6: Voltage Amplification and Phase Shift vs. Frequency

Phase margin and gain margin are different ways of specifying the stability of the circuit. Since rail-to-rail output Op-Amps have higher output impedance, a significant phase shift is seen when driving capacitive loads. This extra phase shift erodes the phase margin, and for this reason most CMOS Op-Amps with rail-to-rail outputs have limited ability to drive capacitive loads.

2.1.10 Settling Time

It takes a finite time for a signal to propagate through the internal circuitry of an Op-Amp. Therefore, it takes a period of time for the output to react to a step change in the input. In addition, the output normally overshoots the target value, experiences damped oscillation, and settles to a final value. Settling time, t_s, is the time required for the output voltage to settle to within a specified percentage of the final value given a step input. Settling time is a design issue in data acquisition circuits when signals are changing rapidly.

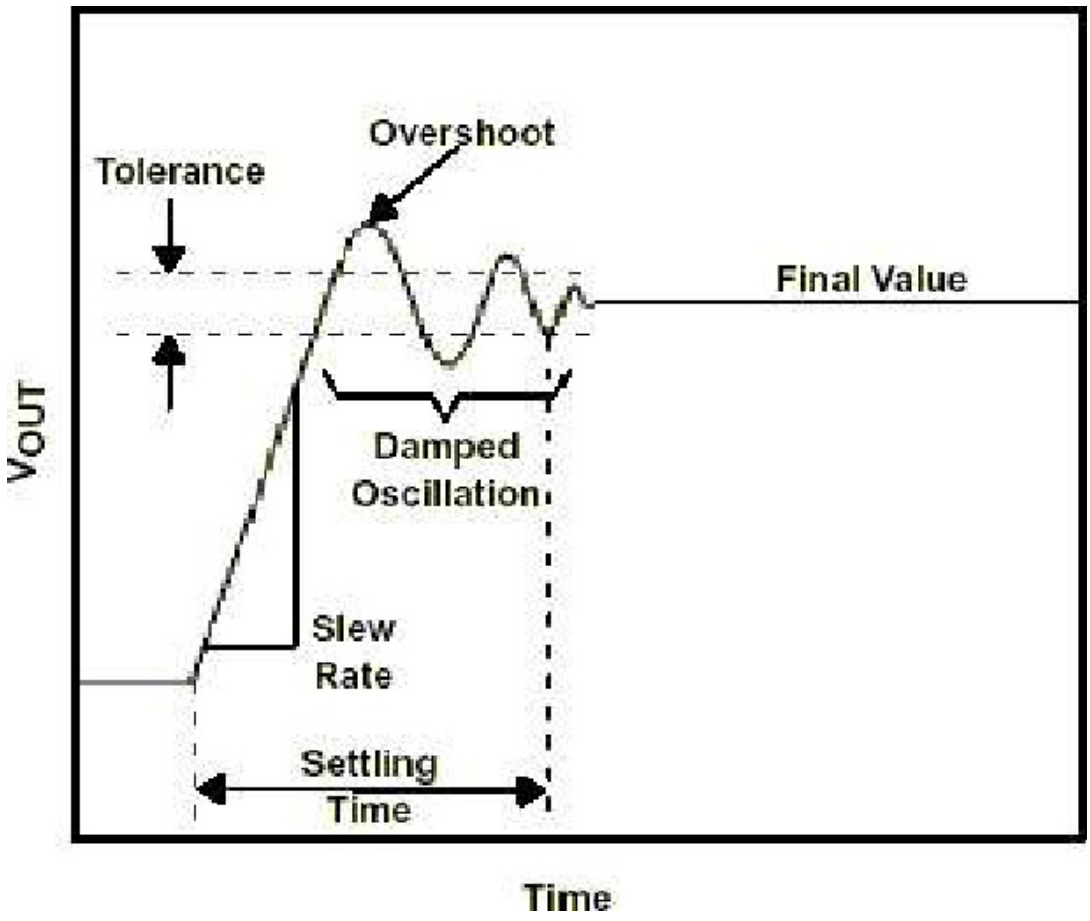


Figure 2.7: Settling Time

2.2 Methodology of Choosing Op-Amp Parameters

The methodology of choosing the parameters of the transistors, and their relationships, then it will be possible to get the desired quiescent point to ensure the ideal wave output.

Here we will to present a method of choosing the parameter in an Op-

Amp circuit, and in the same way we can get a very efficient optimization method. Further more in this way we can learn how to combine different parts of a circuit together, and deal with more complex circuits. First of all we must clarify the relationship among different parameters, then we can finish our job orderly. The quiescent point is very important for our design.

2.3 How to Adjust the Parameters

To simplify the discussion, we will concentrate on the simplest OTA Op-Amp 2.8 and demonstrate how to adjust its parameters to get the proper DC gain. At the same time we try to extend the method to other sophisticated architectures.

2.3.1 Specification

Here we are asked to design an Op-Amp, whose $V_{DD} = 3.3\ V$, $V_{SS} = 0\ V$, input bias voltage = 1.65V (Input $V_0 = 1.65\ V$). Swing of output (Considering the current source V_{DD} will occupy some voltage, the swing should be $0 \rightarrow 3\ V$.)

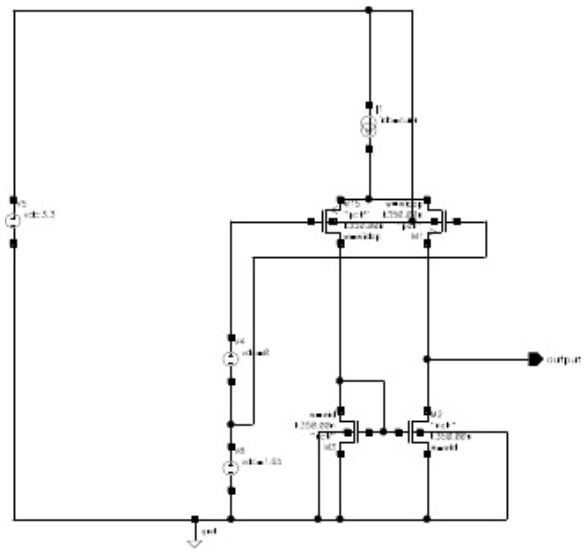


Figure 2.8: Circuit with Default Parameters

2.3.2 Procedure of Optimization

1. Draw a circuit with default parameters.(See Figure 2.8).
2. Adjust the current source value I_0. The current value takes highest priority of all of the parameters, all of the other parameters will be chosen to match the current value.

From the circuit, we know that when the Op-Amp is working in the common mode (which means the $V_1 = V_0 = 1.65\ V$), then the current through the two (2) differential amplifiers is symmetric, so the value of $I_1 = \frac{1}{2} \cdot I_0$. $V_{out} = 1.65\ V$, $V_{ref} = 1.65\ V$, from here we can decide what is the maximum and minimum value we can get through a PMOS. We design a very simple circuit to test the current value from the drain of a PMOS (Figure 2.9). When changing the width of the channel of the PMOS, we can get a set of values of the current value of the drain(Figure 2.10). Considering the width of the active load should not to be too large so we can get better gain. The range of the length should be $400nm \rightarrow 2000\ nm$, then I_1 should be from $86.4366\mu A \quad 800.00\mu A$. So the I_0 should be double I_1 it should be from $170\mu A \rightarrow\rightarrow 1700\mu A$.

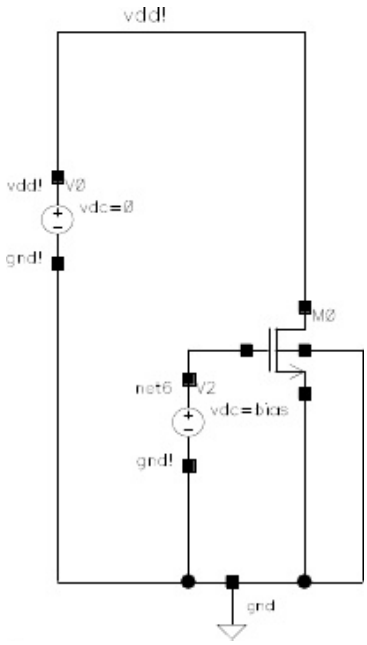


Figure 2.9: Simple Test Circuit for Drain Current

We can choose any value inside the range, so we regard the $400\mu m$ as the initial value of our design.

3. Decide the width of the channel of the active load. From Figure 2.9 we perform a parametric analysis. The value of the width of the channel, through which we can get the proper value for the quiescent point. It is about $1.25\mu m$.

4. We can assign an arbitrary big value to the width of the differential

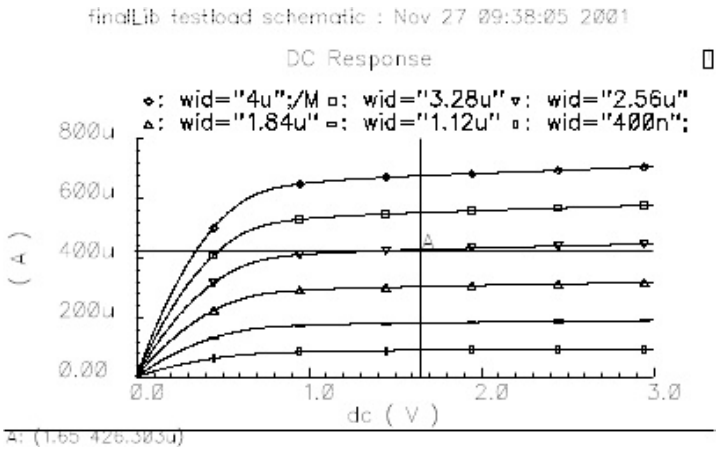


Figure 2.10: Simple Test Circuit - Parametric Analysis of Channel Width

amplifier, suppose we choose a value 5 times bigger than the width of the active load.

5. Do the simulation and compare the gain we get with the gain we want.

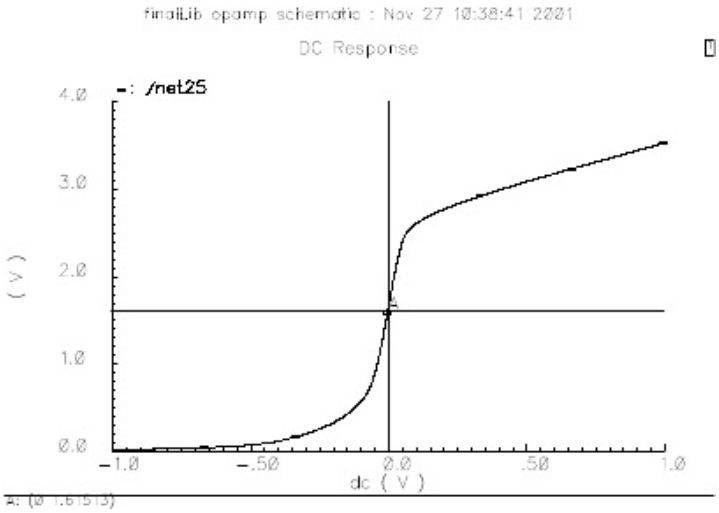


Figure 2.11: Simple Test Circuit - DC Response/Gain

2.3.3 Optimize the Parameters of the Op-Amp

1. According to the gain of the specification, decide the width of the differential amplifier.

$$G_m = \left(2K_n' I_0 \cdot \left(\frac{W}{L}\right)\right)^{\frac{1}{2}}$$

$$R_{out} = V_e \frac{L_1}{I_0}$$

$$A_V = G_m R_{out} = V_e \left(2K'_n \frac{W_1 L_1}{I_0} \right)^{frac12}$$

There are three (3) variables that will affect A_V, W, L and I_0.

If there is small difference between the two (2) gains, then what we need to do is just to adjust the value of the length and the width of the channel of differential amplifier, otherwise we must reduce the I_0.

2. Reduce I_0; according to the fabricating technology, the width of the channel of the transistor cannot be less than $350\mu\ m$, which means we cannot reduce the I_0 less than $170\mu A$. As mentioned above, otherwise the quiescent point cannot be at the middle of the curve. (See Figure 2.12), this will distort the input waveform. Each time I_0 is adjusted the width of the active load should be changed accordingly. Thus another way to adjust I_0 must be devised.

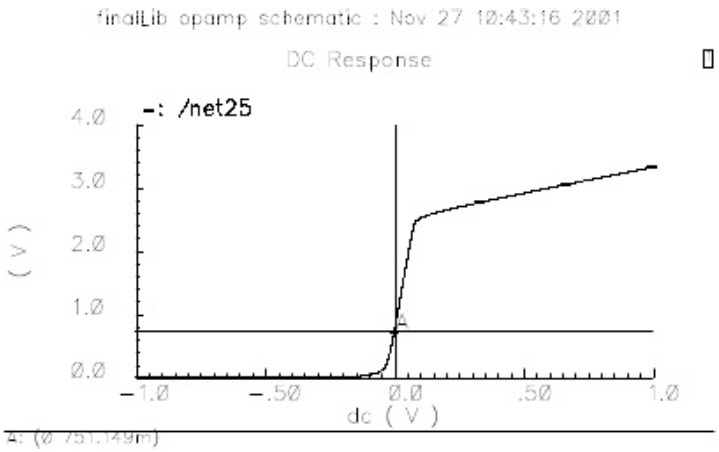


Figure 2.12: Waveform Distortion

3. Further reducing I_0. First, we can cascade active loads together, because the voltage is on the cascade active load, there is less voltage across each transistor, so the I_0 can be reduced dramatically. However, it becomes more complex to further optimize the circuit. See figure 2.13

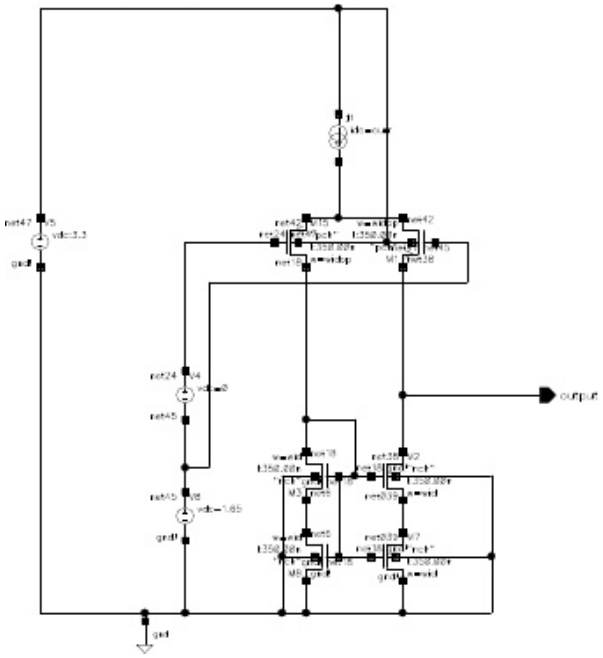


Figure 2.13: Active Loads Cascaded Together

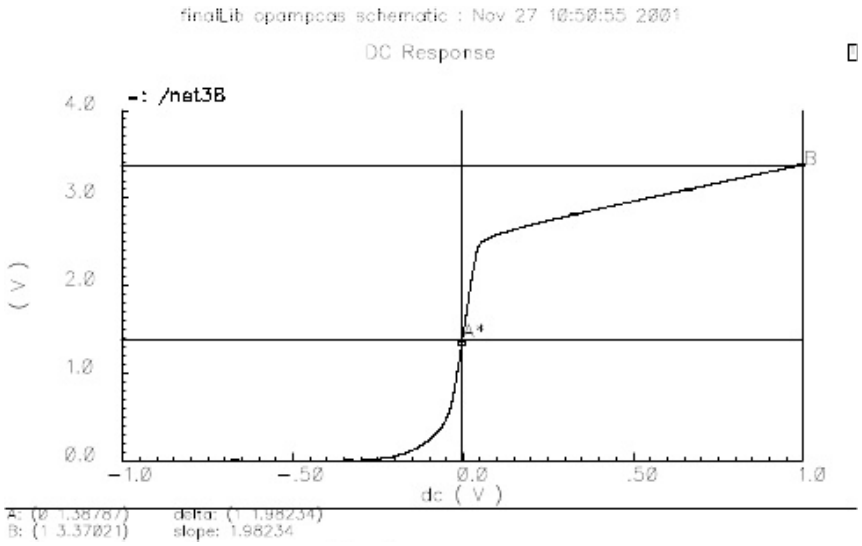


Figure 2.14: Cascaded Active Loads - DC Response/Gain

4. Cascade Op-Amp - adjusting the quiescent point: If after all of the above effort, we still cannot get the proper gain, we have to use a cascade Op-Amp. The key to optimizing the cascade Op-Amp is the quiescent point, which guarantees the proper operation of the circuit.

   Please refer the Figure 2.15 (Output curve of first the stage).
   The output of the first stage is linear in the area of $(0.5\ V \rightarrow 2.15\ V)$.
   So we should adjust the quiescent point of the input of the second stage.

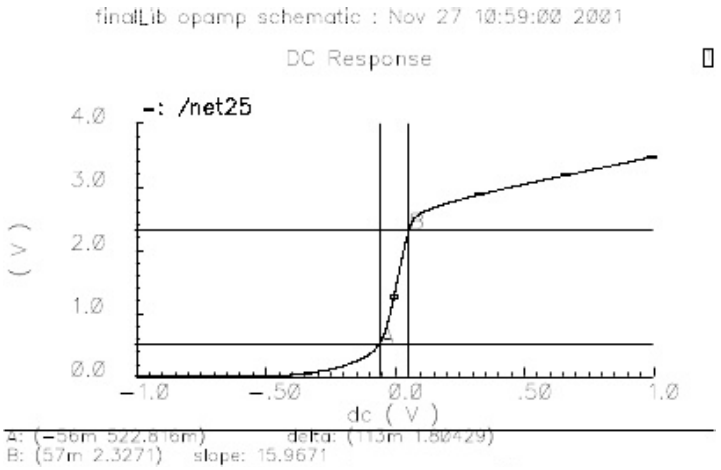


Figure 2.15: Output Curve of the First Stage

Checking the 2 stage Op-Amp, as in Figure 2.16

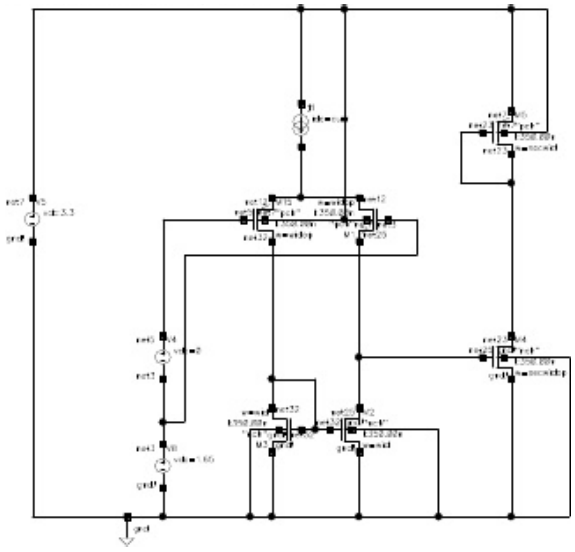


Figure 2.16: Two Stage Op-Amp Circuit

In the second stage amplifier, we get the waveform as shown in Figure 2.17 and Figure 2.18: We notice that the operating point of the amplifier begins to work is about 0V, actually at this point the output of

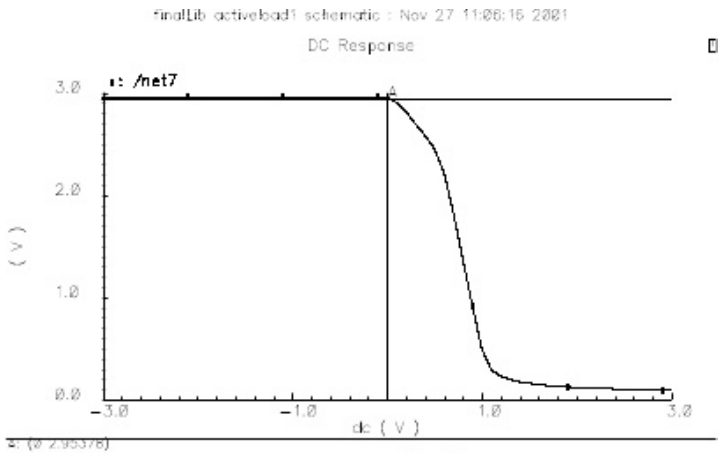


Figure 2.17: Second Stage Waveform

the first stage is in the non-linear area. That means the wave we get isn't the best.

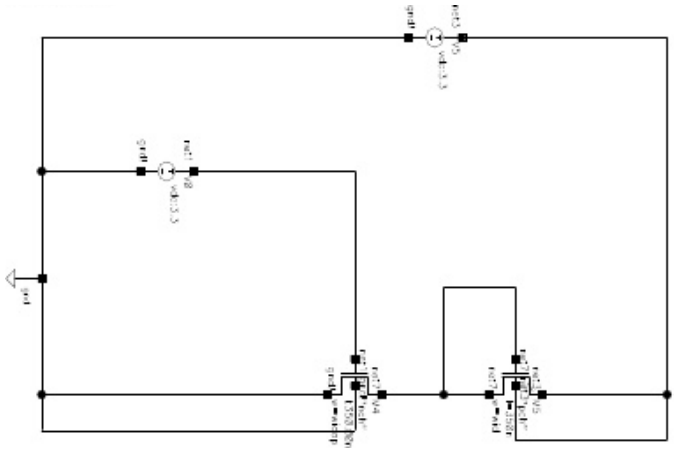


Figure 2.18: Second Stage Circuit

We can change the parameters of the two (2) transistors, however, it will have little affect on the non-linear problem. (See Figure 2.19 Non-Linear Problem). Thus we must use another topology. (Figure 2.20).

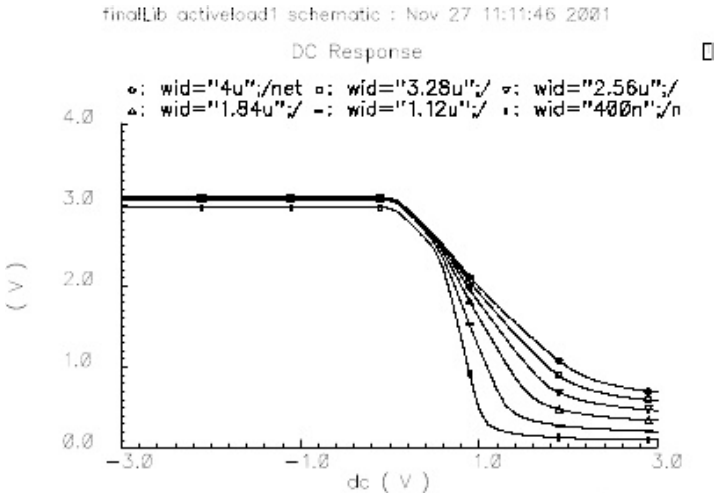


Figure 2.19: Non-Linear Problem

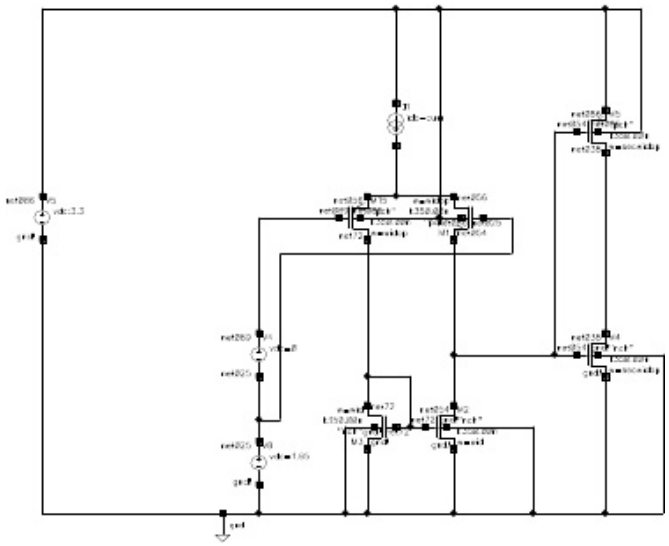


Figure 2.20: Different Topology to overcome Non-Linear Problem

We then get the resulting waveform shown in Figure 2.21.

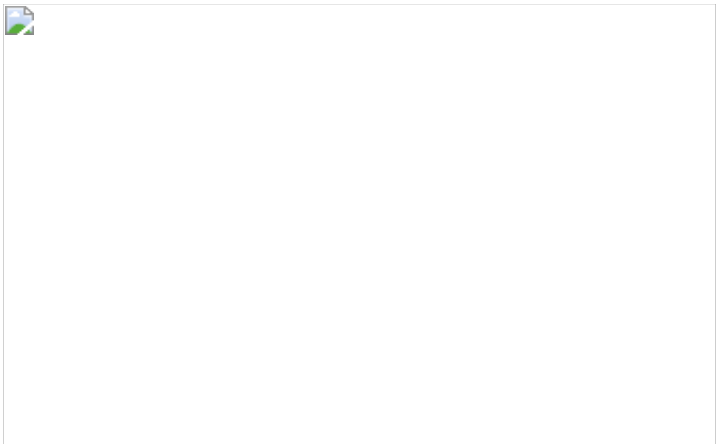


Figure 2.21: Resulting Waveform

We can adjust the circuit in another way, to change the input linear area of the second stage. To simplify the problem we can change the output stage.

Figure 2.22: Circuit with Modified Output Stage

2.3.4 How to get the Quiescent point in a complex circuit

Keeping a good quiescent point is very important and can be easily forgotten as the circuits become more complex. There are certain ways to design with the help of the computer, and establish models for different stages.

2.4 Target Op-Amp Specifications

The table below defines the best and worst cases for several key Op-Amp parameters, in addition the target Op-Amp parameters for this design are listed. These values are based upon textbook values, fabricated Op-Amp datasheets and from other research. During its design these key parameters were always kept at close hand.

Specification	Worst Case	Target Case	Best Case
Gain	$100 \rightarrow 1,000$	$1,000 \rightarrow 100,000$	1,000,000+
Frequency Range (Hz)	10-20,000	10-200,000	5-500,000
Bandwidth	5.0 KHz	20.0 KHz	50.0 KHz
Input Voltage	$\pm 1\ mV$	$\pm 1\ \mu V$	$\pm 0.1\ \mu V$
Output Resistance	$500\ K\Omega$	$1\ M\Omega$	$10\ M\Omega$
Power Consumption	mW	μW	nW
CMRR	$> 40\ dB$	$> 50dB$	$> 60dB$
Slew Rate	$3\ V/\mu sec$	$2\ V/\mu sec$	$0.5\ V/\mu sec$
THD	1%	0.1%	0.01%
Parasitic Capacitance	$1.0\ \mu F$	$1.0\ nF$	$1.0\ fF$
Rise Time	$1\ \mu sec$	$0.1\ \mu sec$	$0.001\ \mu sec$
Settling Time	$10\ \mu sec$	$1\ \mu sec$	$0.1\ \mu sec$

Chapter 3

Current Mirrors and Biasing Networks

One of the most important parts of an analog design is the biasing circuity. The purpose of the bias circuity is establish an appropriate DC operating point for the transistor. With the correct DC operating point established a stable and predictable DC drain current I_D and a DC drain-source voltage ensures operation in the saturation region for all input signals that may be encountered. This component forms the basis for an operational amplifier whereby various circuits like the differential pair, gain stage and output stage rely on its flawless stable operation.

For the Operational Amplifier design five different types of current mirrors were examined; Basic Current Mirror, Cascade/Cascode Current Mirror, Wilson Current Mirror, Modified Wilson Current Mirror and Reduced Cascade/Cascode Current Mirror. The advantages and disadvantages of each type of current mirror will be outlined later.

The five current mirrors which were examined were designed in Cadence and were placed into a standard test circuit consisting of a basic differential pair with active load and basic common-source amplifier output stage with a $10K\Omega$ load. These current mirrors were then subjected to several tests including; DC Sweep, current mirror output impedance and stability of current supplied across dynamic voltage range.

The ability of a current mirror to hold current constant, the number of transistors used and their sizes are the general defining factors on whether a current mirror is "Good" or not. These factors were considered when deciding on the current mirror to be used in the Op-Amp Design.

3.1 Ideal Characteristics of a Current Mirror

1. Output current linearly related to the input current. $I_{out} = A \cdot I_{in}$.
2. Input Resistance is zero.
3. Output resistance is infinity.

3.2 Basic Current Mirror Derivation

Below is the derivation of the simple current mirror.

Q1 is operating in the saturation region since its drain is shorted to its gate. Thus,

$$I_{D1} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2 \tag{3.1}$$

Note we neglect channel-length modulation and assume $\lambda = 0$.

The drain current of Q1 is supplied by V_{DD} through a resistor, R.

Assuming gate currents to be approximately 0.

$$I_{D1} = I_{ref} = \frac{V_{DD} - V_{GS}}{R} \tag{3.2}$$

Now looking at Q2,

It has the same V_{gs} as Q1, and assuming it is operating in saturation, its drain current, which is the output current I_o of the current source will be,

$$I_O = I_{D2} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \tag{3.3}$$

Again neglecting channel-length modulation.

Using equations 1,2 and 3 we are able to relate the output current I_o to the reference current I_{ref}.

Rearranging equation 1 and substituting $I_{ref} = I_{d1}$

$$\frac{I_{ref}}{\left(\frac{W}{L}\right)_1} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_1 (V_{GS} - V_t))^2 \tag{3.4}$$

We know,

$$I_O = \left[\frac{1}{2}K_n \left(V_{GS} - V_t\right)^2\right]\left(\frac{W}{L}\right) \tag{3.5}$$

So substituting into equation 3.5,

$$I_O = \frac{I_{ref}}{\left(\frac{W}{L}\right)_1} \cdot \left(\frac{W}{L}\right)_2$$

$$\frac{I_O}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_2}{\frac{W}{L}_1} \tag{3.6}$$

Thus we have a relationship whereby modifying the width and length we can change the output current. ( )

Thus if the transistors were matched, i.e. width and lengths equal and other parameters the same we have,

$$\frac{I_O}{I_{ref}} = 1 \tag{3.7}$$

$$I^O = I^{ref} \tag{3.8}$$

This is called a current mirror since the reference current is "mirrored" or held constant at the output.

3.3 Benchmark Test Circuit

The purpose of the test circuit is to establish a benchmark which could be used to evaluate the performance and design of each of the different types of biasing circuits. This test circuit was kept the same for all tests and the transistor sizes were set to the smallest possible optimum values. The test circuit itself consists of a basic differential pair (W=1900nm, L=350nm), a basic two transistor active load (W=800nm, L=350nm) and common source amplifier (W=800nm, L=350nm).

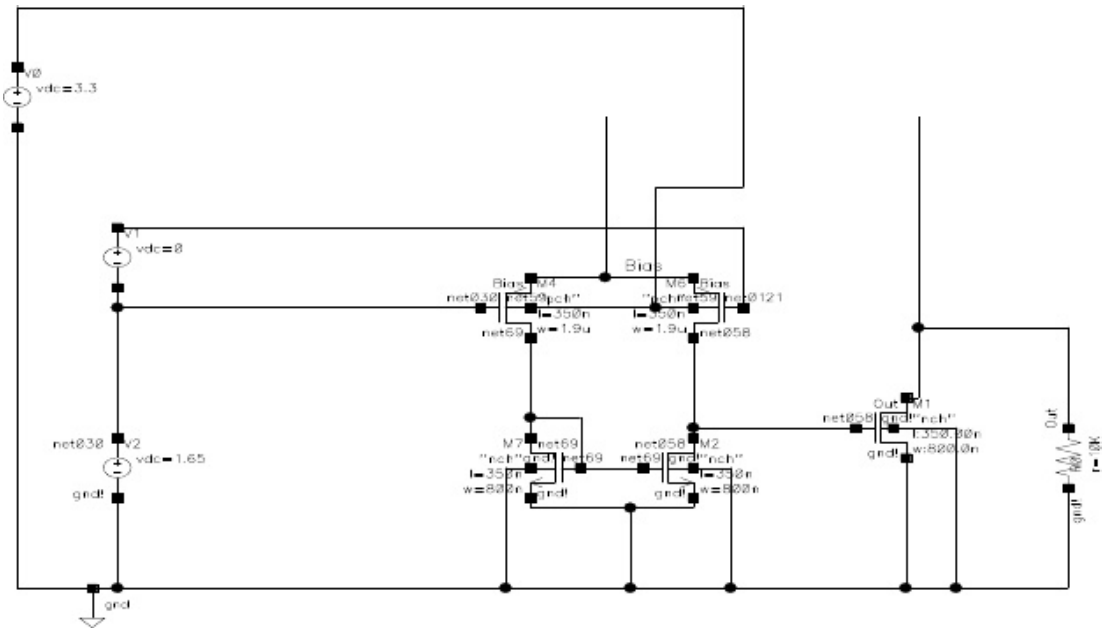


Figure 3.1: Benchmark Test Circuit Schematic

The widths of the transistors were adjusted so that the current supplied to the differential pair was between 6.50μA and 7.00μA. Then the output impedance was measured, as well as, the overall size of the transistors once the desired current was achieved. These results were recorded out would help to choose which current mirror would be the "Winner".

3.4 Examined Current Mirrors

3.4.1 Basic Current Mirror

We will now examine the most fundamental and simple type of current mirror, the Basic Current mirror (See Figure 3.2). This type of current mirror uses a minimum of (3) three transistors. The derivation shown earlier shows the general operation of a current mirror whereby current is held constant regardless of the voltage being supplied.

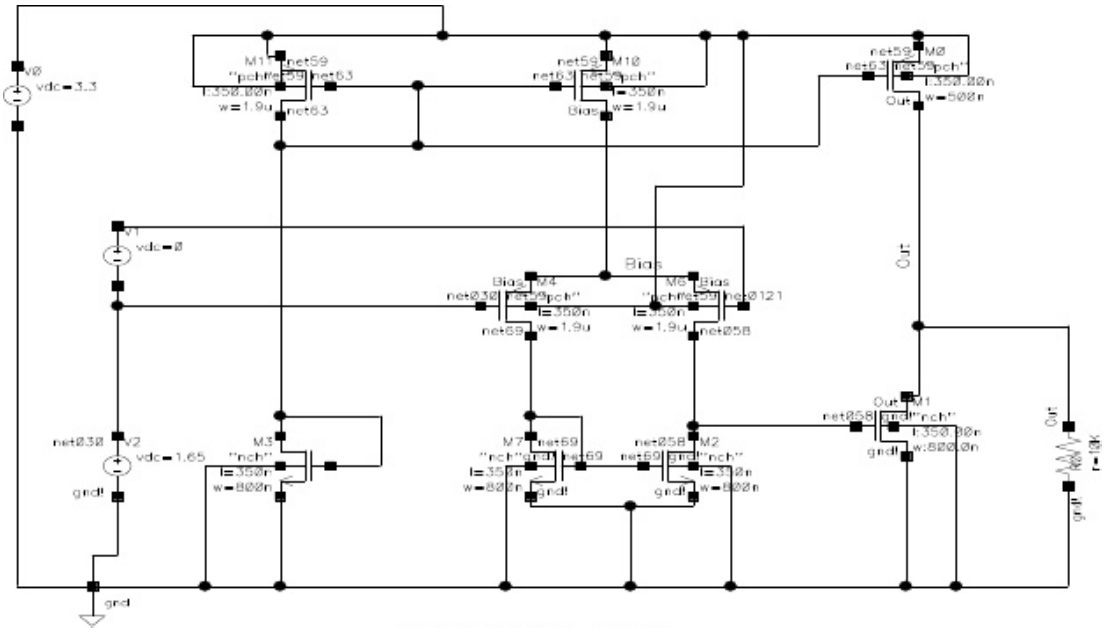


Figure 3.2: Basic Current Mirror Schematic

This circuit is very simple and does a very good job of supplying constant current, however, it does not supply absolutely stable current. See figure 3.3, the output current supplied to the active load and the output impedance.

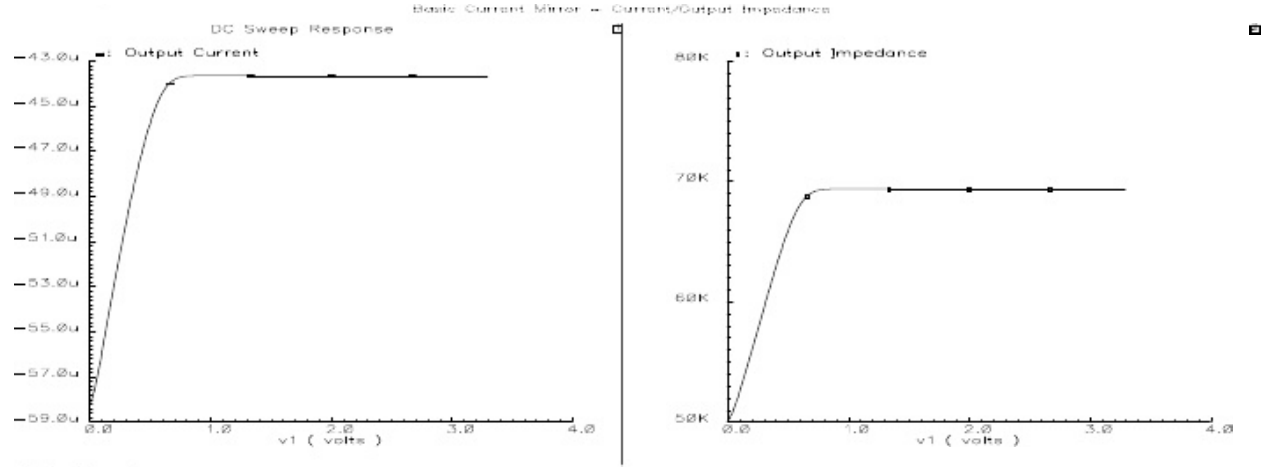


Figure 3.3: Basic Current Mirror Simulation Results

The main advantage of this current mirror is its simplicity and ease of implementation, however, the major disadvantage is that the current supplied is not completely stable.

3.4.2 Cascade/Cascode Current Mirror

The second current mirror examined was the Cascade/Cascode Current Mirror. This current mirror uses a minimum of (5) five transistors, these transistors can be seen in the Figure 3.4.

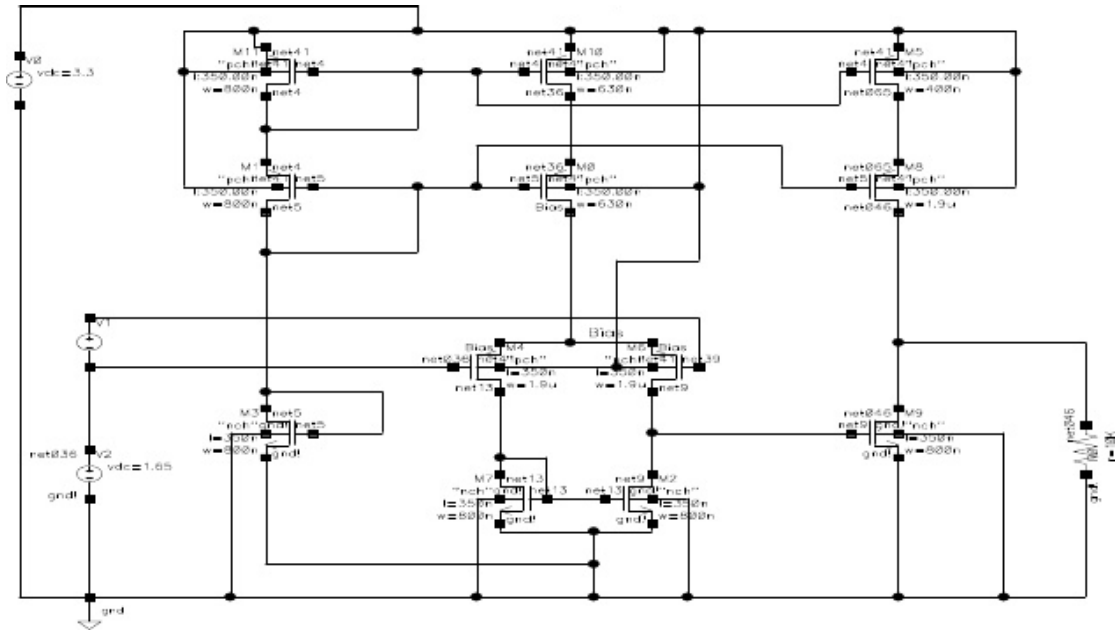


Figure 3.4: Cascade/Cascode Current Mirror Schematic

This circuit is a little bit more complex than the simple current mirror with (2) two extra transistors and would be more than enough for any design. The main disadvantage to this current mirror is that it is not very good at supplying higher amounts of current, in particular to the output stages. It was given very high consideration when deciding which current mirror to use for the Op-Amp design.

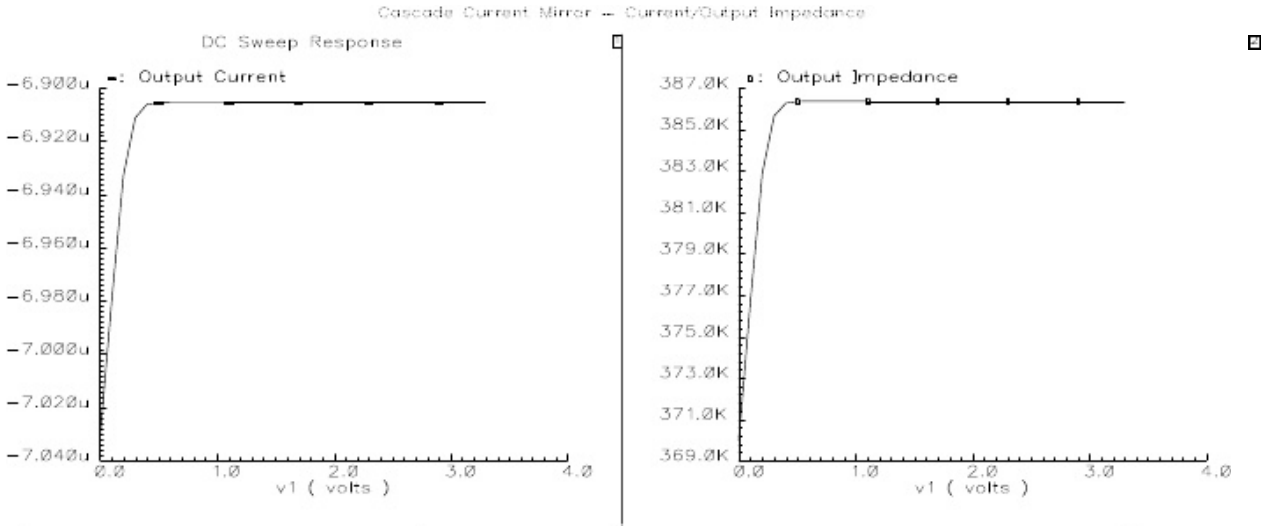


Figure 3.5: Cascade/Cascode Current Mirror Simulation Results

The main advantage to this design is that it provides stable current and it has relatively small transistor sizes. In addition to this we have a higher output resistance compared to the basic current mirror. The main disadvantage to this type of current mirror is a reduced dynamic range. Thus, it scored high in our choice for current mirrors when testing.

3.4.3 Wilson Current Mirror

The third current mirror examined was the Wilson current mirror. This current mirror uses a minimum of (4) four transistors. In the Figure 3.6 you can see the circuit layout.

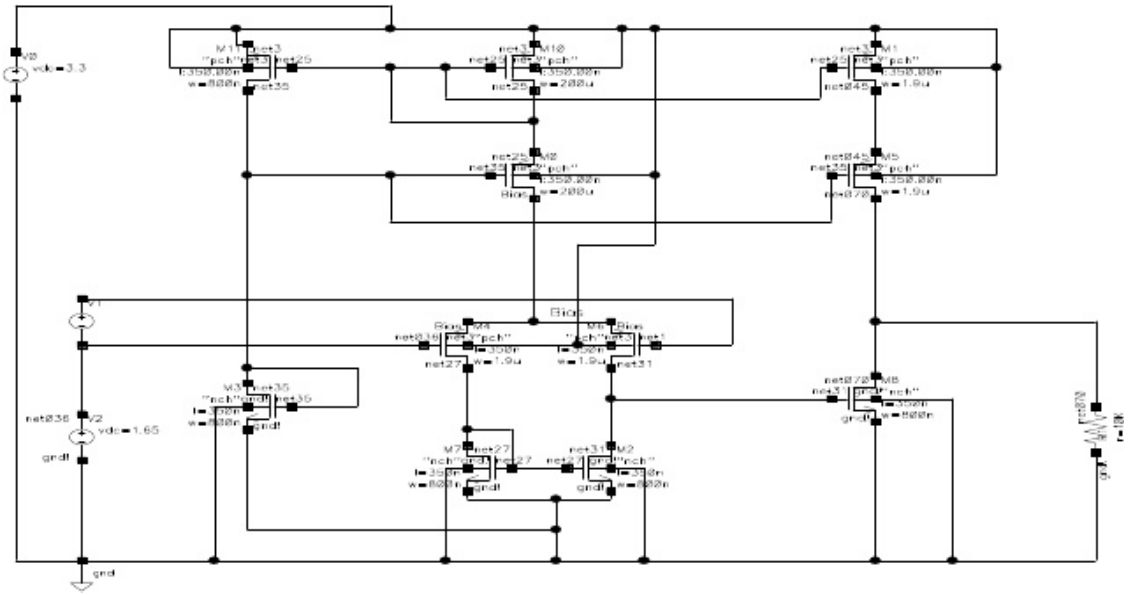


Figure 3.6: Wilson Current Mirror Schematic

This circuit is not as complex as the cascade current mirror and does provide good stable current, however, to provide the benchmark $6.50 \rightarrow 7.00\mu A$ very large transistors ($200\mu m$) had to be used, and thus, given that the current "best", cascade current mirror provided similar qualities but with much smaller transistor sizes this current mirror was ranked very low.

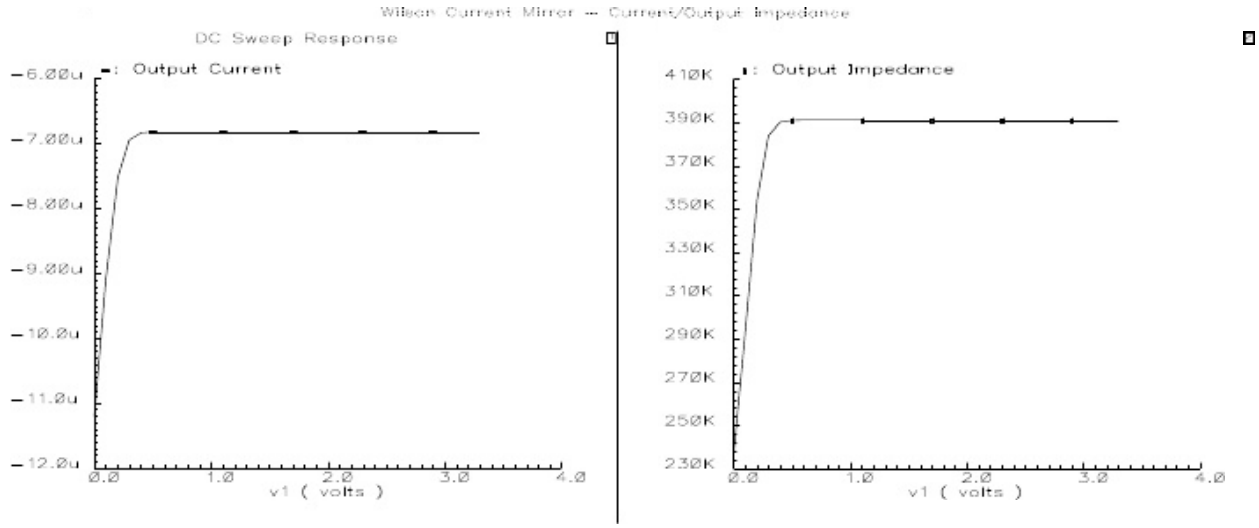


Figure 3.7: Wilson Current Mirror Simulation Results

As stated above this design was not considered for the Op-Amp design and the cascade current mirror was the current best.

3.4.4 Modified Wilson Current Mirror

The fourth current mirror examined was the Modified Wilson current mirror. This current mirror uses a minimum of (5) five transistors and has a similar layout as the cascade current mirror. This current mirror was expected to perform similar to the regular Wilson current mirror. You can see the circuit schematic in Figure 3.8.

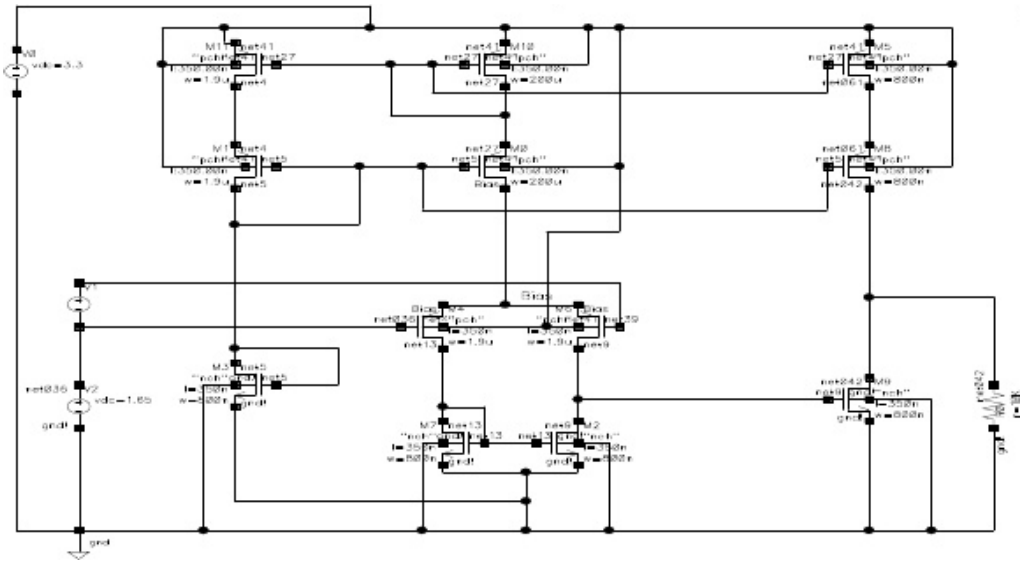


Figure 3.8: Modified Wilson Current Mirror Schematic

Upon testing the results revealed that the initial idea that it would perform similarly to the regular Wilson current mirror were confirmed. It had similar results with the output current as output resistance and the transistor sizes needed to attain the benchmark current we also large (200u).

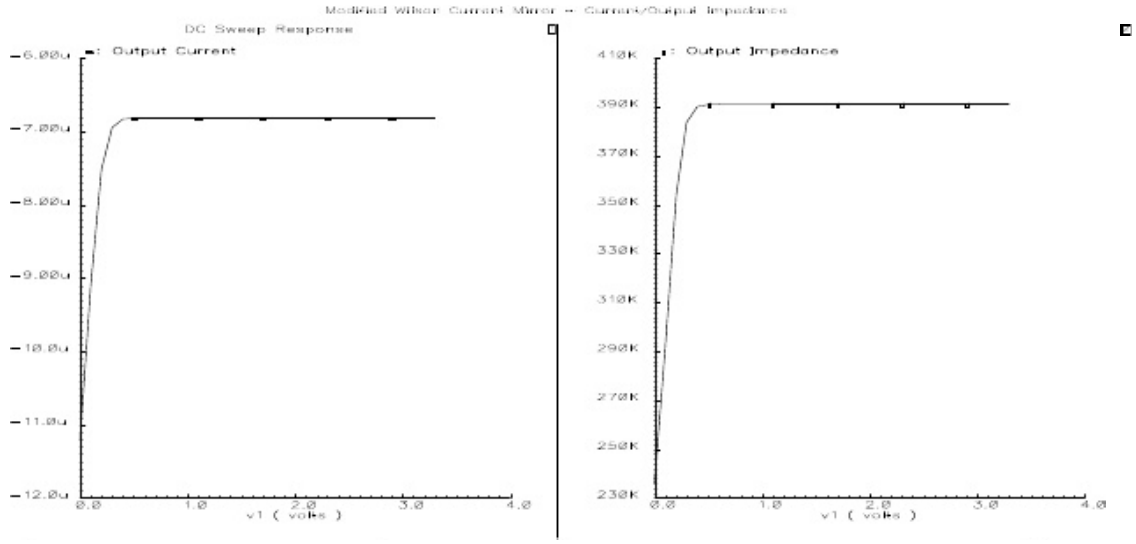


Figure 3.9: Modified Wilson Current Mirror Simulation Results

Upon seeing these results, the Modified Wilson current mirror was not to be chosen as the current mirror for the Op-Amp design.

3.4.5 Reduced Cascade Current Mirror

The fifth and final current mirror examined was the Reduced Cascade current mirror. This current mirror used a minimum of (6) six transistors and had a similar layout to that of the basic cascade current mirror. The word "Reduced" in the name refers to the reduced voltage at which the current reaches a stable output, it is usually about (1/2) one-half of the usual voltage.

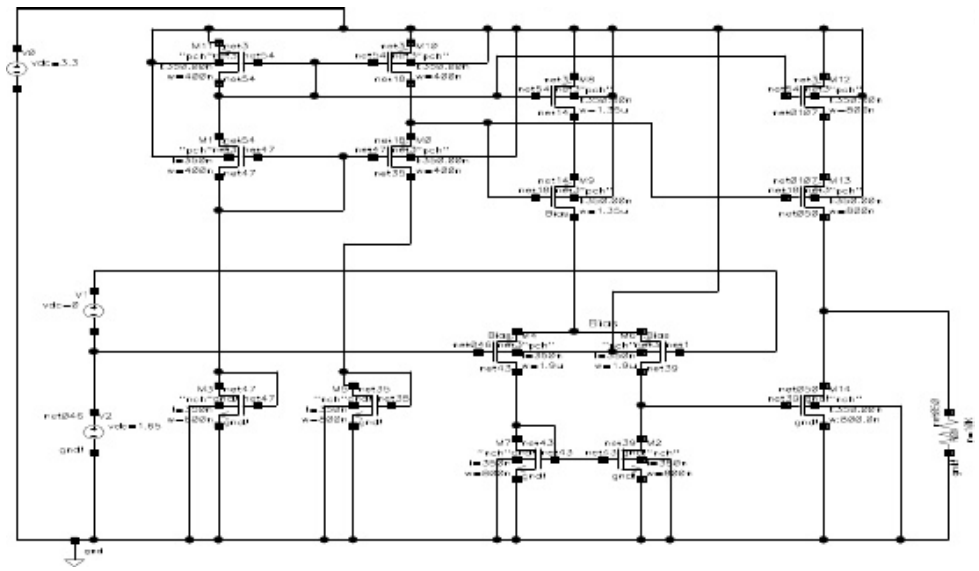


Figure 3.10: Reduced Cascade Current Mirror Schematic

This current mirror is a bit more complex and the transistor sizes are comparable to the basic cascade current mirror. However, the reduced cascade current mirror offers a reduced voltage and is able to provide higher amounts of current. This is very useful in the output stages were higher amounts of current are needed to bias the output stages.

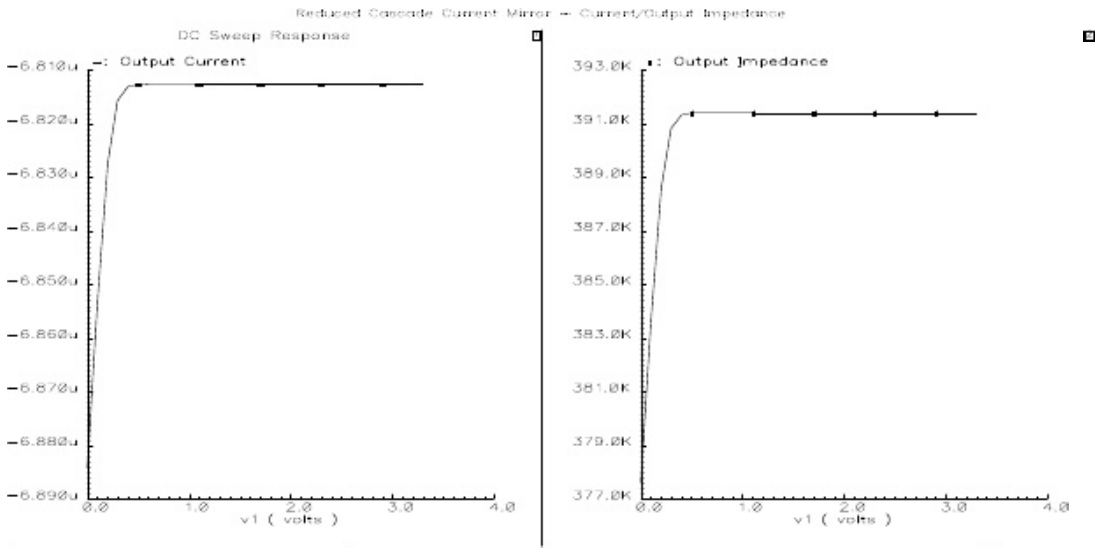


Figure 3.11: Reduced Cascade Current Mirror Simulation Results

The results of this current mirror appeared to be the most promising for the Op-Amp design, it provided stable current, it was able to provide higher amounts of output current if necessary, as well as, it reduced the voltage at which the current was stable compared to the other current mirrors examined.

3.5 Conclusion

The decision to use the Reduced Cascade/Cascode Current Mirror in the design of this Op-Amp are now shown here. First, the reduced cascade/cascode current mirror provided stable and linear current in all test situations. Secondly, it provided very high output resistance and a very low input resistance. Third, it was able to supply larger amounts of current which were needed to drive the output stage. Lastly, given it had a few extra transistors their sizes were small compared to other current mirror setups looked at. In the table below you can see the current mirrors ranked from best to worst (top to bottom) as well as a few of the ranking criterion and their evaluation.

The Basic Cascade/Cascode current mirror would have also done a very good job in the design, however with the reduced cascade's reduced voltage it offered a bit of an advantage over the basic cascade current mirror.

Current Mirrors Ranked: (Best to Worst)	Min # of FET's including I_{ref} Transistors	Current Stability	Output Resistance	Input Resistance	Complexity	Transistor Sizes needed to achieve Ref 7.0μA Current
Reduced Cascade/Cascode	6+2N	Excellent	Very High	Very Low	Very High	Small
Basic Cascade/Cascode	3+2N	Very Good	Very High	Very Low	Very High	Very Small
Basic Wilson	2+2N	Good	High	Very Low	Moderate	Very Large
Modified Wilson	3+2N	Good	High	Very Low	Moderate	Very Large
Basic	2+N	Poor	Low	Very Low	Simple	Small

N = Number of times current is mirrored. (In these designs N = 2, differential Pair Biasing and Output Stage)

Chapter 4

Differential Input Stage

4.1 The Unbuffered Op-Amp

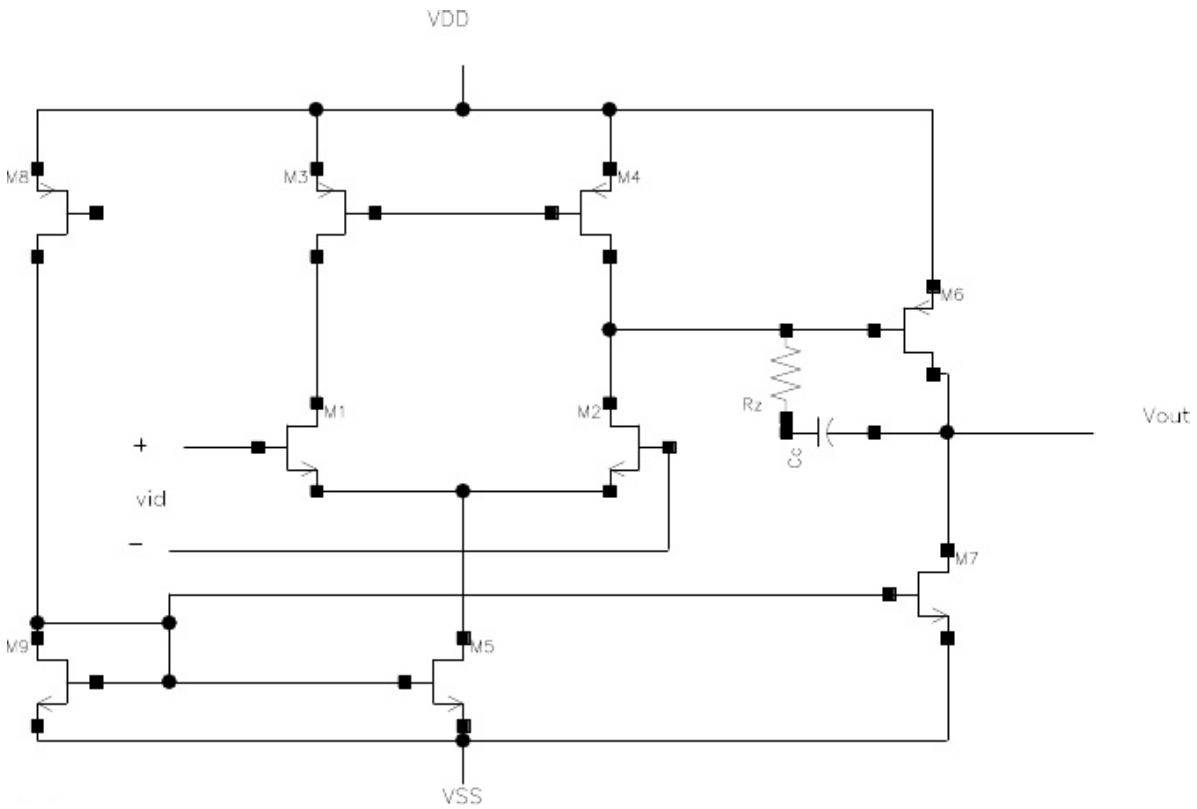


Figure 4.1: Two Stage Op-Amp

The amplifier shown in figure 4.1 can be segregated into:

1. Biasing block.
2. Differential input stage.
3. Output stage.

The biasing block, consists of M8, M9, and M5. The bias current greatly affects the performance of the amplifier. The differential input stage is composed of M1, M2, M3, M4 with: M1 matching M2, M3 matching M4. The output stage consists of M6 and M7.

4.2 Small Signal Equivalent Circuits

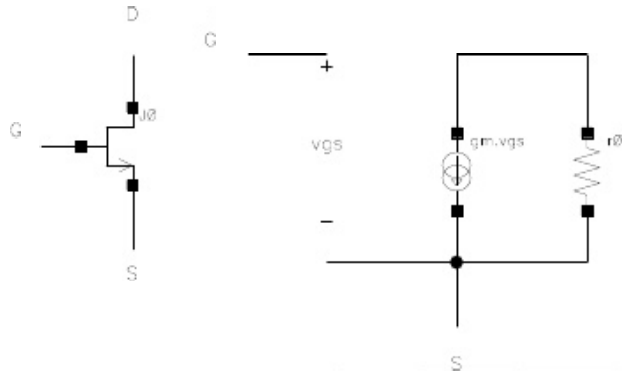


Figure 4.2: NFET and Its Small Signal Model

In the analysis of a FET amplifier circuits, the FET can be replaced by the equivalent circuit model, 4.2. Where:

$$r_o = \frac{|VA|}{I_D}$$

Where $VA = \frac{1}{\lambda}$
g_m is the transconductance parameter $= K_n\prime\frac{W}{L}(V_{GS} - V_t)$
Therefore, the small signal model parameters:

g^m and r^o depends on the DC bias of the FET.

Ideal constant DC voltage sources are replaced by short circuits, this is a result of the fact that the voltage across an ideal constant DC voltage source does not change and thus there will always be a zero voltage signal across a constant DC voltage source. The signal current of an ideal constant DC current source will always be zero thus an ideal constant DC current source can be replaced by an open circuit.

For the gate drain connected FET device, the model is as shown in figure 4.3.

Since $v_{ds} = v_{gs}$ (the effective resistance $= \frac{v_{gs}}{v_{gs} \cdot g_m} = \frac{1}{g_m}$)

Figure 4.4 shows only the differential input stage of the circuit. In figure 4.1 M5 are replaced by current source I_{ss}. The small signal analysis of the

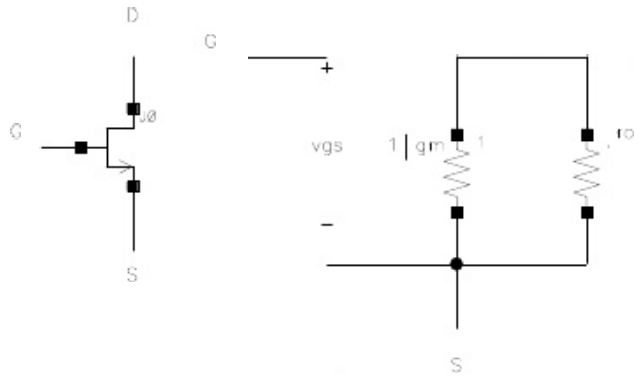


Figure 4.3: MOSFET Resistor and Its Small Signal Model

differential input stage can be accomplished with the assistance of the model shown in figure 4.5 which is only appropriate for differential analysis when both sides of the amplifier are assumed to be perfectly matched. If this condition is satisfied, then the point where the two sources of M1 and M2 are connected can be considered at AC ground. The body effect is neglected.

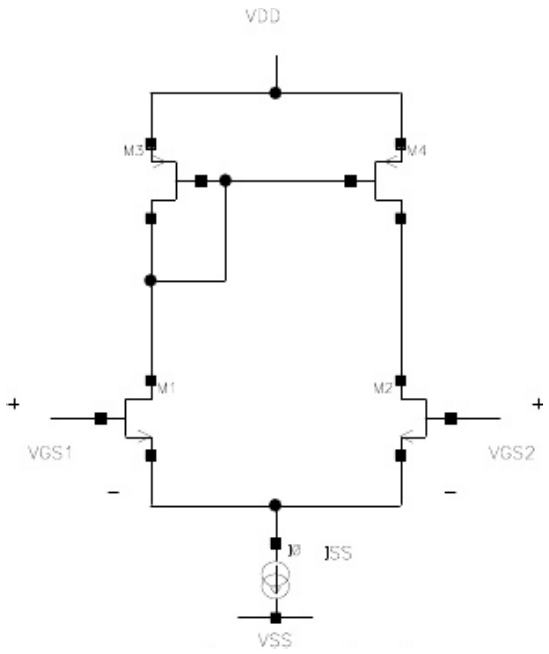


Figure 4.4: CMOS Differential Amplifier using n-channel Input Devices

The model in figure 4.6 is the simplified to the model shown in figure 4.5. Since: M1 matches M2, M3 matches M4 (The point where S1, S2 of M1, M2 are connected can be considered at AC ground.) Since S3, S4 are

and also be mirrored from M3 to M4

$$g_{m4} \cdot v_{gs4} = i_{d1}$$

Now since S1, S2, S3, S4 have the same potential (one node) i_{d1} will also flow from the source to drain of M2. $g_{m2} \cdot v_{gs2} = -i_{d1}$

$$i_{out} = i_{d1} - (-i_{d1}) = 2i_{d1} \tag{4.1}$$

$$r_{out} = r_{o2} \parallel r_{o4} \tag{4.2}$$

$$i_{d1} = g_{m1} \cdot v_{gs1}$$

Since $v_{gs1} = v_{gs2}$

$$v^{id} = v^{gs1} + v^{gs2}$$

Therefore, $v_{id} = 2v_{gs1}$

$$\begin{aligned} \frac{i_{d1}}{v_{id}} &= \frac{g_{m1} v_{gs1}}{2_{vgs}} \\ &= \frac{g_m 1}{2} \\ v^{id} &= \frac{2i_{d1}}{g_{m1}} \end{aligned} \tag{4.3}$$

Now the small signal output voltage is simply:

$$\begin{aligned} v_{out} &= i_{out} r_{out} \qquad (Substitute\ 4.1\ and\ 4.2) \\ v_{out} &= 2i_{d1} \cdot (r_{o2} \| r_{o4}) \end{aligned} \tag{4.4}$$

Now dividing 4.4 over 4.3 :

$$\frac{v_{out}}{v_{id}} = \frac{2i_{d1}(r_{o2} \| r_{o4})}{\frac{2i_{d1}}{g_{m1}}}$$

$$\frac{v_{out}}{vid} = g_{m1,2}(r_{o2} \| r_{o4}) \tag{4.5}$$

Now:

$$g_{m1,2} = (2\beta_{1,2} I_{D1,2})^{\frac{1}{2}}$$

$$(r_{o2} \| r_{o4}) \simeq \frac{1}{2\lambda I_{D,2}} \qquad (since\ r = \frac{1}{\lambda I})$$

Therefore,

$$\frac{v_{out}}{v_{id}} \cong (2\beta_{1,2} I_{D1,2})^{\frac{1}{2}} \cdot \left[\frac{1}{2\lambda I_{D1,2}} \right]$$

$$\frac{v_{out}}{v_{id}} \cong K\prime \cdot \left[\frac{W_{1,2}}{L_{1,2}I_{D1,2}}\right]^{\frac{1}{2}} \cdot \left(\frac{1}{\lambda}\right)$$

$K\prime$ is a constant, uncontrollable by the designer. The effect of λ on the gain diminishes as L increases, such that $\frac{1}{\lambda}$ is directly proportional to the channel length.

Then a proportionality can be established between $\frac{W_{1,2}}{L_{1,2}}$ and the drain current versus the small signal gain such that:

$$\frac{v_{out}}{v_{id}} \propto \left[\frac{W_{1,2}L_{1,2}}{I_{D1,2}}\right]^{\frac{1}{2}}$$

Therefore,

$$small\ signal\ gain \propto \left[\frac{W_{1,2}L_{1,2}}{I_{D1,2}}\right]^{\frac{1}{2}} \tag{4.6}$$

The constant was not included since the value is not dependent on anything the designer can adjust.

Conclusions:

1. Increasing $W_{1,2}$, $L_{1,2}$ or both increases the gain.
2. Decreasing the drain current through M1, M2 which is also $\frac{1}{2}I_{D6}$, increases the gain.

4.3 The Frequency Response

Referring back to the model of the input stage: figure 4.6. We will work to eliminate all low impedance nodes (having high RC time):

$$\frac{1}{c_1 \cdot \frac{1}{g_{m3}}} \gg \frac{1}{[c_2 \cdot (r_{o2} \parallel r_{o4})]}$$

Then the node (D1=D2=G3=G4) is a low impedance node (with large RC time) Now: c_3 is assumed to be zero. In most applications of differential amplifiers, this assumption turns out to be valid. Then the model to be considered for the high frequency response analysis is turned to be as shown in figure 4.7.

In the configuration where the small signal is applied to the gate of M4 while the gate of M2 is grounded, $v_{gs2} = 0,\ v_{id} = v_{gs1}$. Now:

$$g_{m4}v_{gs4} = i_{d1} = g_{m1}v_{gs1} = g_{m1}v_{id}$$

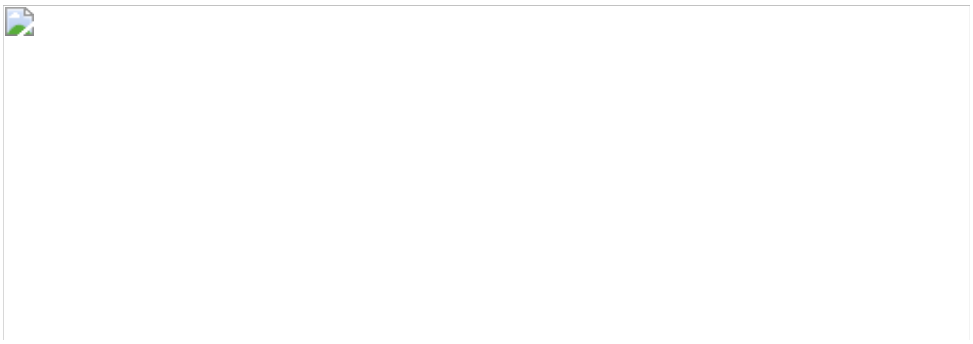


Figure 4.7: High Frequency Small Signal Model with Parasitic Capacitors

Now redrawing the model in Figure 4.7 with the new parameters will result in the model shown in Figure 4.8.

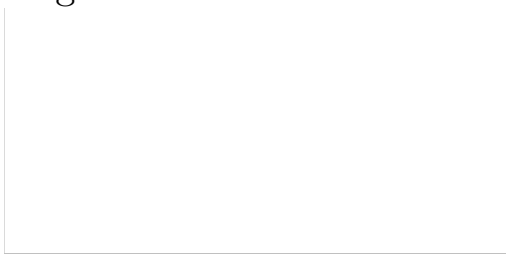


Figure 4.8: Model of the Input Stage used to Determine the Frequency Response

The high frequency output can be given by:

$$v_{o1} = g_{m1} v_{id} \cdot (r_{o2} \parallel r_{o4}) \cdot \frac{1}{\left[1 + S \cdot \frac{1}{c2(r_{o2} \| r_{o4})}\right]}$$

$$\textit{The freq. Response} = \frac{v_{o1}}{v_i d} = g_{m1} \cdot (r_{o2} \parallel r_{o4}) \cdot \frac{1}{\left[1 + S \frac{1}{c_2(r_{o2} \| r_{o4}}\right]}$$

Now let us consider the input and the output stage shown in figure 4.9.

The capacitor C_c in Figure 4.8 is removed for the purpose of the first analysis. C_1, C_2 represent the total lumped capacitance from each ground. Since the output nodes associated with each output is a high impedance, these nodes will be the dominant frequency dependent nodes in the circuit. Since each node in a circuit contributes a high frequency pole, the frequency response will be dominated by the high impedance nodes.

Figure 4.10 is the model derived for Figure 4.9 making use of Figure 4.8 to determine the frequency response of the two-stage Op-Amp.

To determine the exact value for c_1, c_2, Figure 4.11 shows the parasitic capacitors explicitly for the input and the output stage which include the bulk depletion capacitors (c_{gb}, c_{sb}, c_{db}) and the overlap capacitors (c_{gs}, c_{gd}).

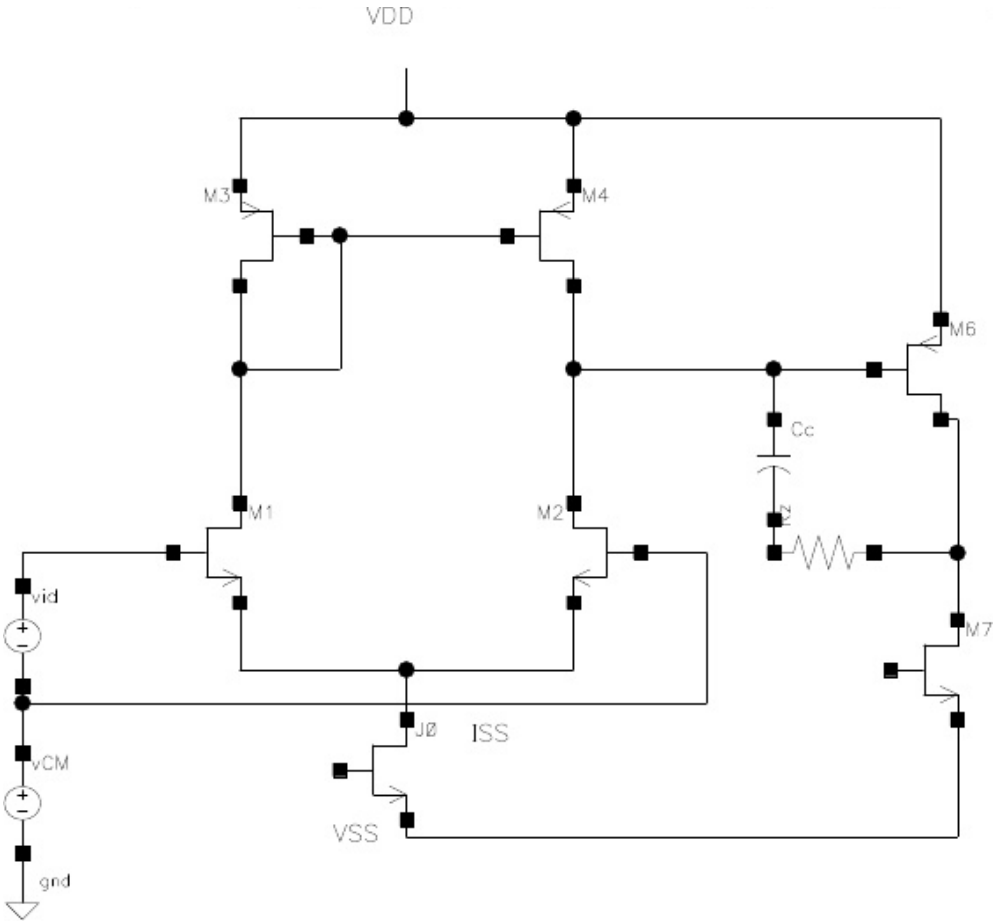


Figure 4.9: Two Stage Op-Amp with Lumped Parasitic Capacitors

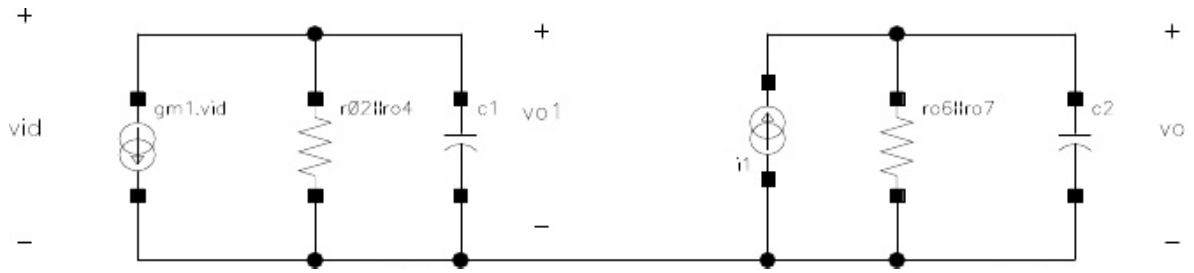


Figure 4.10: Model Used to Determine the Frequency Response of the Two-Stage Op-Amp

Miller theorem was used to determine the effect of the bridging capacitor c_{gd6} connected from the gate to drain of M6. Miller theorem approximates the effects of gate-drain capacitor by replacing the bridging capacitor with an equivalent input capacitor of value $c_{gd}(1+A2)$ and the equivalent output capacitor with a value of $c_{gd}(1+\frac{1}{A2})$. Where:

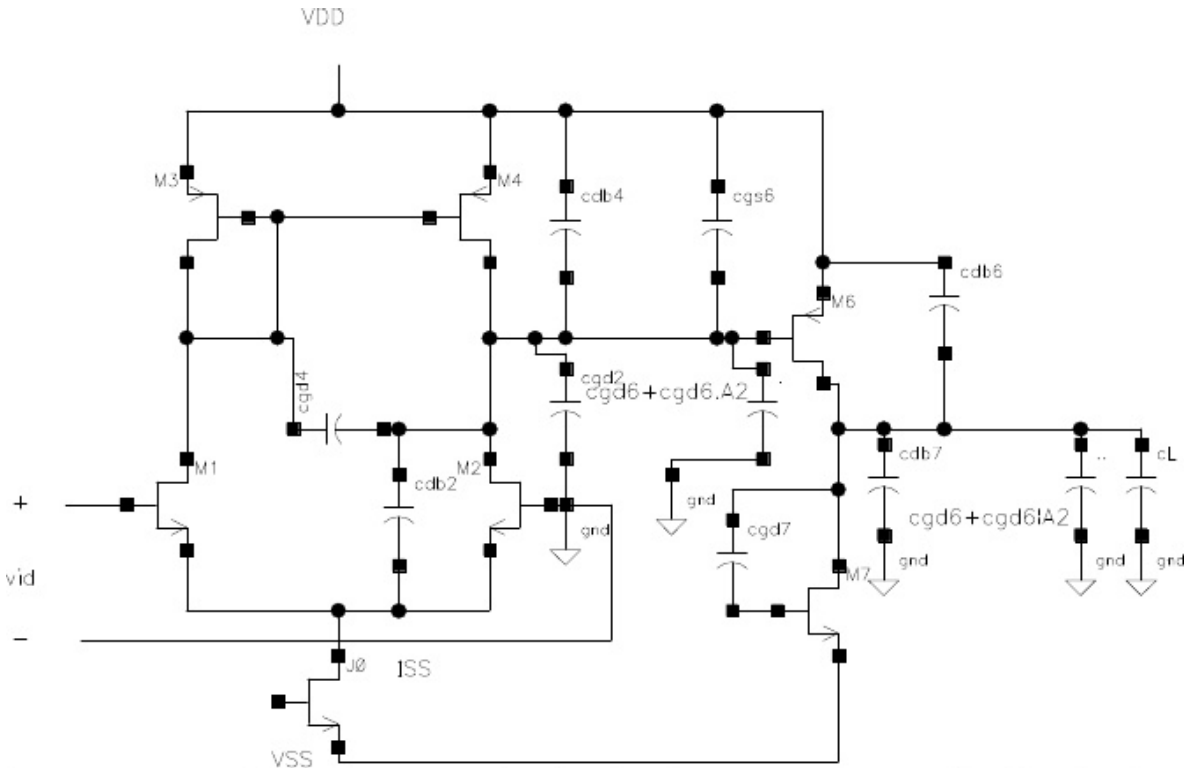


Figure 4.11: Two Stage Op-Amp with Parasitic Capacitors Shown Explicitly

A2: gain across the original bridging capacitor and is, from figure 4.10:

$$\begin{aligned} A2 &= \frac{v_o}{v_{o1}} = -g_{m6} \cdot v_{o1} \frac{r_{o6} \| r_{o7}}{v_{o1}} \\ A2 &= -g_{m6}(r_{o6} \| r_{o7}) \end{aligned} \tag{4.7}$$

Thus c1, c2 for fig(10) can be determined by examining figure 4.11.

$$c_1 = c_{db4} + c_{gd4} + c_{db2} + c_{gd2} + c_{gs6} + c_{gd6} \cdot (1 + A2)$$

$$c_2 = c_{db6} + c_{db7} + c_{gd7} + c_{gd6} \cdot \left(1 + \frac{1}{A2}\right) + c_L$$

Now assume $c_1 < c_2$ (the pole associated with the diff-amp output $\left(\frac{1}{c_1(r_{o2} \| r_{o4})}\right)$ will be lower in frequency than the pole associated with the output of the output stage $\frac{1}{c^2(r_{o6} \| r_{o7})}$.

Also from the high frequency model figure 4.10:

$$\frac{v_o}{v_{id}} = \left[\frac{v_o}{v_{o1}}\right] \cdot \left[\frac{v_{o1}}{v_{id}}\right] \cdot \left[\frac{1}{1 + \frac{S}{c_2 \cdot (r_{o6} \| r_{o7})}}\right] \cdot \left[\frac{1}{1 + \frac{S}{c_1 \cdot (r_{o2} \| r_{o4})}}\right]$$

$$\frac{v_o}{v_{o1}} = g_{m6} \cdot (r_{o6} \parallel r_{o7}) \frac{1}{\left(1 + \frac{S}{c_2 \cdot (r_{o6} \| r_{o7})}\right)}$$

$$\frac{v_{o1}}{v^{id}} = g_{m1} \cdot (r_{o2} \| r_{o4}) \cdot \left[\frac{1}{1 + \frac{S}{c_1 \cdot (r_{o2} \| r_{o4})}}\right]$$

Therefore, the frequency response

$$\frac{v_o}{v_{id}} = [g_{m6} \cdot (r_{o6} \| r_{o7})] \cdot [g_{m1} \cdot (r_{o2} \| r_{o4})] \cdot \left[\frac{1}{1 + \frac{S}{c_1 \cdot (r_{o2} \| r_{o4})}}\right] \cdot \left[\frac{1}{(1 + \frac{S}{c_2 \cdot (r_{o6} \| r_{o7})}}\right] \quad (4.8)$$

And the poles are:

$$P_1 = \frac{1}{c_1 \cdot (r_{o2} \| r_{o4})} \quad (4.9)$$

$$P_2 = \frac{1}{c_2 \cdot (r_{o6} \| r_{o7})} \quad (4.10)$$

4.4 Phase Margin

The phase margin is the difference between the phase at the frequency at which the magnitude plot reaches 0dB and the phase at the frequency at which the phase has shifted -180^o. It is recommended for stability reasons that the phase margin of any amplifier be at least 45^o (60^o is recommended). A phase margin below 45^o will result in long settling time and increased propagation delay. The Op-Amp system can also be thought of as a simple second order linear control system with the phase margin directly affecting the transient response of the system.

Phase margin measurement procedure with the Cadence design tool, the phase margin can be measured by applying the following steps:

1. Obtain the AC response simulation
2. Delete all the outputs in the Affirma window
3. Select the AC response curve (it will turn to yellow).
4. From the Affirma window: Result → direct plot → AC magnitude and phase

5. Follow the prompt at the bottom of the schematic window and select the output node

6. From the Affirma window : output → to be plotted

7. You will get the magnitude and the phase frequency response. Split the graphs.

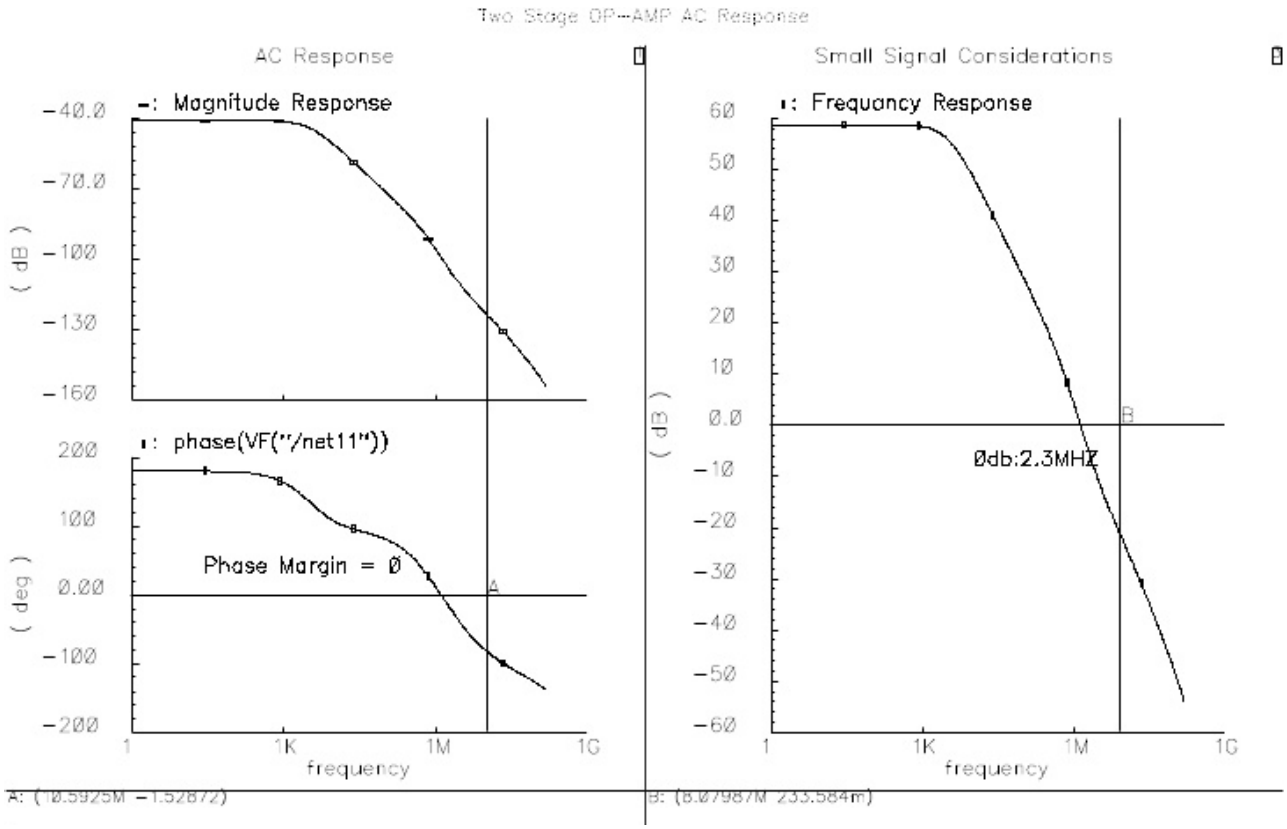


Figure 4.12: Miller Phase Margin Measurement

4.5 Compensation

The goal of the compensation task is to achieve a phase margin greater than 45^o. Now we will include C_c and the model will be as in Figure 4.13

Keeping in mind that the two poles of the system without compensation as determined previously are:

$$P_1 = \frac{1}{c_1 \cdot (r_{o2} \| r_{o4})}$$

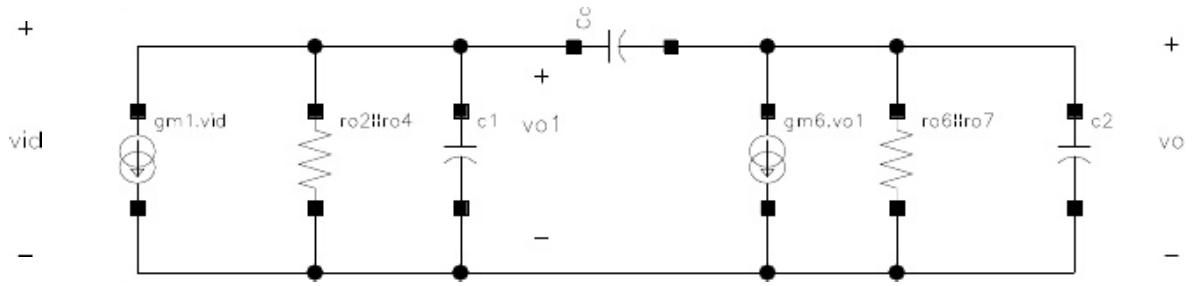


Figure 4.13: Model Used to Determine the Frequency Response of the Two-Stage Op-Amp

$$P_2 = \frac{1}{c_2 \cdot (r_{o6} \| r_{o7})}$$

Two results come from adding the compensation capacitor C_c:

1. The effective capacitance shunting $r_{o2} \| r_{o4}$ is increased by the additive amount of approximately $g_{m1} \cdot r_{o2} \| r_{o4} \cdot C_c$. This moves P_1 down by a significant amount. C_c will dominate the value of c_1 and will cause the pole P_1 to roll off much earlier than without C_c to a new location.

2. P_2 is moved to a higher frequency.

Let $r_1 = r_{o2} \| r_{o4}$, $r_2 = r_{o6} \| r_{o7}$,

$$\frac{v_o}{v_{id}} =$$

$$\frac{g_{m1} g_{m6} r_1 r_2 \left(1 - S\frac{C_c}{g_{m6}}\right)}{1 + S\left[r_1(c_1 + C_c) + r_2(c_2 + C_c) + g_{m6} r_1 r_2\right] + S^2 r_1 r_2 \left[c_1 c_2 + C_c(c_1 + c_2)\right]} \tag{4.11}$$

A general second order polynomial can be written as:

$$P(S) = 1 + aS + bS^2 = \left(1 - \frac{S}{P_1}\right)\left(1 - \frac{S}{P_2}\right) = 1 - S\left(\frac{1}{P_1} + \frac{1}{P_2}\right) + \frac{S^2}{P_1 P_2}$$

If $|P_2| \ll |P_1|$ then:

$$P(S) = 1 - \frac{S}{P_1} + \frac{S^2}{P_1 P_2}$$

Therefore, P_1, P_2 may be written in terms of a, b as:

$$P_1 = \frac{-1}{a}$$

$$P_2 = \frac{-a}{b}$$

The key in this technique is the assumption that the magnitude of the root P_2 is greater than the magnitude of the root P_1

$$P_1 = \frac{-1}{r_1(c_1 + C_c) + r_2(c_2 + C_c) + g_{m6} r_1 r_2 C_c}$$

$$P1 \simeq \frac{1}{g_{m6} r_1 r_2 C_c}$$

$$P_2 = -\frac{r_1(c_1 + C_c) + r_2(c_2 + C_c) + g_{m6} r_1 r_2 C_c}{r1_r 2(c_1 c_2 + C_c(c_1 + c_2))}$$

$$P_2 \cong \frac{-g_{m6} C_c}{c_1 c_2 + c_2 C_c + c_1 C_c}$$

$$P_2 \cong \frac{g_{m6}}{c^2} \tag{4.12}$$

The second pole should not begin to affect the frequency response until after the magnitude response is below 0dB.

It is of interest to note that a zero occurs in the right-hand-plane (RHP) due to the feed forward path through C_c. The RHP zero is located at:

$$Z_1 = \frac{g_{m6}}{C_c} \tag{4.13}$$

This RHP zero has negative consequences on our phase margin, causing the phase plot to shift -180^o more quickly. To avoid the effect of RHP zero, one must try to move the zero well beyond the point at which the magnitude plot reaches 0dB (suggested rule of thumb: factor of 10 greater)

4.6 Adding R_z in series with C_c

One remedy to the "zero problem" is to add a resistor R^z in series with C^c

$$Z_1 = \frac{1}{\left[C_c \left(\frac{1}{g_{m6}} - R_z\right)\right]} \tag{4.14}$$

And the zero can be pushed into the LHP where it adds phase shifts and increases phase margin if:

$$R_z > \frac{1}{g_{m6}} \tag{4.15}$$

The zero location is in the RHP, when $R^z = 0$. As R^z increases in value, the zero gets pushed to infinity at the point at which $R_z = \frac{1}{g_{m6}}$. Once $R_z > \frac{1}{g_{m6}}$, the zero appears in the LHP where its phase shifts adds to the overall phase response. Thus improving the phase margin. This type of compensation is referred to as lead compensation and is commonly used as a simple method for improving the phase margin. One should be careful about using R_z, since the absolute values of the resistors are not well predicted. The value of the resistor should be simulated over its max and min values to ensure that no matter if the zero is pushed into the LHP or RHP, that value of the zero is always 10 times greater than the gain bandwidth product.

4.7 Gain Bandwidth Product

GBW for the compensated Op-Amp is the open loop gain multiplied by the bandwidth of the amplifier (as set by P_2).

$$\begin{aligned} GBW &= g_{m1} r_1 g_{m6} r_2 \cdot \left[\frac{1}{g_{m6} r_1 C_c r_2} \right] \\ GBW &\cong \frac{g_{m1}}{C_c} \\ GBW &\propto \frac{\left[I_{D1,2} \cdot \frac{W_{1,2}}{L_{1,2}} \right]^{\frac{1}{2}}}{C_c} \end{aligned} \tag{4.16}$$

Therefore, the most efficient way to increase GBW is to decrease C_c. The value of C_c must be large enough to affect the initial roll-off frequency as larger C_c improves phase margin. Therefore, to know the value of C_c:

1. We need to know the GBW specification.
2. Iteratively choosing the values for $\frac{W_{1,2}}{L_{1,2}}$ and $I_{D1,2}$ and then solving for C_c.

Conclusions:
P_2 should be $> GBW$ Therefore, $\frac{g_{m6}}{c_2} > \frac{g_{m1,2}}{C_c}$

$$C_c > C_2 \cdot \left(\frac{g_{m1,2}}{g_{m6}} \right) \tag{4.17}$$

Practically speaking, the load capacitor usually dominates the value of c_2, so $c_2 = c_L$

$$C_c > c_L \cdot \left(\frac{g_{m1,2}}{g_{m6}} \right) \tag{4.18}$$

Therefore, the effect of c^L on phase margin is as follows: Minimum size of Cc directly depend on the size of c_L. For example if the zero is 10 times larger than GBW, then in order to achieve a 45^o phase margin, P_2 must be least 1.22 times higher than GBW. And to get a phase margin of 60^o P_2 must be 2.2 times greater than GBW.

4.8 Large Signal Consideration

Analysis and design can be greatly simplified by separating DC or bias calculations from small signal calculations. That is once a stable operating point has been established and all DC quantities are calculated, we may then perform AC analysis. Figure 4.14 shows the large signal equivalent circuit model for n-channel MOSFET in saturation. The model for p-channel CMOS is similar except for K'_p instead of K'_n.

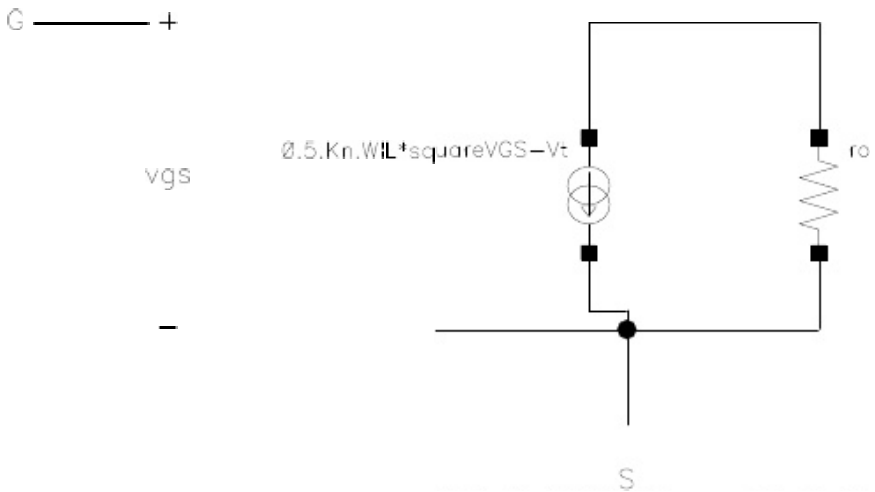


Figure 4.14: Large-Signal Equivalent Circuit Model in Saturation

For N-channel MOSFET to be in saturation:

1. $V_{GS} \geq V_t$
2. $V_{DS} \geq (V_{GS} - V_t)$

And the drain saturation current is given by:

$$I_D = \frac{1}{2} \cdot K_n\prime \cdot \frac{W}{L} \cdot (V_{GS} - V_t)^2$$

If $\beta = K'_n \cdot \frac{W}{L}$ Then,

$$I_D = \frac{1}{2} \cdot \beta \left(V_{GS} - V_t\right)^2 \tag{4.19}$$

For P-channel MOSFET to be in saturation:

1. $V_{GS} \leq V_t$
2. $V_{DS} \leq (V_{GS} - V_t)$

Equation 4.19 can be written as:

$$V_{GS} = \left(\frac{2I_D}{\beta}\right)^{\frac{1}{2}} + V_t \tag{4.20}$$

For the N-channel:

1. $V_{DS} \geq (V_{GS} - V_t)$. Now by substituting V_{GS}:
2. $V_{DS} \geq \left(\frac{2I_D}{\beta}\right)^{\frac{1}{2}}$

The large signal characteristics that are important include the Common-mode range, slew rate, and output signal swing

4.9 Slew Rate

The slew rate is defined as the maximum rate of change of the output voltage due to change in the input voltage. For this particular amplifier, the maximum output voltage is ultimately limited by how fast the tail current device M5 can charge and discharge the compensation capacitor, the slew rate can then be approximated as:

$$SR = \frac{dV_o}{dt}$$

$$SR \approx \frac{I_{D5}}{C_c}$$

Typically, the diff-amp is the major limitation when considering slew rate. However, the tradeoff issues again come into play. If I_{D5} is increased too much, the gain of the diff-amp may decrease below a satisfactory amount. If Cc is made too small then the phase margin may decrease below an acceptable amount.

4.10 The Common-Mode Range

Common-mode range is defined as the range between the maximum and minimum common-mode voltages for which the amplifier behaves linearly.

Referring to 4.15, suppose that the common mode voltage is DC value and that the differential signal is also shown. If the common mode voltage is swept from ground to V_{DD}, there will be a range for which the amplifier will behave normally and where the gain of the amplifier is relatively constant. Above or below that range, the gain drops considerably because the common-mode voltage forces one or more devices into the triode region.

The maximum common-mode voltage is limited by both M1 and M2 going into triode. This point can be defined by a borderline equation in which

(For M1, M2 to stay in saturation)

$$V_{D1,2} \geq (V_{G1,2} - V_{t1})$$

Now:

$$V_{D1} = V_{DD} - V_{SG3}$$

Therefore,

$$V_{G1} \leq V_{DD} - V_{G3} + V_{t1}$$

Substitute the value of V_{GS} from equation 4.20 and $V_{t3} = -ve$ value because it is p type CMOS:

$$V_{G1} \leq V_{DD} - \left(\frac{2I_{D3}}{\beta_3}\right)^{\frac{1}{2}} - V_{t3} + V_{t1}$$

Now since $I^{D3} = \frac{1}{2} I^{D5}$:

$$V_{G1} \leq V_{DD} - \left(\frac{I_{D5}}{\beta_3}\right)^{\frac{1}{2}} - V_{t3} + V_{t1} \tag{4.21}$$

$$V_{G1} \leq V_{DD} - \left[\frac{L_3 I_{D5}}{W_3 K_3}\right]^{\frac{1}{2}} - V_{t3} + V_{t1} \tag{4.22}$$

The minimum voltage is limited by M5 being driven into non-saturation by the common-mode voltage source.

$$V_{D5} \geq V_{SS} + V_{G5} - V_{t5}$$

$$V_{D5} = V_{G1,2} - V_{GS1,2}$$

Therefore,

$$V_{G1,2} - V_{GS1,2} \geq V_{SS} + V_{G5} - V_{t5}$$

$$V_{G1,2} \geq V_{SS} + V_{G5} - V_{t5} + V_{GS1,2}$$

Since, $V_{GS} = \left(\frac{2I_D}{\beta}\right)^{\frac{1}{2}} + V_t$ (From 4.20)
Therefore,

$$V_{G1,2} \geq V_{SS} + \left(\frac{2I_{D5}}{\beta_5}\right)^{\frac{1}{2}} + \left(\frac{I_{D5}}{\beta_1}\right)^{\frac{1}{2}} + V_{t5} - Vt5 + V_{t1}$$

$$V_{G1,2} \geq V_{SS} + \left(\frac{2I_{D5}}{\beta_5}\right)^{\frac{1}{2}} + \left(\frac{I_{D5}}{\beta_1}\right)^{\frac{1}{2}} + V_{t1}$$

$$V_{G1,2} \geq V_{SS} + \left[\frac{2L_5 I_{D5}}{W_5 K_5}\right]^{\frac{1}{2}} + \left[\frac{L_1 I_{D5}}{W_1 K_1}\right]^{\frac{1}{2}} + V_{t1} \qquad (4.23)$$

Determining the CMR for the two-stage Op-Amp (Figure 4.15).

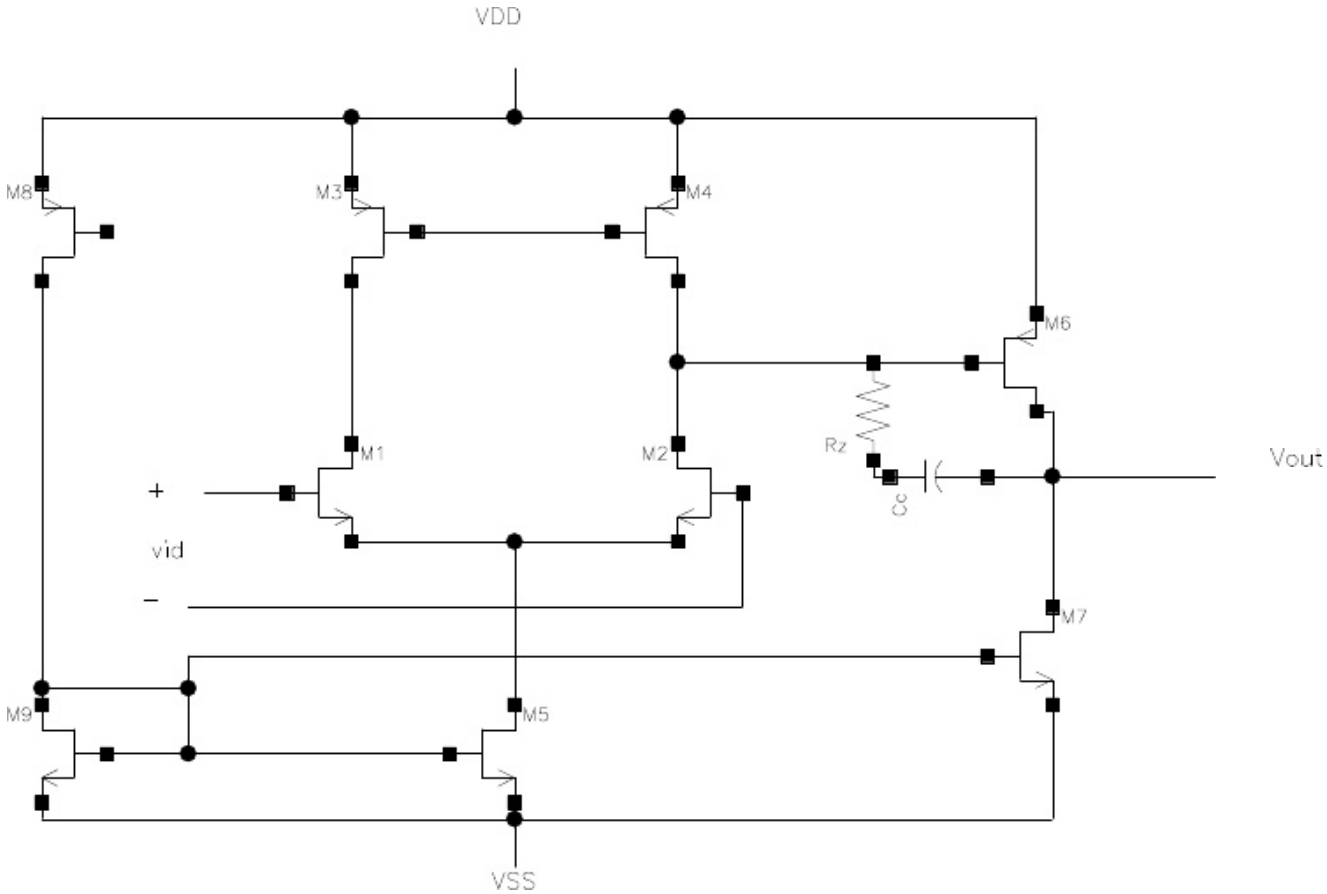


Figure 4.15: Determining the CMR for the Two-Stage Op-Amp

4.13 Design Methodology for the Two Stage Op-Amp

Design methodology is a topology dependent subject and it is highly dependent on the analysis of the circuit. The purpose on the design tool is not to replace the analysis completely. The analysis rather guides the designer's thoughts and while doing the design and helps to make the results of the design tool make sense.
The following design methodology is developed for the two stage Op-Amp analyzed above.

1. To define the requirements, set the specifications, and define the boundary conditions. Boundary conditions The TSMC 0.35 CMOS Technology is used. Process specifications: V_t , K', C_{ox}, ..etc. Because there are 12 models for N-FET and 12 models for P-FET automatically selected within Cadence tool so the process parameters cannot be determined at this stage.

   Supply voltage: $0 \rightarrow 3.3\ V$ Operating temperature: 0 to 70^o C, Requirements, Gain, GBW, CMRR Slew rate, Input common mode range: $V_{in}(min)$, $V_{in}(max)$, Output voltage swing: $V_{out}(max)$, $V_{out}(min)$, PSRR, Offset, Output Load.

2. Choose the smallest length that will keep the channel modulation parameter (constant and give good matching for current mirrors. The value used is 350nm

3. Design the two stages without C_c, R_z, or C_L, for the best dc response.

   Design the devices sizes for proper dc performance. It is important that before any AC analysis is performed, the values of the DC points in the circuit be checked to ensure that every device is in saturation. Failure to do so will result in very wrong answers. This step is accomplished as follows:

   (a) Calculate the minimum value for the compensation capacitor C_c.

   From 40: C^c 0.22 C^L. Get C^L from the requirements
   (b) Get the slew rate from the requirement and then calculate the minimum value for the tail current I_{D5} from: ID5 = SR. C_c

(c) Using cadence design tool, simulate the two stage amplifier with starting widths of: 800nm for n type devices, 1.9μm for p type devices. Get the circuit to work and test the DC response.

(d) Measure I_{D5}. Now try to optimize the Op-Amp for maximum gain by:

i. Measure the existing I_{D5}. To get the desired value of I_{D5} calculated in B, simultaneously change W5 and the width of the related devices:

$$W_{3,4} = 1.5W_5$$

$$W_6 = 6W_5$$

$$W_7 = 2W_5$$

ii. Check the operating points of all the devices (M1, M2, M3, M4, M5, M6, and M7) to make sure that the devices are in saturation. All design parameters can be known from Cadence by doing the following:

Affirma Window: Results → Print → DC Operating Points

iii. Increase the gain by increasing the size of $W^{1,2}$. You may perform parametric analysis for different width size. You can not decide on the final value of W1,2 at this point even you may get high gain, because of the trade off issues and the secondary effect, particularly on the phase margin which can not be measured till the ac analysis is performed.

iv. At this point you can extract the process parameters: V_t, K, C_{ox} ...etc. Knowing K for the devices is now important to calculate V_G(min) and $V_{G1}(max)$ to make sure that M1, M2, M3, M4 and M5 are not operating near the boundary, 4.22,4.23 causing one of the devices to operate outside the saturation region.

v. If any of the devices are brought out of saturation or are working at the minimum condition required for saturation, then it should be brought back to saturation.

vi. Repeat 1-4 until all the transistors are in saturation while the dc gain is increased.

(e) Measure the CMR and the gain. Compare with the required specifications.

4. (a) Add up C_c and C_L to the amplifier. The value of C_L is from the specifications while the value of C^c is previously calculated in Step3-A

(b) Check the phase margin condition (4.18), as now you can know all the process parameter from cadence.

(c) Verify that the phase margin is $> 45^o$ by measuring it using the procedure in 4-4.

(d) If the phase margin is not $> 45^o$ then it should be corrected by changing the value of C^c or R^2, referring to (4.15, 4.18). A parametric analysis may be preformed for different C_c sizes.

(e) Calculate the slew rate according to the new Cc value that makes the phase margin $> 45^o$. If it is less than the specification then perform the following steps:

i. Calculate the required I_{D5} from (22). Substitute the last value of C_c and the required SR.

ii. Perform DC analysis only and return back to Step3-D, with the desired value of I_{D5} as calculated above.

5. (a) Calculate the required R_z using (4.14)

(b) Add R_z to the circuit and perform an AC analysis. Check the difference in the phase response.

6. Measure the slew rate, GBW, P2 and the phase margin. Compare with the specifications.

4.14 Design Example

Figure 4.16 shows a two stage op-amp designed using the above design methodology and optimized for maximum gain. Figure 4.17 shows the gain for the large signal consideration(DC response). Figure 4.18 shows the frequency response. Figure 4.19 shows the phase margin measurements.

Figure 4.16: Two-Stage Op-Amp using design Methodology

Figure 4.17: Gain for the Large Signal Analysis

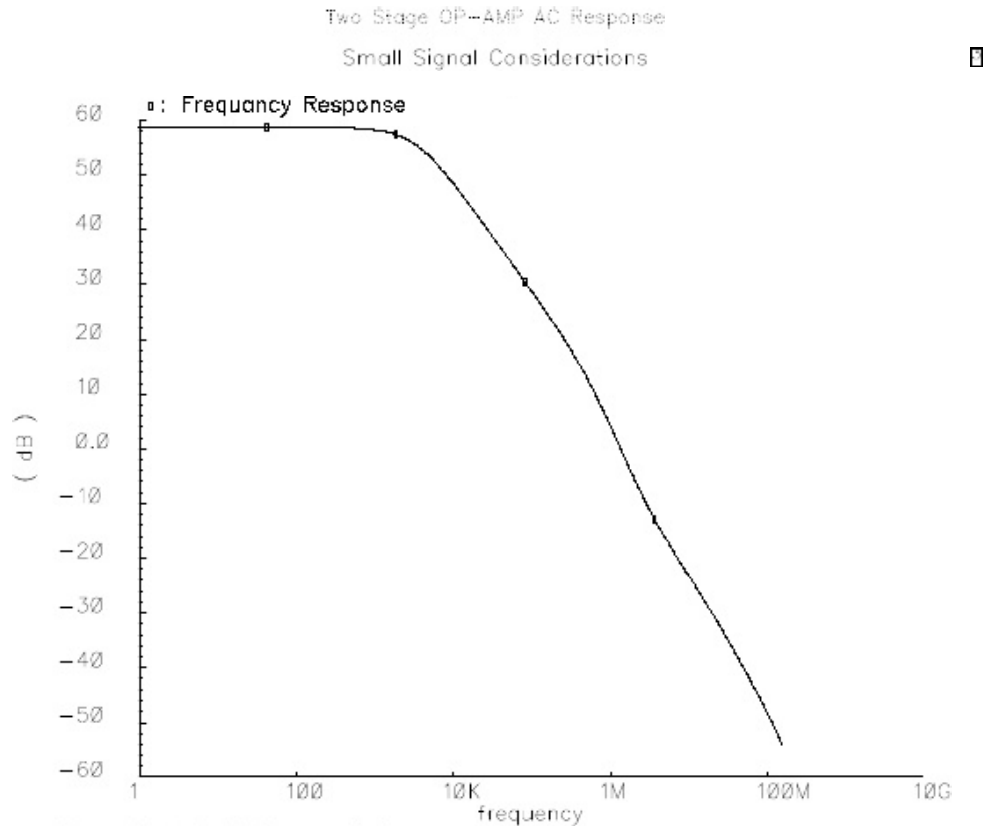


Figure 4.18: Frequency Response

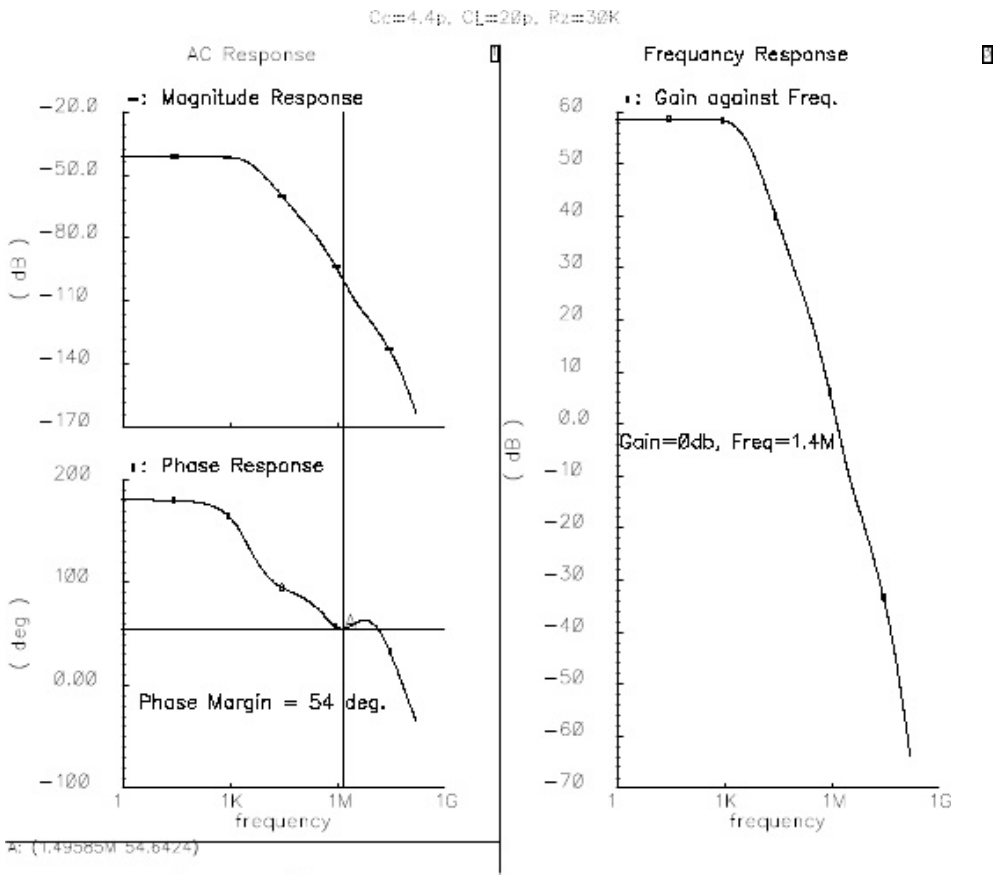


Figure 4.19: Phase Margin

4.15 Limitations of the Two Stage Op-Amp

1. Insufficient gain
2. Limited stable bandwidth caused by the instability to control the higher order poles of the op-amp.
3. Poor power supply rejection ratio.

4.16 The Cascode Op-Amp

The motivation for using the cascode configuration to increase the gain can be seen by examining how the gain of the two-stage op-amp could be increased. There are three ways in which the gain of the two stage op-amp could be increased:

1. Add additional gain stage
2. Increase the transconductance of the first or the second stage.
3. Increase the output resistance seen by the first or second stage.

Due to possible instability, the first approach is not attractive. Of the latter two approaches, the third is the more attractive way because the output resistance increases in proportion to a decrease current [$r_o = 1/\lambda$], whereas the transconductance increases as the square root of the increase in bias current [$g_m = (2 * B * I_D)^1/2$]. Thus it is generally more efficient to increase ro rather than g_m.

Figure 4.20 shows a cascode differential stage. Figure 4.21 shows the DC response for an unoptimized configuration to serve as indication for the whole project and to help in deciding about the best input stage to be considered in the final op-amp design. The transistors Mc1 and Mc2 perform the resistance multiplication, while Mc3 is used to keep the drain voltage of the input transistor matched, which helps to reduce the voltage offset.

Rout ([gmc2 . roc2 . ro4] —— [gmc1. roc1. ro2]. A = gm1.R_{out}

One of the disadvantages of this design is the requirement for the additional bias voltages V_{B1}, V_{B2}. Further more, the common mode input range is reduced due to the extra voltage drop required by the two cascode devices, Mc1, Mc2. In many cases, the CMR limitation is not important since the non-inverting input of the op-amp will be connected to ground.

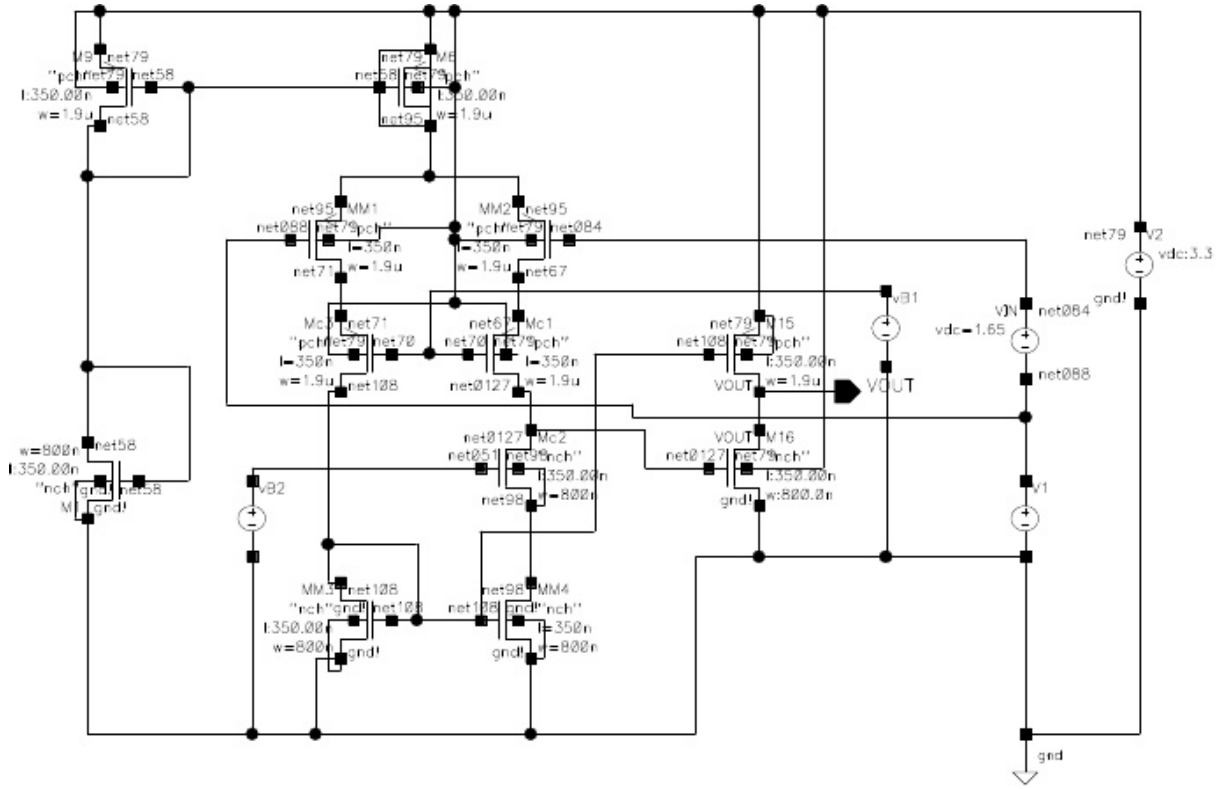


Figure 4.20: Cascode Differential Stage

Folded Cascode Op-Amp Figure 4.22 shows a folded cascode differential stage. Figure 4.23 shows the DC response for an unoptimized configuration to serve as indication for the whole project and to help in deciding about the best input stage to be considered in the final op-amp design.

This circuit uses a current-folding circuit technique to permit direct connection of the drains of the p-channel differential amplifier to the sources of the cascode devices. This requires two additional transistors (M5 and M6), operate in much the same manner as the previous cascode circuit. Here however, the input common-mode range is larger because only three transistors are now stacked in the input chain between the two power supplies (as compared to five in the conventional cascode circuit). The folded cascode circuit is frequently used as a single-stage op-amp. Its voltage gain can be determined as: A = gm1 R^o Where Ro is the output resistance: R^o = [gmc1. roc1(ro6———ro2)] ——— [gmc2. roc2. ro3)]

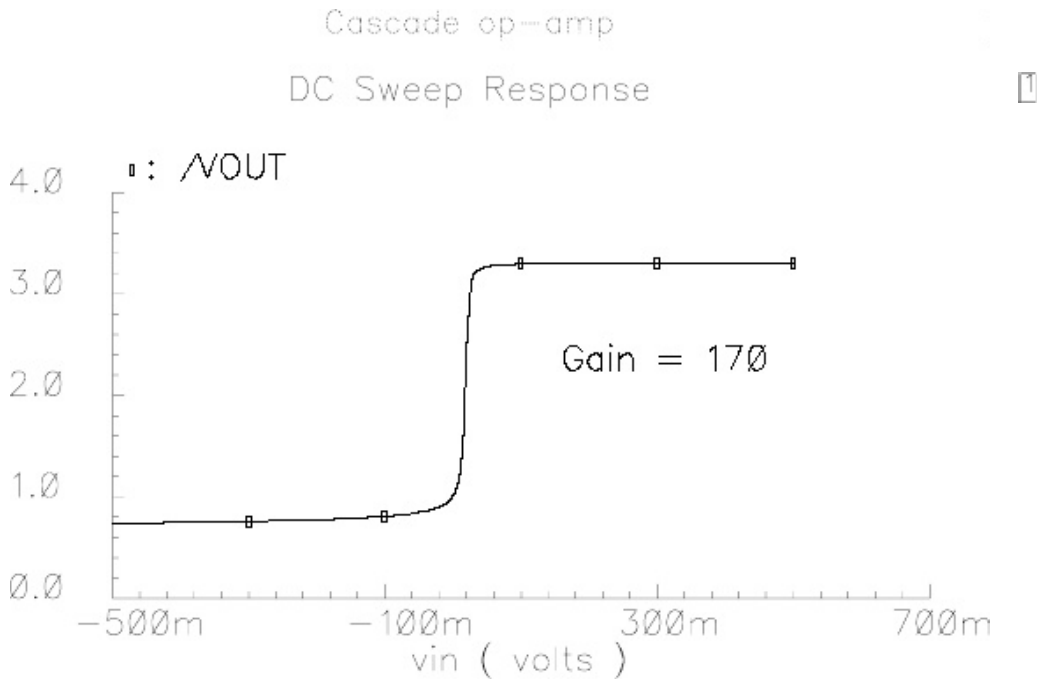


Figure 4.21: DC Response for Unoptimized Circuit

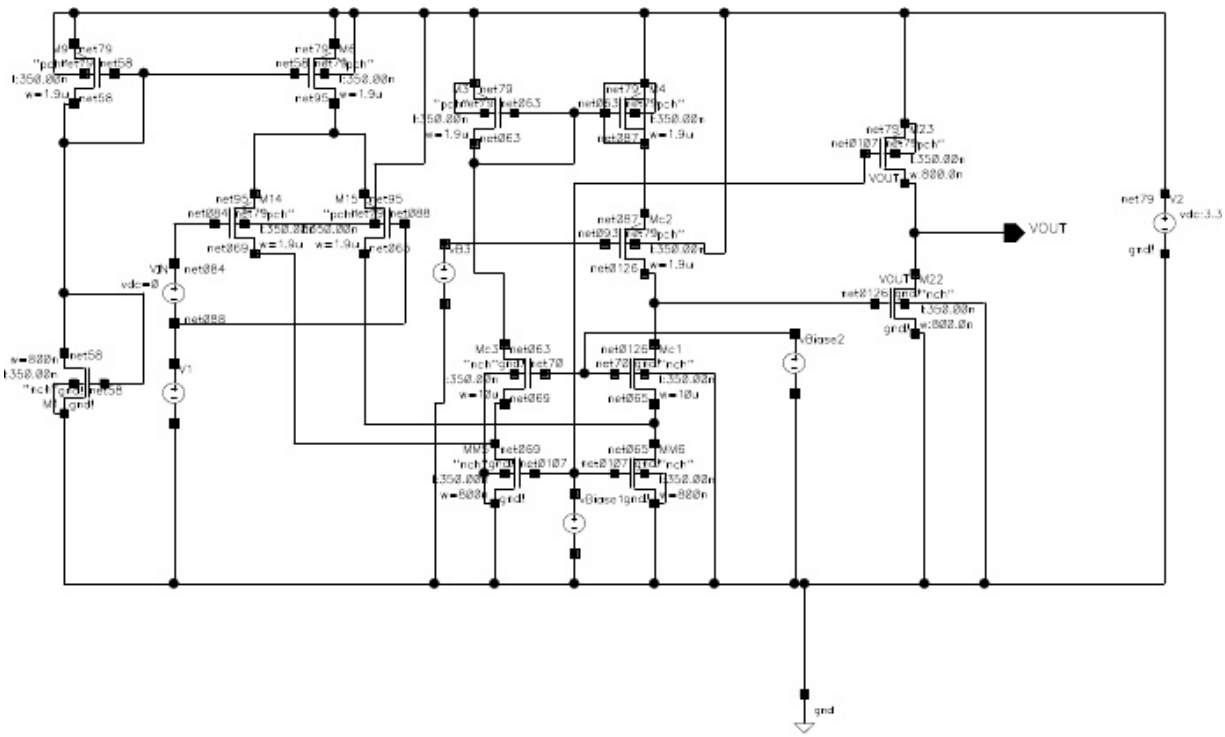


Figure 4.22: Folded Cascode Differential Stage

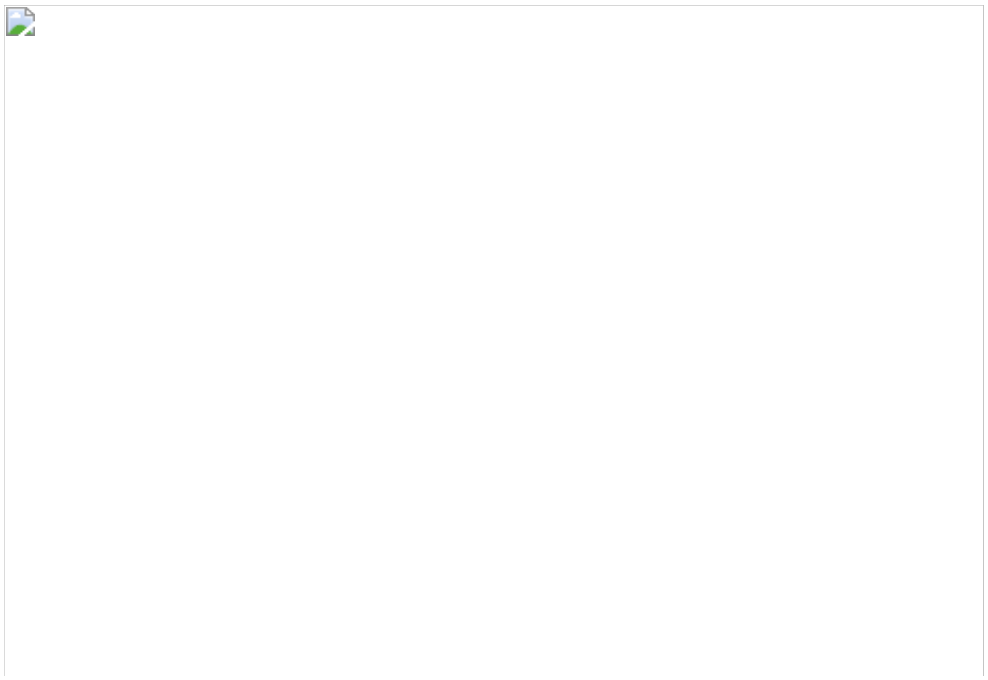


Figure 4.23: DC Response for Unoptimized Circuit

Chapter 5

Inverting Amplifiers

In this section, we introduce an important configuration that is extensively employed in the design of integrated circuits: the inverting amplifier. The inverting amplifier is also called common-source amplifier or inverter. It is usually used as the basic gain stage for CMOS circuits. Later we will see that inverter is used in the gain stage of the final circuit.

Typically, the inverter has three kinds of configurations. The first one uses the common-source configuration with an active resistor as a load. The second one uses a current sources/sink as an active load. The third one uses the input voltage to control both the amplifying transistor and the load transistor, this configuration is also known as push-pull amplifier. In this section, the three configurations will be discussed respectively in terms of their output swing, small-signal voltage gain, input and output resistance and -3 dB frequency.

5.1 Inverter with Active Resistor Load

The typical circuit of the first type has been shown in Figure 5.1. This circuit uses a common-source, N-channel transistor M1 with a P-channel transistor M2 as the load of M1.

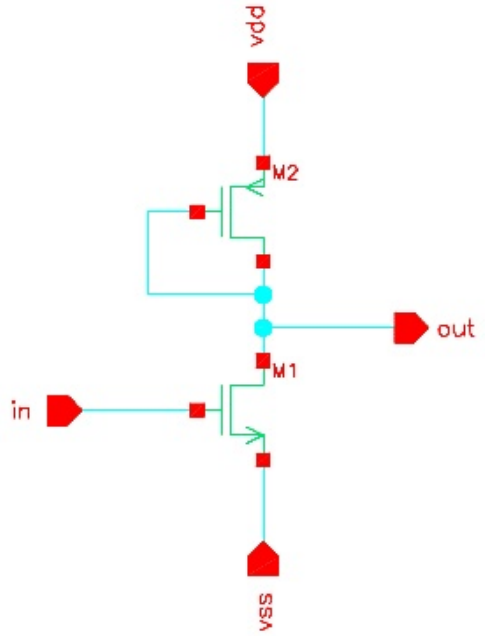


Figure 5.1: Simple Inverter Circuit

The parameters of the circuit are as follows: $V_{DD} = 3.3V$, $V_{SS} = 0V$; $W_1 = 10.8\mu m$, $L_1 = 10\mu m$, $V_{TN} = 0.5V$; $W_2 = 28\mu m$, $L_2 = 10\mu m$, $V_{TP} = -0.7V$. We set the operating point at 1.65V and DC current at $106.7\mu A$, so $V_{gs1} = 1.65V$, $I_{d1} = 106.7\mu A$, $I_{d2} = \quad 106.7\mu A$ Under these conditions, $V_{ds1} = 1.365V$ $V_{ds2} = V_{gs2} = -1.935V$. –Thus we can calculate β_1 and β_2 which we will need for future calculations. Since

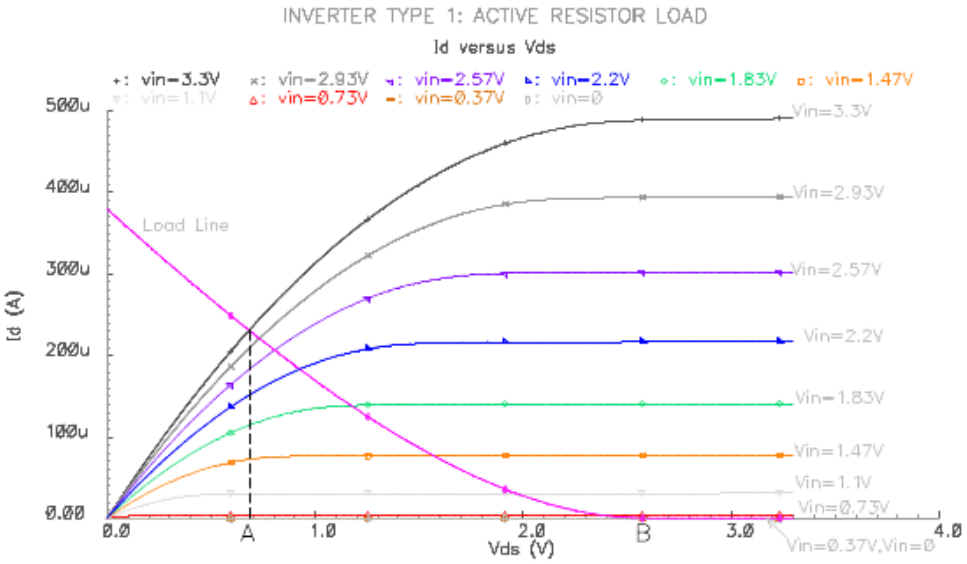
$$\begin{aligned} I_{d1} &= \frac{\mu_N C_{ox} W_1}{2L_1} (V_{gs1} - V_{TN})^2 \\ 106.7 \cdot 10^{-6} &= \frac{\mu_N C_{ox} W_1}{2L_1} (1.65 - 0.5)^2 \end{aligned}$$

So $\beta_1 = \frac{\mu_N C_{ox} W_1}{2L_1} = 171.6\mu A/V^2$, $K_p\prime = \mu_p C_{ox} = 52.9\mu A/V^2$
Use the same way, we have:

$$\beta_2 = \frac{\mu_P C_{ox} W_2}{L_2} = 148.2\mu A/V^2, \; K_p\prime = \mu_P C_{ox} = 52.9\mu A/V^2$$

1. **Transfer Characteristics**

Figure 5.2 illustrates the Cadence simulation result of the large-signal characteristics of this circuit. This plot shows the I_d versus V_{ds} characteristics of M1 and the "load line" plotted on the same graph. The volta



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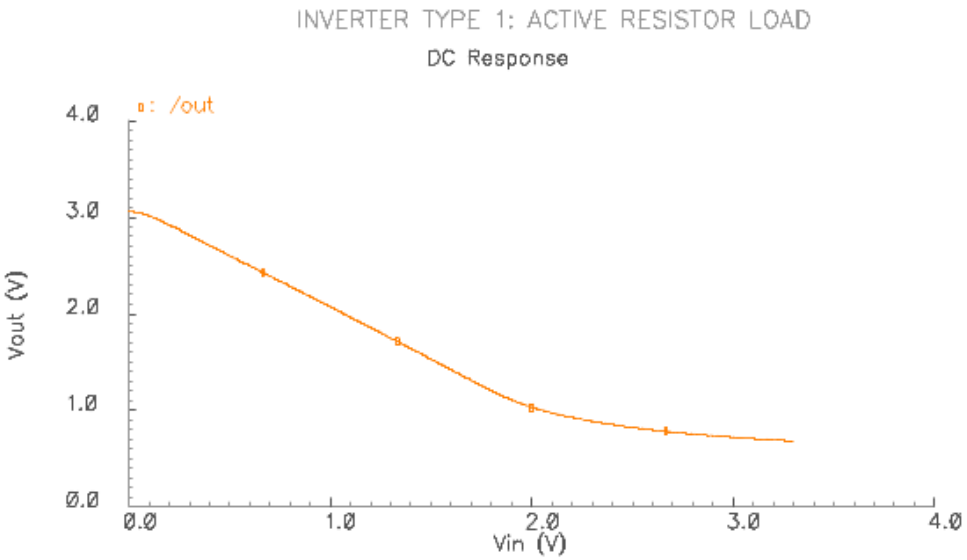

Figure 5.3: Voltage-Transfer Curve

From these figures, we can observe that this type of inverting amplifier has low gain since the slope of the V_{out} versus V_{in} is small.

2. **Output Swing**

From these curves, it is obvious that this inverter has limited output voltage range (point A and point B in Figure 5.2). We will find the maximum output voltage and minimum output voltage.

With the gate and drain connected together, M2 always works in the saturated region as long as $\mid V_{ds2} \mid > \mid V_{TP} \mid$, and $V_{ds2} = V_{gs2} = \mid V_{TP} \mid + \sqrt{\frac{2I_{d2}}{\beta_2}}$. When V_{in} is zero, M1 is cutoff, and the drain current of M1 I_{d1} is also zero, $V_{ds2} = \mid V_{TP} \mid$. So $V_{out}(max)$ is approximately equal to:

$$V_{out}(max) = V_{DD} - \mid V_{TP} \mid = 3.3 - 0.7 = 2.6(V)$$

When V_{in} increases until $V_{in} > V_{TN}$, M1 conducts, and V_{out} begins to drop. When $V_{out} > V_{in} - V_{TN}$, M1 enters saturated region. When V_{out} further drops until $V_{out} < V_{in} - V_{TN}$, M1 enters non-saturated region. This is the region where the minimum output voltage happens. Since M1 is in non-saturated region, the drain current of M1 should be:

$$I_{d1} = \beta_1 \left[(V_{DD} - V_{SS} - V_{TN})(V_{out} - V_{SS}) - \frac{(V_{out} - V_{SS})^2}{2} \right]$$

Because M2 is in saturated region, the drain current of M2 should be:

$$I_{d2} = \frac{\beta_2}{2} (V_{DD} - V_{out} - \mid V_{TP} \mid)^2$$

Equating the above two equations, and simplifying $V_{TN} = \mid V_{TP} \mid = V_T$ in order to simplify the calculation. We can get the approximate value of $V_{out}(min)$.

$$\begin{aligned} V_{out}(min) &\approx V_{DD} - V_T - \frac{V_{DD} - V_{SS} - V_T}{\sqrt{1 + \frac{\beta_2}{\beta_1}}} \\ &= 3.3 - 0.5 - \frac{3.3 - 0.5}{\sqrt{1 + \frac{148.2}{171.6}}} = 0.7\ V \end{aligned}$$

You may notice that in Figure 5.3, the $V_{out}(max)$ is around 3V, different from our calculation. This is because the subthreshold effect of transistors. We usually suppose that no current flows in transistors when $V_{in} < V_{TN}$. But in reality, there is current conducting through transistors when $V_{in} < V_{TN}$, and I_d has an exponential relationship with V_{ds} at this region. This is called subthreshold effect. It is this

effect that results in the difference between our calculation and the simulation result.

3. **Small-Signal Voltage Gain.**

There are two methods to calculate the small-signal voltage gain.

(a) The principle of the first method is this: the gain is found when M1 works in saturated region, and the drain current of M1 and M2 are always equal. Therefore, I_{d1} is:

$$I_{d1} = \frac{\beta_1}{2}\left(V_{in} - V_{SS} - V_{TN}\right)^2$$

and since M2 always operates in saturation, I^{d2} is:

$$I_{d2} = \frac{\beta_2}{2}\left(V_{DD} - V_{out} - V_{TP}\right)^2$$

Equating the above equations. Because A_V is the derivative of $\frac{V_{out}}{V_{in}}$, we have

$$A^V = \frac{\partial V_{out}}{\partial V_{in}} = -\left(\frac{\beta_1}{\beta_2}\right)^{\frac{1}{2}} = -\left(\frac{K'_N \frac{W_1}{L_1}}{K'_P \frac{W_2}{W_1}}\right)^{\frac{1}{2}}$$

(b) . del. The r load is

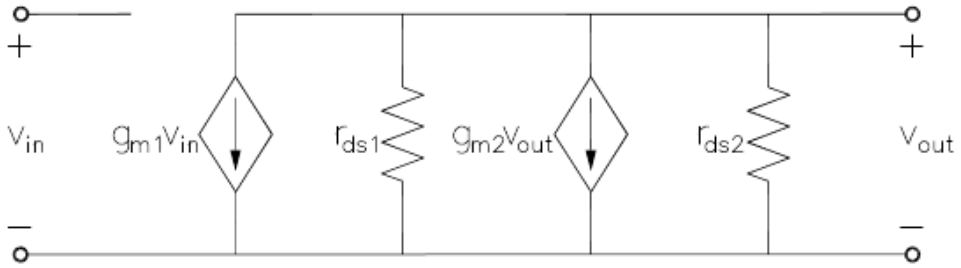

Figure 5.4: Inverter: Small-Signal Model

The gain can be expressed as:

$$A_V = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{m2} + g_{ds2}} \cong -\left(\frac{K'_N \frac{W_1}{L_1}}{K'_P \frac{W_2}{L_2}}\right)^{\frac{1}{2}}$$

where $g_{m2} \gg g_{ds1}, g_{ds2}$.

We get the same results from the two methods. According to the Cadence simulation result, $g_{m1} = 172\mu$, $g_{m2} = 155.5\mu$, so $A_V = 1.1$, which is a fairly low gain. So this type of inverter is suitable for situations where low-gain inverting stage is desired. Besides, we can see from the A_V expression that in order to improve the gain, we can either increase the ratio of $\frac{W_1}{L_1}$ or decrease the ratio of $\frac{W_2}{L_2}$.

4. **Input and Output Resistance**

From the small-signal model, we can find that the input and output resistance is

$$\begin{aligned} r_{in} &= \infty \\ r_{out} &= \frac{1}{g_{ds1} + g_{m2} + g_{ds2}} \cong \frac{1}{g_{m2}} = \frac{1}{155.5 \cdot 10^{-6}} = 6.4\ k\Omega \end{aligned}$$

We can see that the output resistance of the active-resistor load inverter is low because of the diode-connected transistor M2. The resulting low output resistance can be very useful in situations where a large bandwidth is the main expectation from an inverting gain stage.

5. **Upper -3 dB Frequency**

When discussing the frequency response of the inverter, we need to take the internal capacitors into consideration. Figure 5.5 illustrates the resulting small-signal model.

$$\begin{aligned} C_1 &= C_{gs1} \\ C_2 &= C_{bd1} + C_{gs2} + C_{bd2} \\ C_3 &= C_{gd1} \\ r_2 &= r_{out} = \frac{1}{g_{out}} \\ r_1 &= r_{in} = \infty \end{aligned}$$

Using nodal analysis, we may write:

$$V_{out}(s)(g_{out} + sC_2) + C_3\left[V_{out}(s) - V_{in}(s)\right] + g_m V_{in}(s) = 0,$$

where $s = j\omega$

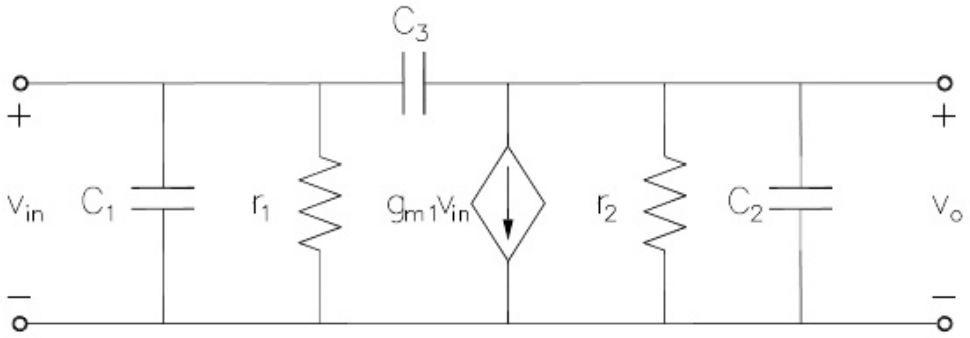

Figure 5.5: Inverter: Small-Signal Model

So the transfer function $\frac{V_{out}(s)}{V_{in}(s)}$ is:

$$A_V(s) = -\frac{g_m\left[1 - s\left(\frac{C_3}{g_m}\right)\right]}{g_{out}\left(1 + s\left[\frac{(C_2+C_3)}{g_{out}}\right]\right)} = A_{VM}\frac{1-\frac{s}{Z_1}}{1+\frac{s}{P_1}} \tag{5.1}$$

where A_{VM} is the midband gain, Z_1 is the zero and P_1 is the pole and

$$A_{VM} = -\frac{g_{m1}}{g_{out}} = \frac{-g_{gm1}}{g_{ds1} + g_{m2} + g_{ds2}}, \quad Z_1 = \frac{g_{m1}}{C_2}, \quad P_1 = \frac{-g_{out}}{C_2 + C_3}$$

From this formula, we find that inverter has a first-order transfer function. So the -3 dB frequency can be written as:

$$\omega_H = \frac{g_{out}}{C_2 + C_3} = \frac{g_{m2} + g_{ds1} + g_{ds2}}{C_{db1} + C_{gd1} + C_{gs2} + C_{db2}} \tag{5.2}$$

From this equation, we can get to the conclusion that the -3 dB frequency of the active resistor load inverter is approximately proportional to the square root of the drain current. So in order to increase the bandwidth, we can increase the drain current because r_{out} will decrease. Unfortunately, this will also decrease the gain.

Lacking of accurate values of these capacitors, we cannot calculate an accurate value of the -3 dB frequency. But it still can be found from the frequency response because -3 dB frequency is the point where the gain drops to $0.707A_V$. Simulation results of the frequency response of the active-resistor load inverter is shown in Figure 5.6. From this curve, we determine the -3 dB frequency to be 26.12MHz, which is a fairly wide bandwidth.

Figure 5.6: Frequency Response of the Active-Resistor Load Inverter

5.2 Inverter with Current Source/Sink Load

The second type of inverter uses active load. There are a number of ways to configure active load, such as cascade current sink, current mirror, reduced cascade current sink and so on. Here we will use current mirror. The circuit is shown in Figure 5.7.

In order to compare the performances of this type with the first one, set the operating point the same as the first one, i.e. $V_{gs1} = 1.65V$, $I_{d1} = 106.7\mu A$, $V_{gs2} = -1.935V$, $I_{d2} = -106.7\mu A$, $I_{d3} = I_{d4} = 106.7\mu A$.

From

$$I^d = \frac{\mu C_{ox} W}{2L} (V^{gs} - V^T)^2, \; K^{'N} = 158.9\mu A/V^2, \; K^{'P} = 52.0\mu A/V^2$$

We can calculate out:

$$\begin{aligned} W_1 &= 10.8\mu m; L_1 = 10\mu m; W_2 = 28\mu m; L_2 = 10\mu m; \\ W_3 &= 28\mu m; L_3 = 10\mu m; W_4 = 18.5\mu m; L_4 = 10\mu m \end{aligned}$$

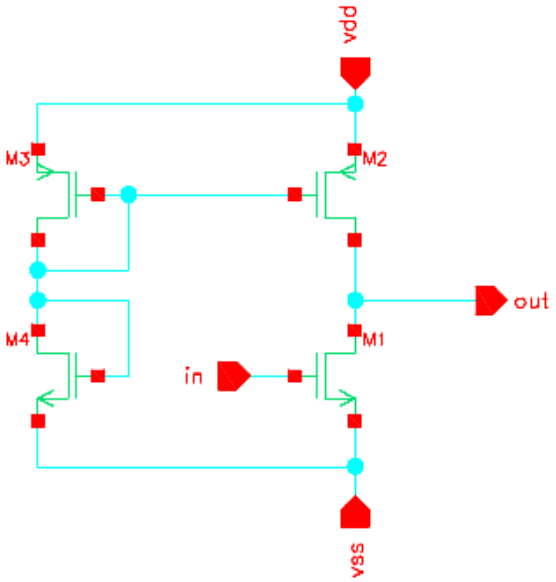

Figure 5.7: Inverter Circuit with Current Source/Sink Load

1. Output Swing.

   The large-signal characteristics and voltage-transfer curve are respectively

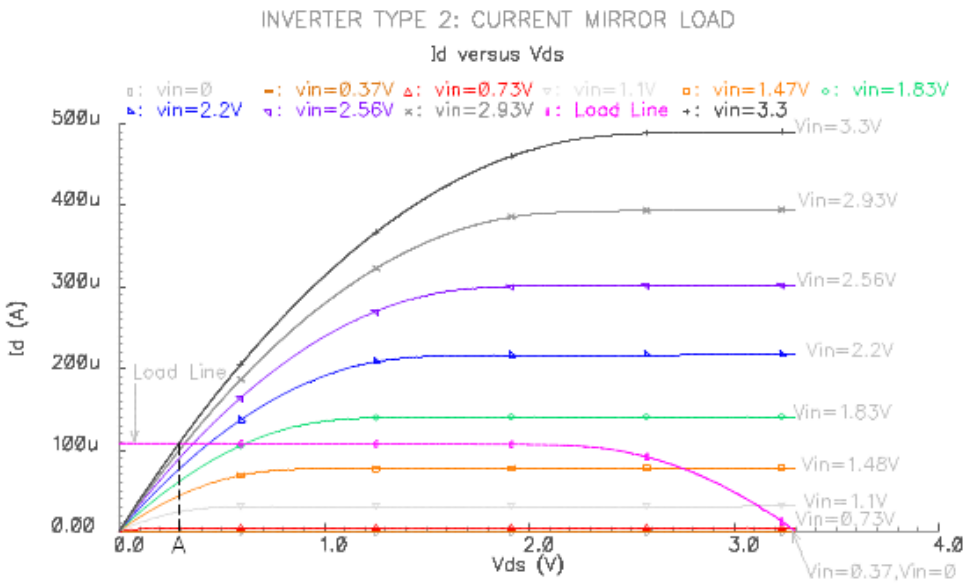

Figure 5.8: Inverter Type 2: Parametric Analysis sweeping V^{in}

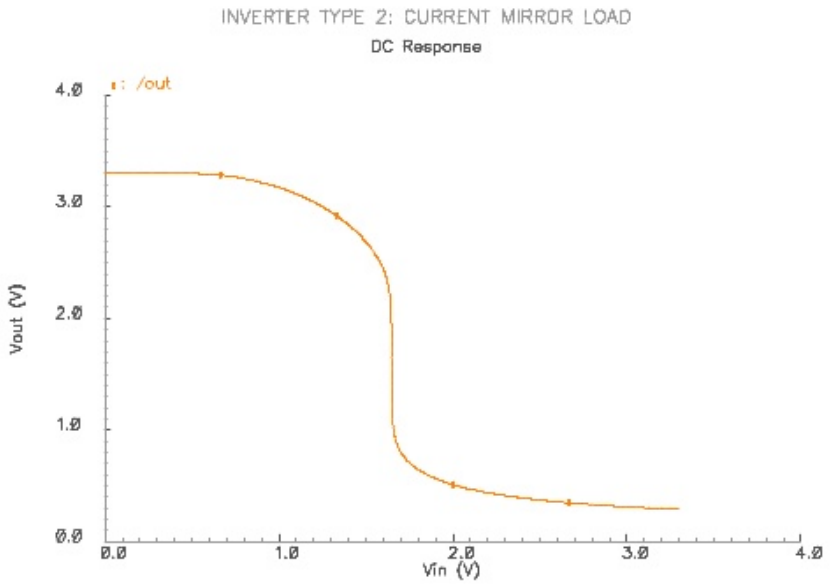

Figure 5.9: Voltage-Transfer Curve

Observing these curves, we can find that this type of inverter still experiences the limitation for output swing(point A in Figure 5.8). This limitation can be found by a method similar to that used for the active resistor inverter.

Basically, we can divide the transfer curve into four distinct segments. In segment 1, $V_{in} < V_{TN}$, M1 is cutoff. M2 is conducted, but there is no current. So $V_{out}(max)$ is equal to V_{DD} since M2 can pull output voltage up to V_{DD} . In segment 2, V_{in} increases to $V_{in} > V_{TN}$, M1 begins to conduct, and V_{out} decreases as V_{in} increase. M2 works in non-saturation region. In segment 3, V_{in} further increases, making both M1 and M2 operates in saturation. V_{out} dropped quickly. The transfer curve is almost linear and very steep, indicating large voltage gain. In segment 4, V_{in} increases to $V_{in} > V_{out} + V_{TN}$, and M1 enters non-saturation region. This is the segment where $V_{out}(min)$ happens. From the above analysis, we can see that $V_{out}(max) = V_{DD} = 3.3\ V$, and the lower limit can be found when M1 is in the non-saturation

region. $V_{out}(min)$ can be written as

$$\begin{aligned} V_{out} &= (V_{DD} - V_{TN}) \left\{ 1 - \left[1 - \frac{\beta_2}{\beta_1} \frac{V_{DD} - (V_{DD} - V_{gs2}) - \mid V_{TP} \mid}{V_{DD} \quad V_{TN}} \right]^2 \right. \\ &= (3.3 - 0.5) \left\{ 1 - \left[1 - \left(\frac{148.2}{171.7} \right) \left(\frac{3.3 - 1.365 - 0.7}{3.3 - 0.5} \right)^2 \right]^{\frac{1}{2}} \right\} \\ &= 0.3\ V \end{aligned}$$

2. Small Signal Voltage Gain

The small signal model Figure 5.10:

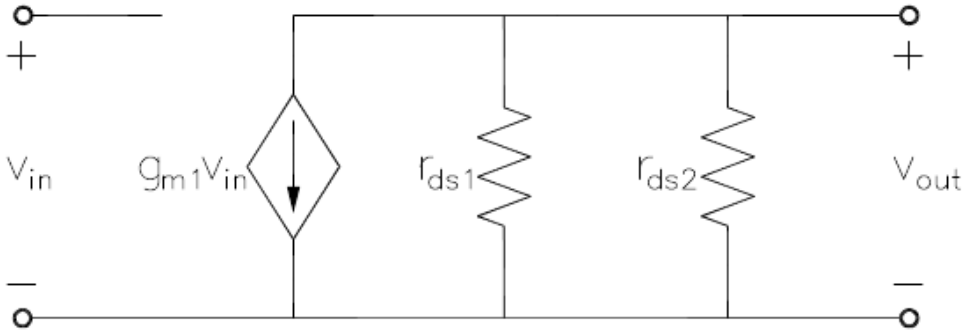

Figure 5.10: Inverter Type 2: Small Signal Model V_{in}

The gain can be expressed as

$$A_V = \frac{v_{out}}{v_{in}} = -g_{m1} \left(r_{ds1} \| r_{ds2} \right) = \frac{-g_{m1}}{g_{ds1} + g_{ds2}}$$

Because $g_{ds1} = \lambda_1 I_d$,$g_{ds2} = \lambda_2 I_d$ and $g_{m1} = \sqrt{2\beta_1 I_d}$

$$A_V = -\sqrt{\frac{2\mu_N C_{os} W_1}{L_1 I_d}} \left(\frac{1}{\lambda_1 + \lambda_2} \right)$$

Here we notice a significant result. The gain increases as the DC operating current decreases. This occurs because the output conductance r_{ds1} and r_{ds2} is inversely proportional to the current whereas the transconductance g_{m1} is proportional to square root of the bias current. So we can increase the gain of this type of inverter by decreasing

the biasing current I_d. According to the Cadence simulation result, $g_{m1} = 172.3\mu$, $g_{ds1} = 392.3n$, $g_{ds1} = 855.9n$, so

$$A_V = \frac{g_{m1}}{-g^{ds1} + g^{ds2}} = \frac{172.3 \cdot 10^{-6}}{-392.3 \cdot 10^{-9} + 855.9 \cdot 10^{-9}} = 137.6$$

3. Output Resistance.

   From the small-signal model, we can find that the output resistance is

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}} = \frac{1}{392.3 \cdot 10^{-9} + 855.9 \cdot 10^{-9}} = 0.8M\Omega$$

   From these calculation results, we can see that under the same biasing conditions, this current source load inverter has a much higher gain and output resistance when comparing to the active resistor load inverter. But you will see soon that the high output resistance results in a narrow bandwidth.

4. -3 dB Frequency. The frequency response can be found by using Figure 5.5. But in this case, C is

$$\begin{aligned} C_1 &= C_{gs1} + C_{gs2} \\ C_2 &= C_{db1} + C_{db2} \\ C_3 &= C_{gd1} + C_{gd2} \end{aligned}$$

   So -3 dB frequency is

$$\omega^H = \frac{g_{out}}{C_2 + C_3} = \frac{g_{ds1} + g_{ds2}}{C_{db1} + C_{gd1} + C_{gd2} + C_{bd2}} \tag{5.4}$$

   Simulation result of the frequency response of this inverter is shown in Figure 5.11. From this curve, we measure the -3 dB frequency is 3.75MHz, which is a lower frequency compared to the active resistor load inverter. This is due to the higher output resistance.

5.3 Push-Pull Inverter

One of the disadvantages of the current source inverter introduced above is that it requires a biasing voltage. If the gate of M2 in Figure 5.7 is taken to the gate of M1, the push-pull CMOS inverter is achieved. In this circuit,

Figure 5.11: Frequency Response of the Inverter with Current Source/Sink Load

Figure 5.12: Push-Pull Inverter Circuit

both biasing and amplifying transistors are driven by the input signal. The typical circuit is shown in Figure 5.12.

Still, like the above two circuits, set the operating point at 1.65V, i.e. $V_{gs1} = 1.65V$, $I_{d1} = 106.7\mu A$, $V_{gs2} = -1.65V$, $I_{d2} = -106.7\mu A$ From

$$I_d = \frac{\mu C_{ox} W}{2L} (V_{gs} - V_T)^2, \quad K'_N = 158.9\mu A/V^2, \quad K'_P = 52.9\mu A/V^2$$

We can get,

$$W_1 = 10.8\mu m, \quad L_1 = 10\mu m, W_2 = 48.1\mu m, L_2 = 10\mu m;$$

1. Output Swing.
The large-signal characteristics and voltage-transfer curve are respectively illustrated in Figure 5.13 and Figure 5.14

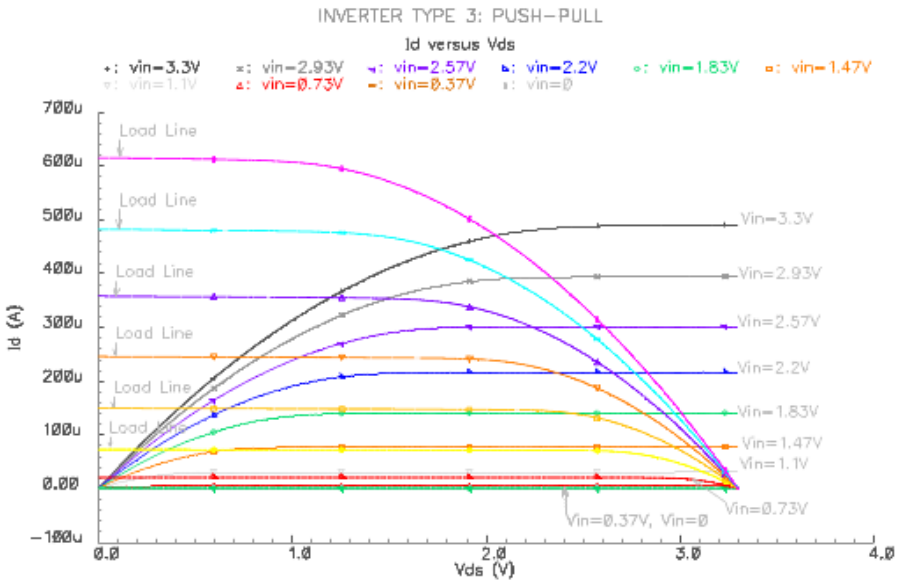

Figure 5.13: Inverter Type 3: Parametric Analysis Sweeping V_{in}

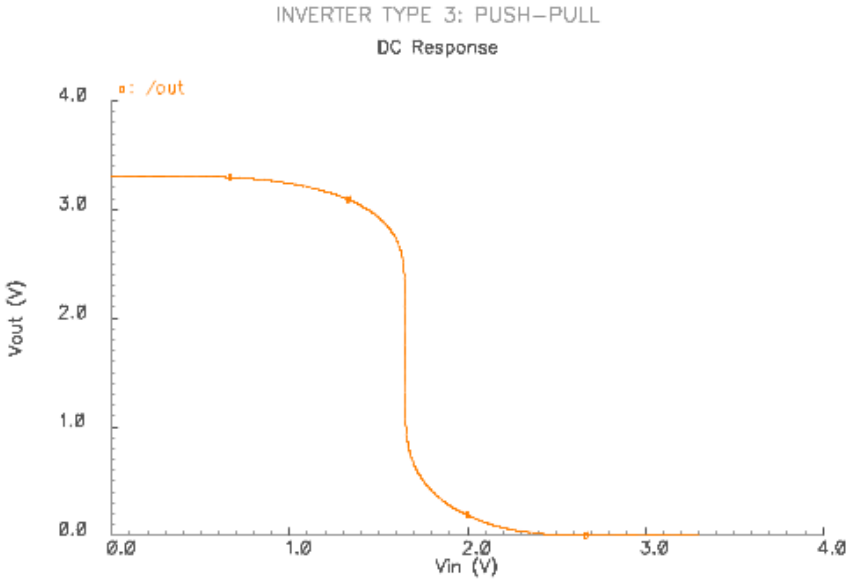

Figure 5.14: Voltage-Transfer Curve

Comparing the large-signal voltage transfer characteristics between the current-mirror and push-pull inverter, it is seen that this type of inverter shows two advantages. First, the push-pull inverter will have a higher gain. This is due to the fact that both transistors are being driven by V^{in}. Second, the output swing of push-pull inverter is capable of operating from V_{DD} to V_{SS}, whereas a current mirror inverter cannot drive all the way to V_{SS}.

2. Small Signal Voltage Gain.

The small-signal voltage gain can be found from its small-signal model Figure 5.15.

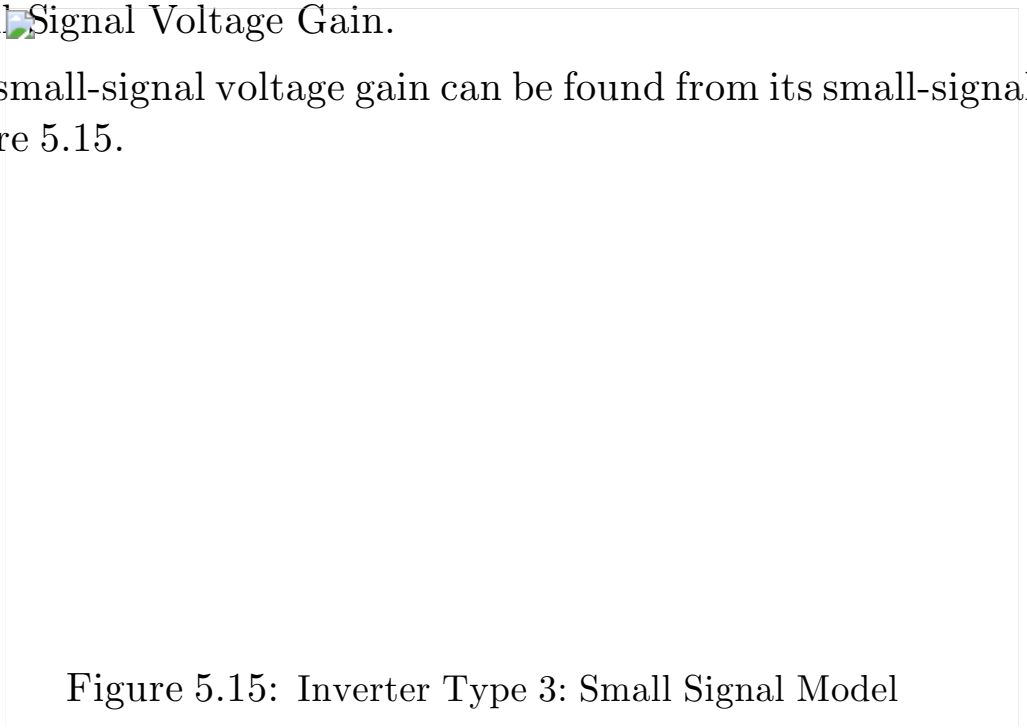

Figure 5.15: Inverter Type 3: Small Signal Model

The small-signal voltage gain can be expressed as

$$A_V = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}}$$

Because $g_{ds1} = \lambda_1 I_d$, $g_{ds2} = \lambda_2 I_d$, $g_{m1} = \sqrt{2\beta_1 I_d}$ and $g_{m2} = \sqrt{2\beta_2 I_d}$:

$$A_V = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} = -\frac{(2\beta_1)^{\frac{1}{2}} + (2\beta_2)^{\frac{1}{2}}}{(\lambda_N + \lambda_P)\sqrt{I_d}} \tag{5.5}$$

From this equation, we can get to the conclusion that the small-signal voltage gain of pull-pull inverter is inversely proportional to the square root of DC current. In order to increase gain, we can decrease the DC operating current. This is the same as the current mirror inverter. According to the Cadence simulation result, $g_{m1} = 172.1\mu$, $g_{ds1} = 547.7n$, $g_{m2} = 208.2\mu$, $g_{ds1} = 761.4n$, so

$$A_V = \frac{v_{out}}{v_{in}} = -\frac{g_{m1} + g_{m2}}{g_{ds1} + g_{ds2}} = -\frac{172.1 \cdot 10^{-6} + 208.2 \cdot 10^{-9}}{547.7 \cdot 10^{-9} + 761.4 \cdot 10^{-9}} = -290.5$$

This result shows that under the same DC current, push-pull inverter has a much higher gain than the other two types.

3. Output Resistance and -3 dB Frequency ω_H.

   From the small-signal model, we can find that the output resistance and -3 dB frequency are the same as the current mirror inverter, which are

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2}}$$

   and

$$\omega_H = \frac{g_{out}}{C_2 + C_3} = \frac{g_{ds1} + g_{ds2}}{C_{bd1} + C_{gd1} + C_{gd2} + C_{bd2}}$$

   In this case,

$$r_{out} = \frac{1}{547.7 \cdot 10^{-9} + 761.4 \cdot 10^{-9}} = 0.76\ M\Omega$$

   Simulation result of the frequency response of the push-pull inverter is shc

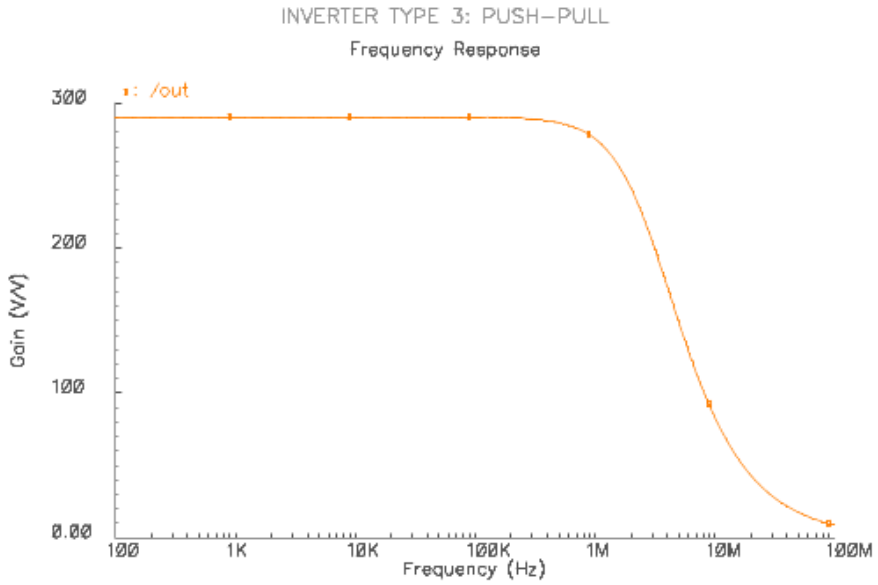

Figure 5.16: Frequency Response of the Push-Pull Inverter

5.4 Comparison

We have finished the analysis of the three types of inverters: active load inverter, current source inverter and push-pull inverter. Main performances of the three inverters are concluded in the following table.

	Type 1 Active Resistor Load	Type 2 Current Source Load	Type 3 Push-Pull
Operating Point	$V_{gs1} = 1.65,\ I_{d1} = 1.06.7\mu A$		
Output Swing	$V_{out}(max) = 2.6V$ $V_{out}(min) = 0.8V$	$V_{out}(max) = 3.3V$ $V_{out}(min) = 0.3V$	$V_{out}(max) = 3.3V$ $V_{out}(min) = 0V$
Gain	1.1	137.6	290.5
Output Resistance	$64k\Omega$	$0.8M\Omega$	$0.76M\Omega$
-3dB Frequency	26.12MHz	3.75MHz	2.98MHz

The comparison shows that under the same DC current, the active resistor load inverter has the lowest gain but the best bandwidth. So this type of inverter is suitable for situations where low gain and wide bandwidth is desired. Push-pull inverter has the highest gain and output swing. But we all know that this type of inverter may cause cross-over distortion. The performance of the current source load inverter is between the other two types, which is a modest gain and output swing.

5.5 Application

In the final circuit, the second type of inverter is used to make a crossover stage. The purpose of this stage is to provide gain and drive to the two output transistors. Figure 5.17 illustrates the basic configuration of a crossover stage.

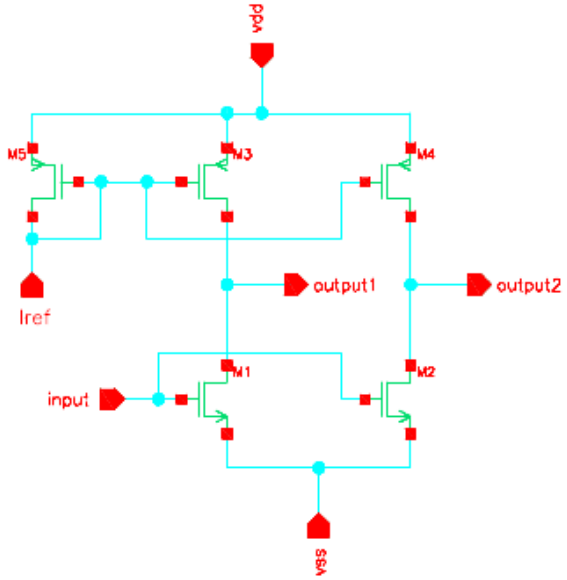

Figure 5.17: Application 1

In this diagram, the two inverters consisting of M1, M3 and M2, M4 are the crossover stage. You can see that these two inverters are the current mirror load inverter introduced above. Figure 5.18 shows the practical circuit in th

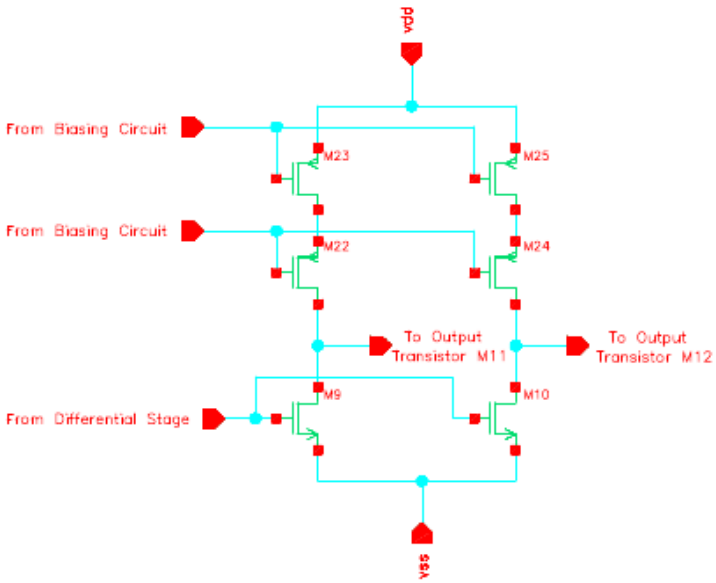

Figure 5.18: Application 2

In this circuit, the crossover stage is achieved with transistors M9, M22, M23 and M10, M24, M25. Here the current mirror is replaced by reduced cascade current source to bias the inverting amplifier, and it comes from

our biasing subcircuit. The input of the inverters is from the first stage, i.e. differential stage. The output of the first inverter consisting of M9, M22, M23 will drive transistor M11 of the output stage, and the second inverter consisting of M10, M24, M25 will drive M12 of the output stage.

The performance of the two inverters is similar to that of the current mirror load inverter introduced above. This is the specific application of the current source load inverter. This stage can provide high gain for the circuit. It's high input and output resistance make it match well with both the differential stage and the output stage.

Chapter 6

Control Network and Output Stage

The primary objective of the CMOS output stage is to function as a current transformer. Most output stages have a high current gain and a low voltage gain. The specific requirements of an output stage might be:

1. Provide sufficient output power in the form of voltage or current.;
2. Avoid signal distortion.;
3. Be efficient. (The efficiency can be defined as the ratio of the power dissipated on the load against the power delivered from the supply);
4. Provide protection from abnormal conditions. (Short circuit, over temperature and so on).

The second requirement results from the fact that the signal swings are large and the non-linearity normally not encountered in small-signal amplifiers will become important. The third requirement is born out of the need to minimize power dissipation in the driver transistors themselves compared with that dissipated in the load. The fourth requirement is normally met with CMOS output stages since MOS devices are self-limiting.

An important function of the output stage is to provide the amplifier with a low output resistance so that it can deliver the output signal to the load without loss of gain. Since the output stage is the final stage of the amplifier, it usually deals with relatively large signals. Thus the small-signal approximations and models either are not applicable or must be used with care. Nevertheless, linearity remains a very important requirement. In fact,

a measure of quality of the output stage is the total harmonic distortion (THD) it introduces.

6.1 Classification of Output Stage

Several approaches to implementing the output amplifier will now be introduced here. Output stages are classified according to the drain current waveform that results when an input signal is applied. For example, in a Class-A amplifier, the transistor conducts for the entire cycle of the input signal, while in a Class-B amplifier, a transistor only conducts for half of the cycle of the input sine wave. And the Class-AB amplifier, involves biasing the transistor at a nonzero DC current much smaller the peak current of the sine-wave signal. As a result, the transistor conducts for an interval slightly greater than half a cycle. The resulting conduction angle is greater than 180^o but much less than 360^o. The Class-AB amplifier has another transistor that conducts for an interval slightly greater than that of the negative half-cycle, and the currents from the two transistors are combined in the load.

6.2 Class-A Output Stage

Here we introduce two kinds of Class-A amplifier output stages:

6.2.1 Simple output amplifier using a Class-A, current-source inverter

The circuit in Figure 6.1 will reduce the output resistance and increase the current driving capability. The output resistance can also be seen in Figure 6.2.

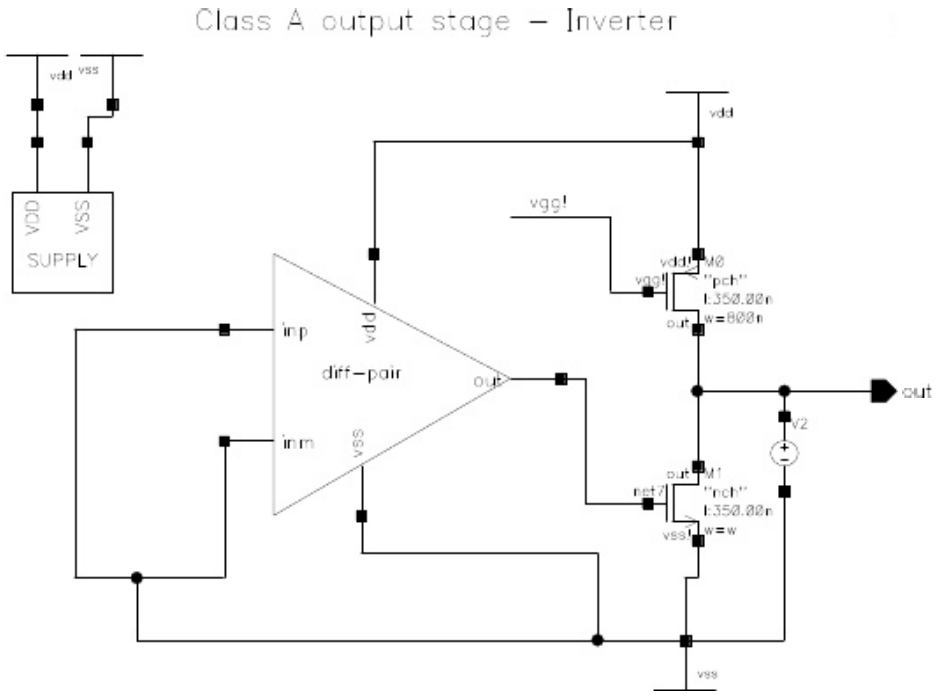

Figure 6.1: Reduced Output Resistance/Increased Current Driving Circuit.

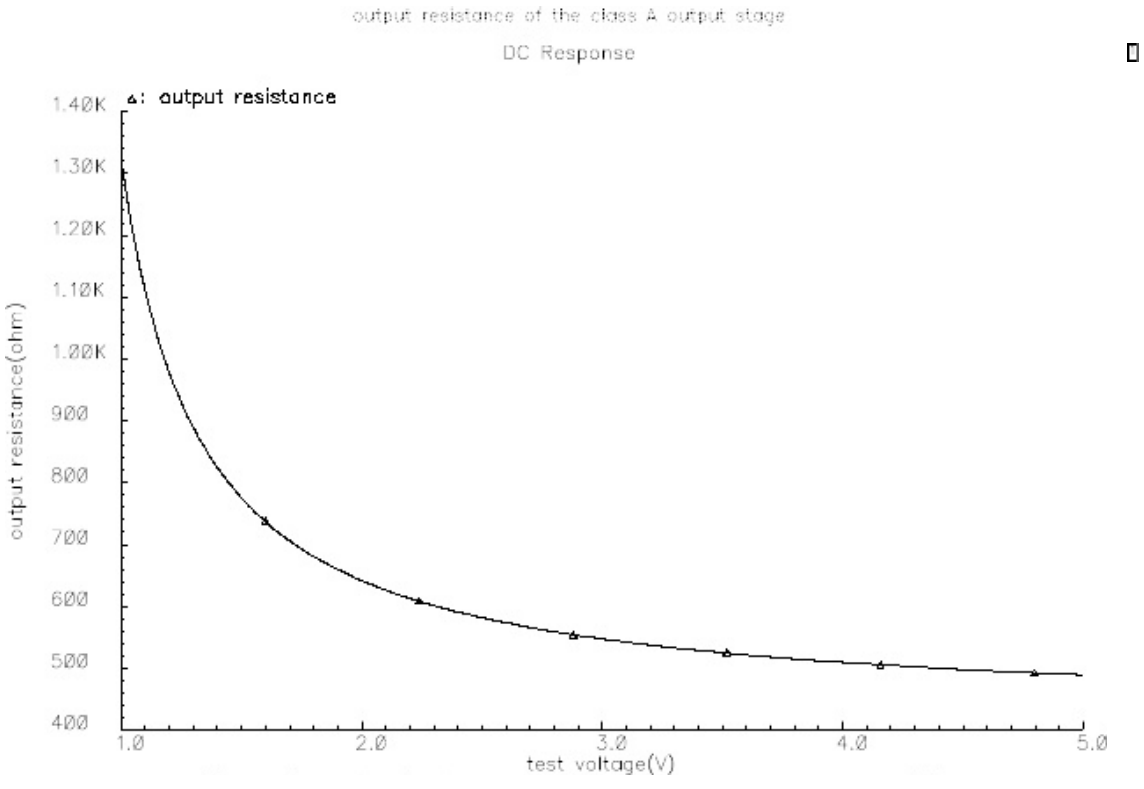

Figure 6.2: Output Resistance for a Class-A Output Stage.

6.2.2 Common-Drain (Source-Follower) Output Amplifier

The circuit configuration shown in Figure 6.3 has both large current gain and low output resistance. But since the source is the output node, the MOS device becomes dependent on the body effect. The body effect causes the threshold voltage V_t to increase as the output voltage is increased, creating a situation where the maximum output is substantially lower than V_{DD}. It is seen that two N-channel devices are used, rather than a P-channel and an N-channel.

The efficiency of the source follower can be shown to be similar to the class-A amplifier. The distortion of the source follower will be better than the Class-A amplifier because of the inherent negative feedback of the source follower. Efficiency is defined as the ratio of the power dissipated in R^L (load resistor) to the power required from the power supplies.

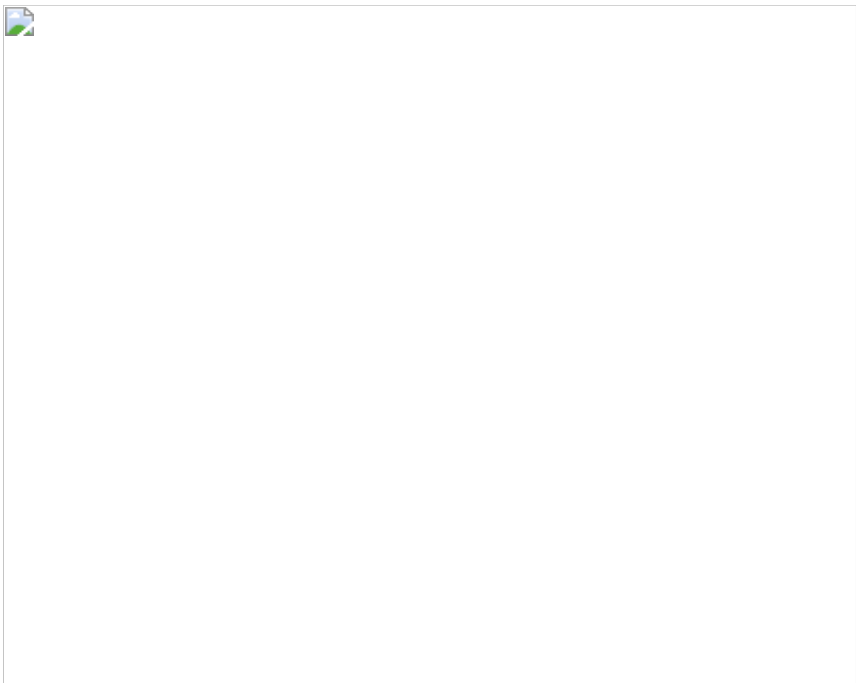

Figure 6.3: Class-A Output Stage - Source Follower Circuit.

6.2.3 Power Analysis

Next, we see that if the bias current, I, is properly selected the output voltage can swing from 0 to V_{DD} with the quiescent value being 1.65V (the absolute maximum value should be $\frac{V_{DD}}{2}$). Now, assuming that the bias current, I, is selected to allow a maximum negative load current of $\frac{V_{DD}}{2R_L}$, the drain current of the upper transistor will swing from $0 \rightarrow 2I$ with the quiescent value being I. So the instantaneous power dissipation in the transistor should

be: $PD_1 = V_{ds1} \cdot i_{d1}$. The maximum instantaneous power dissipation in the upper transistor is $V_{DD} \cdot \frac{I}{2}$. So the upper transistor must be able to withstand a continuous power dissipation of $V_{DD} \cdot \frac{I}{2} (I = \frac{V_{DD}}{2 * R_L})$.

The power conversion efficiency of an output stage is defined as

$$E_{ff} = \frac{load\ power(P_L)}{supply\ power(P_S)} \tag{6.1}$$

For the Class-A output stage, the average load power will be

$$P_L = \frac{V_o^2}{2 \cdot R_L} \tag{6.2}$$

Since the current in the lower transistor is constant (I), the power drawn from the negative supply is $V_{DD} \cdot \frac{I}{2}$. The average current in the upper transistor is equal to I, and thus the average power drawn from the positive supply is $V_{DD} \cdot \frac{I}{2}$. Thus, the maximum efficiency attainable is 25% when $V_o = \frac{1}{2} \cdot V_{DD}$. Because this is a rather low value, the Class-A output stage is rarely used in large power applications. Note, that in practice the output voltage is limited to lower values in order to avoid transistor saturation and associated nonlinear distortion. Thus, the efficiency achieved is usually in the 10% to 20% range.

6.3 Class-B Output Stage

6.3.1 Push-Pull, Inverting CMOS amplifier

The Push-Pull amplifier (Figure 6.4) has the advantage of better efficiency. It is well known that a Class-B, push-pull amplifier has a maximum efficiency of 78.5% which means that less quiescent current is needed to meet the output-current demands of the amplifier. The circuit operates in a push-pull fashion: N-channel transistor pushes current into the load when V_{in} is positive, and P-channel transistor pulls current from the load when V_{in} is negative. Note that there exists a range of V_{in} centered around zero where both transistors are cut off and V_{out} is zero. This "Dead Band" results in the crossover distortion. The crossover distortion of a Class-B output stage can be reduced substantially by employing a high-gain Op-Amp and overall negative feedback. A more practical method for reducing and almost eliminating crossover distortion is found in the Class-AB amplifier. The output voltage swing is limited to a threshold voltage below V_{DD} and above V_{SS}.

Figure 6.4: Class-B Output Stage - Push-Pull Circuit.

Figure 6.5: Class-B Output Stage - Transfer Characteristics.

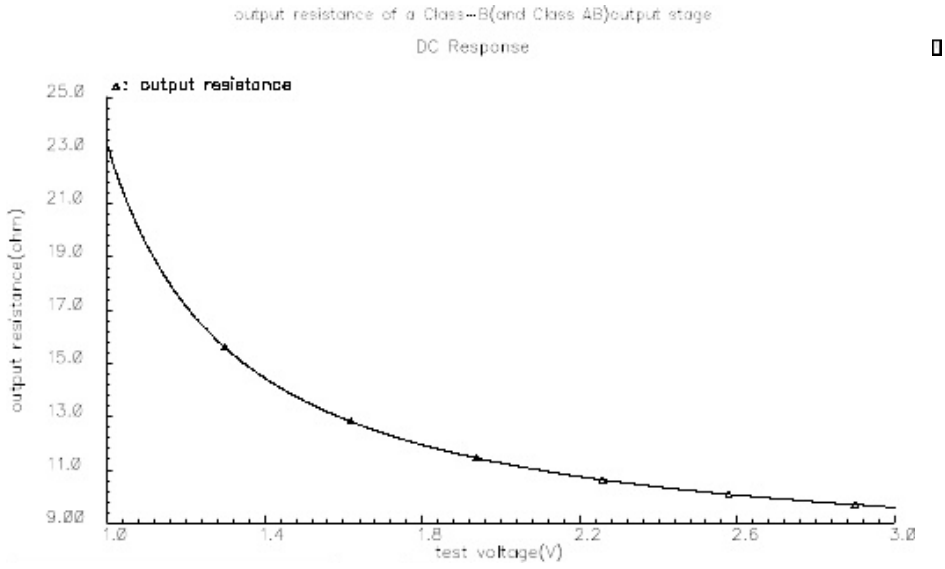

Figure 6.6: Output Resistance for a Class-B (and Class-AB) Output Stage.

6.3.2 Power Analysis

To calculate the power-conversion efficiency, E^{ff}, of the Class-B stage, we neglect the crossover distortion and consider the case of an output sinusoid of peak amplitude V_o. So $P_L = \frac{V_o^2}{2 \cdot R_L}$ The current drawn from each supply will consist of half sine waves of peak amplitude. Thus, the average current drawn from each of the two power supplies will be $\frac{V_o}{\pi} \cdot R_L$.

$$E_{ff} = \frac{load\ power(P_L)}{supply\ power(P_S)}$$

It follows that the maximum efficiency is obtained when V_o is at its maximum $\frac{V_{DD}}{2}$. The power-conversion efficiency is 78.5%. This value is much larger than that obtained in the Class-A stage.

6.4 Class-AB Output Stage

Crossover distortion can be virtually eliminated by biasing the complementary output transistor at a small nonzero current. The result is the Class-AB output stage. (See Figure 6.7). The Class-AB stage operates in much the same manner as the Class-B circuit, with one important exception: for small input, both transistors conduct, and as input is increased or decreased,

one of the two transistors takes over the operation. Since the transition is a smooth one, crossover distortion will be almost totally eliminated.

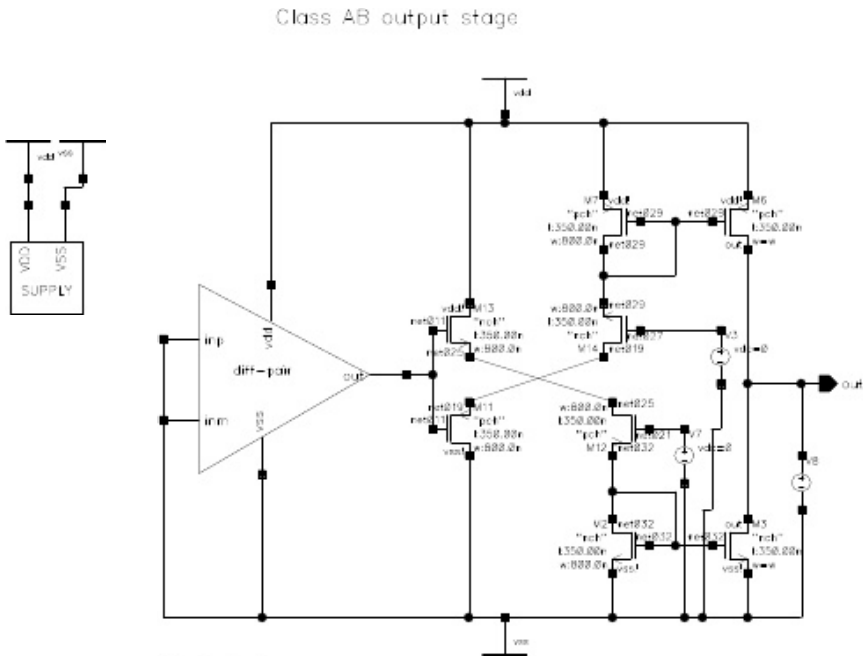

Figure 6.7: Class-AB Output Stage Schematic.

This type of amplifier is sometimes called an operational transconductance amplifier (OTA). It is very useful in driving capacitive loads. And because it based on a floating current source, the output voltage can swing from V_{SS} to V_{DD}. And the power relationships in the Class-AB stage are almost identical to those derived for Class-B circuit in the previous section.

6.5 Short Circuit Protection

The circuit shown in Figure 6.8 shows a Class-AB output stage equipped with protection against the effect of short-circuiting the output while the stage is sourcing current. The large current that flows through M1 in the event of a short circuit will develop a voltage drop across R1 of sufficient value to turn M2 on. The drain of M2 will then conduct most of the current I_{bias}, robbing M1 of its base drive. The current through M1 will thus be reduced to a safe operating level. This method of short-circuit protection is effective in ensuring device safety, but it has the disadvantage that under normal operation about 0.5V drop might appear across each R. This means that the voltage swing at the output will be reduced by that much, in each direction. On the other hand, the inclusion of the resistors provides the additional benefit of protecting the output transistors against thermal runaway.

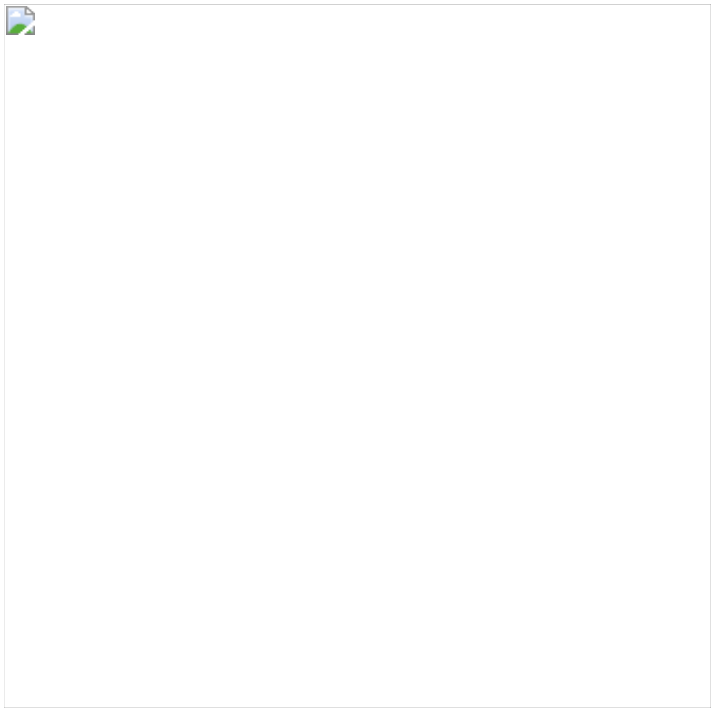

Figure 6.8: Short-Circuit Protection Circuit Schematic.

6.6 Conclusion

After having studied several different kinds of the output stages, and based on the analysis above, the decision to use the Class-AB output stage was final. Again, the most important factors being:

1. It has high power-conversion efficiency (Maximum 78.5%).
2. It has low output resistance.
3. It can eliminate the crossover distortion in Class B.

Figure 6.9 shows the final output stage used: the Crossover-Class-B output stage. It can be divided to two stages: one is the normal Class-B stage, the other is the crossover stage. It provides the gain, bias, compensation and drive to the two transistors in the final stage. These two stages form the Class-AB stage, and provide good performance. The total harmonic distortion in this circuit is very small, only 0.05%. Figures 6.10, 6.11 and 6.13 show the three main types of analysis performed, AC Response, DC Response and Transient Response, respectively.

Harmonic Analysis: The distortion of an amplifier is always identified by its response to the sinewave input signal. It is generated by the non-linearity of the amplifier transfer characteristics. So if we know that the input signal is:

$$V_{in}(\omega) = V \sin \omega t \tag{6.3}$$

Figure 6.9: Final Output Stage with Crossover + Class-B.

Figure 6.10: AC Response of The Final Output Stage.

Then the output distortion should be:

$$V^{out}(\omega) = a^1 \cdot V \sin(\omega t) + a^2 \cdot V \sin(2\omega t) + a^3 \cdot V \sin(3\omega t) + ... + a^n \cdot V sin(n\omega t) \tag{6.4}$$

So the i^{th} harmonic distortion (HD) is defined as the magnitude of the i^{th} harmonic to the magnitude of the 1^{st} harmonic. For example, the second harmonic distortion is $HD_2 = \frac{a_2}{a_1}$ And the total harmonic distortion (THD)

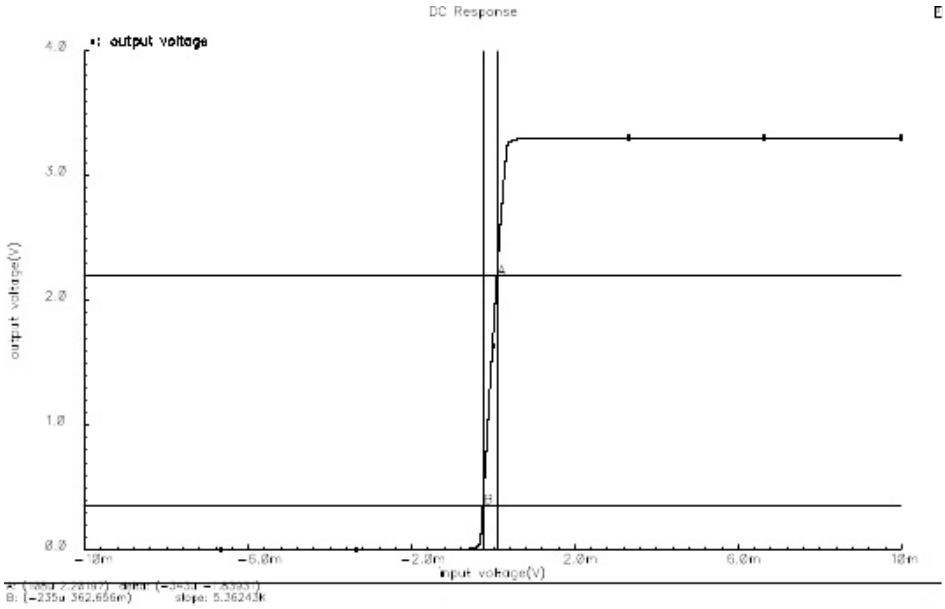

Figure 6.11: DC response of The Final Output Stage.

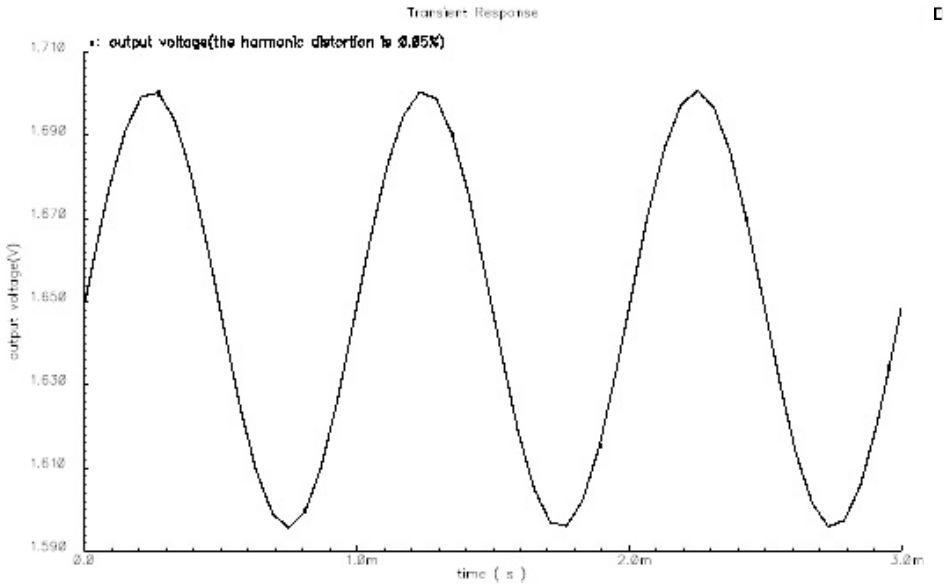

Figure 6.12: Transient Response of The Final Output Stage.

is defined as:

$$THD = \frac{\sqrt{\left[a_2^2 + a_3^2 + ... + a_n^2\right]}}{a_1} \tag{6.5}$$

Normally, the harmonic distortion of an ideal amplifier should be less than 1.0%.

6.7 Design Considerations

While working on the output stage, an important phenomena was seen: when the gain is increased the slope is increased and the linear range will decrease. So if the gain is very high and the input signal is not small enough, there will be harmonic distortion. In the final circuit, the magnitude of the input signal is 1μ, so there is almost no harmonic distortion. If the magnitude of the input signal is increased harmonic distortion will begin to appear. For example, when the magnitude is $100\mu V$, the harmonic distortion is around 10%. Is there a way that could deal with the harmonic distortion when the input signal is increased to get higher output swing?

6.7.1 Negative Feedback

Negative feedback is always employed in the amplifier design to effect one or more of the following properties:

- Desensitize the gain: that is, make the value of the gain less sensitive to variations in the value of circuit components, such as variations that might be caused by the changes in temperature.
- Reduce nonlinear distortion: that is, make the output proportional to the input, make the gain constant independent of signal level.
- Reduce the effect of noise: that is, minimize the contribution to the output of unwanted electric signals generated by the circuit components and extraneous interference.
- Control the input and output impedances: that is, raise or lower input and output impedances by the selection of appropriate feedback topology.
- Extend the bandwidth of the amplifier.

All of the above desirable properties are obtained at the expense of a reduction in gain and at the risk of the amplifier becoming unstable (that is oscillating).

6.7.2 Frequency Compensation

From the bode plot, we know that if the closed-loop-Amplifier has one or two poles, it is stable because the maximum phase shift of output is always less than 180 degrees. But if there are more than 2 poles, it will become unstable.

That means the amplifier will oscillate. So in order to keep it stable, we must use the frequency compensation. A popular method for frequency compensation involves connecting a feedback capacitor to an inverting stage in the amplifier. This causes the pole formed at the input of the amplifier stage to shift to a lower frequency and thus become dominant, while the pole formed at the output of the amplifier stage is moved to a very high frequency and thus becomes unimportant. This process is known as pole splitting. And there are two parameters that are very important in the feedback amplifier design: gain margin and phase margin. The gain margin represents the amount by which the loop gain can be increased while stability is maintained. Feedback amplifiers are usually designed to have sufficient gain margin to allow for the inevitable changes in loop gain with temperature, time and so on. On the other hand, for a stable amplifier, the phase lag must be less than 180^o. And feedback amplifiers are normally designed with a phase margin of at least 45^o. The amount of phase margin has a profound effect on the shape of the close-loop magnitude response.

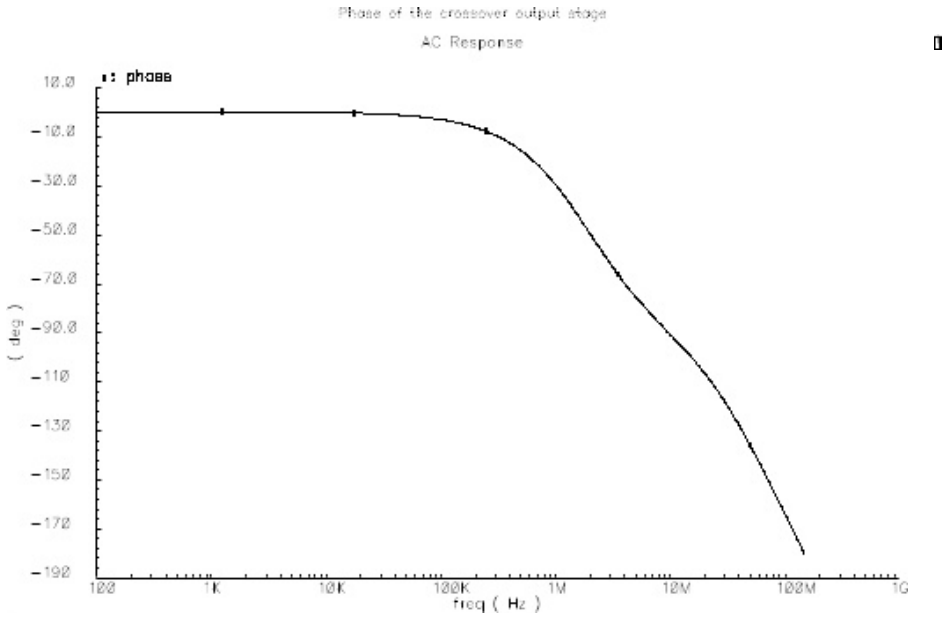

Figure 6.13: Phase of the Crossover Output Stage.

Chapter 7

Integrating the Sub-Circuits

The last steps in the design flow are to combine the circuits and test the full schematic in order to ensure that there are no unexpected interactions between the various sub-circuits. The larger the design the more difficult these interactions can become to understand. Figure 7.1 shows the full schematic representations.

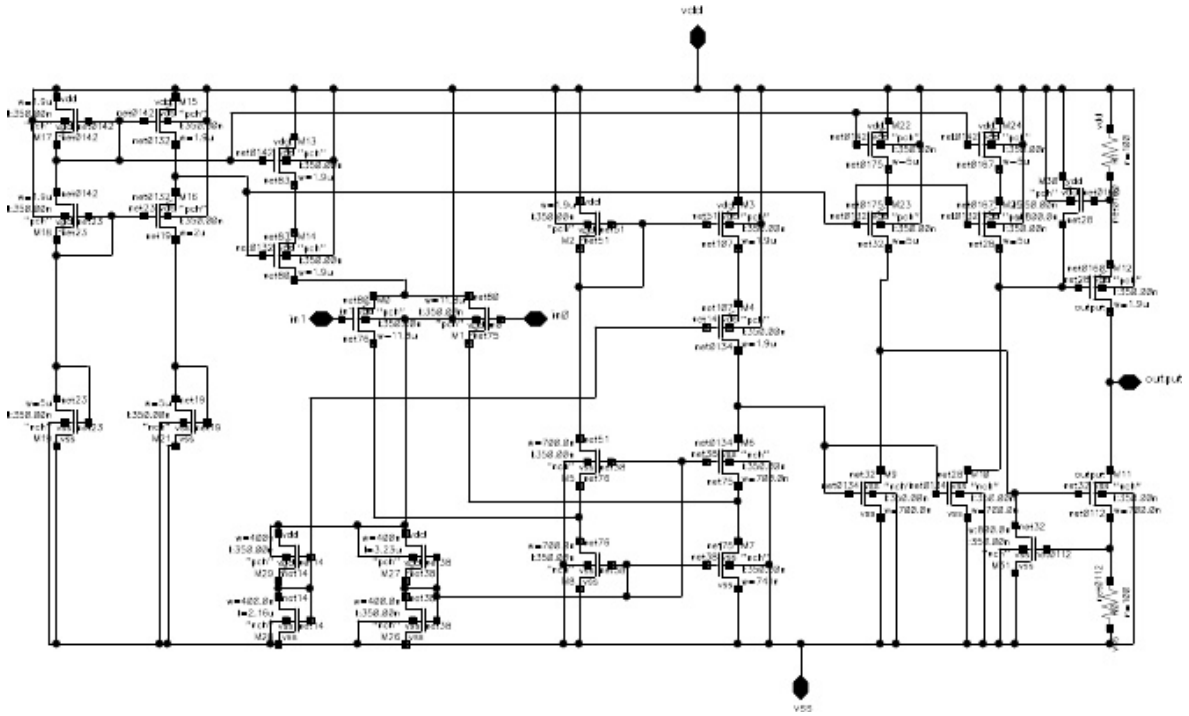

Figure 7.1: Schematic of Entire Op-Amp

7.1 Overall Performance

A simulation of the completed circuit was performed with a purely resistance load of 100 $M\Omega$s (shown in figure 7.2) and an input signal of 1KHz with a magnitude of 1 μV. It can be seen from the transient analysis that the output waveform is linearly amplified around the operating voltage of 1.65 V. The gain is approximately $95 \cdot 10^4$ (easily seen on the AC Response). The differential input voltage, in the DC Sweep, is being measured relative to the operating voltage of 1.65 V.

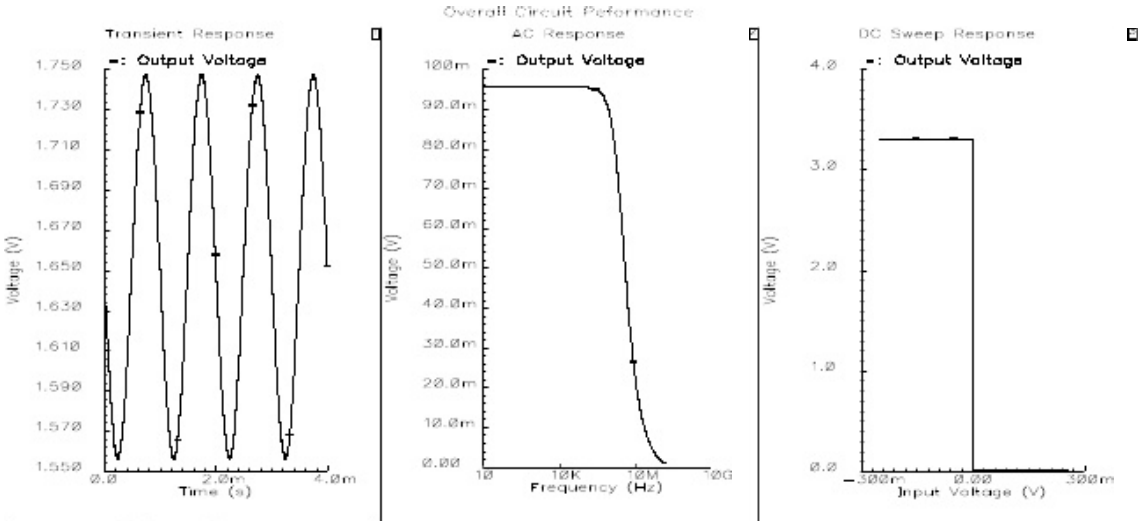

Figure 7.2: Overall Performance with 1 μV,1KHz Input

A close up of the DC Sweep transition region can be seen in figure 7.3. The input voltage swing range can be seen to be approximately 16 μV

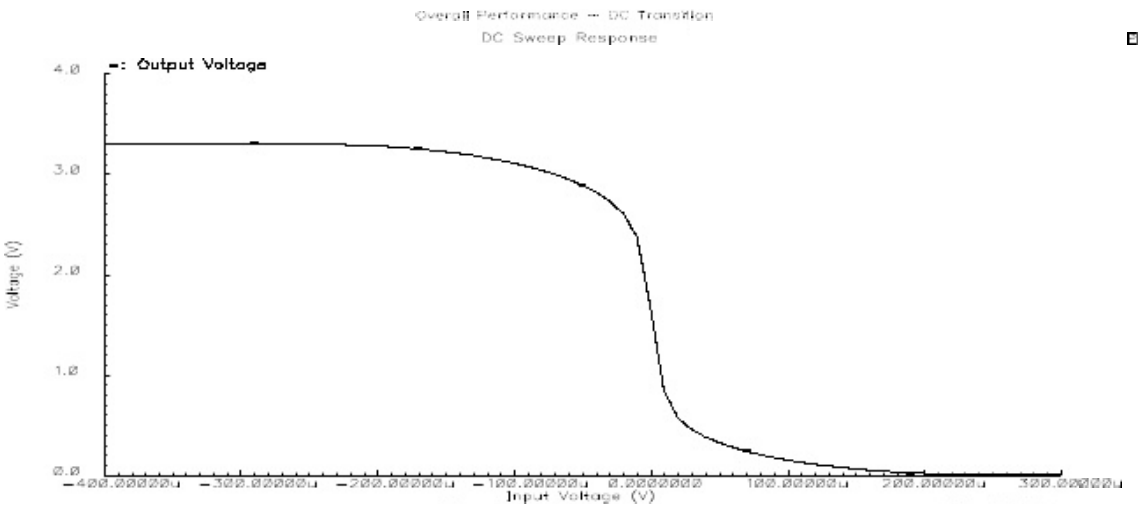

Figure 7.3: DC Performance – with 1 μV,1KHz Input

7.2 The Measurement of Some Main Parameters

In this part, we introduce some methods to measure parameters and then apply some of them into the design of the Op-Amp to evaluate it.

7.2.1 Input Offset Voltage

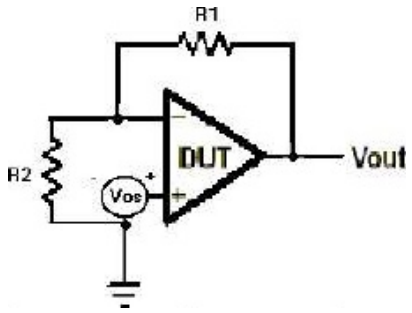

Figure 7.4: Measurement of Offset Voltage

Method: in 7.4, DUT is the Op-Amp measured. We presume it's an ideal Op-Amp which has it's non-inverting pin connected to an offset voltage source. Although there is no input signal, V_{out} doesn't equal to zero because of the offset voltage (V_{os}).

For an ideal Op-Amp: $V_+ = V_-$
For this circuit: $V_+ = V_{os}$
$V_- = V_{out} \cdot \left(\frac{R_2}{R_1+R_2}\right)$
Then $V_{os} = V_{out} \cdot \left(\frac{R_2}{R_1+R_2}\right)$

The result curve shows that when $V_{in} = 0$, $V_{out} = 2.173V$, because

$$\frac{R_2}{R_1 + R_2} = \frac{100}{100 + 1M} = 10^{-4}$$

so

$$V_{os} = 2.173 \cdot 10^{-4} = 0.217mv$$

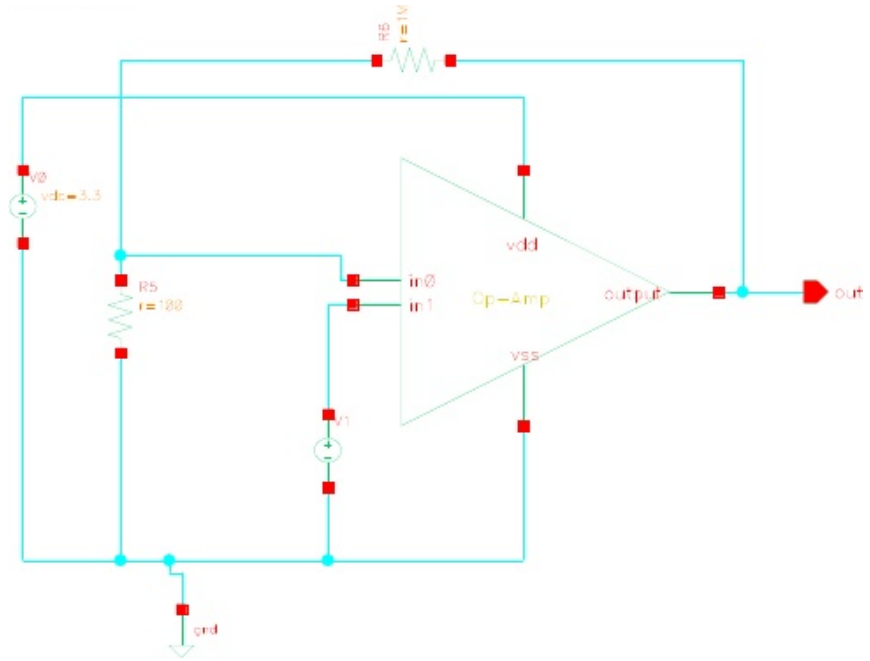

Figure 7.5: Schematic for Measuring Offset Voltage

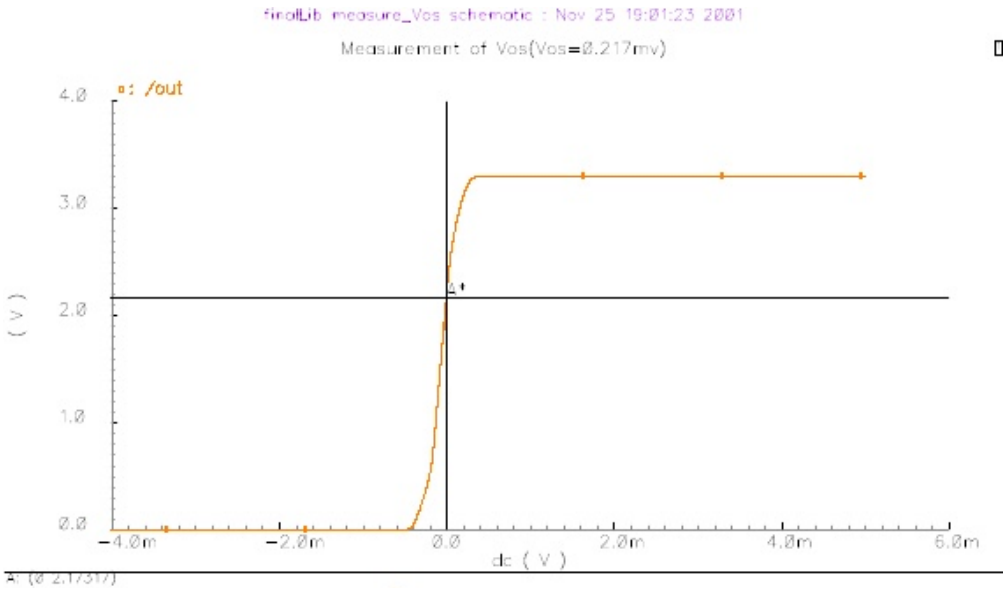

Figure 7.6: Result Plot of Offset Voltage Test

7.2.2 Common-Mode Rejection Ratio (CMRR)

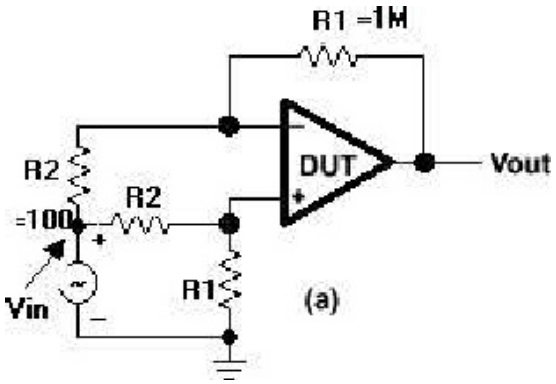

Figure 7.7: Measurement of CMRR

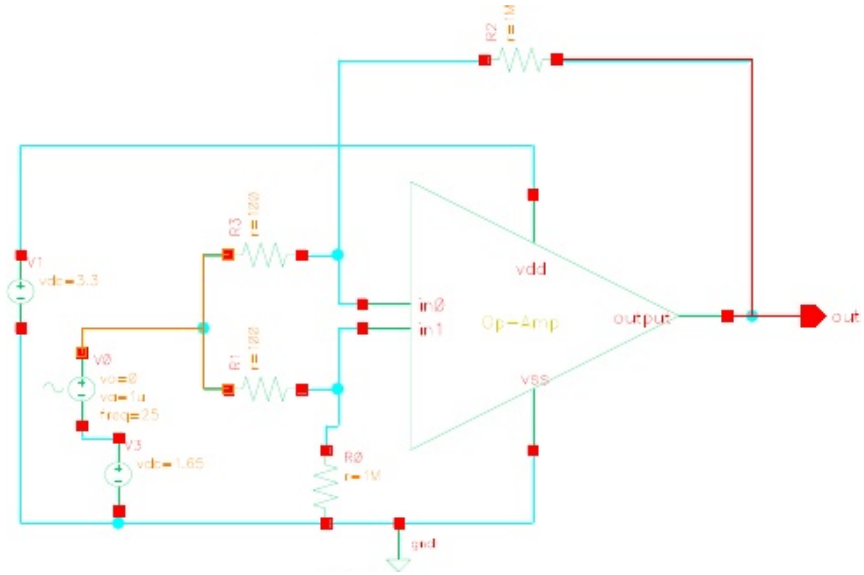

Figure 7.8: Schematic for Measuring CMRR

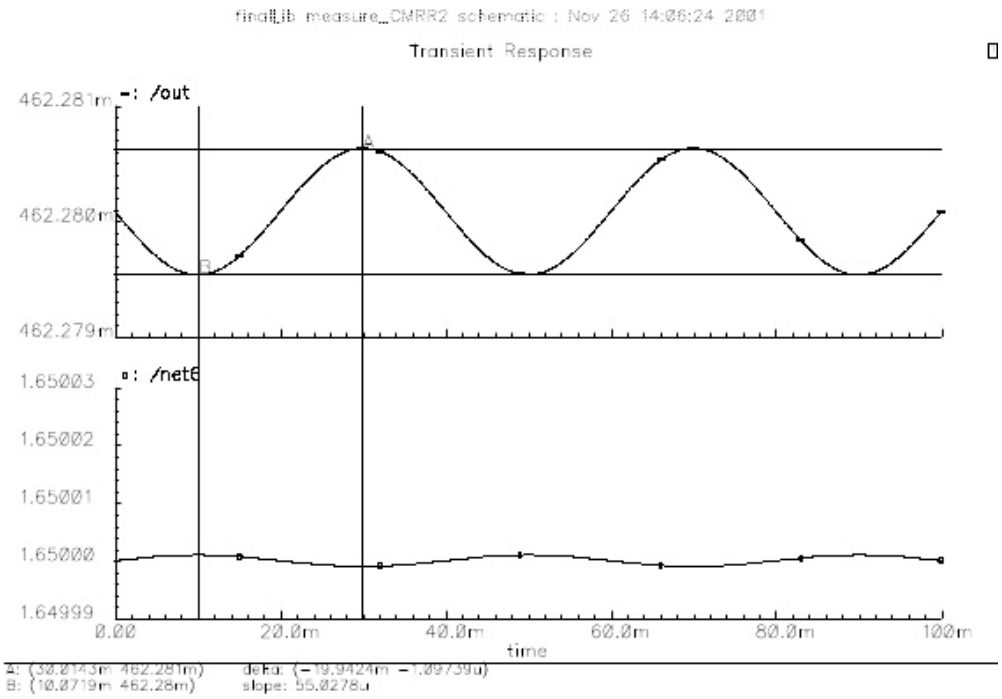

Figure 7.9: Test Results of CMRR Simulation

Method:

$$CMRR(dB) = 20\log\frac{A_d}{A^c} \tag{7.1}$$

A_d is the differential mode signal gain of Op-Amp.
A_c is the common mode signal gain of Op-Amp.

For the 7.11, signal source is a low frequency AC signal. We get the following:

$$\begin{cases} \dot{V}+ = \dfrac{\dot{V}in*R1}{R1+R2} \\ \dot{V}- = \dfrac{\dot{V}in*R1 + \dot{V}out*R2}{R1+R2} \end{cases}$$

$$\dot{V}out = 0.5*Ac[\dot{V}+ + \dot{V}-] + Ad[\dot{V}+ - \dot{V}-]$$

Figure 7.10: Equation

By calculating it:

$$\dot{V}out*[R1+R2*(1+Ad-Ac/2)] = \dot{V}in*R1*Ac$$

Figure 7.11: Equation

$$\dot{V}out*R2*Ad \approx \dot{V}in*R1*Ac$$

Figure 7.12: Equation

Generally, $A^d \gg A^c$, $A^d \gg 1$, and $(1 + A^d) \cdot R^2 \gg R^1$, so approximately,

$$CMRR = \frac{A_d}{A_c} = \frac{\frac{R_1}{R_2}}{\frac{V_{out}}{V_{in}}} \tag{7.2}$$

In the test circuit – 7.11, $\frac{R_1}{R_2} = 10^4$, so

$$CMRR\,(dB) = 20 \log 10^4 \quad \frac{V_{in}}{\cdot\, V^{out}} \tag{7.3}$$

From the curve of 7.9, the amplitude of V_out is about $0.55mV$ and the amplitude of the input signal has been set to $1mV$. So we can get the result of our design's CMRR is

$$CMRR(dB) = 20 \log \left(10^4 \cdot \frac{1}{0.55} \right) = 85.2\ dB \tag{7.4}$$

7.2.3 Output Resistance - R_o

Method: Mr.Sedra and Mr.Smith provide us a method to get the close-loop output resistance. (≪microelectronic circuits≫. Third edition. Pages 94 to 95). The schematic is below:

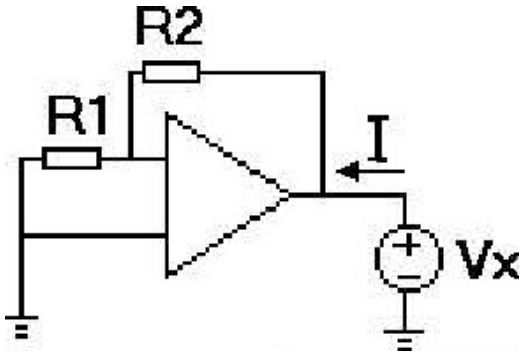

Figure 7.13: Derivation of the closed-loop output resistance

In order to find the output resistance of a closed-loop-Amplifier, we short the signal source, which makes the inverting and non-inverting configurations identical and apply a test voltage V_x to the output as shown in Figure 7.14. Then the output resistance $R_{out} = \frac{Vx}{I}$ can be obtained by straightforward analysis of the circuit.

We get the result directly(procedures omitted):

$$R_{out} = (R_1 + R_2)||(\frac{R_o}{1 + Ab}) \tag{7.5}$$

Note that R_{out} is the "closed-loop resistance of Op-amp" and R_o is the "open-loop resistance". The former one varies according to different feedback networks but the latter is a very important inherent characteristic of the Op-amp. From equation 7.5, Normally R_o is much smaller than $R_1 + R_2$, so we get:

$$R_{out} = \frac{R_o}{1 + Ab} \tag{7.6}$$

b is defined as: $b = \frac{R_1}{R_1+R_2}$

Consider the situation described as the schematic below:

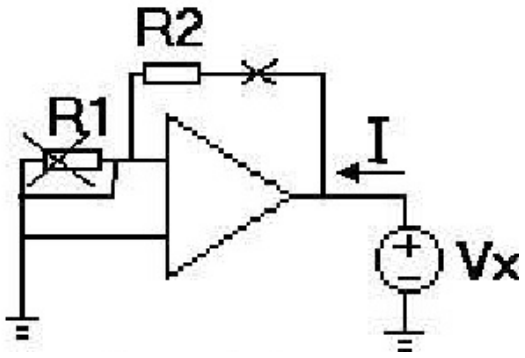

Figure 7.14:

At this situation, $R_1 \Rightarrow 0$ and $R_2 \Rightarrow \infty$, then $b = 0$, $R_{out} = R_o$. So by calculating $R_{out} = \frac{V_x}{I}$, we should get the open-loop resistance simultaneously.

Simulation result of our Op-amp's output resistance is some curves like:

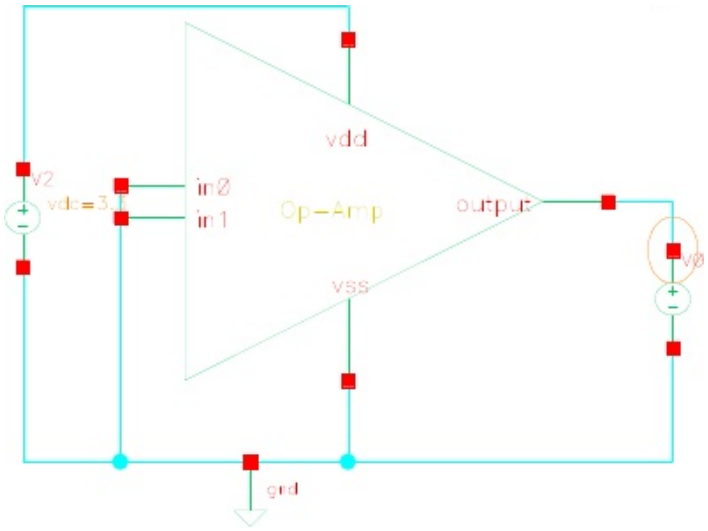

Figure 7.15: Schematic for Measuring Output Resistance

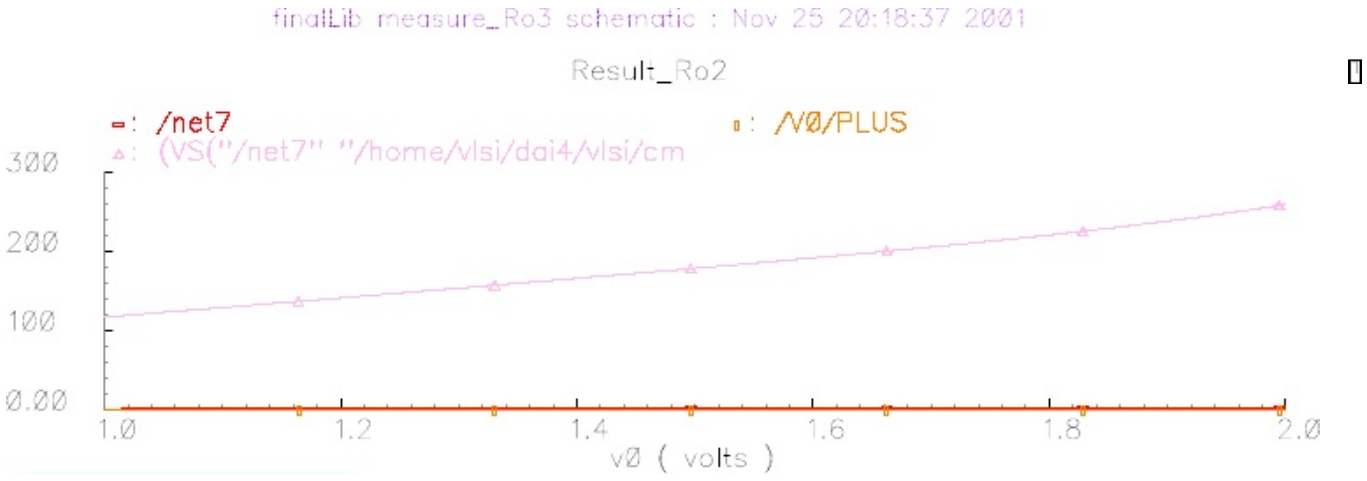

Figure 7.16: Result of Output Resistance Test

7.3 Delivering Power to the Load/Instantaneous Power

The maximum amount of power which can be delivered to the load can easily be tested by decreasing the resistance of the load. We shall see that the if the load becomes too small the Op-Amp will not be able to maintain the correct output voltage. See Figure 7.17.

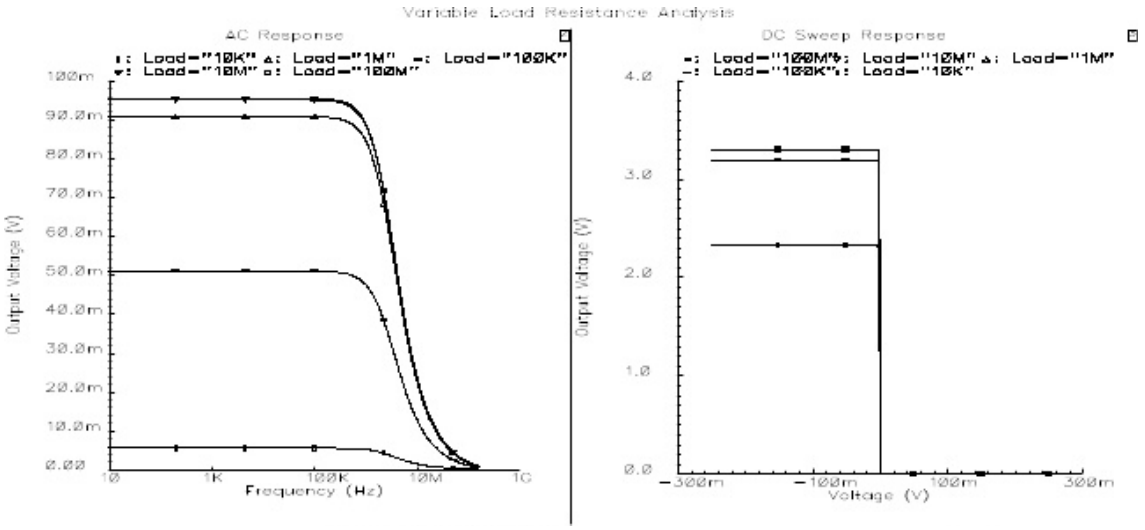

Figure 7.17: AC & DC Simulation for a Parametric Load with 1 μV,1KHz Input

It is obvious that the amount of current which the circuit can supply is not enough. In order to increase the driving power which the circuit has, it is necessary to increase the strength $\left(\frac{W}{L}\right)$ of the push-pull output transistors. Figure 7.18 shows the instantaneous power of the Op-Amp at 1KHz through a $10M\Omega$ load.

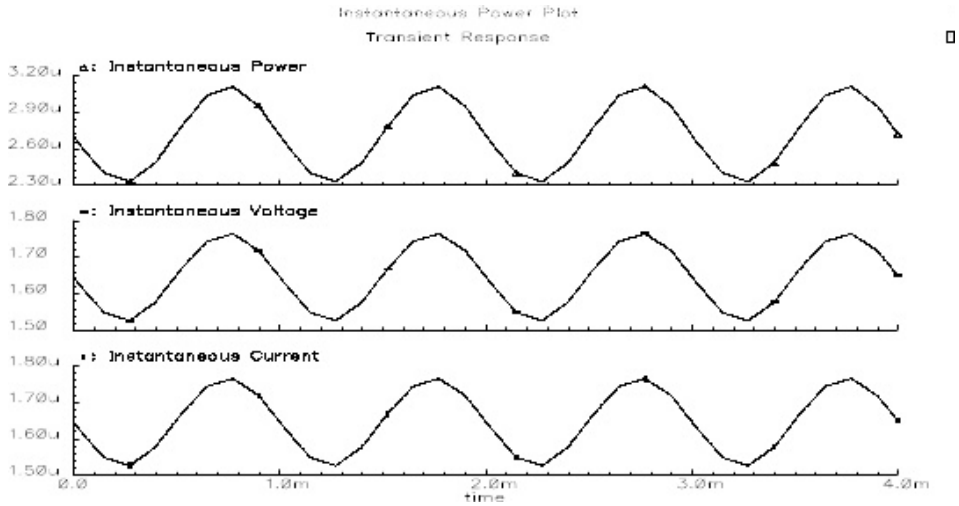

Figure 7.18: Instantaneous Power

7.4 Improving the Output Buffer

A simplified schematic for testing the improved output buffer is shown in figure 7.19. By increasing the transistor widths to: $15\mu m$ for the N-channel and $32.84\mu m$ for the P-channel; we can improve the amount of power the Op-Amp can supply. Two capacitors have been added to the control network in this schematic. These *Miller Capacitors* are required for stability.

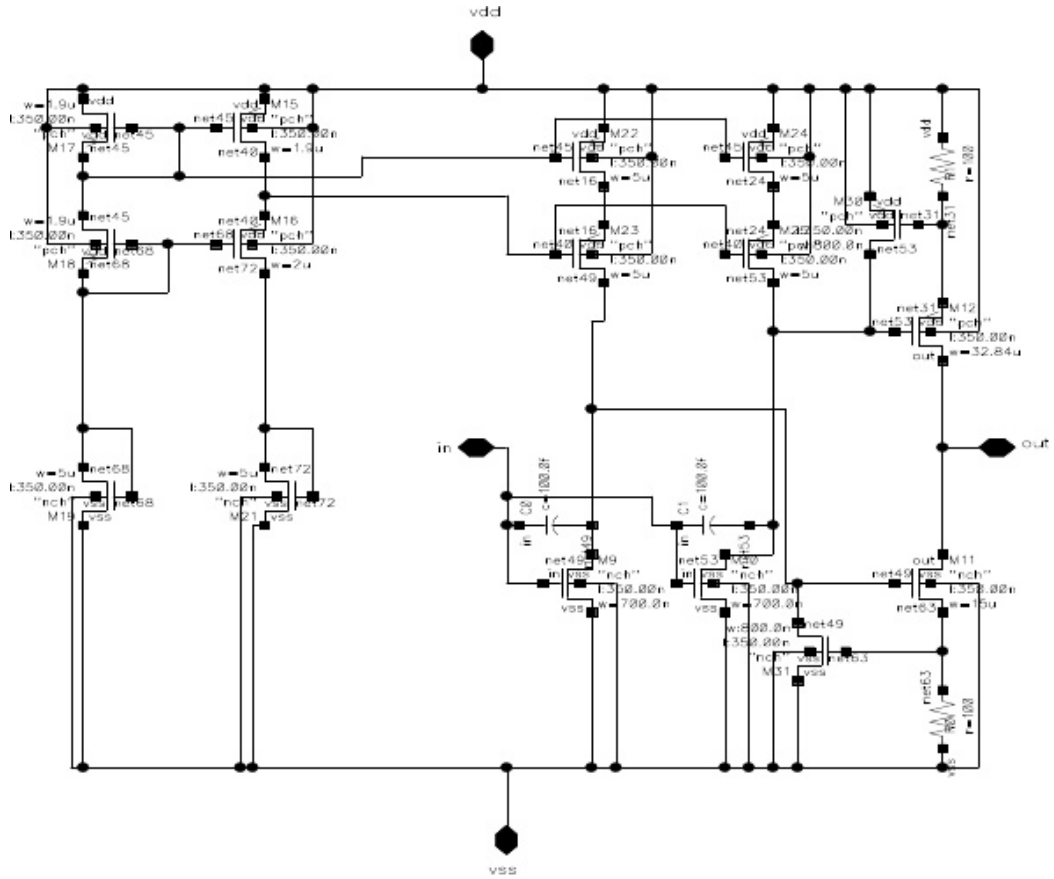

Figure 7.19: Output Test Schematic

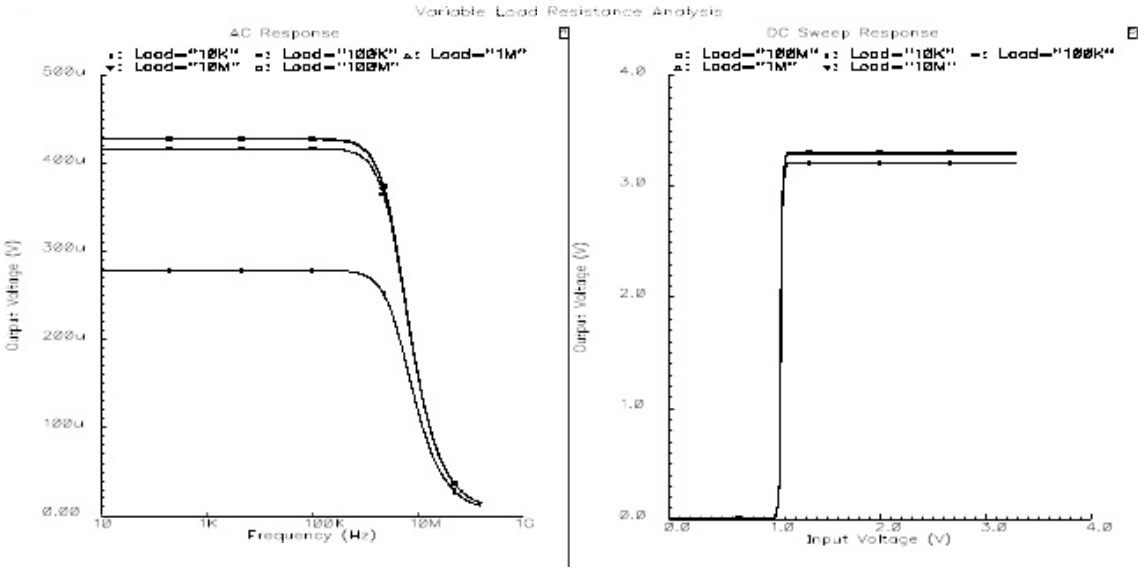

Figure 7.20: AC & DC Simulation with larger Output Transistors for 1 μV,1KHz Input

The size of the output transistors may be increased further if the design specifications require more current to be delivered. The larger the output transistors the more care must be taken in making sure that the transistors are equally matched.

7.4.1 Stabilizing the Output

Without the new *Miller Capacitors* the Op-Amp becomes unstable. This was found in preliminary results; shown in figure 7.21. It should be noted that the *noise* on the output is increasing with time, however, this instability is not seen in the frequency simulation. This seems to be a limitation of the HSPICE AC simulation.

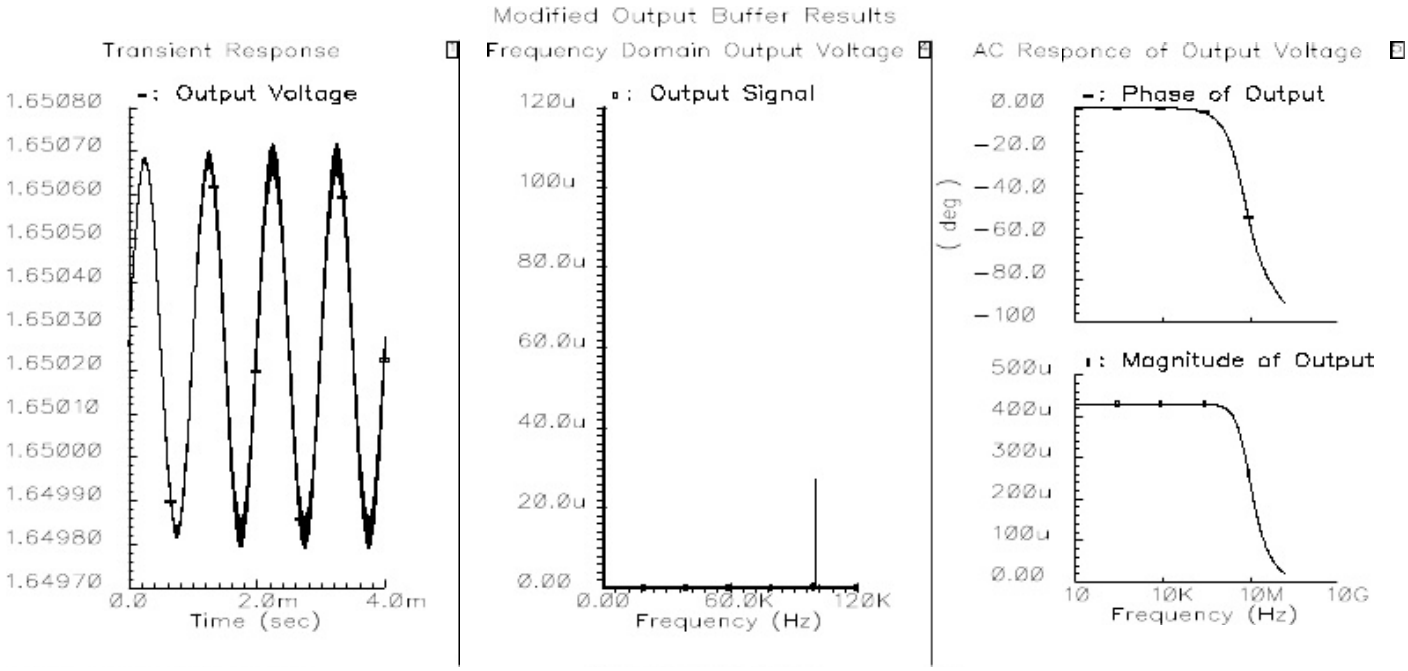

Figure 7.21: Instability due to lack of *Miller Capacitors*

The frequency domain representation of the transient signal was calculated from the 3 $msec \rightarrow 4$ $msec$, using a rectangular data window. The *noise* can be seen clearly at approximately 100KHz. Once the *Miller Capacitors* are in place (with a value of 0.1 pF) this harmonic is completely removed.

Chapter 8

Closing Remarks

8.1 Conclusion

This project was a huge success from its beginning to its tentative completion. By using a team oriented approach to the design methodology it was possible to bring together such an intricate project. Many challenges were incurred and resolved soundly and swiftly through the cooperation and input of all of the group members. Each member of the group has become a "Mini-expert" in their area of their design and since these designs all fit together in a larger puzzle knowledge of the other areas has also been gained my each group member.

Chapter 9

Bibliography

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