

Cadence Inverter Transistor Sizing Tutorial
Cadence Inverter Ocean Introduction
Cadence Inverter Corners Tutorial
Cadence Inverter VerilogA Tutorial
Cadence Inverter Vout vs Vin Tutorial

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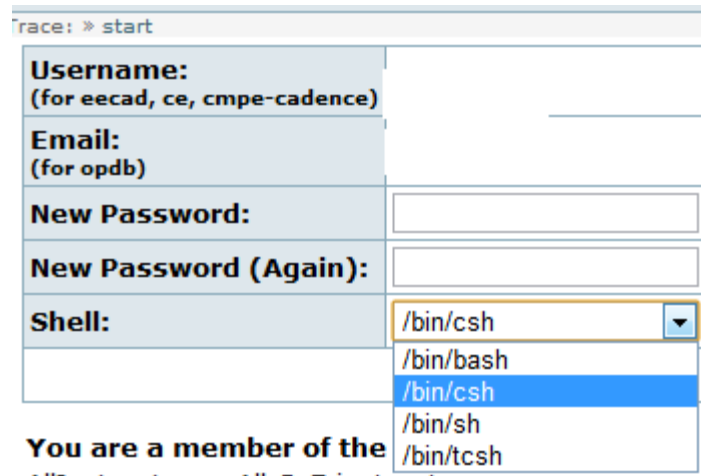
Unix account and Cadence Setup Instructions

1. Set up a Unix account by visiting the following website.

<https://unix.engr.sjsu.edu/wiki/doku.php>

2. Complete the Cadence Tutorial. This will setup cadence on your account and provide you with a general idea on how to use cadence. **Type "csh" in linux terminal to switch to your directory.**

Alternatively, you can also go to your unix account management online and set it up as csh there.



Trace: » start

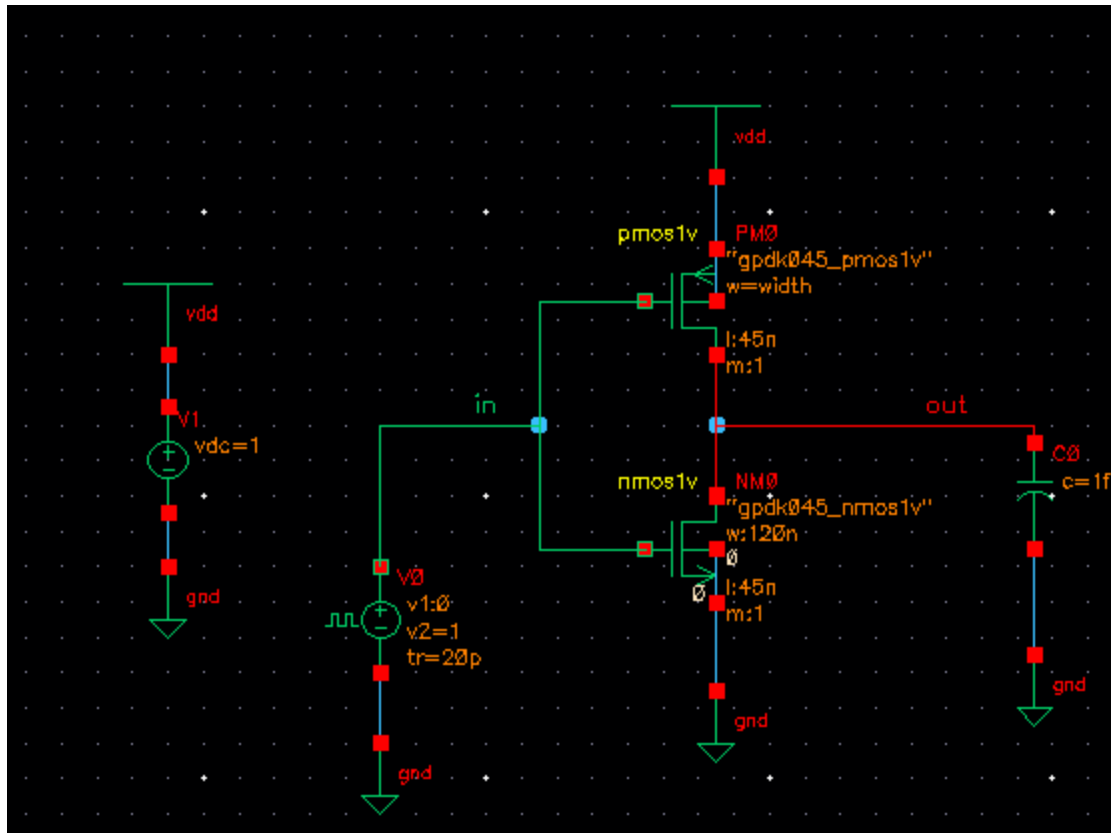
Username: (for eecad, ce, cmpe-cadence)	<input type="text"/>
Email: (for opdb)	<input type="text"/>
New Password:	<input type="password"/>
New Password (Again):	<input type="password"/>
Shell:	<div><div>/bin/csh</div><div><div>/bin/csh</div><div>/bin/bash</div><div>/bin/sh</div><div>/bin/tcsh</div></div></div>

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All members All C&E instructors

<http://www.engr.sjsu.edu/mjones/cadence6.pdf>

Testbench

1. Create a Inverter Testbench as follows:



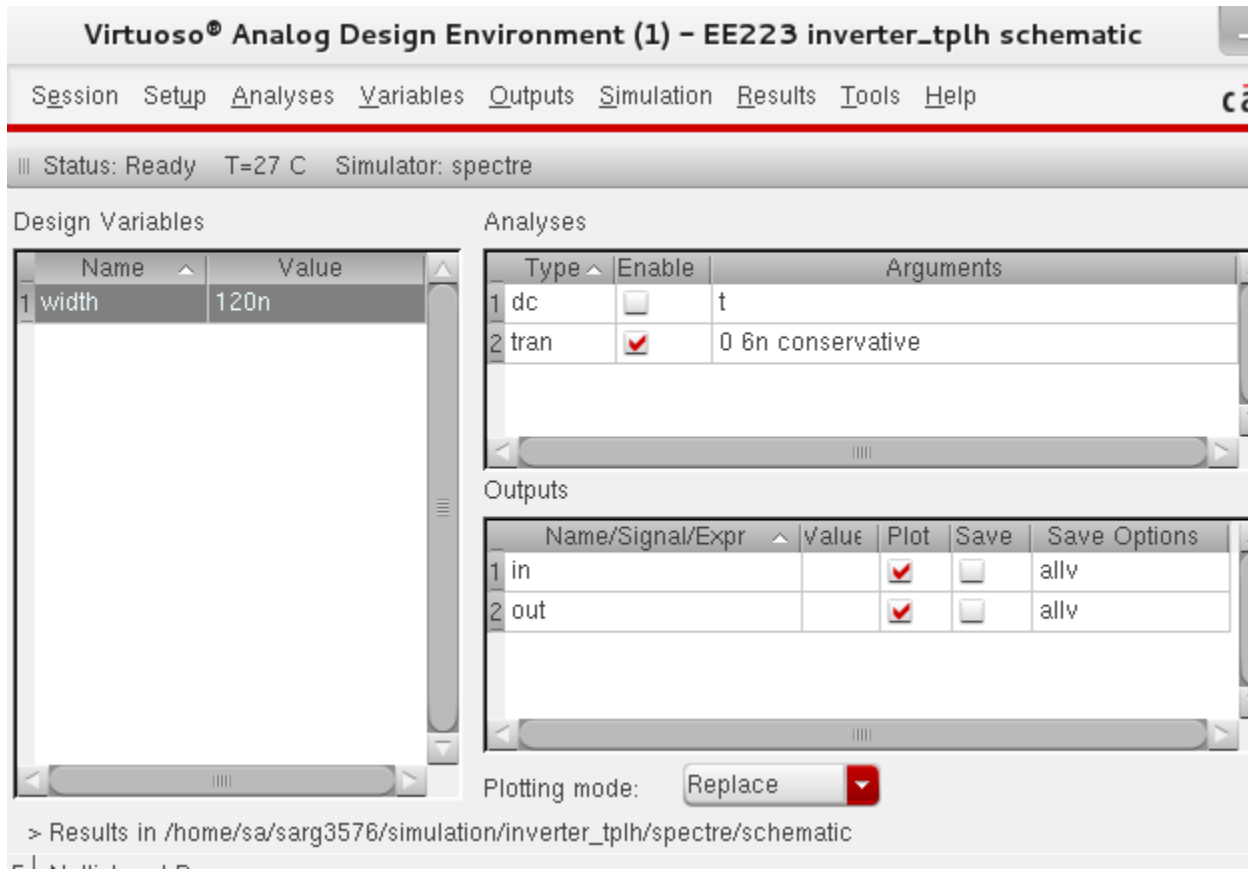
2. Vpulse is created as follows:

Library Name	analogLib	
Cell Name	vpulse	
View Name	symbol	
Instance Name	V0	

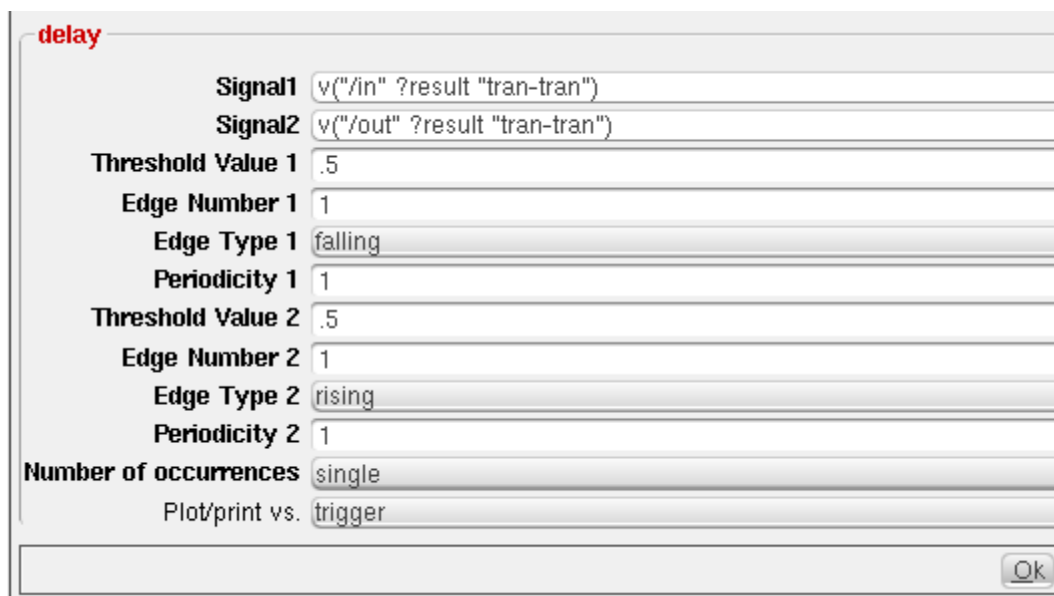
	<input type="button" value="Add"/>	<input type="button" value="Delete"/>	<input type="button" value="Modify"/>
User Property	Master Value	Local Value	
Ivsignore	TRUE		

CDF Parameter	Value
Frequency name for 1/period	
Noise file name	
Number of noise/freq pairs	0
DC voltage	
AC magnitude	
AC phase	
XF magnitude	
PAC magnitude	
PAC phase	
Voltage 1	0 V
Voltage 2	1 V
Period	2n s
Delay time	
Rise time	20p s
Fall time	20p s
Pulse width	1n s
Temperature coefficient 1	
Temperature coefficient 2	

- Launch ADE L and set up the following:



- Run the ADE L once and launch calculator. Set up the following two test benches for tphl and tphi. We will be using the delay function in calculator. tphl



Switch rising and falling.

Signal1	v("/in" ?result "tran-tran")
Signal2	v("/out" ?result "tran-tran")
Threshold Value 1	.5
Edge Number 1	1
Edge Type 1	rising
Periodicity 1	1
Threshold Value 2	.5
Edge Number 2	1
Edge Type 2	falling
Periodicity 2	1
Number of occurrences	single
Plot/print vs.	trigger
Ok	

To find tp, average them both.

```
.5*delay(v("/in" ?result "tran-tran") .5 1 "rising" v("/out" ?result "tran-tran") .5 1 "falling" 0 0 nil nil )
+.5*delay(v("/in" ?result "tran-tran") .5 1 "falling" v("/out" ?result "tran-tran") .5 1 "rising" 0 0 nil nil )
```

- Run a parametric analysis sweeping the width. In ADE L , under Tool select Parametric Analysis.

Parametric Analysis – spectre(O): EE223 inverter_tplh schematic

Tool Sweep Setup Analysis Help caden

Sweep 1 Variable Name width Add Specification ▼

Range Type From/To ▼ From 120n To 300n

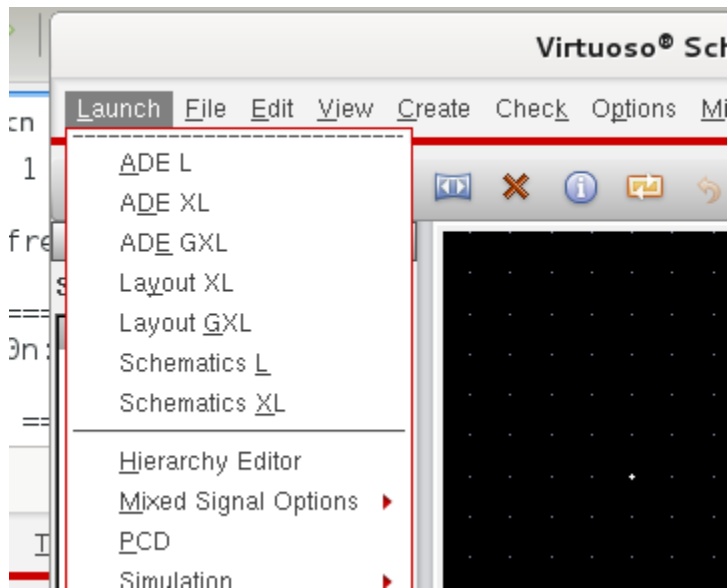
Step Control Linear Steps ▼ Step Size 10n Select ☐

- After the parametric analysis is complete, go back to calculator and plot the functions to find the optimal size for your transistors.
- You can also use risetime and falltime to get the correct width value. We have to use the ymax function so we can extract a value since rise time and falltime are continuous functions in cadence. See below.

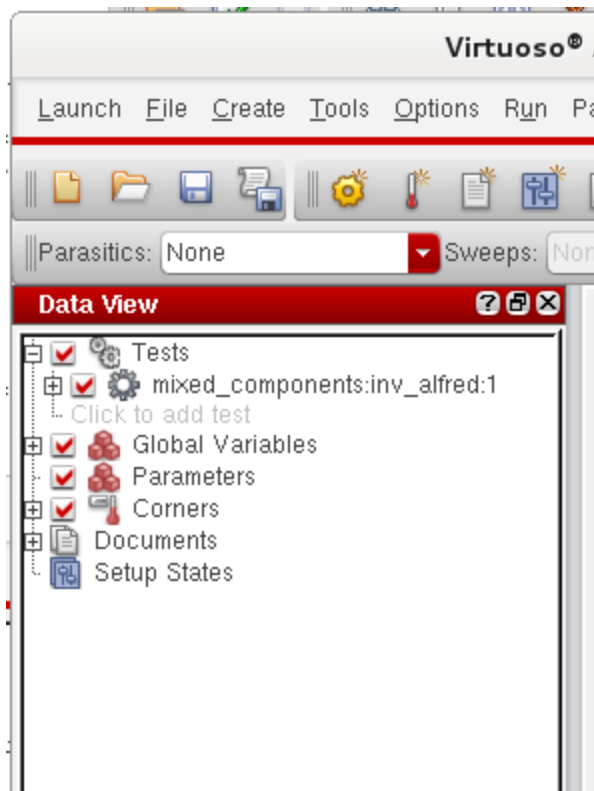
Test ^	Name	Type	Expression/Signal/File	Plot	Save
mixed_c...		signal	/vout	<input type="checkbox"/>	<input type="checkbox"/>
mixed_c...		signal	/vin	<input type="checkbox"/>	<input type="checkbox"/>
mixed_c...	risetime	expr	riseTime(VT("/vout") 0 nil 1 nil 10 90 t "time")	<input type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	falltime	expr	riseTime(VT("/vout") 1 nil 0 nil 10 90 t "time")	<input type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	ristimev...	expr	ymax(riseTime(VT("/vout") 0 nil 1 nil 10 90 t "time"))	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	falltime...	expr	ymax(riseTime(VT("/vout") 1 nil 0 nil 10 90 t "time"))	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	tp _{hl}	expr	delay(VT("/vin") 0.5 1 "rising" VT("/vout") 0.5 1 "fallin...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	tp _{lh}	expr	delay(VT("/vin") 0.5 1 "falling" VT("/vout") 0.5 1 "risin...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
mixed_c...	tp	expr	((0.5 * delay(VT("/vin") 0.5 1 "rising" VT("/vout") 0.5 1...	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

OCEAN and ADE XL

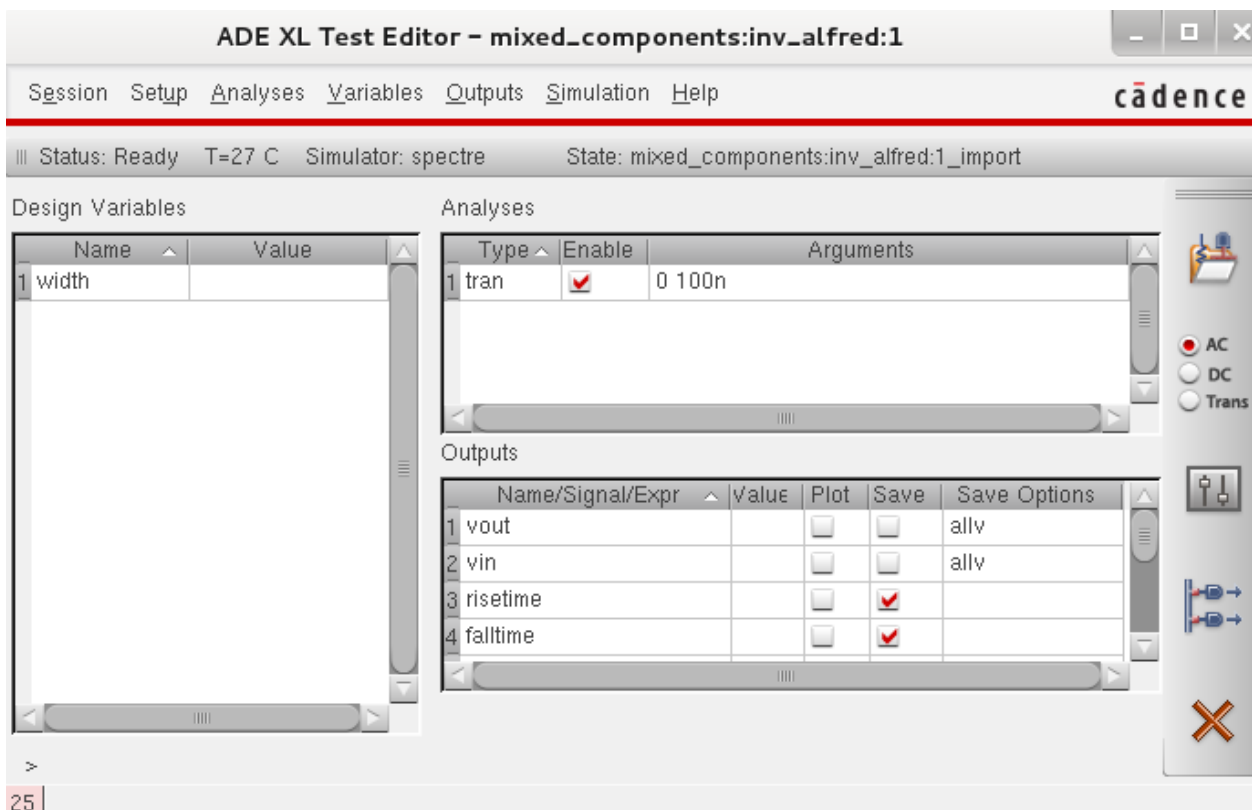
8. Ocean. Lets say you want to use a different transistor for whatever reason and want to find its sizing. We can simply save a couple of scripts (inside ADE L and XL) and modify some files to get desired results instead of recreating the whole test bench. The following uses XL.
9. Start by opening up ADE XL and setting up a test bench inside it. Select "Create New View" and press OK.



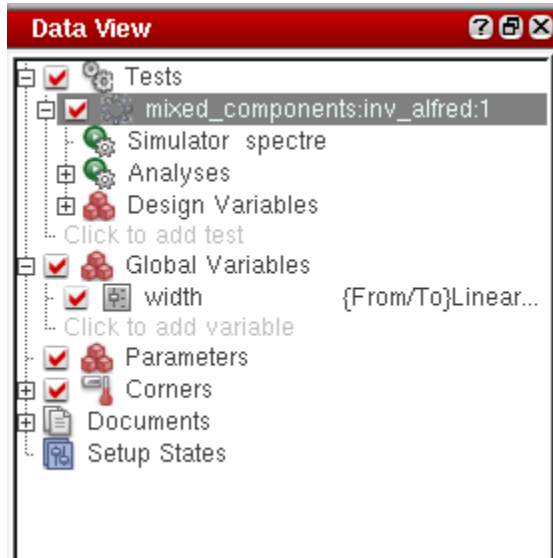
10. Underneath data view you will see a couple of options.




11. Click and click to add test and it will open a window similar to ADE L.

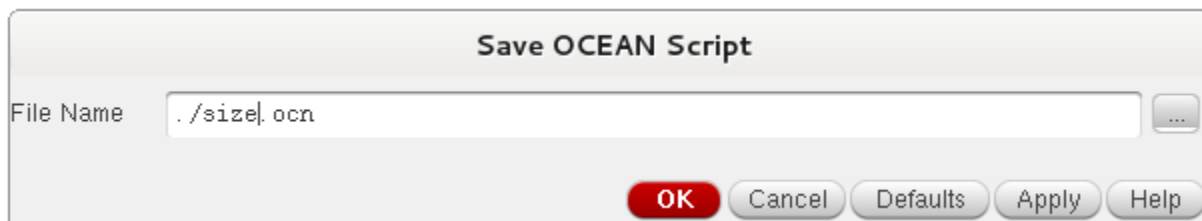


12. This is very similar to L. Set up the test bench similar to what you did before. Run a transient analysis and select outputs and rise times, fall times, delays, etc. **Leave width blank.**
13. Under global variables in Data View you can add width. You can either set it up as a single value or run a sweep for certain variables.

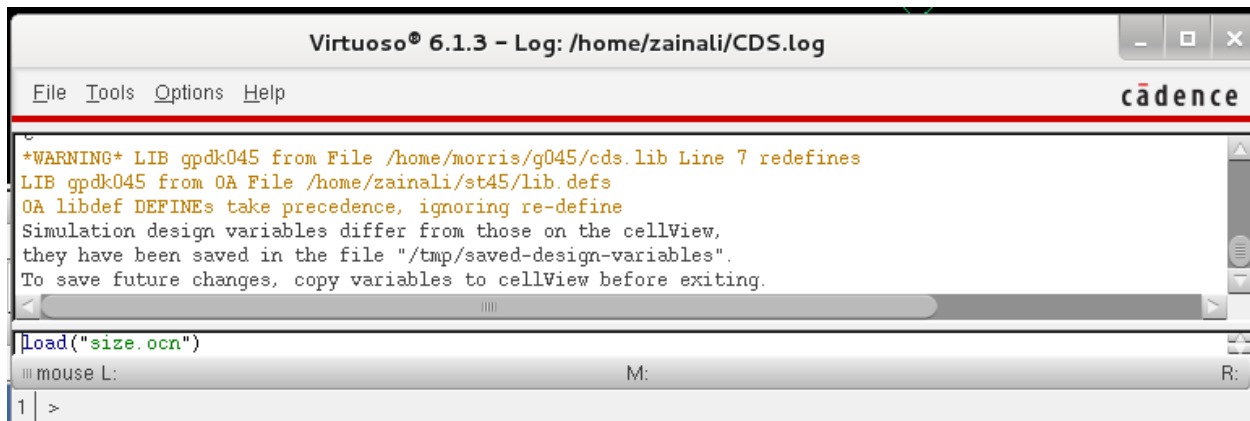


14. ADE XL is much easier for running parametric analysis. Next we will save an ocean script.

15. You can either click on File→ Save script or Click on the Save script icon () next to the normal button on the toolbar. Next step is to run the ocean script. The default directory will be the st45 folder where you ./s45 script to start virtuoso is located.



16. To run the ocean script simply type load("size.ocn") in the main virtuoso window and hit enter. Be patient, it will take a while to run depending on your sweep size.



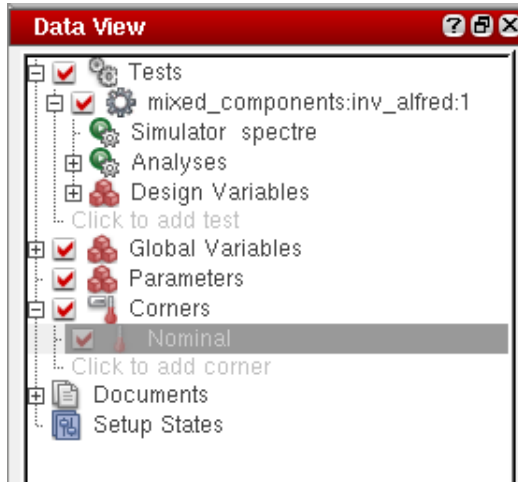
17. If the plot window keeps closing go back to your ocean script. At the end there is a "End XL Mode command" section. Just comment `ocnxlEndXLMode()` by pulling a semicolon in front of it. Rerun the ocean file and it won't close the plot anymore.

```
;===== End XL Mode command =====
;ocnxlEndXLMode()
```

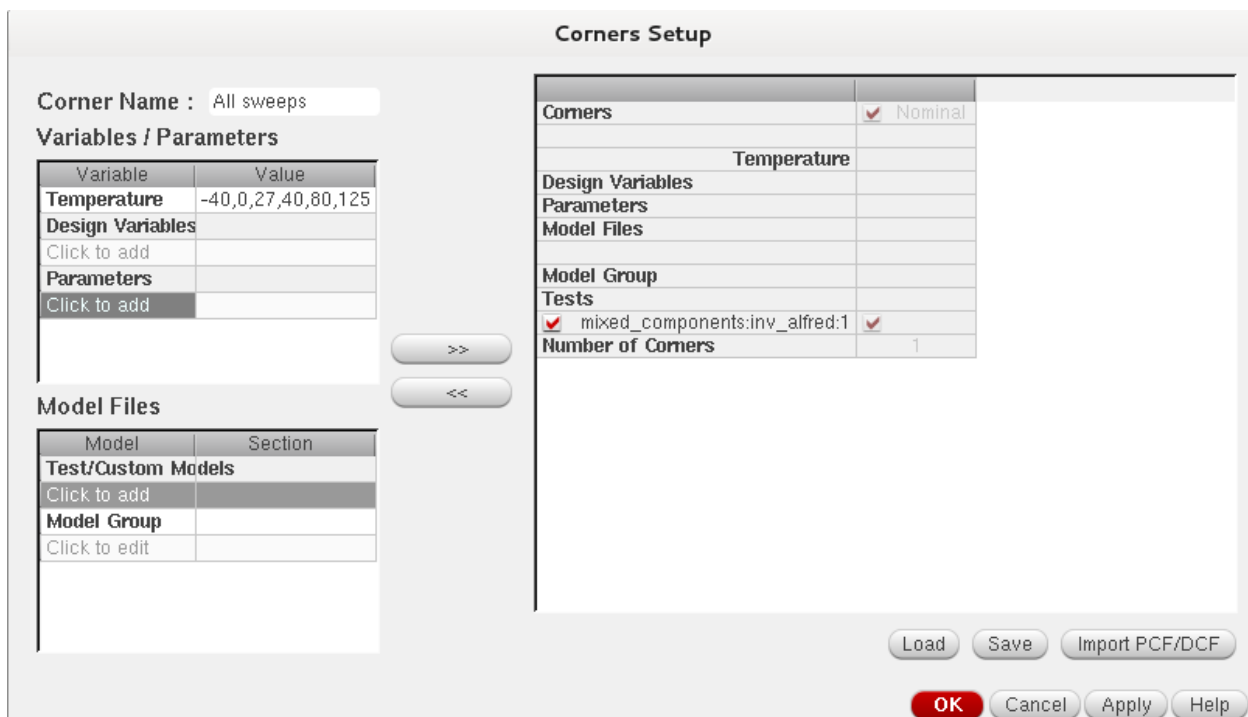
18. Once you have the plot you can figure out what the correct width ratio is.
19. Make a new schematic and name it `inv_lowvt`. Copy and paste the original components and simply change the transistors with `pmos1v_lvt` and `nmos1v_lvt`. Keep everything else the same.
20. Make a copy of `size.ocn` and name it `size_lvt.ocn`. Open it with a text editor (such as `gedit`) and replace all instances of `inv` with `inv_lowvt`. Run file `size_lvt.ocn` and it will plot the data with lowvt transistors. You can repeat the above steps with `highvt` and whatever else is in your library.
21. **Note: This is just a proof of concept.** If you are more comfortable with the ADE L/XL environment, just use that. This might help people process some information slightly faster. If you are interested in ocean just google a manual and look up functions.

Corners

22. **Corners:** Under data view select “Click to add corner”. (If you are using ADE L then look under setup and then model libraries and you can do the same thing).




23. You will get the following window. Temperature is a predefined variable in Virtuoso. You can simply enter values. We are testing from -40 to 125. It's in degrees Celsius. You can also add parameters and design variables and sweep them here.




24. Under Model Group Select “Click to edit”. You will get the following window. Select “Click to add”. It might take a little while to load. Do not Click on the little explore button. Make sure you click on “Click to add”.

Add/Edit Model Groups

Model Groups

Model Groups: 


Model Files

Model		Section
Click to add		








25. Mirror it to the image below. You can just type it in once and copy paste the model path. Make sure red arrow is selected and you should see a drop down menu. Add six of these so you can add all the different corners as shown below. Hit Ok.

Add/Edit Model Groups

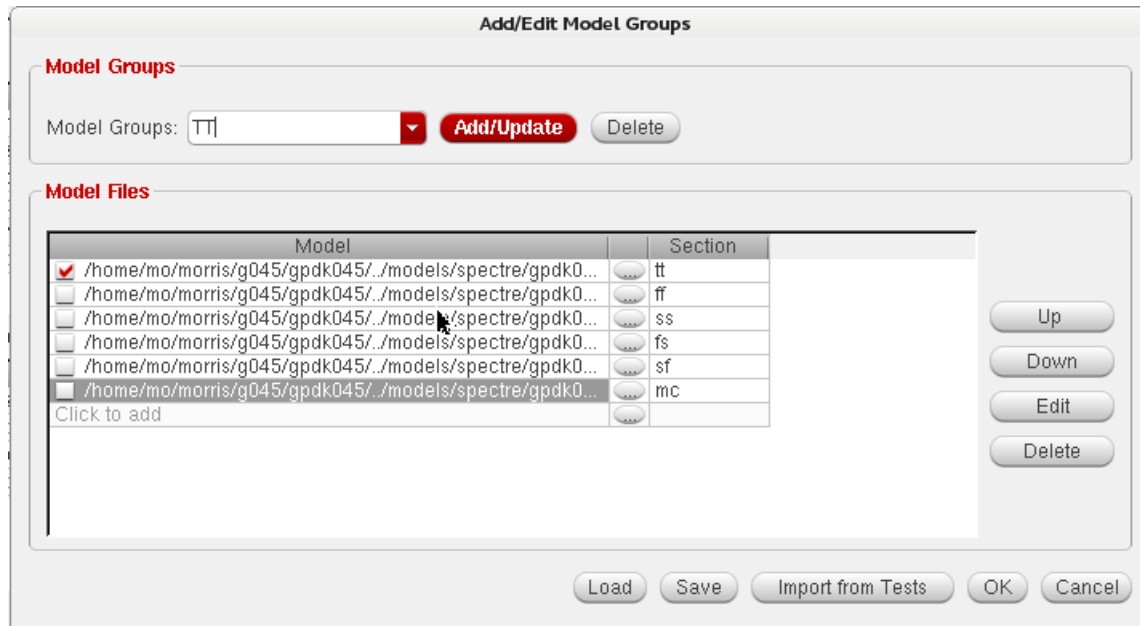
Model Groups

Model Groups: 

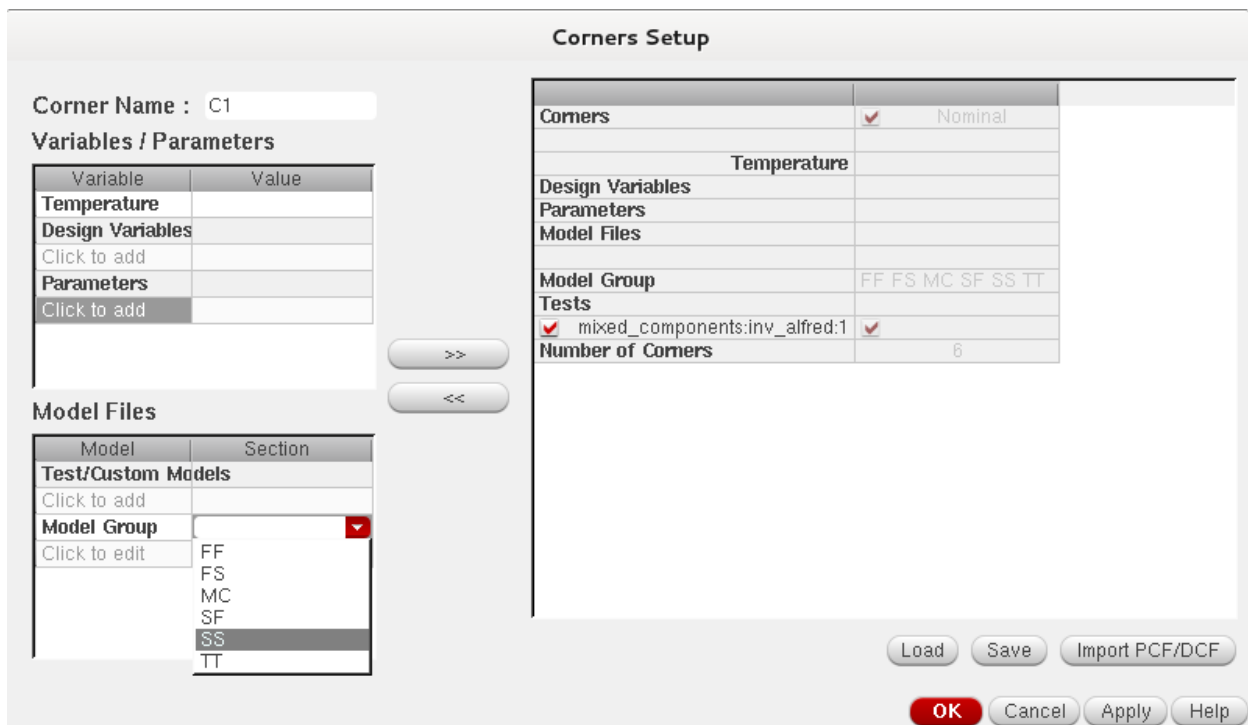
Model Files

Model		Section
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		tt
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		ff
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		ss
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		fs
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		sf
<input checked="" type="checkbox"/> /home/mo/morris/g045/gpdk045/./models/spectre/gpdk045.scs		mc
Click to add		

26. It is very important you add all the names one by one. So for TT click on add/update after selecting it. Repeat for FF, SS and so on.



27. Once you add all of them you can see a dropdown menu Now go back to your Corner setup window. In the Model Group under Section you will see the 6 models if you set it up properly. Add all 6 of them one by one.



28. Now that temperature and Models are added simply hit the Add/Update Corner button(it's the red one below) and you should get something similar to this.

Corners Setup

Corner Name : C2

Variables / Parameters

Variable	Value
Temperature	
Design Variables	
Click to add	
Parameters	
Click to add	

Model Files

Model	Section
Test/Custom Models	
Click to add	
Model Group	
Click to edit	

Corners Setup Table:

Corners	Nominal	C1
Temperature		-40,0,27,40,80,125
Design Variables		
Parameters		
Model Files		
Model Group	FF FS MC SF SS TT	FF FS MC SF SS TT
Tests		
<input checked="" type="checkbox"/> mixed_components:inv_alfred:1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Number of Corners	6	36

Buttons: Load, Save, Import PCF/DCF, OK, Cancel, Apply, Help

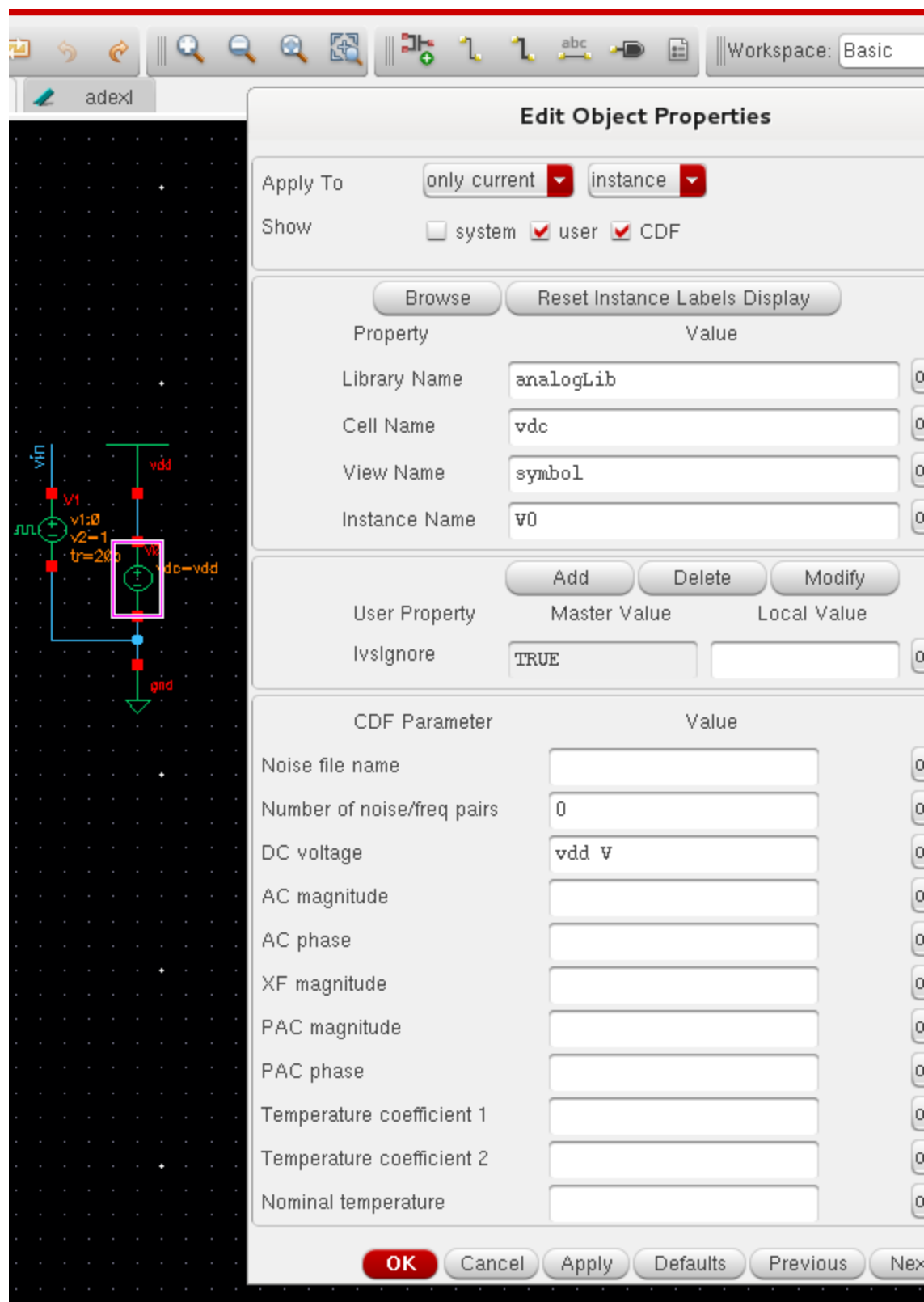
29. Save your sweep file using the Save button. Next time you need to run a corner analysis, simply reload the file and you can skip all of the above steps.
30. Go back to data view and make sure corner is selected.

Data View

- ☒ Tests
 - ☒ mixed_components:inv_alfred:1
 - ☒ Simulator spectre
 - ☒ Analyses
 - ☒ Design Variables
 - Click to add test
 - ☒ Global Variables
 - ☒ Parameters
 - ☒ Corners
 - ☒ Nominal
 - ☒ C0
 - temperature -40,0,27,40,8...
 - Model Group FF FS MC SF...
 - Click to add corner
 - ☒ Documents
 - ☒ Setup States

Buttons: Data, History

31. Make sure you only have one value for width. Rerun the simulation. If you sweep width again it will simply run $36 \times (\text{number of widths})$ that you sweep. It will give you your rise and fall times for various corners.
32. Change the main power supply in the schematic and just call it vdd instead of 1V.



33. In Corners, under design variables , now select vdd and enter values 0.9, 1, 1.1.

Corners Setup

Corner Name : C0

Variables / Parameters

Variable	Value
Temperature	-40,0,27,40,80,125
Design Variables	
vdd	0.9,0.95,1,1.05,1.1
Click to add	
Parameters	
Click to add	

>> <<

Model Files

Model	Section
Test/Custom Models	
Click to add	
Model Group	...FS MC SF SS TT
Click to edit	

Corners	<input checked="" type="checkbox"/> Nominal	<input checked="" type="checkbox"/> C0
Temperature		-40,0,27,40,80,125
Design Variables		
vdd		
Parameters		
Model Files		
Model Group		FF FS MC SF SS TT
Tests		
<input checked="" type="checkbox"/> mixed_components:inv_alfred:1	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Number of Corners	1	36

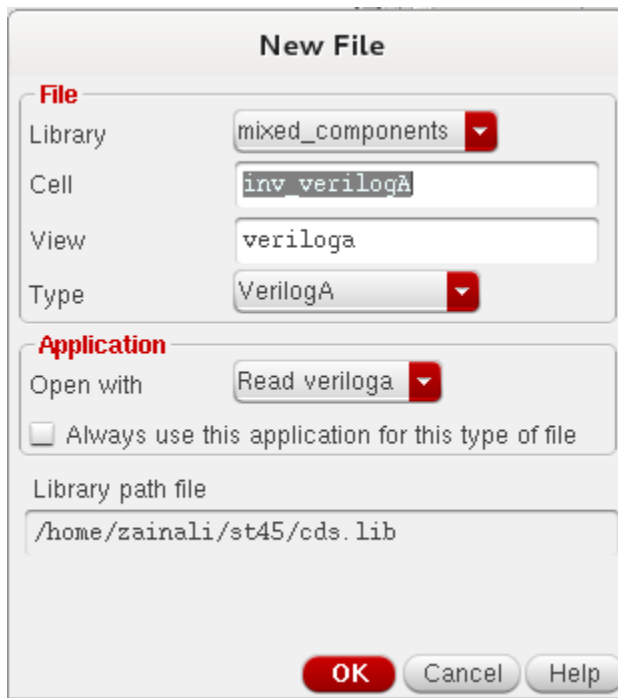
Load Save Import PCF/DCF

OK Cancel Apply Help

34. Re-run the simulation. Now you will have your voltage corners too. You can vary the numbers as required. Just keep it mind, each variation adds 36 tests already in there. Modify the test bench for faster results.

Verilog - A

35. In the main virtuoso window type in editor = "gedit" and press enter. This will change the editor to gedit. (If you really like to use vi, you can skip this step. If you don't know what vi is, then just change your editor to gedit)
36. Create a new file. Use the following template. Save it in the same library as your inverter. We are basically making a verilogA file. It will open with gedit (if you set it up correctly). **Name the file inv_verilogA . If you name it the same as your inverter you will not be able to create a symbol.**



37. Write your Verilog code. If you did it properly, it will ask you to create a symbol. Else it will give you syntax errors. Sample code is below.

// VerilogA for mixed_components, inv_verilogA, verilogA

```
`include "constants.vams"
`include "disciplines.vams"
```

```
module inv_verilogA(in,out, vss, vdd);
```

```
  inout vdd, vss;
  input in;
  output out;
```

electrical in, out, vss, vdd;

analog begin

if(V(in)>((V(vdd)-V(vss))/2))

V(out)<+ V(vss);

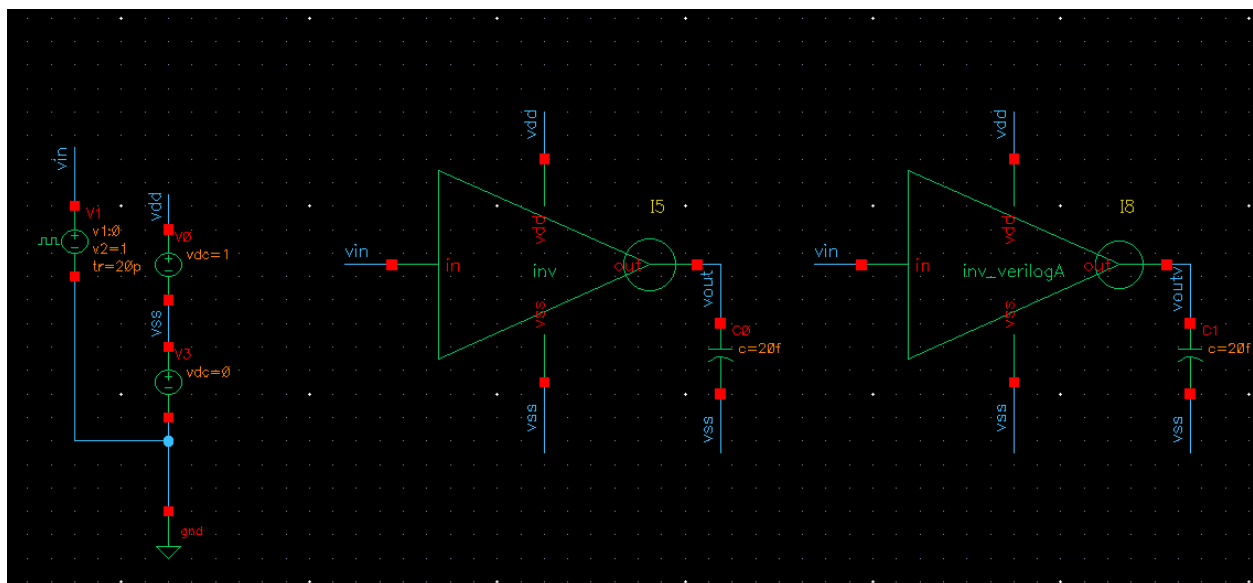
else

V(out)<+ V(vdd);

end

endmodule

38. Put everything in the same inverter test bench.

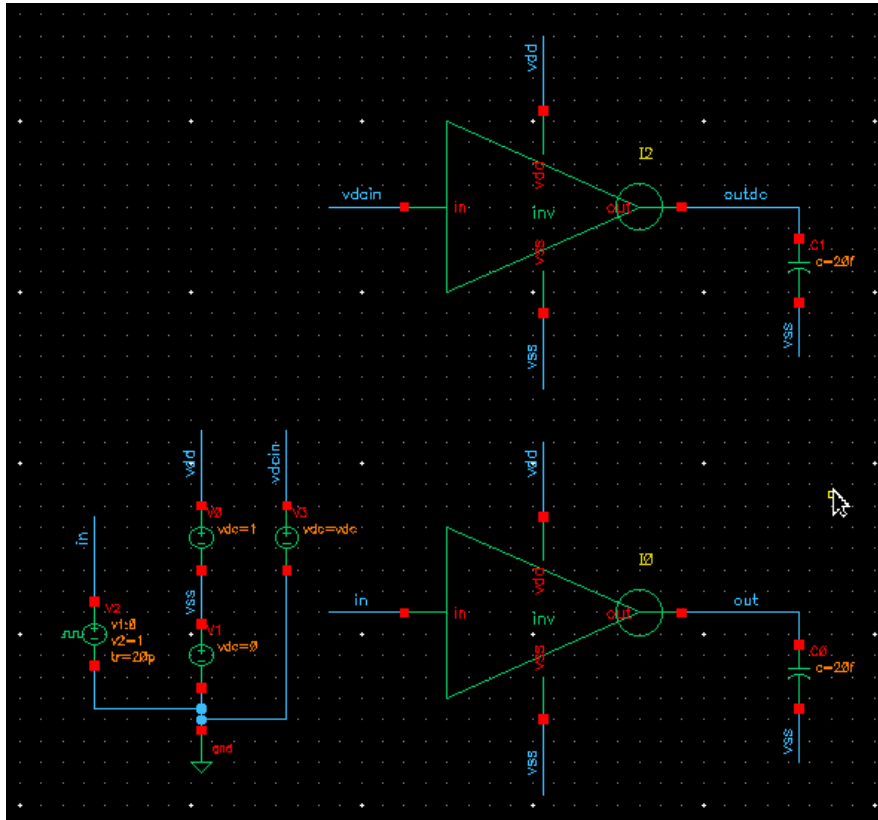


39. In ADE , plot the vin, vout and voutv. You can see the difference between an ideal model (verilogA) and actual transistor level implementation.

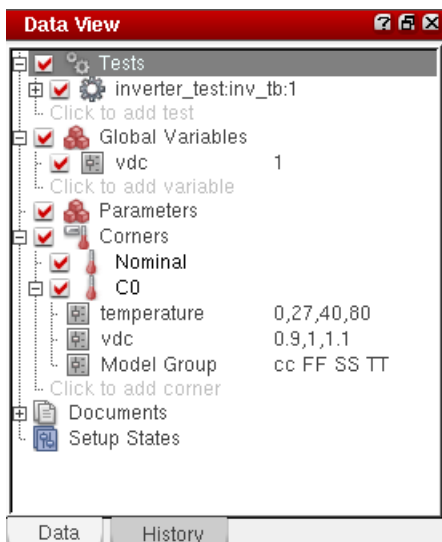
40. VerilogA becomes more useful when you are trying to implement complex systems. You might need to model it in varying ways depending on your output requirement.

Vout vs Vin + PVT

41. Copy and paste the inverter symbol one more time . Also add a DC source and declare it as a variable. I named my input dc souce as vcd, and changed input to the inverter to vcdin and output to outdc.



42. Declare the vdc as 1 under global variables and then select your corners to run.



43. Choose the analysis under DC analysis under tests in ADE XL.

Choosing Analyses -- Virtuoso® Analog Design Enviror

Analysis: ☐ tran ☒ dc ☐ ac ☐ noise
☐ xf ☐ sens ☐ dcmatch ☐ stb
☐ pz ☐ sp ☐ envlp ☐ pss
☐ pac ☐ pstb ☐ pnoise ☐ pxf
☐ psp ☐ qpss ☐ qpac ☐ qpnoise
☐ qpxf ☐ qpasp

DC Analysis

Save DC Operating Point ☒
Hysteresis Sweep ☐

Sweep Variable

☐ Temperature
☒ Design Variable Variable Name: vdc
☐ Component Parameter Select Design Variable
☐ Model Parameter

Sweep Range

☒ Start-Stop Start: 0 Stop: 1
☐ Center-Span

Sweep Type

Linear ☐ Step Size
☒ Number of Steps: 101

Add Specific Points ☐

Enabled ☒ Options...

OK Cancel Defaults Apply Help

44. Add the outputs vdcin and outdc to your results window.

Test	Name	Type	Expression/Signal/File	Plot	Save	Spec	Weight
inverter_test:inv_tb:1		signal	/in	<input type="checkbox"/>	<input type="checkbox"/>		
inverter_test:inv_tb:1		signal	/out	<input type="checkbox"/>	<input type="checkbox"/>		
inverter_test:inv_tb:1		signal	/vdcin	<input checked="" type="checkbox"/>	<input type="checkbox"/>		
inverter_test:inv_tb:1		signal	/outdc	<input checked="" type="checkbox"/>	<input type="checkbox"/>		

45. In calculator, select the cross function. Subtract input from output to get the crossing point.
`cross((VS("/outdc") - VS("/vdcin")) 0 1 "either" nil nil)`

cross

Signal: VS("/outdc")-VS("/vdcin")

Threshold Value: 0

Edge Number: 1

Edge Type: either

Number of occurrences: single

Plot/print vs.: time

46. Add the cross time equation to outputs.

ADE XL Test Editor - inverter_test:inv_tb:1

Session Setup Analyses Variables Outputs Simulation Help

Status: Ready T=27 C Simulator: spectre State: inverter_test:inv_tb:1_active

Design Variables

Name	Value
1 vdc	

Analyses

Type	Enable	Arguments
1 dc	<input checked="" type="checkbox"/>	t 0 1 101 Linear Number of Steps Start-Stop
2 tran	<input type="checkbox"/>	0 100n

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
1 in		<input type="checkbox"/>	<input type="checkbox"/>	allv
2 out		<input type="checkbox"/>	<input type="checkbox"/>	allv
3 vdcin		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
4 outdc		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv

Setting Outputs -- Virtuoso® Analog Design Environment (1)

Selected Output

Name (opt): crosstime

Expression: VS("/vdcin") 0 1 "either" nil nil

Calculator: Open Get Expression Close

Will be: ☒ Plotted/Evaluated

Measure type: ☒ Sig/Exp ☐ OCEAN ☐ MATLAB

Add Delete Change Next New Expression

Table Of Outputs

Name/Signal/Expr	Value	Plot	Save Option
1 in		no	allv
2 out		no	allv
3 vdcin		yes	allv
4 outdc		yes	allv

OK Cancel Apply Help

47. Run the simulation. (Note: My run does not have all process corners). Should see something like this.

inv_tb		adexl															
Outputs Setup		Results		Diagnostics													
View: Default		Show	Evaluate	Plot All	Replace	Export	Spec Summary										
		Parameter	Nominal					C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7	C0_8	
		Model G...						FF	FF	FF	FF	FF	FF	FF	FF	FF	
		temperat...	27					0	27	40	80	0	27	40	80	0	
		vdc	1					900m	900m	900m	900m	1	1	1	1	1.1	
Test	Output	Value	Spec	Weight	Pass/Fail	Min	Max	C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7	C0_8	
inverter_testinv_tb:1	/vdcin	pending						pending	pending	pending	pending	pending	pending	pending	pending	pending	
inverter_testinv_tb:1	/outdc	pending						pending	pending	pending	pending	pending	pending	pending	pending	pending	
inverter_testinv_tb:1	crosstime	pending						pending	pending	pending	pending	pending	pending	pending	pending	pending	

48. You will receive plots of V_{out} vs V_{in} and then points of crossing for the V_{in} vs PVT. You can change axes on the graph or extract data and plot in Matlab.