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Research on cascade multilevel inverter with single DC source by using three-phase transformers

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ABSTRACT

One of the most significant recent advances in power electronics is the multilevel inverter. Using this concept the power conversion is performed with enhanced power quality. In this scenario cascade H-bridge multilevel inverter (CHBMLI) is an exceptional one and it has many inherent benefits like: (1) its modular structure, (2) it can be easily implemented through the series connection of identical H-bridges, (3) generate near sinusoidal voltages with only fundamental frequency switching and finally and (4) no electromagnetic interference or common-mode voltages. This flexibility has resulted CHBMLI topology in various applications like medium-voltage industrial drives, electric vehicles and the grid connection of photovoltaic-cell generation systems. But one of the major limitations of the cascade multilevel converters is requirement of isolated dc voltage sources for each H-bridge, this increases the converter cost and reduces the reliability of the system. This drawback is the key motivation for the present work. The present paper investigates different cascade multilevel inverter (CMI) based topologies with reduced dc sources and finally the proposed CMI with single dc source by employing low frequency transformers is presented. Proposed topology significantly reduces size when compared with conventional topologies and increases the reliability. To verify the performance of proposed architecture, prototype experiments are carried out and adequate results are presented.

1. Introduction

Multilevel converter gives massive advantages compared with conventional and very well known two level converters like; high power quality waveforms, low switching losses, high voltage capability, low electromagnetic compatibility (EMC) etc. [1–3]. Fig. 1 shows the most common multilevel power converters and the classical two level converters. But one of the most significant multilevel topology is cascade H-bridge multilevel-inverter (CHBMLI) [4,5]. CHBMLI has numerous advantages over diode-clamped (DCMC), flying-capacitor (FCMC) and p2 multilevel converters (P2MC) [6,7]. All these converters are compared in terms of feasibility of their utilizations and applications [8].

According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components [9], so less the components more the reliability. Compared to *m-level* DCMC, FCMC, and P2MC, which use $m-1$ capacitors on the dc bus, the CMC uses only $(m-1)/2$ capacitors for same *m-level*. Clamping diodes are not required for FCMC, P2MC and CMC [10]. In overall P2MC undeniably require too many components as compared to other multilevel converters, so it is not suitable for higher voltage levels. However comparing CMC with DCMC, FCMC and P2MC, it requires least number of components and its dominant advantage is circuit layout with flexibility. According to recent survey CHBMLI are extensively used in compressors (82%) [11,12], synchronous motors (92%) [13,14], converters (98%) [15–17] and power generation plants (47%) [18]. In addition it is best suited for the power quality devices like, STATCOMs and universal power quality conditioners [19–21,24]. Although this inverter topology is more preferable still there are some aspects that require further development and research. The primary issue that strikes about conventional CHBMLI is that, it uses separate dc source for each H-bridge, this not only yield significant cost but also drastically effects efficiency and reliability of a converter. This issue becomes the core motivation for this paper. In the present paper we have investigated different cascade multilevel inverter (CMI) based topologies, which use reduced number of dc sources and attains high power quality waveforms. Finally our proposed CMI with single DC source is presented. The relative performance is evaluated with prototype experiments.

The rest of the paper is organized as follows. The conventional CMI structures, working principles, their advantages and disadvantages are described in Section 2. Proposed CMI with single dc source using three-phase transformers is introduced in Section 3.

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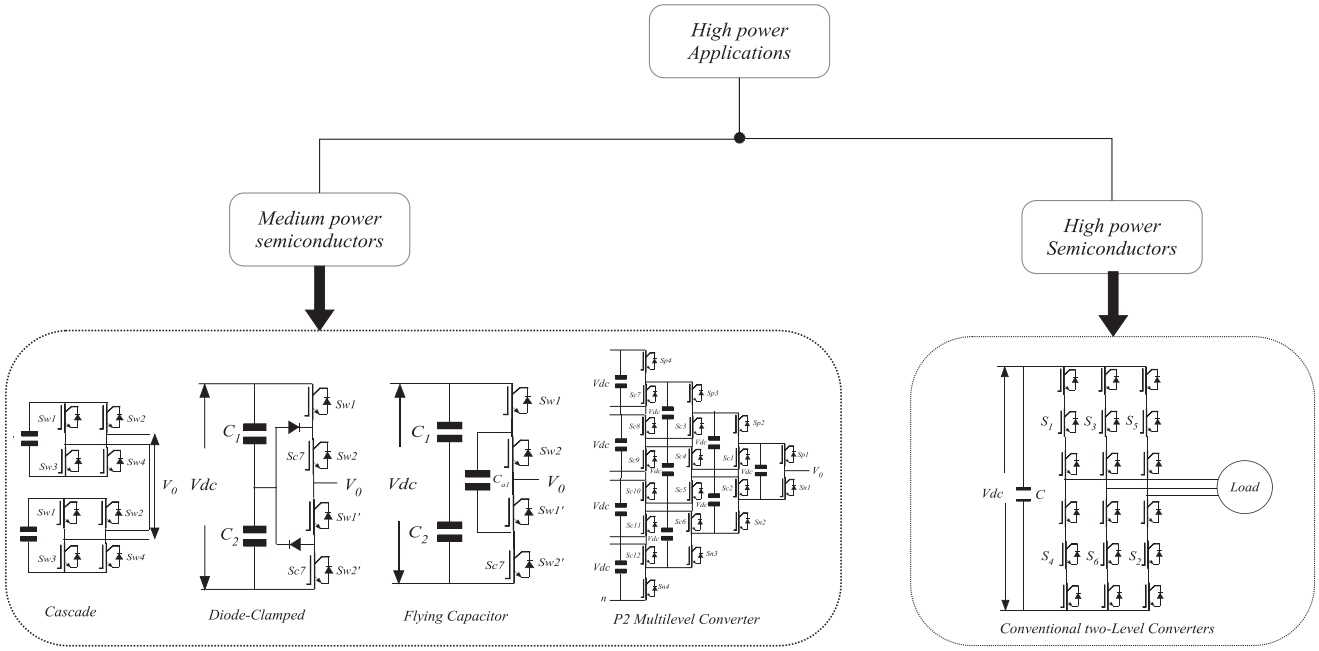


Fig. 1. Classical two level power converters versus most common mutlilvel power converters.

Comparative study between conventional and proposed converter is discussed in Section 4. Finally conclusions and discussion are presented in Section 5.

1.1. Switching techniques

Recurrently three major PWM techniques are applied in multilevel inverters: (1) sinusoidal PWM (SPWM), (2) third harmonic injection PWM (THPWM), and (3) space vector PWM (SVM) [29–31]. Lezana et al. [21] had reported about multicarrier based PWM techniques. To be specific, sinusoidal carrier based PWM approaches are quite good to handle. According to literature survey two major carrier based PWM approaches are available. Namely, phase shifted PWM and level shifted PWM techniques. Fig. 2 demonstrates the carrier based PWM approaches. However an in-depth assessment between PWM methods can be found in [22,23].

In brief, rather than level shifted PWM, phase shifted PWM technique had finite merits like; no rotation in switching, less switching losses and easy to implement. However, in present article all productive topologies are implemented with sinusoidal PWM approach. Next sections provide the details of conventional topologies and their operating principles and finally figure out the merits and demerits.

2. Conventional cascade H-bridge topologies

2.1. Cascade H-bridge with separate dc sources

Architecture shown in Fig. 3a demonstrates three-phase series H-bridge inverter appeared in 1975 [20], but several recent patents have been obtained for this topology as well. Since this topology consist of series power conversion cells, the voltage and power

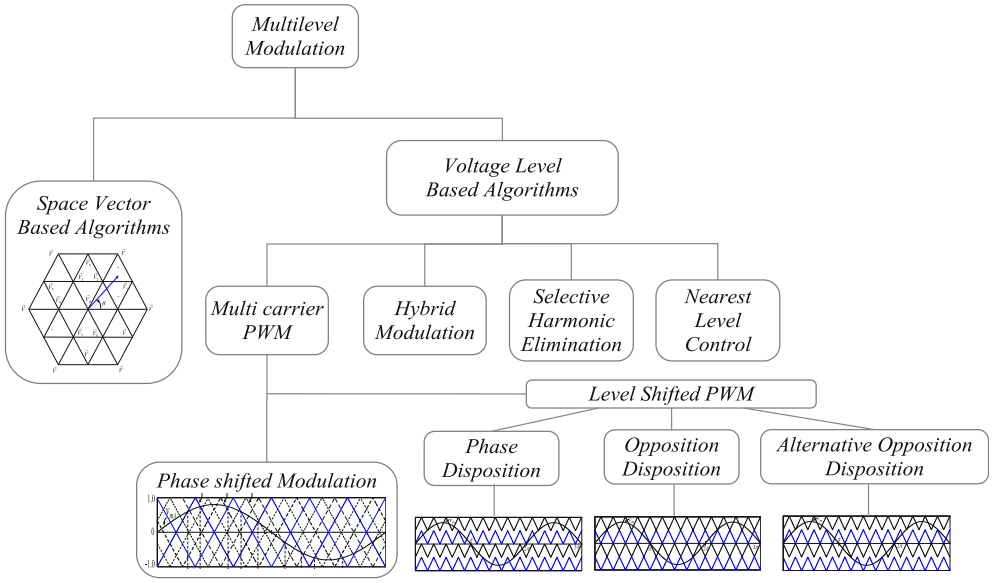
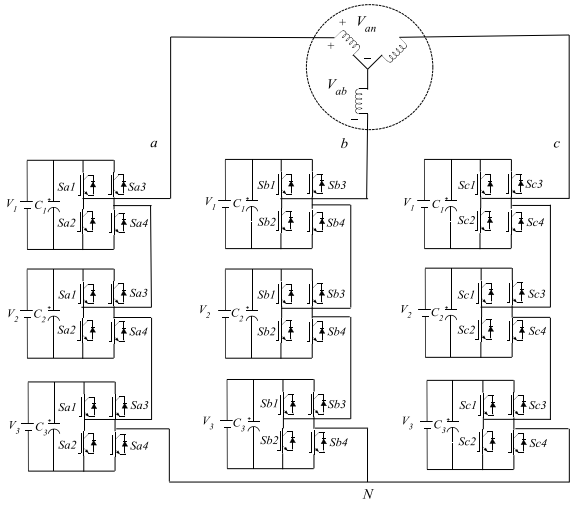
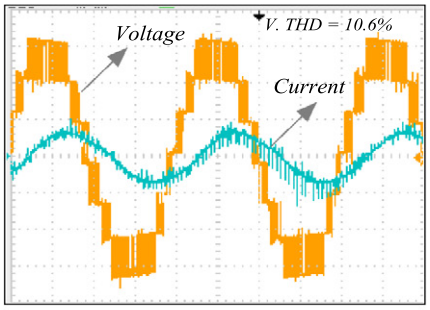


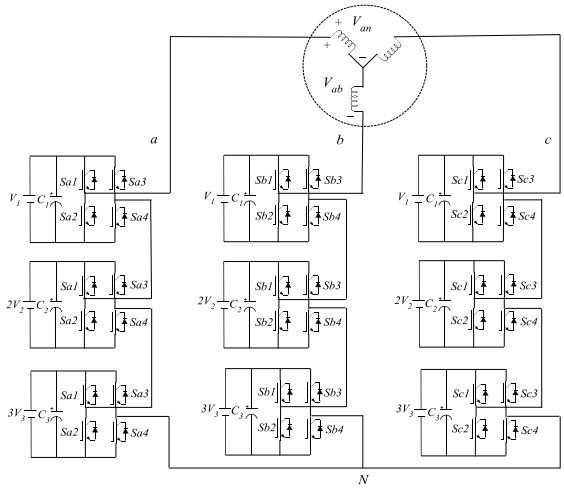
Fig. 2. Details of phase shifted and level shifted PWM techniques (top to bottom).



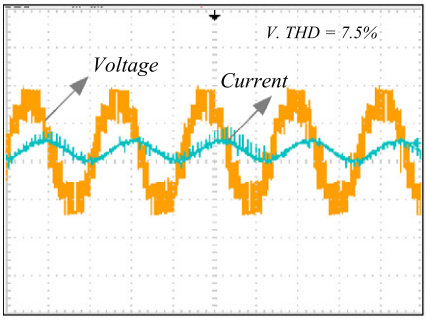
(a) Details of conventional cascade H-Bridge inverter.



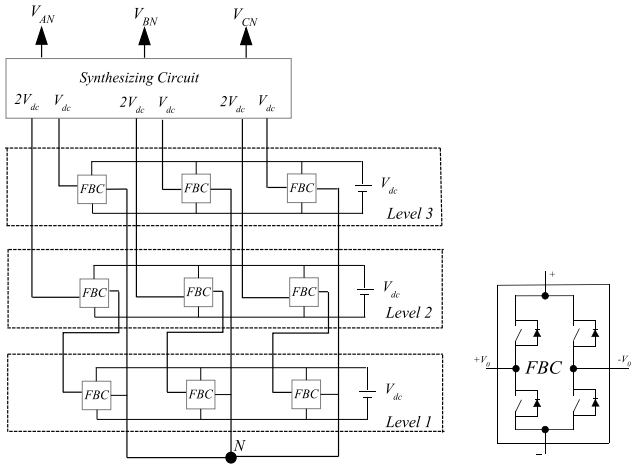
(b) Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), Time scale: 5 ms/div.



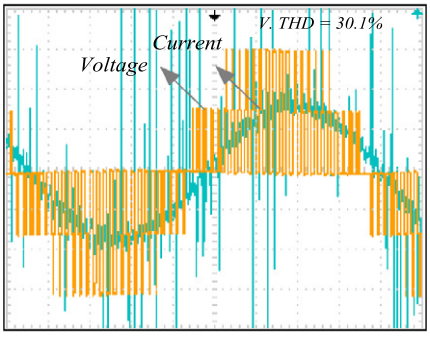
(c) Details of conventional cascade H-Bridge inverter with unequal DC sources.



(d) Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), Time scale: 9 ms/div.

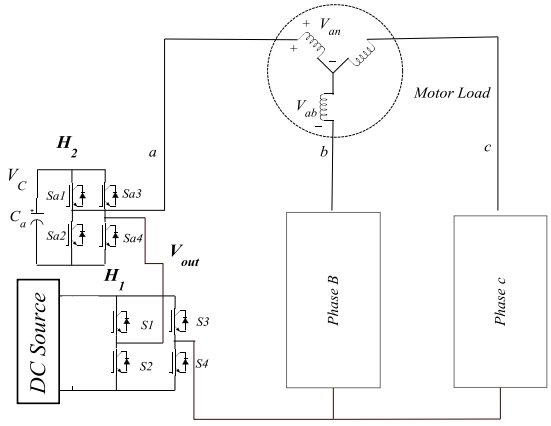


(e) Details of conventional cascade H-Bridge multilevel with reduced DC sources.

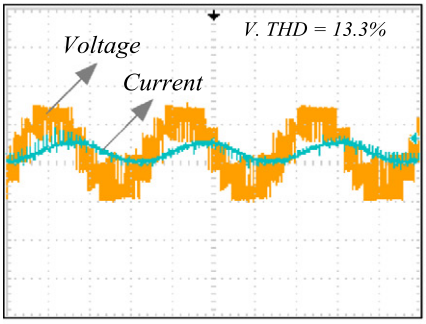


(f) Details of output voltage (scale: 60 V/div), output current (scale: 2 A/div), Time scale: 2 ms/div.

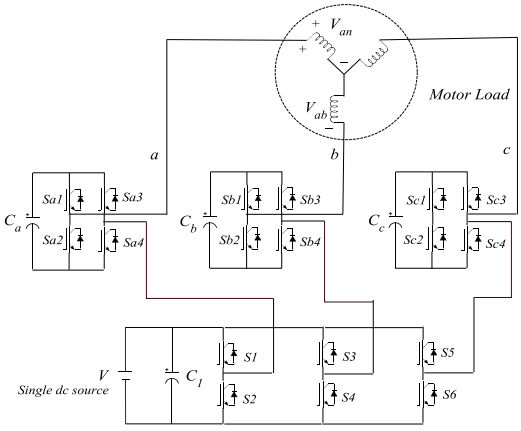
Fig. 3. (a and b) Presents details of conventional CMI and output voltage waveform, (c and d) presents details of conventional CMI with unequal dc voltages and output voltage waveform, (e and f) presents details of CMI with reduced DC sources and output voltage waveform, (g and h) presents details of hybrid CMI with h-bridge cells and output voltage waveform, (i and j) presents details of hybrid CMI with bottom three leg inverter and output voltage waveform and (k and l) presents details of cascade CMI with single dc sources by using single-phase transformers.



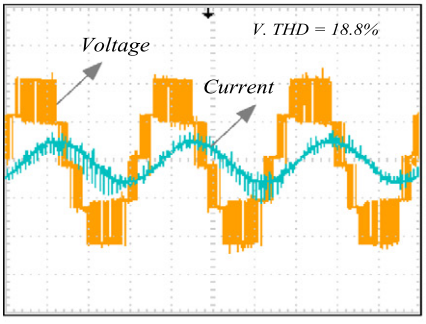
(g) Details of hybrid cascade multilevel inverters with H-Bridge cells.



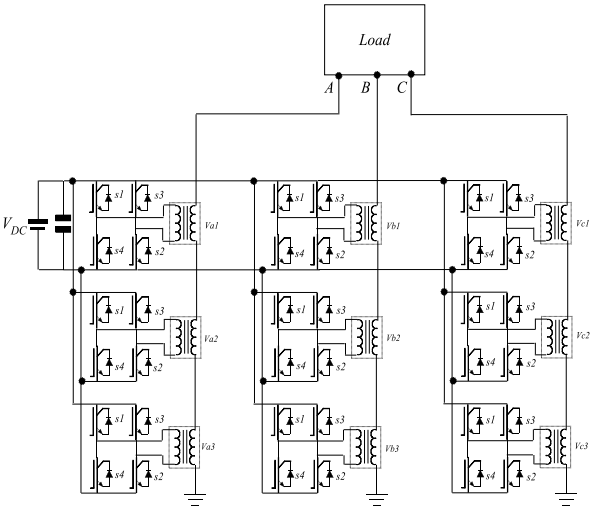
(h) Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), Time scale: 6 ms/div.



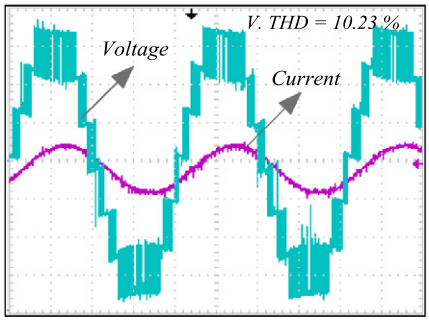
(i) Details of hybrid cascade multilevel inverters with bottom three leg inverter.



(j) Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), Time scale: 6 ms/div.



(k) Details of cascade multilevel inverter with single-phase transformers.



(l) Details of output voltage (scale: 60 V/div), output current (scale: 5 A/div), Time scale: 5 ms/div.

Fig. 3 (*continued*)

level may be easily scaled. Numerous advantages have been figured out using this topology, which are extensively used in medium and high power applications. Fig. 3b provides output voltage waveform for seven level H-bridge cell. Examining Fig. 3b, the output phase voltage can be expressed as $V = v_1 + v_2 + v_3$, this is because all the inverters are connected in series. In fact, each single-phase full bridge inverter can generate three level outputs V_{dc}, 0 and $-V_{dc}$ and this is made possible by connecting the dc sources sequentially to the ac side via the four switching devices. Three such inverters provide seven level output waveform. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels. However, greatest limitation of this class of converter is separate dc source for each H-bridge cells. This not only increases the cost but also affects the reliability of a system. However, this inverter exhibits high degree in modularity and possible to connect directly for medium and high power applications.

2.2. Cascade H-bridge with unequal dc sources

Basically the dc voltages of the H-bridge power cells introduced in the preceding section are all the same. On the other hand, different dc voltages may be selected for the power cells [25–27,37]. Fig. 3c constructed with unequal dc voltages, the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This permit more voltage steps in the inverter and thereby yields improved voltage waveform for same number of power cells. In the presented structure the dc voltages for H_1, H_2 and H_3 are E, $2E$, $3E$ respectively. With this scenario, three-cell inverter leg is able to produce 13 level voltage waveform i.e. the voltage waveform constitutes: $6E$, $5E$, $4E$, $3E$, $2E$, E, 0, $-E$, $-2E$, $-3E$, $-4E$, $-5E$, $-6E$. Fig. 3d provides the output voltage waveform for such prospects. Thus, with the present structure, quality of waveform can be improved predominantly, but at the same time there are some drawbacks associated with the CMI using unequal dc voltages. The merits of the modular structure are basically lost. In addition, switching pattern design becomes much more difficult due to the reduction in redundant switching states. Therefore, this inverter topology has limited industrial applications.

2.3. Cascade multilevel inverter with minimum dc sources

This is one of the productive topology from CMI family. Sirisukprasert [28] had finite contribution on this archetype. CMI with minimum dc sources is shown in Fig. 3e. Presented structure is with three dc sources and nine H-bridge cells which is demonstrated in Fig. 3e. With appropriate switch combinations of each full bridge cell (FBC), three output-voltage levels can be synthesized, i.e., $+V_{dc}$, 0 and $-V_{dc}$. Herein the FBCs in levels 1 and 2 are cascade to generate a three-phase output voltage of $\pm 2V_{dc}$, while the FBCs in level 3, which is independent from levels 1 and 2 are used to generate $\pm V_{dc}$ three-phase output voltages. Fig. 3f provides experimental verification at modulation index 1. Observing output waveforms, ripple content is very high in the output voltage, which indicates poor voltage quality. Due to this, harmonic content is very high, which is not acceptable. But comparing with conventional seven level structures this converter requires only three dc sources. Thus converter is economical but not efficient. These classes of converters are extensively used in motor drive application.

2.4. Hybrid cascade multilevel inverter

The topology hybrid multilevel inverter is shown in Fig. 3g, which includes complete three-phase architecture [31,32,29,33]. One H-bridge is connected to a dc source, another H-bridge is connected to a capacitor. However dc source for first H-bridge (H_1) could be a battery or a fuel cell. The output voltage of the first H-bridge is denoted by v_1 and the output of the second H-bridge is denoted by v_2. The output voltage v_1 can be maintained at V_{dc} [34,35]. This v_1 is allied in series with an H-bridge, which in turn is provided by a capacitor voltage. The capacitor which is integrated in second H-bridge (H_2) should be maintained at the voltage V_c. Further by opening and closing the switches of H_1 appropriately, the output voltage v_1 can be made equal to $-V_{dc}$, 0, or V_{dc}, while similarly the output voltage of H_2 can be made equal to $-V_c$, 0, or V_c. As of before, modulation index range should extend greater than 1 so that converter gains adequate time to charge up and regulate the voltage. Performance verifications are shown in Fig. 3h. Observing, voltage and current waveforms are quite good. In reality, converters are extensively used in motordrive application. However, the limitation of this converter is that, it fails to operate at lower modulation indexes. Additionally, as level increase component count increases drastically, thereby reliability comes down. There are number of topologies based on this architecture, but basic principle is same. Similarly, Fig. 3i and j provide the details of another hybrid CMI with bottom three leg inverter [29,30]. Observing keenly, this architecture may use less number of components, but as of before, converter fail to operate at lower modulation indexes.

2.5. Cascade multilevel inverter with single dc source

The configurations of CMI with single dc source are illustrated in Fig. 3k. Dixon et al. [36] and Kang [38] had finite contribution regarding this archetype, in fact these class of converter highly visible in grid connected systems. However number of dc sources has been considerably reduced, because of transformer coupling on the secondary side. Further in principle of operation, it is obvious that three bridges will generate three output voltages, which results in generating a seven-level output waveform. In practice such performances are just identical to conventional CMI with separate dc sources. However, Fig. 3l provides the experimental details. On observing, output voltage quality is extremely fine and performance is fairly good and attractive. But one of the greatest limitations of this archetype is that it uses large number of transformers, so the size of the converter will increase for each additional level in output voltage.

Further, it is to be noted that, all productive topologies mentioned in Fig. 3 are tested with 3-phase, 415 V, 50 Hz, 1-HP induction motor. In case of CMI with single-phase transformers constant frequency load is used with rating 0.5 kW.

In over all, from above discussion it is concluded that, though converters are relatively good from structure point of view, but still they have drawbacks such as, usage of many dc sources, poor dc bus capacitors, and excessive number of transformers and lack of output voltage quality. For this reason, we proposed a new structure with single dc source by using three-phase transformers. Proposed structure drastically improves the output voltage quality with single dc source and single dc bus capacitance. Adding to that, proposed converter features a high modularity degree because each converter can be module with similar circuit topology and it significantly fit to attain a higher efficiency, because the devices can be switched at minimum frequency.

3. Proposed CMI with single DC source by using three-phase transformers

Before proceeding, consider Fig. 3k CMI with single dc source by employing single-phase transformers. To be noticed, these classes of converters are extensively visible in utility interfacing applications [38]. Aforesaid, this structure utilizes the single-phase

transformers for each H-bridge, which makes the converter size big and thereby increasing the cost. Besides this aspect, we proposed architecture similar in fashion, but it uses three-phase transformers on secondary side. Proposed archetype is demonstrated in Fig. 4. Readers may have idea that three-phase transformer size is quite bigger than single-phase transformers, practically it is true. But suggested topology have many inherent benefits, like high quality output voltages and input currents, low switching losses, compact in size, easy to adopt etc. however, proposed architecture dealt exhaustively with necessary illustrations with both mathematical and logical approach. Coming to structure point of view, each primary terminal of the transformer is connected to an H-bridge module so as to synthesize output voltages of $+V_{DC}$, *Zero*, $-V_{DC}$. Every secondary of transformer is connected in series to enhance the output voltage level. Further, each phase terminal is delta connected to restrain the third harmonic component. Fig. 4 articulates primary of each phase is three-phase and secondary is single-phase terminal and all three terminals are series connected and responsible for generating phase voltage. Therefore each phase can be expressed independently. As a result each phase multilevel inverter can be depicted as an isolated H-bridge cascade multilevel inverter. We can obtain the relation between input and output voltages of three-phase transformer as

$$[V_{AK};\ V_{BK};\ V_{CK}] = N[T]\begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix} \tag{1}$$

V_{ak}, V_{bk}, V_{ck} are primary terminal of phase "a", phase "b" and phase "c"

Where T is transformation matrix and defined as

$$T = \begin{bmatrix} 2/3 & -1/3 & -1 \\ -1/3 & 2/3 & -1/3 \\ -1/3 & -1/3 & 2/3 \end{bmatrix} \tag{2}$$

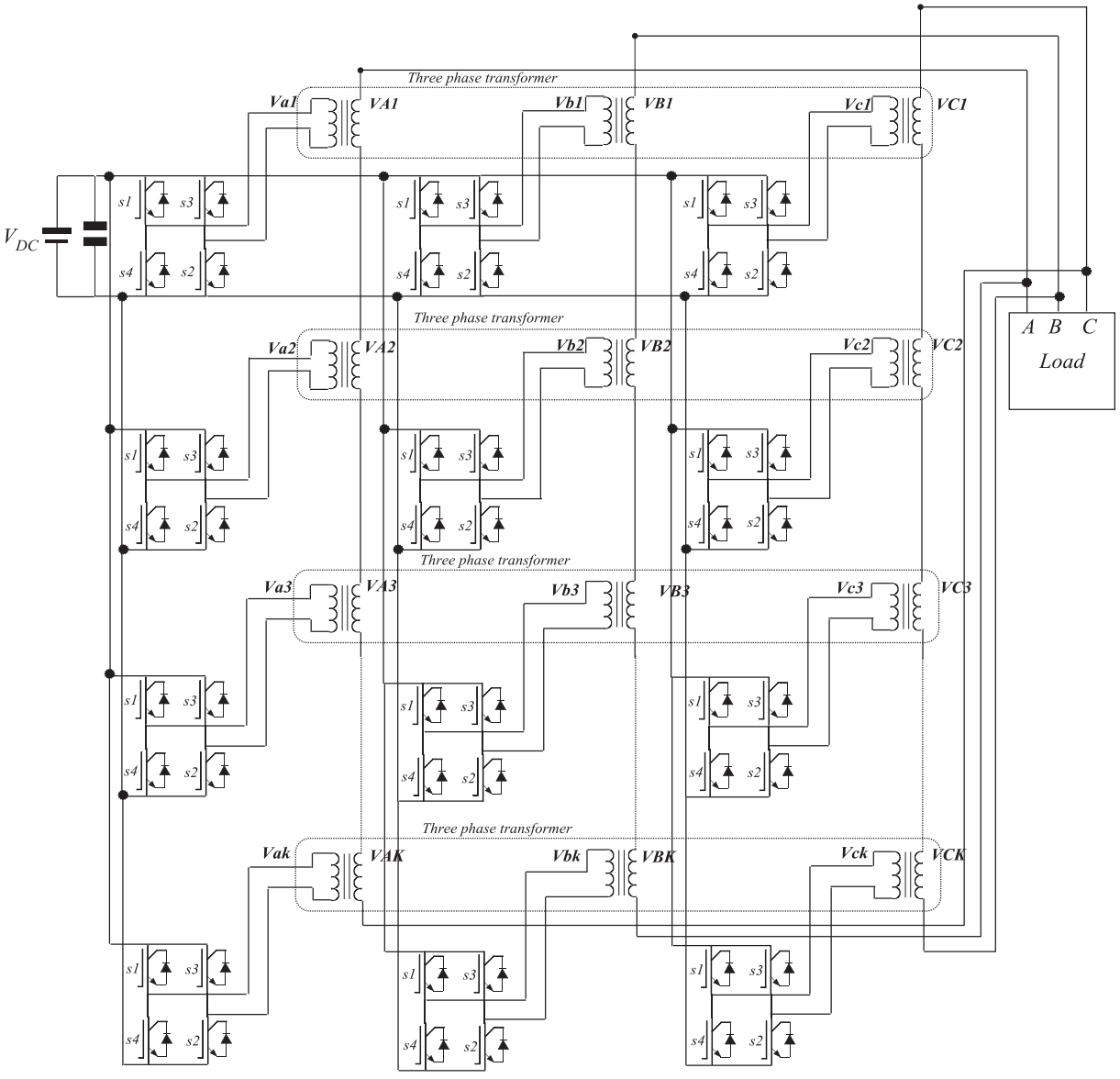


Fig. 4. Details of cascade multilevel inverter with single dc source by employing three-phase transformers.

Similarly, N is the transformation ratio (n_2/n_1) between primary and secondary and if there is a balanced input, then sum of each phase voltage would become zero.

$$V_{ak} + V_{bk} + V_{ck} = 0 \tag{3}$$

$$\begin{bmatrix} V_{Ak} \\ V_{Bk} \\ V_{Ck} \end{bmatrix} = N \begin{bmatrix} V_{ak} \\ V_{bk} \\ V_{ck} \end{bmatrix} \tag{4}$$

From (4) CMI with three-phase configuration, we are obtaining each phase output voltage of transformer as product of input voltage and transformation matrix N. But under unbalanced condition, Eq. (4) is not satisfied because primary of transformer is connected to an H-bridge cell generating V_{dc}, zero, $-V_{dc}$. So, the output voltage of V_{ak}, V_{bk}, and V_{ck} are equal to V_{dc}. Thus summation of three voltages is not equal to zero; due to this fact output voltage is unbalanced. However Eq. (1) holds good for all conditions. In other terms, we can generate voltages at $V_{ak} = V_{DC}$, $V_{bk} = -V_{DC}$, and $V_{ck} = 0$. Summation of such voltages will result to zero. However, the fundamental idea behind this is, magnetic circuit concept, notifying that flux at the primary of phase "a" will be equally influenced on phase "b" and phase "c" and becomes -1, so unbalanced relationship is also included in Eq. (1). As shown in Fig. 4, proposed multilevel inverter secondaries are connected in series so that the output is the sum of three voltages. Thus it can be represented as

$$[V_{AS};\ V_{BS};\ V_{CS}] = \left[\sum_{i=1}^{k} V_{Ai};\ \sum_{i=1}^{k} V_{Bi};\ \sum_{i=1}^{k} V_{Ci}\right] \tag{5}$$

Herein, output voltage V_{AS} is defined as summation of phase "a" voltages i.e. $V_{A1} + V_{A2} + V_{A3}$. In a similar fashion corresponding summation will produce V_{BS} and V_{CS}. Further, to confirm the proposed CMI working pattern, output voltage characteristics are examined in the next section.

3.1. Output voltage characteristics

Output voltage of the three-phase transformer will be determined by combination of A, B and C voltages and there are three possibilities in output voltage of transformer. Switching pattern of each phase and output voltage of each transformer is shown in Fig. 5. It is to be noted that, presented voltages are resultant voltages of phase "a" and such voltages are obtained by summation of three voltages i.e. V_{a1}, V_{b1} and V_{c1}. However, output voltage of proposed inverter is sum of secondary terminal voltages of transformer, which are connected in series and all these are independent of switching range from $0 < \alpha_k < \pi/2$.

From above Fig. 5, output voltage of phase "a" (V_A) is symmetrical in nature. In general form, Fourier expression can be written as:

$$V_{AK} = \sum_{n=1}^{\infty} b_{nk} \sin(n\theta) \tag{6}$$

where b_{nk} is a constant.

Output characteristics of phase "a" voltage can be obtained between three switching ranges i.e. $0 \leqslant \alpha_k \leqslant \pi/6$, $\pi/6 \leqslant \alpha_k \leqslant \pi/3$, $\pi/3 \leqslant \alpha_k \leqslant \pi/2$. And these are shown in Fig. 5.

For case-1 i.e. $0 \leqslant \alpha_k \leqslant \pi/6$, $\pi/6$:

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\int_{\alpha_k}^{\frac{\pi}{3-\alpha_k}} \sin(n\theta)\, d\theta + \frac{3}{3}\int_{\frac{\pi}{3-\alpha_k}}^{\frac{\pi}{3+\alpha_k}} \sin(n\theta)\, d\theta + \frac{4}{3}\int_{\frac{\pi}{3+\alpha_k}}^{\frac{\pi}{2}} \sin(n\theta)\, d\theta\right]$$

$$\text{i.e. } b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k) \tag{7}$$

For case-2, i.e. $\pi/6 \leqslant \alpha_k \leqslant \pi/3$, $\pi/3$:

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\int_{\frac{\pi}{3-\alpha_k}}^{\alpha_k} \sin(n\theta)\, d\theta + \frac{3}{3}\int_{\alpha_k}^{\frac{2\pi}{3-\alpha_k}} \sin(n\theta)\, d\theta + \frac{2}{3}\int_{\frac{2\pi}{3-\alpha_k}}^{\frac{\pi}{2}} \sin(n\theta)\, d\theta\right]$$

$$b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k). \tag{8}$$

For case-3, i.e. $\pi/3 \leqslant \alpha_k \leqslant \pi/2$:

$$b_{nk} = \frac{4V_{dc}}{\pi}\left[\int_{\alpha_k-\frac{\pi}{3}}^{\frac{2\pi}{3-\alpha_k}} \sin(n\theta)\, d\theta + \frac{2}{3}\int_{\alpha_k}^{\frac{\pi}{2}} \sin(n\theta)\, d\theta\right]$$

$$b_{nk} = \frac{4V_{dc}}{n\pi}\cos(n\alpha_k). \tag{9}$$

From Eqs. (7)–(9), Fourier progression is same. In a similar fashion Fourier transform for primary voltages of transformer V_{ak}, V_{bk}, V_{ck} are given as

$$V_{ak} = \sum_{n=1}^{\infty} b_{nk} \sin(n\theta)$$

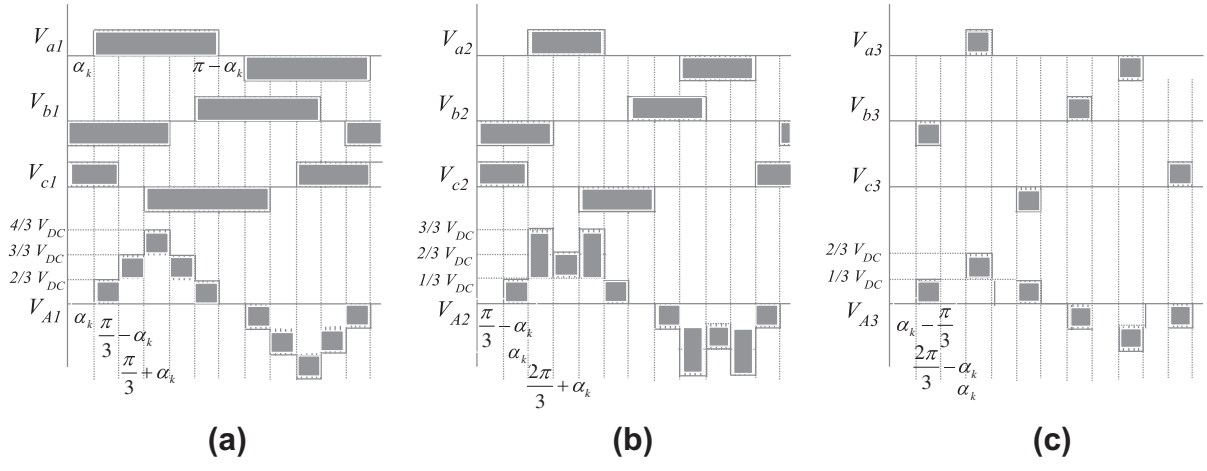


Fig. 5. Details of switching pattern and output voltage waveform characteristics for CMI with three-phase transfomers.

$$V_{bk} = \sum_{n=1}^{\infty} b_{nk} \sin\left(n\theta - \frac{2n\pi}{3}\right)$$

$$V_{ck} = \sum_{n=1}^{\infty} b_{nk} \sin\left(n\theta + \frac{2n\pi}{3}\right) \quad (10)$$

Which are 120° apart from each phase and coefficients of b_{nk} and V_{ak} are half wave symmetries, henceforth odd function can be written as

$$b_{nk} = \frac{4V_{dc}}{n\pi} \cos(n\alpha_k). \quad (11)$$

Using Eq. (1), output phase voltage of V_{AK} can be expressed as:

$$V_{AK} = \sum_{n=1}^{\infty} b_{nk} \sin(n\theta) - 1/3 \times \sum_{n=1}^{\infty} b_{nk}\left(\sin(n\theta) + 2\sin(n\theta)\cos\left(\frac{2n\pi}{3}\right)\right) \quad (12)$$

In above equation if $n = 3, 9 \ldots 3(p-2), 3p$, then equation becomes zero i.e.

$$V_{AK} = 0 \quad (13)$$

This represents, all triplen harmonic component does not appear in the three-phase output voltage.

And if $n = 1, 5, 7, 11 \ldots p$, then equation becomes

$$V_{AK} = \sum_{n=1}^{\infty} b_n \sin(n\theta) \quad (14)$$

Thus least harmonic in output waveform will be 5, 7, 11, $p-2$, p.

3.2. Switching and phase shifting

For multicell switching, phase shifting is important criterion. In the present case for experimentation, CMI utilizes only nine H-bridge cells and for each phase, it uses three cells. Thus three carriers are chosen with appropriate phase shift. In general a multicell converter requires $(m-1)/2$ triangle carriers to generate *m-level* output with unipolar switching. But in the present case $(m-1)/4$ carriers are required, which signifies that carrier count is drastically reduced for higher number of levels. For example for 13 level output waveform, (13–1)/2 carriers are needed in conventional structures, where as it is half in present case i.e. (13–1)/4. On the other hand triangle carriers had same frequency and same peak

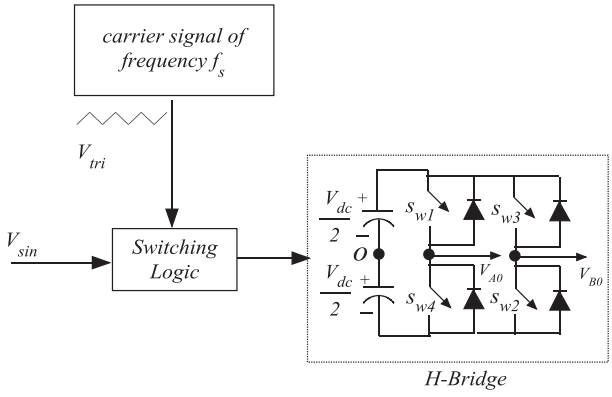


Fig. 6. Details of single H-bridge cell.

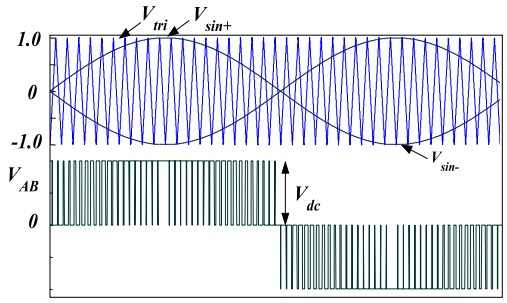


Fig. 7. Details of unipolar switching.

to peak amplitude but then phase difference between two adjacent carriers are given by:

$$\varphi_{cr} = 360/(m-1)/4 \quad (15)$$

By using above equation appropriate phase shift can be included.

3.3. Unipolar switching

Unipolar switching scheme is considered for generating pulses. Figs. 6 and 7 provide details of single H-bridge operation and unipolar switching criteria. Herein, the 13 level voltage source modulations is accomplished by comparing the duty cycles with a set of carrier waveforms. The switching function V_{sin} is compared with triangular carrier V_{tri} of frequency f_s and with definite amplitude.

Switching function V_{sin} is modulated with carrier following the principle of unipolar PWM i.e.

Condition: 1.1 $V_{sin} > V_{tri}$. Then SW1 is on and resultant voltage $V_{A0} = +1/2V_{dc}$.
Condition: 1.2 $V_{sin} < V_{tri}$. Then SW4 is on and resultant voltage $V_{A0} = -1/2V_{dc}$.

In a similar fashion for other phase leg of H-bridge,
Condition: 2.1 $V_{sin} > V_{tri}$. Then SW3 is on and resultant voltage $V_{BO} = +1/2V_{dc}$.
Condition: 2.2 $V_{sin} < V_{tri}$. Then SW2 is on and resultant voltage $V_{BO} = -1/2V_{dc}$.

Therefore net voltage levels obtained for one H-bridge are V_{dc}, 0, and $-V_{dc}$. The process is repeated for other H-bridges with a carrier phase shifted by the corresponding angles. Sum of all these three voltages results in producing resultant output waveform. However, to clarify the principle of operation for proposed archetype, consider the waveforms which are demonstrated in Fig. 5. Although each bridge generates voltage V_{DC}, but the resultant voltage always depends on the output of a transformer. However, net output voltage of each phase i.e. V_{AK}, V_{BK}, and V_{CK} is a combination of each terminal of three-phase transformer, in other terms, all individual phase voltages are dependent on other phases too. This is the finite reason why twice output levels are achieved at the resultant voltage waveform. To be specific, in preset case nine H-bridge modules are used, due to this reason 13 level output waveform can be attained. However, in-depth assessment of proposed configuration is verified with prototype experiments and observations are demonstrated in next section.

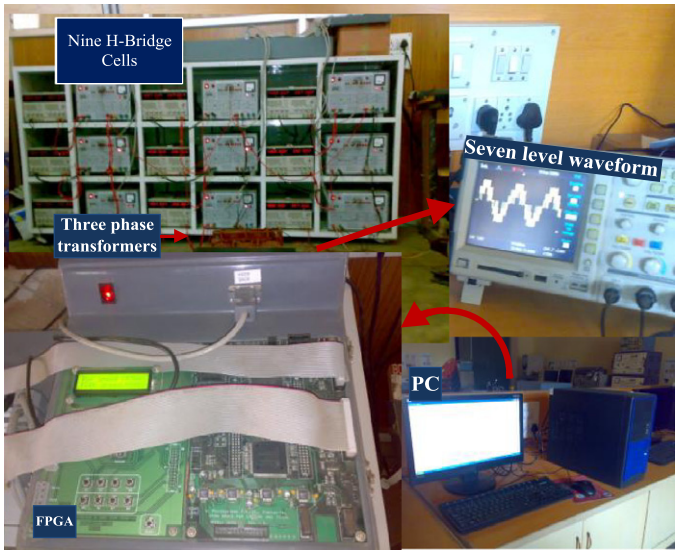


Fig. 8. Details of prototype set up for proposed cascade multilevel inverter with three-phase transformers.

Table 1
Hardware specifications.

Items	Specifications and features
Switching devices	FGH20N60UFD 600 V, 20 A fair child semiconductors
Transformers	El lamination (3EA)1:1 ratio
Input voltage	1-single DC, 60 V
Output voltage	13-level, 220 V
FPGA	Xilinx Spartan3 Device Generate PWM signals
Translator	SN74LVCC3245A Bi-directional voltage translator
Current sensor	LTS25-NP25A
Voltage sensor	LV25-P 1200 V
Load parameters	R = 400 Ω, L = 1000 mH

3.4. Experimental verification

A prototype model of the proposed converters is developed and verified in the laboratory. The experiment was carried out for a star connected load. For the experimentation FPGA based module was utilized. An analog expansion daughter board interfaced between the FPGA module and insulated gate bipolar transistor (IGBT) inverter. Proposed circuit topology and control strategy was realized with code composer. Fig. 8 indicates the construction of CMI using three-phase transformers. The measured quantities are the load current, load voltages, which are measured with hall-effect voltage and current transducers. The transformer ratios are scaled in power of 1. Input dc voltage is taken as 60 V. The load parameters are R = 400 Ω, L = 1000 mH per phase. Further details of prototype setup are demonstrated in Table 1. Fig. 9 highlights the performance of CMI and provide experimental output voltages and FFT result of the phase "a", at modulation indexes 1, 0.9, 0.7, 0.5 and 0.2 respectively. At modulation index 1 corresponding FFT reports complete elimination of lower order harmonics and least harmonic component is 29th, rest all the harmonics are suppressed and as modulation index reduces, all odd harmonic components are noticed.

Interesting features of proposed converter is that, it produces 13 level output waveform with just nine H-bridge cells. This defines the inherent potential of a converter. In fact, converter produces twice output levels when compared to conventional single-phase archetypes and generated output voltage is almost sinusoidal in fashion with improved THD. In Fig. 10 THD and DF variations of output voltages based on different modulation indexes are demonstrated. It is observed that THD of voltage harmonics gradually increases with decrease in modulation index and at modulation index 1 its THD is 4% and at 0.2 it is around 17%. But for all the modulation indexes it is evident that third harmonic component is completely absent. Thus power quality has been improved predominantly when compared to conventional converters.

(a) Important features of proposed CMI

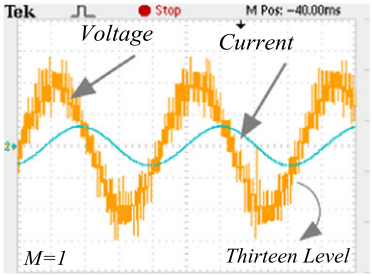
Besides above issues, conventional cascade multilevel inverters use a circulating switch pattern in order to maintain the same ratio in switch utilization. Therefore, they employ switches which are identical in the voltage and current ratings. Assuming that the magnitude of the output voltages and output power are equivalent, the voltage ratings of each switch are determined by the number of series-connected switches. Consequently, we can say that the proposed method is more advantageous as far as numbers of components are used. Most importantly there is significant improvement in output voltage quality which is not possible in other structures. In addition, usually, these traditional multilevel inverters employ a three 3-phase low-frequency transformer at the output terminal for a high-power grid connection. In this point, the proposed circuit topology has a valuable merit. Considering that the output voltage is synthesized by an accumulation of each transformer output, it does not require an additional transformer for galvanic isolation. Although the proposed scheme needs three three-phase transformers, the cost and size will be slightly increased, because the capacity of the transformer is 1/3 of the transformer which is applied to the conventional method.

4. Comparative study

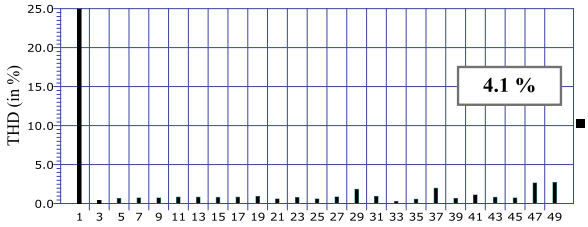
After comparing it is observed that, conventional multilevel inverter requires too many dc sources and dc capacitors to generate 13 output voltage levels. We can find that a conventional multilevel inverter needs 18 dc sources with 72 switches or single dc source with 18 single-phase transformers to generate 13 level output. In the case of CMI with reduced sources it requires nine dc sources with 84 switches and in Hybrid converters, 15 dc bus capacitors are required for the generation of 13-level outputs. But the proposed converter requires only single dc source. Detail comparison is given in Table 2.

Further, it is also viable to compare proposed CMI with conventional multilevel inverters. So, to explore the significance of proposed CMI with traditional multilevel inverter Table 3 is presented. On investigating in case of diode clamped, a large number of clamping diodes are the worst drawback. Plenty of balancing capacitors are a weak point in flying capacitor type inverter. Among them, the cascade full-bridge cell type looks good to increase the number of output levels. However, each cell has an isolated power supply. The provision of isolated supply becomes a limitation in the power electronic circuit design. Moreover, complexity in control and voltage imbalance problems also arises. However, such problems are evaded with proposed technique, because it uses single dc source and further switch count considerably reduced.

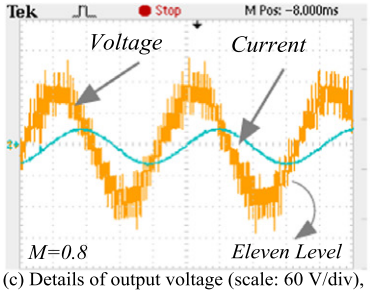
Further comparing with Neutral Point Converter (NPC), the proposed CMI confirms promising characteristics. Recently it is



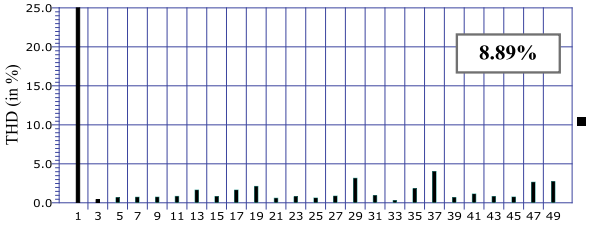
(a) Details of output voltage (scale: 60 V/div), output current (scale: 10 A/div), Time scale: 5 ms/div



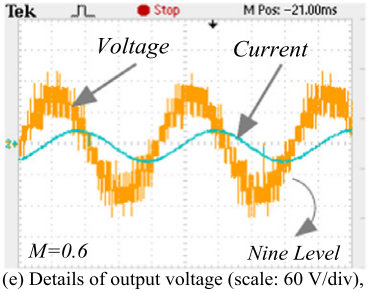
(b) Harmonic order



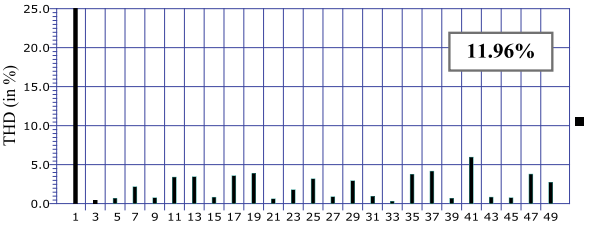
(c) Details of output voltage (scale: 60 V/div), output current (scale: 10 A/div), Time scale: 5 ms/div



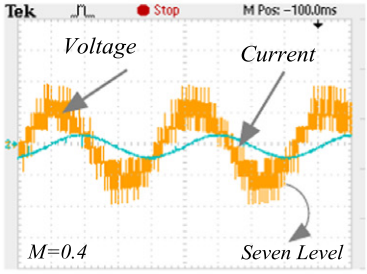
(d) Harmonic order



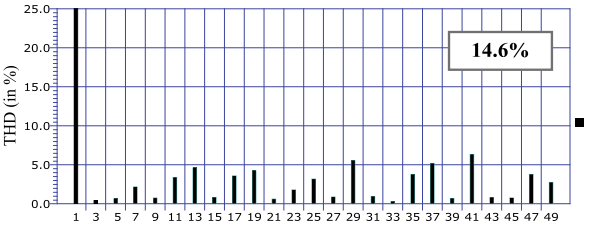
(e) Details of output voltage (scale: 60 V/div), output current (scale: 10 A/div), Time scale: 5 ms/div



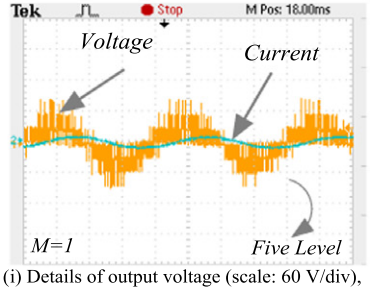
(f) Harmonic order



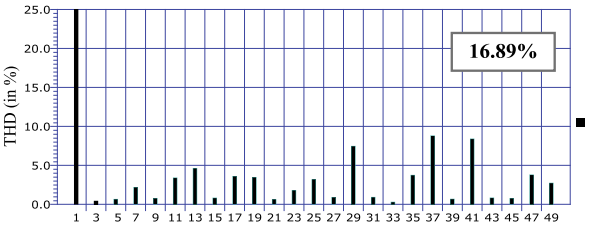
(g) Details of output voltage (scale: 60 V/div), output current (scale: 10 A/div), Time scale: 5 ms/div



(h) Harmonic order



(i) Details of output voltage (scale: 60 V/div), output current (scale: 10 A/div), Time scale: 5 ms/div



(j) Harmonic order

Fig. 9. Output voltage and current waveform and respective FFT spectrums for 13 level CMI at (a and b) modulation index = 1, (c and d) modulation index = 0.8, (e and f) modulation index = 0.6, (g and h) modulation index = 0.4 and (i and j) modulation index = 0.2.

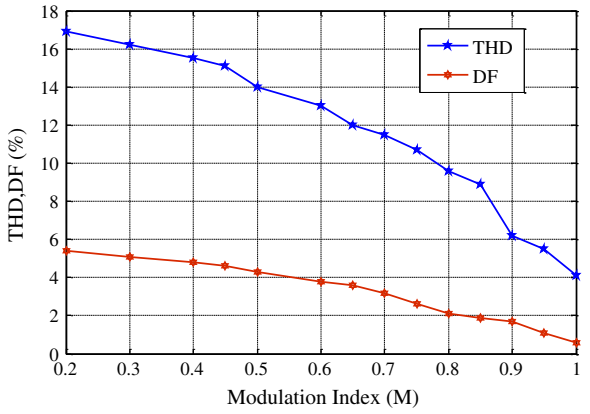


Fig. 10. THD and DF of output voltage on the variation of modulation index.

observed that, Neutral Point Converter (NPC) employing zigzag transformers is used in transmission and distribution systems, because converter provides high quality voltage and current waveforms with lower harmonic content. In reality NPC with zigzag transformer size is quite larger because large numbers of components are utilized. However, in-spite of that archetype, presented converter can effectively replace in such areas. This is because present CMI is coupled with low frequency three phase transformers. Further in presence of PWM operation, voltage and current waveforms are almost equal to that of NPC converters performance. All these features facilitate the converter to operate perfectly for utility applications. Therefore, proposed CMI is perfectly suited for applications like STATCOM (static synchronous compensators), SSSC (static series compensators), UPQC (unified power quality conditioners) etc.

5. Conclusion

Present paper figured out the technical aspects and performance of cascade multilevel inverters with reduced dc sources. Further, this paper proposed CMI with PWM approach by using single dc source and three-phase transformers. The effectiveness and validity of the proposed approach is demonstrated with prototype experiments. Since less number of components are utilized, the proposed structure is reliable, efficient, cost-effective and compact. The attractive features of the proposed converters are: low switching frequency and reduce electromagnetic interference problems, increase utilization rate because of single dc source, removal of third harmonic component as three-phase transformer are employed on secondary side. Consequently, this characteristic allows one to achieve high quality output voltages and input currents. Also it has outstanding availability due to their intrinsic component redundancy. Due to these features, proposed architecture is superior over the conventional structures. The remarkable attributes of the proposed converter is well suitable for grid-connected photovoltaic/wind-power generator, flexible alternating current systems.

Table 2
Components comparison with conventional cascade multilevel inverter.

Type	Item						
	Conventional cascade H-bridge	Conventional CMI with unequal DC sources	CMI with minimum DC sources	Hybrid CMI with bottom three-leg inverter	Hybrid CMI bottom H-bridge inverter	CMI with single phase transformers	CMI with three-phase transformers
Main switching devices	72	36	84	106	60	72	36
DC-bus capacitors	18	36	9	15	12	1	1
Input DC sources	18	18	9	1	3	1	1
Output transformers	0	0	0	0	0	18	3

Table 3
Components comparison with conventional multilevel inverter.

Item / Type	Switch	Clamping diode	Balancing capacitor	DC-Bus	Transformers
Diode Clamped	$(m-1)\times 2\times 3$	$(m-1)\times(m-2)\times 3$	N.A	$(m-1)\times 3$	N.A
	72	396		36	
Flying capacitor	$(m-1)\times 2\times 3$	N.A	$[(m-1)\times(m-2)]\times 3/2$	$(m-1)\times 3$	N.A
	24		210	36	
Cascaded FB-cell	$(m-1)\times 2\times 3$	N.A	N.A	$(m-1)\times 3/2$	Multi-winding outputs
	72			18	
Proposed converter	$(m-1)\times 2/2$	N.A	N.A	single	three
	36				

References

[1] Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: survey of topologies, controls, and applications. IEEE Trans Ind Appl 2002;49(4):724–38.

[2] Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM. The age of multilevel converters arrives. IEEE Ind Electron Mag 2008;2(2):28–39.

[3] Malinowski Mariusz, Gopakumar K, Rodriguez Jose, Pérez Marcelo A. A survey on cascaded multilevel inverters. IEEE Trans Ind Electron 2010;57(7).

[4] Colak Ilhami, Kabalci Ersan, Bayindir Ramazan. Review of multilevel voltage source inverter topologies and control schemes. Energy Convers Manage 2011;52:1114–28.

[5] Nabae A, Takahashi I, Akagi H. A new neutral-point clamped PWM inverter. IEEE Trans Ind Appl IA 1981(17):518–23.

[6] Lai JS, Peng FZ. Multilevel converters – a new breed of power converters. IEEE Trans Ind Appl 1996;32:509–17.

[7] Sirisukprasert S, Xu Z, Zhang B, Lai JS, Huang AQ. A high-frequency 1.5 MVA H-bridge building block for cascaded multilevel converters using emitter turn-off thyrister. Proc IEEE-APEC 2002:27–32.

[8] Corzine Keith A, Wielebski Mike W, Peng Fang Z, Wang Jin. Control of cascaded multilevel inverters. IEEE Trans Power Electron 2004;19(3).

[9] Song Sung Geun, Kang Feel Soon. Cascaded multilevel inverter employing three-phase transformers and single DC input. IEEE Trans Ind Electron 2009;56(6).

[10] Suresh Y, Panda AK. Performance of cascade multilevel h-bridge inverter with single dc source by employing low frequency three-phase transformers. Proc IEEE-IECON 2010:1975–80.

[11] Tolbert LM, Peng FZ, Habetler T. Multilevel converters for large electric drives. IEEE Trans Ind Appl 1999;35:36–44.

[12] Rahim NA, Selvaraj J, Krismadinata C. Five-level inverter with dual reference modulation technique for grid-connected PV system. Renew Energy 2010;35:712–20.

[13] Dixon J, Breton AA, Rios FE, Rodriguez J, Pontt J, Perez MA, et al. High-power machine drive, using non redundant 27-level inverters and active front end rectifiers. IEEE Trans Power Electron 2007;22(6):2527–33.

[14] Manjrekar MD, Steimer P, Lipo TA. Hybrid multilevel power conversion system: a competitive solution for high power applications. IEEE Trans Ind Appl 2000;36(3):834–41.

[15] Soto D, Green TC. A comparison of high-power converter topologies for the implementation of FACTS controllers. IEEE Trans Ind Electron 2002;49(5): 1072–80.

[16] Carpita M, Marchesoni M, Pellerin M, Moser D. Multilevel converter for traction applications: small-scale prototype tests results. IEEE Trans Ind Electron 2008;55(5):2203–12.

[17] Wen J, Smedley KM. Synthesis of multilevel converters based on single- and/or three-phase converter building blocks. IEEE Trans Power Electron 2008;23(3): 1247–56.

[18] Khomfoi S, Tolbert LM. Multilevel power converters, power electronics handbook, 2nd ed. Elsevier; 2007. p. 451–82 [Chapter17, ISBN 978-0-12-088479-7].

[19] Songa Sung-Geun, Parkb Sung-Jun, Joungc Yeun-Ho, Kang Feel-soon. Multilevel inverter using cascaded 3-phase transformers with common-arm configuration. Electric Power Syst Res 2011;81:1672–80.

[20] Babaei Ebrahim, Moeinian Mohammad Sadegh. Asymmetric, cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem. Energy Convers Manage 2010;51:2272–8.

[21] Lezana P, Rodriguez J, Oyarzun DA. Cascaded multilevel inverter with regeneration capability and reduced number of switches. IEEE Trans Ind Electron 2008;55(3):1059–66.

[22] Colaka Ilhami, Kabalcib Ersan, Machines Gazi Electrical. Gazi Electrical Machines and Energy Control (GEMEC) Group, Practical implementation zof a digital signal processor controlled multilevel inverter with low total harmonic distortion for motor drive applications. J Power Sources 2011;196: 7585–93.

[23] Sirisukprasert S, Lai JS, Liu TH. A novel cascaded multilevel converter drive system with minimum number of separated DC sources. Proc IEEE-APEC 2001.

[24] Akagi Hirofurni, Inoue Shigenori, Yoshii Tsurugi. Control and performance of a transformer-less Cascade PWM STATCOM with star configuration. IEEE Trans Ind Appl 2007;43(4).

[25] Wu Bin. High power converters and AC drives. IEEE Press A Jon Wiley & Sons, Inc., Publication.

[26] Kuhn H, Rüger NE, Mertens A. Control strategy for multilevel inverter with non-ideal DC sources. In: IEEE power electronics specialists conference, 2007. PESC; 2007. p. 632–38.

[27] Lu Shuai, Mariéthoz S, Corzine KA. Asymmetrical cascade multilevel converters with noninteger or dynamically changing DC voltage ratios: concepts and modulation techniques. IEEE Trans Ind Electron 2010;57(7):2411–8.

[28] Sirisukprasert Siriroj. The modeling and control ff a cascaded-multilevel converter-based STATCOM. Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University; 2004.

[29] Du Z, Ozpineci B, Tolbert LM, Chiasson JN. DC–AC cascaded h-bridge multilevel boost inverter with no inductors for electric/hybrid electric vehicle applications. IEEE Trans Ind Appl 2009;45(3):963–70.

[30] Cheng Z, Wu B. A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency. IEEE Trans Power Electron 2007;22(6):2138–45.

[31] Khoucha Farid, Lagoun Soumia Mouna, Marouani Khoudir, Kheloui Abdelaziz, El Hachemi Benbouzid Mohamed. Hybrid cascaded H-bridge multilevel-inverter induction-motor-drive direct torque control for automotive applications. IEEE Trans Ind Electron 2010;57(3).

[32] Vazquez S, Leon JI, Franquelo LG, Padilla JJ, Carrasco JM. DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source. IEEE Trans Ind Electron 2009;56(7):2513–21.

[33] Fukuda Shoji, Yoshida Takatsugu, Ueda Shigeta. Control strategies of a hybrid multilevel converter for expanding adjustable output voltage range. IEEE Trans Ind Appl 2009;45(2):827–35.

[34] Du Zhong, Tolbert Leon M, Ozpineci Burak, Chiasson John N. Fundamental frequency switching strategies of a seven-level hybrid cascade H-Bridge multilevel inverter. IEEE Trans Power Electron 2009;24(1).

[35] Ruiz-Caballero Domingo A, Ramos-Astudillo Reynaldo M, Mussa Samir Ahmad, Heldwein Marcelo Lobo. Symmetrical hybrid multilevel DC–AC converters with reduced number of insulated DC supplies. IEEE Trans Ind Electron 2010;57(7):2307–14.

[36] Dixon J, Pereda J, Castillo C, Bosch S. Asymmetrical multilevel inverter for traction drives using only one DC supply. IEEE Trans Veh Technol 2010;59(8):3736–43.

[37] Bandara Kapila, Sweet Tracy, Ekanayake Janaka. Photovoltaic applications for off-grid electrification using novel multi-level inverter technology with energy storage. Renew Energy 2012;37:82–8.

[38] Kang FS, Park SJ, Lee MH, Kim C-U. An efficient multilevel synthesis approach and its application to a 27-level inverter. IEEE Trans Ind Electron 2005;52(6):1600–6.