Multilevel Inverters: A Survey of Topologies, Controls, and Applications

José Rodríguez, *Senior Member, IEEE*, Jih-Sheng Lai, *Senior Member, IEEE*, and Fang Zheng Peng, *Senior Member, IEEE*

***Abstract*—Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate dc sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulsewidth modulation, multilevel selective harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future development are addressed.**

***Index Terms*—Medium-voltage drives, multilevel converter, multilevel inverter, power converters.**

I. Introduction

IN RECENT YEARS, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled ac drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium-voltage grids (2.3, 3.3, 4.16, or 6.9 kV). For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels [1]–[3].

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1(a)], while the three-level inverter generates three voltages, and so on.

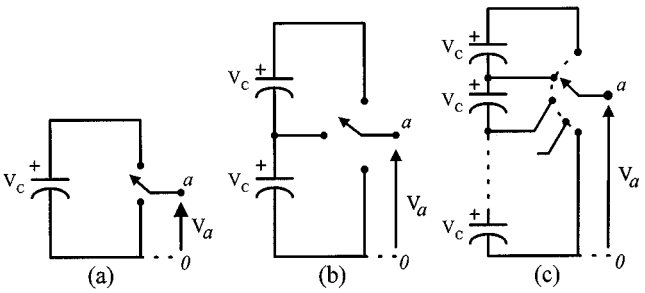

Fig. 1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

Considering that m is the number of steps of the phase voltage with respect to the negative terminal of the inverter, then the number of steps in the voltage between two phases of the load k is

$$k = 2m + 1 \tag{1}$$

and the number of steps p in the phase voltage of a three-phase load in wye connection is

$$p = 2k - 1. \tag{2}$$

The term multilevel starts with the three-level inverter introduced by Nabae *et al.* [4]. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. However, a high number of levels increases the control complexity and introduces voltage imbalance problems.

Three different topologies have been proposed for multilevel inverters: diode-clamped (neutral-clamped) [4]; capacitor-clamped (flying capacitors) [1], [5], [6]; and cascaded multicell with separate dc sources [1], [7]–[9]. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulsewidth modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).

The most attractive features of multilevel inverters are as follows.

1) They can generate output voltages with extremely low distortion and lower dv/dt.

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J. Rodríguez is with the Departamento de Electronica, Universidad Técnica Federico Santa María, Valparaiso, Chile (e-mail: jrp@elo.utfsm.cl).

J.-S. Lai is with Virginia Polytechnic Institute and State University, Blacksburg, VA 24061-0111 USA.

F. Z. Peng is with the Department of Electrical and Computer Engineering, Michigan State University, East Lansing, MI 48826-1226 USA.

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2) They draw input current with very low distortion.
3) They generate smaller common-mode (CM) voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated [8].
4) They can operate with a lower switching frequency.

The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. An early traceable patent appeared in 1975 [9], in which the cascade inverter was first defined with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived [10]. The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. The application of the NPC inverter and its extension to multilevel converter was found in [11]. Although the cascade inverter was invented earlier, its applications did not prevail until the mid–1990s. Two major patents [12], [13] were filed to indicate the superiority of cascade inverters for motor drive and utility applications. Due to the great demand of medium-voltage high-power inverters, the cascade inverter has drawn tremendous interest ever since. Several patents were found for the use of cascade inverters in regenerative-type motor drive applications [14]–[16]. The last entry for U.S. multilevel inverter patents, which were defined as the capacitor-clamped multilevel inverters, came in the 1990s [17], [18]. Today, multilevel inverters are extensively used in high-power applications with medium voltage levels. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

This paper presents state-of-the-art multilevel technology, considering well-established and emerging topologies as well as their modulation and control techniques. Special attention is dedicated to the latest and more relevant industrial applications of these converters. Finally, the possibilities for future development are addressed.

II. Inverter Topologies

A. Diode-Clamped Inverter

A three-level diode-clamped inverter is shown in Fig. 2(a). In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors *n* can be defined as the neutral point. The output voltage v_{an} has three states: $V_{\rm dc}/2$, 0, and $-V_{\rm dc}/2$. For voltage level $V_{\rm dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{\rm dc}/2$, switches $S_1{}'$ and $S_2{}'$ need to be turned on; and for the 0 level, S_2 and $S_1{}'$ need to be turned on.

The key components that distinguish this circuit from a conventional two-level inverter are D_1 and $D_1{}'$. These two diodes clamp the switch voltage to half the level of the dc-bus voltage. When both S_1 and S_2 turn on, the voltage across *a* and 0 is $V_{\rm dc}$, i.e., $v_{a0} = V_{\rm dc}$. In this case, $D_1{}'$ balances out

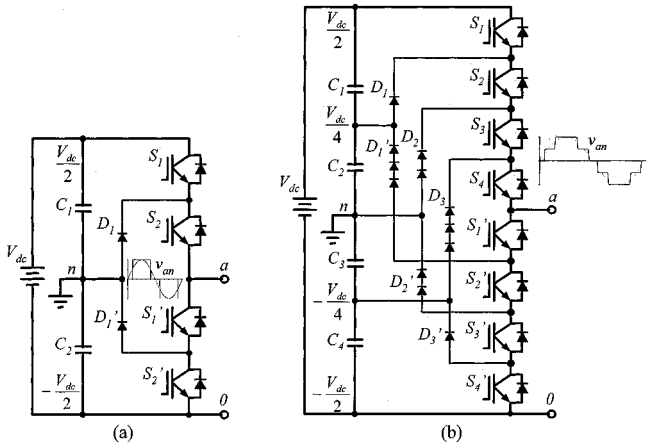

Fig. 2. Diode-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level.

the voltage sharing between $S_1{}'$ and $S_2{}'$ with $S_1{}'$ blocking the voltage across C_1 and $S_2{}'$ blocking the voltage across C_2. Notice that output voltage v_{an} is ac, and v_{a0} is dc. The difference between v_{an} and v_{a0} is the voltage across C_2, which is $V_{\rm dc}/2$. If the output is removed out between *a* and 0, then the circuit becomes a dc/dc converter, which has three output voltage levels: $V_{\rm dc}$, $V_{\rm dc}/2$, and 0.

Fig. 2(b) shows a five-level diode-clamped converter in which the dc bus consists of four capacitors, C_1, C_2, C_3, and C_4. For dc-bus voltage $V_{\rm dc}$, the voltage across each capacitor is $V_{\rm dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{\rm dc}/4$ through clamping diodes.

To explain how the staircase voltage is synthesized, the neutral point *n* is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across *a* and *n*.

1) For voltage level $V_{an} = V_{\rm dc}/2$, turn on all upper switches S_1–S_4.
2) For voltage level $V_{an} = V_{\rm dc}/4$, turn on three upper switches S_2–S_4 and one lower switch $S_1{}'$.
3) For voltage level $V_{an} = 0$, turn on two upper switches S_3 and S_4 and two lower switches $S_1{}'$ and $S_2{}'$.
4) For voltage level $V_{an} = -V_{\rm dc}/4$, turn on one upper switch S_4 and three lower switches $S_1{}'$–$S_3{}'$.
5) For voltage level $V_{an} = -V_{\rm dc}/2$, turn on all lower switches $S_1{}'$–$S_4{}'$.

Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are $(S_1, S_1{}')$, $(S_2, S_2{}')$, $(S_3, S_3{}')$, and $(S_4, S_4{}')$.

Although each active switching device is only required to block a voltage level of $V_{\rm dc}/(m-1)$, the clamping diodes must have different voltage ratings for reverse voltage blocking. Using $D_1{}'$ of Fig. 2(b) as an example, when lower devices $S_2{}' \sim S_4{}'$ are turned on, $D_1{}'$ needs to block three capacitor voltages, or $3V_{\rm dc}/4$. Similarly, D_2 and $D_2{}'$ need to block $2V_{\rm dc}/4$, and D_{a3} needs to block $3V_{\rm dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1)\times(m-$

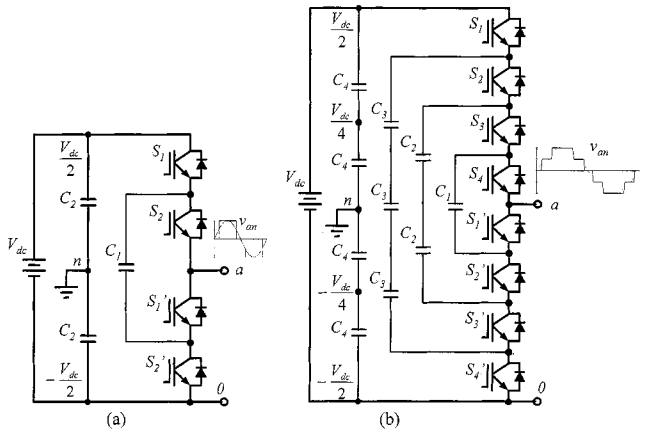

Fig. 3. Capacitor-clamped multilevel inverter circuit topologies. (a) Three-level. (b) Five-level.

2). This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

B. Capacitor-Clamped Inverter

Fig. 3 illustrates the fundamental building block of a phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter [1], [5], [6] with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 3(a) provides a three-level output across *a* and *n*, i.e., $v_{an} = V_{\rm dc}/2$, 0, or $-V_{\rm dc}/2$. For voltage level $V_{\rm dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{\rm dc}/2$, switches $S_1{}'$ and $S_2{}'$ need to be turned on; and for the 0 level, either pair $(S_1, S_1{}')$ or $(S_2, S_2{}')$ needs to be turned on. Clamping capacitor C_1 is charged when S_1 and $S_1{}'$ are turned on, and is discharged when S_2 and $S_2{}'$ are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 3(b) as the example, the voltage of the five-level phase-leg *a* output with respect to the neutral point *n*, V_{an}, can be synthesized by the following switch combinations.

1) For voltage level $V_{an} = V_{\rm dc}/2$, turn on all upper switches S_1–S_4.
2) For voltage level $V_{an} = V_{\rm dc}/4$, there are three combinations:
   a) S_1, S_2, S_3, $S_1{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-V_{\rm dc}/4$ of C_1);
   b) S_2, S_3, S_4, $S_4{}'$ ($V_{an} = 3V_{\rm dc}/4$ of C_3's $-V_{\rm dc}/2$ of lower C_4's); and
   c) S_1, S_3, S_4, $S_3{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-3V_{\rm dc}/4$ of C_3's $+V_{\rm dc}/2$ of C_2's).
3) For voltage level $V_{an} = 0$, there are six combinations:
   a) S_1, S_2, $S_1{}'$, $S_2{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-V_{\rm dc}/2$ of C_2's);
   b) S_3, S_4, $S_3{}'$, $S_4{}'$ ($V_{an} = V_{\rm dc}/2$ of $C_2 - V_{\rm dc}/2$ of lower C_4);
   c) S_1, S_3, $S_1{}'$, $S_3{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-3V_{\rm dc}/4$ of C_3's $+V_{\rm dc}/2$ of C_2's $-V_{\rm dc}/4$ of C_1);
   d) S_1, S_4, $S_2{}'$, $S_3{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-3V_{\rm dc}/4$ of C_3's $+V_{\rm dc}/4$ of C_1);
   e) S_2, S_4, $S_2{}'$, $S_4{}'$ ($V_{an} = 3V_{\rm dc}/4$ of C_3's $-V_{\rm dc}/2$ of C_2's $+V_{\rm dc}/4$ of $C_1 - V_{\rm dc}/2$ of lower C_4's); and
   f) S_2, S_3, $S_1{}'$, $S_4{}'$ ($V_{an} = 3V_{\rm dc}/4$ of C_3's $-V_{\rm dc}/4$ of $C_1 - V_{\rm dc}/2$ of lower C_4's).
4) For voltage level $V_{an} = -V_{\rm dc}/4$, there are three combinations:
   a) S_1, $S_1{}'$, $S_2{}'$, $S_3{}'$ ($V_{an} = V_{\rm dc}/2$ of upper C_4's $-3V_{\rm dc}/4$ of C_3's);
   b) S_4, $S_2{}'$, $S_3{}'$, $S_4{}'$ ($V_{an} = V_{\rm dc}/4$ of $C_1 - V_{\rm dc}/2$ of lower C_4's); and
   c) S_3, $S_1{}'$, $S_3{}'$, $S_4{}'$ ($V_{an} = V_{\rm dc}/2$ of C_2's $-V_{\rm dc}/4$ of $C_1 - V_{\rm dc}/2$ of lower C_4's).
5) For voltage level $V_{an} = -V_{\rm dc}/2$, turn on all lower switches, $S_1{}'$–$S_4{}'$.

In the preceding description, the capacitors with positive signs are in discharging mode, while those with negative sign are in charging mode. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. Similar to diode clamping, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level converter will require a total of $(m-1) \times (m-2)/2$ clamping capacitors per phase leg in addition to $(m-1)$ main dc-bus capacitors.

C. Cascaded Multicell Inverters

A different converter topology is introduced here, which is based on the series connection of single-phase inverters with separate dc sources [7]. Fig. 4 shows the power circuit for one phase leg of a nine-level inverter with four cells in each phase. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{\rm dc}$, 0, and $-V_{\rm dc}$. This is made possible by connecting the capacitors sequentially to the ac side via the four power switches. The resulting output ac voltage swings from $-4V_{\rm dc}$ to $+4V_{\rm dc}$ with nine levels, and the staircase waveform is nearly sinusoidal, even without filtering.

Another version of cascaded multilevel inverters using standard three-phase two-level inverters has recently been proposed [8]. Its circuit, shown in Fig. 5, uses an output transformer to add the different voltages. In order for the inverter output voltages to be added up, the inverter outputs of the three modules need to be synchronized with a separation of 120° between each phase. For example, obtaining a three-level voltage between outputs *a* and *b*, the voltage is synthesized by $V_{ab} = V_{a1-b1} + V_{b1-a2} + V_{a2-b2}$. The phase between b_1 and a_2 is provided by a_3 and b_3 through an isolated transformer. With three inverters synchronized, the voltages V_{a1-b1}, V_{b1-a2}, V_{a2-b2} are all in phase; thus, the output level is simply tripled.

D. Generalized Multilevel Cells

A generalized multilevel inverter topology has previously been presented [19]. The existing multilevel inverters such as

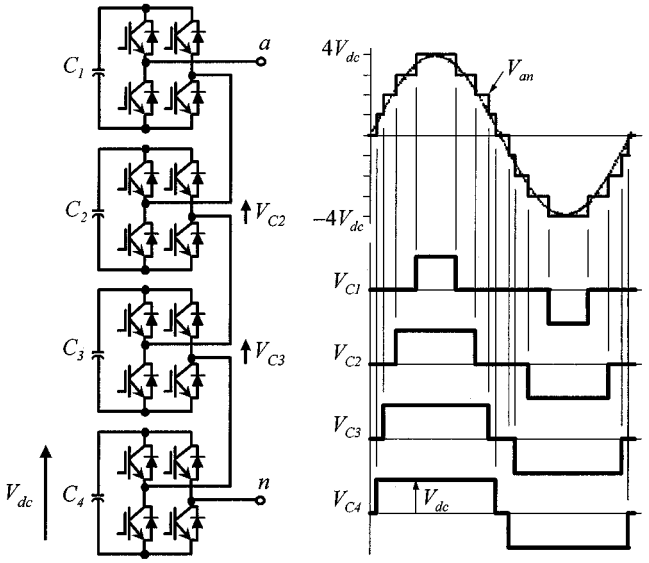

Fig. 4. Cascaded inverter circuit topology and its associated waveform.

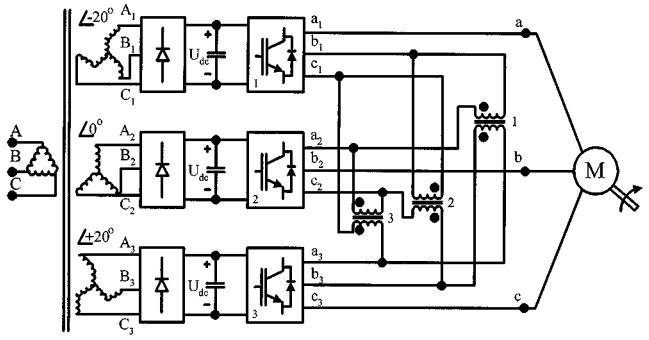

Fig. 5. Cascaded inverter with three-phase cells.

diode-clamped and capacitor-clamped multilevel inverters can be derived from this generalized inverter topology. Moreover, the generalized multilevel inverter topology can balance each voltage level by itself regardless of load characteristics. Therefore, the generalized multilevel inverter topology provides a true multilevel structure that can balance each dc voltage level automatically at any number of levels, regardless of active or reactive power conversion, and without any assistance from other circuits. Thus, in principle, it provides a complete multilevel topology that embraces the existing multilevel inverters.

Fig. 6 shows the P2 multilevel inverter structure per phase leg. Each switching device, diode, or capacitor's voltage is $1V_{\rm dc}$, i.e., $1/(m-1)$ of the dc-link voltage. Any inverter with any number of levels, including the conventional two-level inverter can be obtained using this generalized topology.

As an application example, a four-level bidirectional dc/dc converter, shown in Fig. 7, is suitable for the dual-voltage system to be adopted in future automobiles. The four-level dc/dc converter has a unique feature, which is that no magnetic components are needed. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived [19].

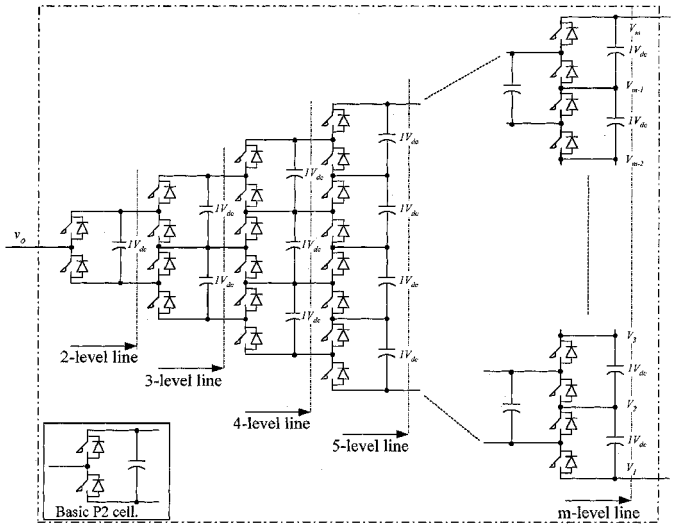

Fig. 6. Generalized P2 multilevel inverter structure.

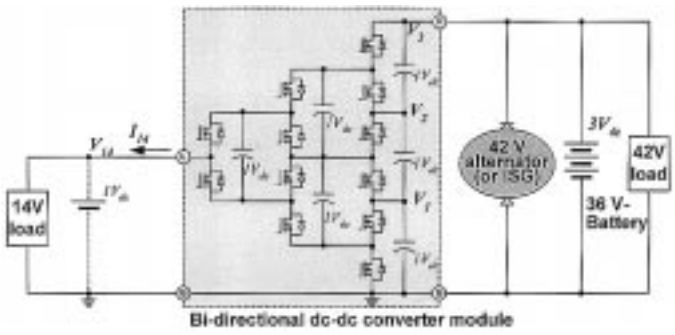

Fig. 7. Application example: a four-level P2 converter for the dual-voltage system in automobiles.

E. Emerging Multilevel Inverter Topologies

1) Mixed-Level Hybrid Multilevel Cells: For high-voltage high-power applications, it is possible to adopt multilevel diode-clamped or capacitor-clamped inverters to replace the full-bridge cell in a cascaded inverter [20]. The reason for doing so is to reduce the amount of separate dc sources. The nine-level cascaded inverter shown in Fig. 4 requires four separate dc sources for one phase leg and twelve for a three-phase inverter. If a three-level inverter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate dc sources are needed for one phase leg and six for a three-phase inverter. The configuration can be considered as having mixed-level hybrid multilevel cells because it embeds multilevel cells as the building block of the cascaded inverter. Fig. 8 shows the nine-level cascaded inverter incorporating a three-level capacitor-clamped inverter as the cell. It is obvious that a diode-clamped inverter can replace the capacitor-clamped inverter to be a mixed-level hybrid multilevel cell.

2) Asymmetric Hybrid Multilevel Cells: In previous descriptions, the voltage levels of the cascade inverter cells equal each other. However, it is possible to have different voltage levels among the cells [21], [22], and the circuit can be called as asymmetric hybrid multilevel inverter. Fig. 9 shows an example of having two separate dc-bus levels, one with $V_{\rm dc}$, and the

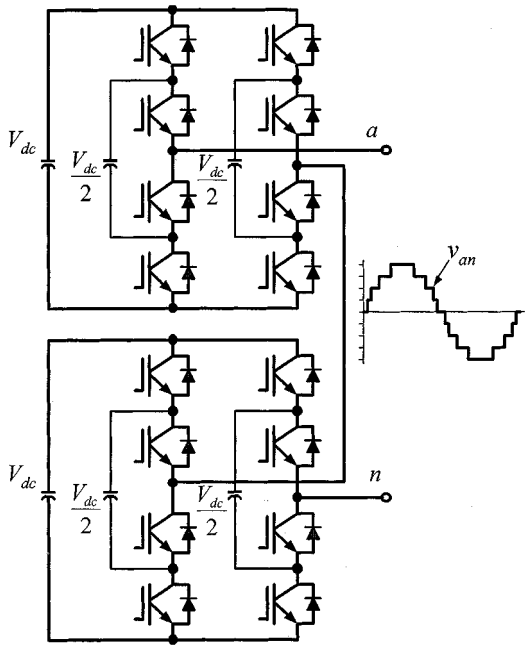

Fig. 8. A mixed-level hybrid cell configuration using the thee-level diode-clamped inverter as the cascaded inverter cell to increase the voltage levels.

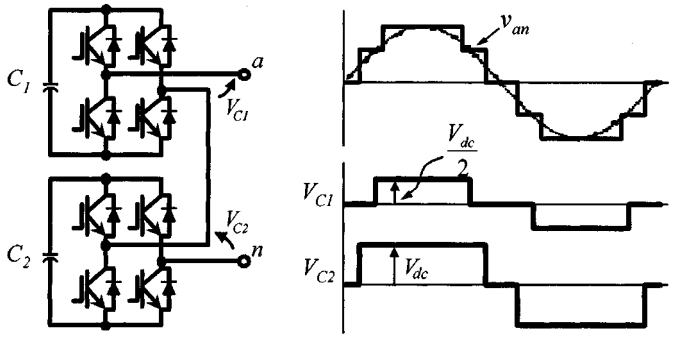

Fig. 9. Asymmetric hybrid cascaded inverter cell arrangement with different voltage levels.

other with $V_{\rm dc}/2$. Depending on the availability of dc sources, the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage, and thus reduces the harmonic contents with less cascaded cells required.

Even with the same voltage level among them, it is also possible to use high-frequency PWM for one cell, while the other switches at a lower rate. Fig. 10 shows an example with two different devices. The top full-bridge cell uses the insulated gate bipolar transistor (IGBT), and the low cell uses the gate-turn-off thyristor (GTO) as its switching device. The GTO-based cell switches at a lower frequency, typically the fundamental frequency, and the IGBT-based cell switches at a PWM frequency to smooth the waveform [21], [22].

3) Soft-Switched Multilevel Inverters: There are numerous ways of implementing soft-switching methods to reduce the switching loss and to increase efficiency for different multilevel inverters. For the cascaded inverter, because each inverter cell is a two-level circuit, the implementation of soft switching is not

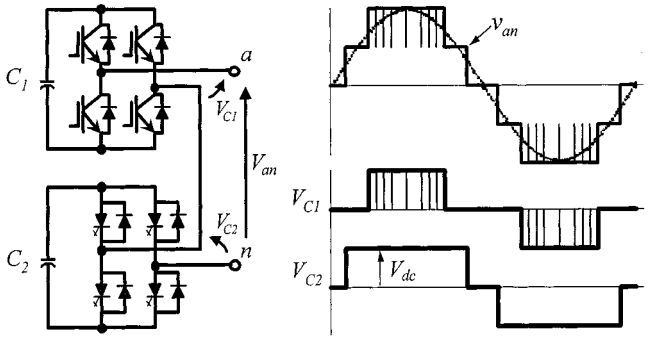

Fig. 10. Asymmetric cascade inverter cell arrangement with different switching frequencies.

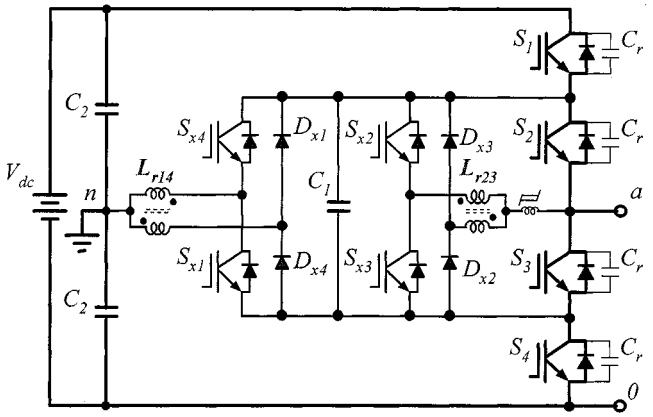

Fig. 11. Zero-voltage-switching capacitor-clamped inverter circuit.

at all different from that of conventional two-level inverters. For capacitor- or diode-clamped inverters, however, the choices of soft-switching circuit can be found with different circuit combinations [23]–[29]. Although zero-current switching is possible [30], most literatures proposed zero-voltage-switching types including auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations. Fig. 11 shows an example of combining the ARCP and coupled-inductor ZVT techniques for a capacitor-clamped three-level inverter.

The auxiliary switches S_{x2}, S_{x3}, D_{x2}, and D_{x3} are used to assist the inner main switches S_2 and S_3 to achieve soft switching. With L_{r23} as the coupled inductor, the bridge-type circuit formed by S_{x2}, S_{x3}, S_2, and S_3 forms a two-level coupled-inductor ZVT. The basic principle of a two-level ZVT can be found in [31]–[35]. For the outer main switches, the soft switching relies on S_1 and S_4, S_{x1}, S_{x4}, D_{x1}, D_{x4}, coupled inductor L_{r14}, and split-capacitor pair C_2 to form an ARCP type soft-switching inverter. Detailed soft-switching circuit operation for inner devices and outer devices can be found in [24], [26].

III. Control and Modulation Strategies

A. Classification of Modulation Strategies

The modulation methods used in multilevel inverters can be classified according to switching frequency, as shown in Fig. 12 [36], [37]. Methods that work with high switching frequencies

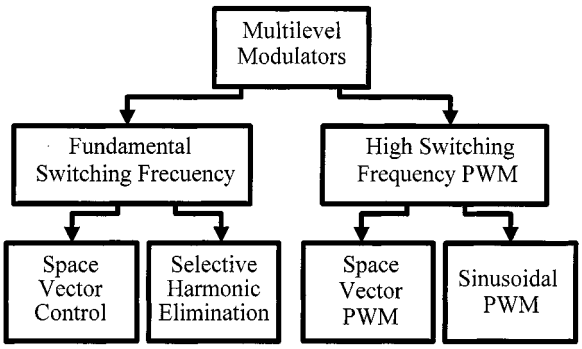

Fig. 12. Classification of multilevel modulation methods.

have many commutations for the power semiconductors in one period of the fundamental output voltage. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage [7], [38], [39]. Another interesting alternative is the SVM strategy, which has been used in three-level inverters [36].

Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltages, generating a staircase waveform. Representatives of this family are the multilevel selective harmonic elimination [40], [41] and the space-vector control (SVC) [42].

B. Multilevel SPWM

Several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical SPWM with triangular carriers. Some methods use carrier disposition and others use phase shifting of multiple carrier signals [38], [43], [44]. Fig. 13(a) shows the typical voltage generated by one cell for the inverter shown in Fig. 4 by comparing a sinusoidal reference with a triangular carrier signal.

A number of N_c–cascaded cells in one phase with their carriers shifted by an angle $\theta_c = 360°/N_c$ and using the same control voltage produce a load voltage with the smallest distortion. The effect of this carrier phase-shifting technique can be clearly observed in Fig. 14. This result has been obtained for the multi-cell inverter in a seven-level configuration, which uses three series-connected cells in each phase. The smallest distortion is obtained when the carriers are shifted by an angle of $\theta_c = 360°/3 = 120°$.

A very common practice in industrial applications for the multilevel inverter is the injection of a third harmonic in each cell, as shown in Fig. 13(b), to increase the output voltage [7], [20]. Another advantageous feature of multilevel SPWM is that the effective switching frequency of the load voltage is N_c times the switching frequency of each cell, as determined by its carrier signal. This property allows a reduction in the switching frequency of each cell, thus reducing the switching losses.

C. SVM

The SVM technique can be easily extended to all multilevel inverters [45]–[51]. Fig. 15 shows space vectors for the traditional two-, three-, and five-level inverters. These vector diagrams are universal regardless of the type of multilevel inverter. In other words, Fig. 15(c) is valid for five-level diode-clamped, capacitor-clamped, or cascaded inverter. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle (T_j, T_{j+1}, and T_{j+2}) for each vector

$$\mathbf{V}^* = \frac{(T_j\mathbf{V}_j + T_{j+1}\mathbf{V}_{j+1} + T_{j+2}\mathbf{V}_{j+2})}{T}. \tag{3}$$

Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications.

As the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically. Some authors have used decomposition of the five-level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify con-

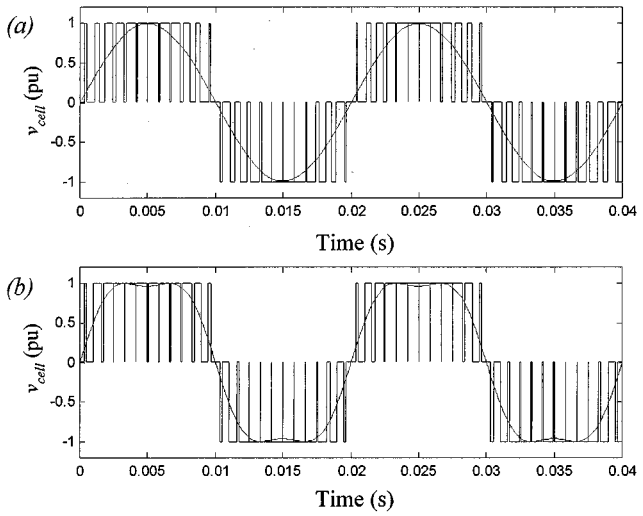

Fig. 13. Inverter cell voltages. (a) Output voltage and reference with SPWM. (b) Output voltage and reference with injection of sinusoidal third harmonic.

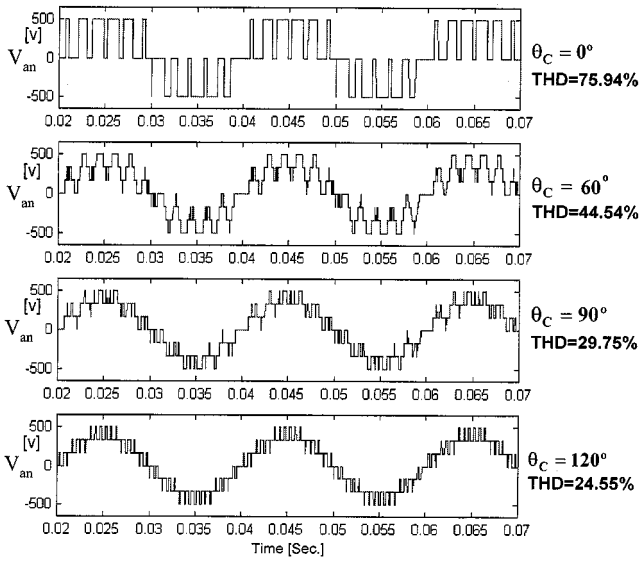

Fig. 14. Total voltage of three cells in series connection for different phase displacement in the carriers.

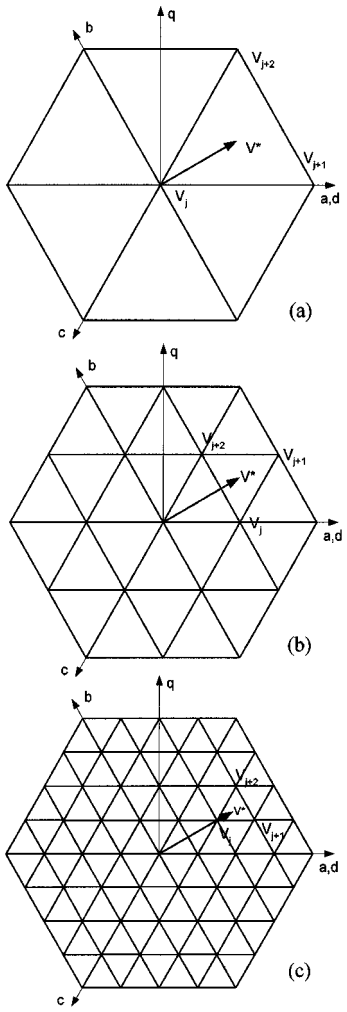

Fig. 15. Space-vector diagram: (a) two-level, (b) three-level, and (c) five-level inverter.

trol [48]. Additionally, a simple space-vector selection method was introduced without duty cycle computation of the adjacent three vectors [37].

D. Selective Harmonic Elimination

Fig. 16 shows a generalized quarter-wave symmetric stepped-voltage waveform synthesized by a $(2m+1)$-level inverter, where m is the number of switching angles. By applying Fourier series analysis, the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as (4), whereas the amplitudes of all even harmonics are zero

$$h_n = \frac{4}{n\pi}\sum_{k=1}^{m}[V_k \cos(n\alpha_k)] \tag{4}$$

where V_k is the k^{th} level of dc voltage, n is an odd harmonic order, m is the number of switching angles, and α_k is the kth switching angle. According to Fig. 16, α_1 to α_m must satisfy $\alpha_1 < \alpha_2 < \cdots < \alpha_m < \pi/2$.

To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $m-1$ harmonic

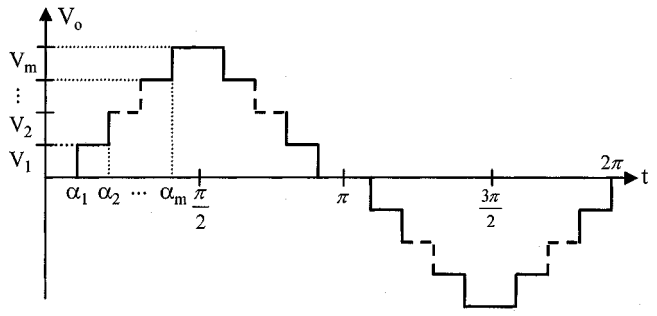

Fig. 16. Generalized stepped-voltage waveform.

contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different-level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. According to (4), to keep the number of eliminated harmonics at a constant level, all switching angles must be less than $\pi/2$. However, if the switching angles do not satisfy the condition, this scheme no longer exists. As a result, this modulation strategy basically provides a narrow range of modulation index, which is its main disadvantage. For example, in a seven-level equally stepped waveform, its modulation index is only available from 0.5 to 1.05. At modulation indexes lower than 0.5, if this scheme is still applied, the allowable harmonic components to be eliminated will reduce from 2 to 1. The total harmonic distortion (THD) increases correspondingly.

In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms, a generalized selected harmonic modulation scheme was proposed [40], [41]. The method can be illustrated by Fig. 17, in which the positive half-cycle of seven-level stepped waveforms are shown with different modulation index levels. In this case, the range of modulation indices can be divided into three levels, such as high, middle, and low. An output waveform with a high modulation index level is shown in Fig. 17(a). Whenever α_3 is greater than $\pi/2$, this waveform no longer exists. Therefore, an output waveform shown in Fig. 17(b), which gives middle modulation index level, will be applied instead. When the switching angles α_1 to α_3 in Fig. 17(b) are not converged at a low modulation index level, the output waveform shown in Fig. 17(c) will replace it. In general, a stepped waveform, which comprises m switching angles, can be divided into m modulation index levels. By using this technique, low switching frequencies with minimized harmonics in the output waveforms can be achieved with wide modulation indexes.

Through mathematical manipulation and observation of Fig. 17(a)–(c), a generalized harmonic expression for multilevel stepped voltage has been derived [41] and is expressed as the following equation:

$$h_n = \frac{4}{n\pi} \times [V_1 \cos(n\alpha_1) \pm V_2 \cos(n\alpha_2) \pm \cdots \pm V_m \cos(n\alpha_m)]. \tag{5}$$

In this expression, the positive sign implies the rising edge, and the negative sign implies the falling edge.

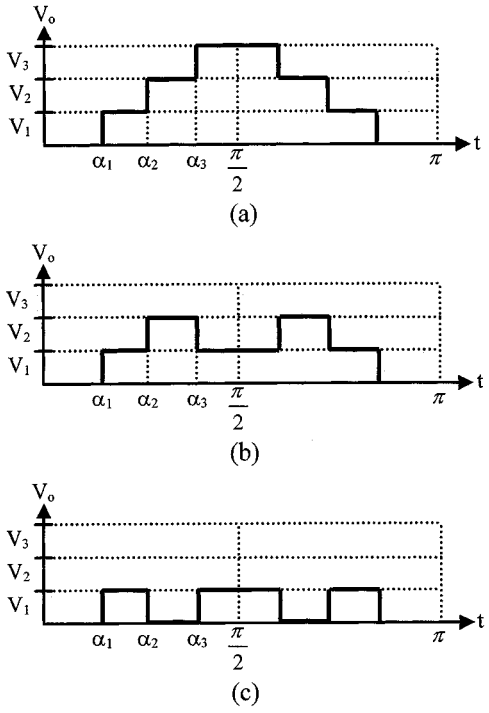

Fig. 17. A positive half-cycle of a seven-level stepped waveform with different modulation indexes. (a) High modulation index. (b) Middle modulation index. (c) Low modulation index.

E. SVC

A conceptually different control method for multilevel inverters, based on the space-vector theory, has been introduced [37]. This control strategy, called SVC, works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of SVM.

Fig. 18 shows the 311 different space vectors generated by an 11-level inverter. The reference load voltage vector $v_{\rm ref}$ is also included in this figure. The main idea in SVC is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector $v_{\rm ref}$. The high density of vectors produced by the 11-level inverter (see Fig. 18.) will generate only small errors in relation to the reference vector; it is, therefore, unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference.

The shaded hexagon of Fig. 18 shows the boundary of highest proximity, which means that when the reference voltage $v_{\rm ref}$ is located in this area, vector v_c must be selected, because it has the greatest proximity to the reference.

Fig. 19(a) presents the voltage generated by one cell in an eleven-level multicell inverter with five cells per phase and an output frequency of 50 Hz. The load voltage of the inverter for the same frequency and modulation index 0.99 is shown in Fig. 19(b).

Finally, Fig. 20 shows the reference vector and the vectors generated by the inverter using SVC [37]. This method is simple and attractive for high number of levels. As the number of levels decreases, the error in terms of the generated vectors with respect to the reference will be higher; this will increase the load current ripple.

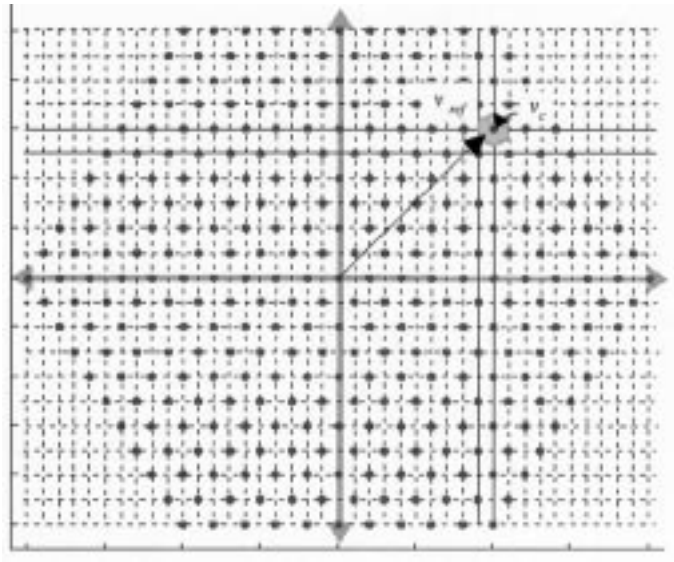

Fig. 18. Load voltage space vectors generated by an 11-level inverter.

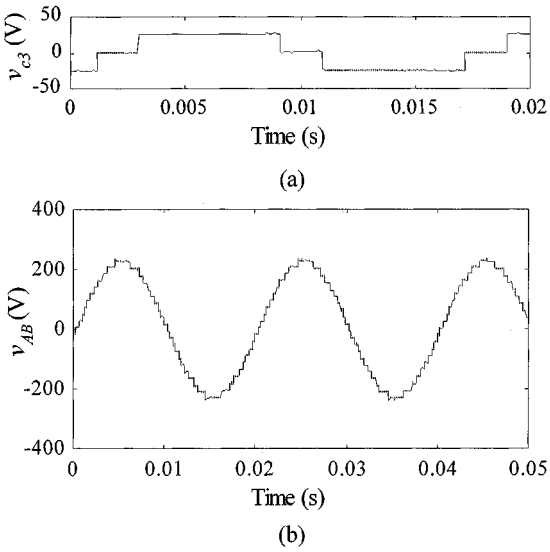

Fig. 19. Voltages generated by an 11-level inverter with SVC. (a) One-cell voltage. (b) Resulting load voltage.

F. Direct Torque Control (DTC)

The DTC technique has been developed for low-voltage two-level inverters as an alternative to the field oriented method to effectively control torque and flux in ac drives [52]. DTC and hysteresis current control techniques have also been applied in multilevel inverters [53]. It must be noticed that one major manufacturer has been selling medium-voltage three-level diode-clamped inverters controlled with DTC [54].

G. Capacitor Balancing Techniques

In [55], the voltage unbalancing problem and the mechanism of the diode-clamped multilevel inverter were discussed. The paper demonstrated that the diode-clamped multilevel inverter could not have balanced voltages for real power conversion without sacrificing output voltage performance. Thus, the paper proposed that the diode-clamped multilevel inverter be applied to reactive and harmonic compensation without voltage

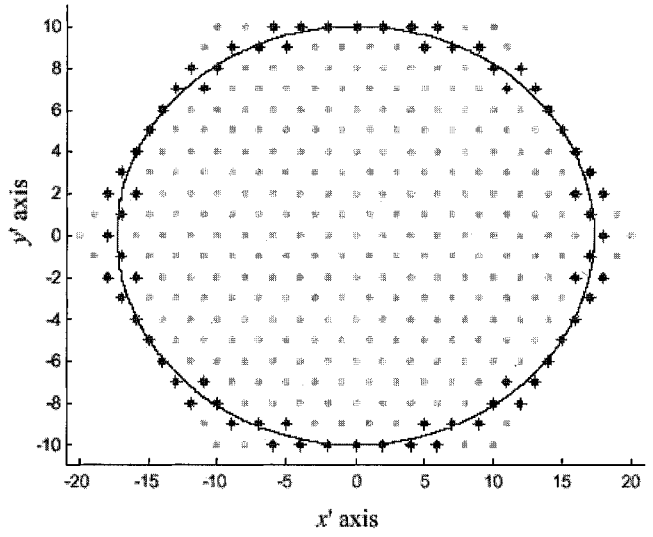

Fig. 20. Reference and output voltage vectors in an 11-level inverter with SVC.

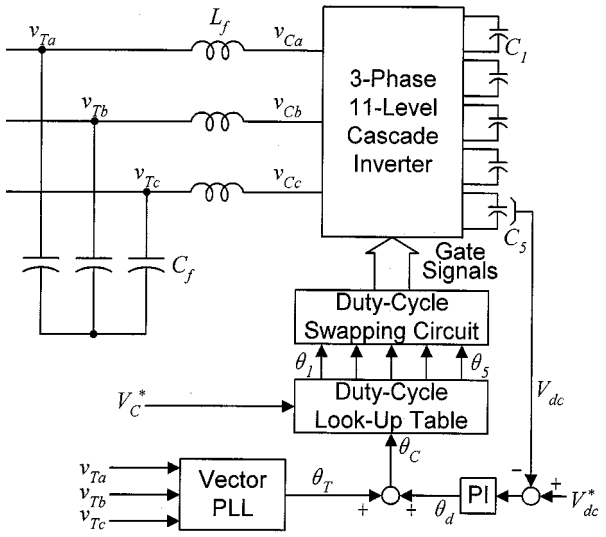

Fig. 21. Control diagram of the 11-level cascaded inverter.

balancing problem. Reference [56] suggested that the voltage unbalance problem could be solved by using a back-to-back rectifier/inverter system and proper voltage balancing control. Other papers [57]–[59] suggested the use of additional voltage balancing circuits, such dc chopper, etc.

The capacitor-clamped structure was originally proposed for high-voltage dc/dc conversions [60]. It is easy to balance the voltages for such applications because the load current is dc. For the capacitor-clamped multilevel inverter, voltage balancing is relatively complicated [60], [61]. It has been shown theoretically that the capacitor-clamped inverter cannot have self-balanced voltage when applied to power conversion in which no real power is involved, such as reactive power compensation. However, since each phase leg has its own floating capacitors that handle the phase current, the voltage balancing and ripple become troublesome.

The cascaded multilevel inverter was first introduced for motor drive applications, in which an isolated and separate dc source is needed for each H-bridge unit [7]. However, another paper presented the idea of using cascade multilevel inverter for reactive and harmonic compensation, from which isolated dc sources can be omitted [56]. Additional work further demonstrated that the cascaded inverter is suitable for universal power conditioning of power systems, especially for medium-voltage systems [62], [63]. The inverter provides lower costs, higher performance, less electromagnetic interference (EMI), and higher efficiency than the traditional PWM inverter for power line conditioning applications, both series and parallel compensation. Although the cascaded inverter has an inherent self-balancing characteristic, because of the circuit component losses and limited controller resolution, a slight voltage imbalance can occur. A simple control scheme, which ensures dc voltage balance, has been proposed for reactive and harmonic compensation [56]. Fig. 21 shows its control block diagram that contains a proportional–integral (PI) regulator to adjust the trigger angle and to ensure zero steady-state error between the reference dc voltage and the dc-bus voltage.

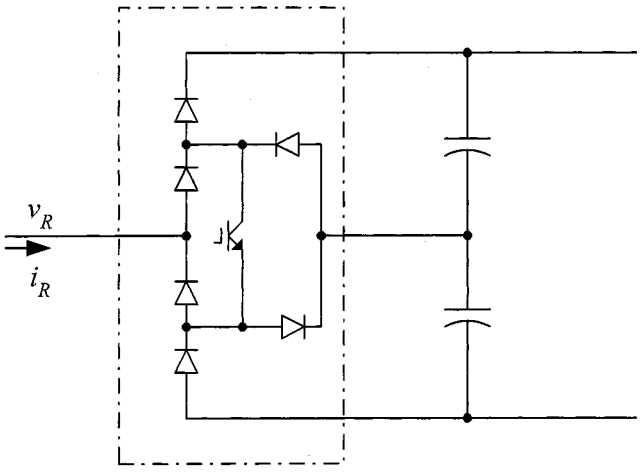

Fig. 22. Vienna rectifier phase-leg structure.

IV. Industrial Applications and Technological Aspects

A. Multilevel Rectifier

Traditionally, multipulse rectifiers have been used for the reduction of harmonics in the line current. These multipulse (12-pulse, 18-pulse, and so on) rectifiers use transformers for phase shifting in order to eliminate harmonics. To eliminate the phase-shift transformers, multilevel rectifiers have been proposed.

For those applications that require no regenerative capability, simplified (or reduced) multilevel rectifiers have been proposed in [64]. This specific rectifier, named the Vienna rectifier, has been used for telecommunication power supplies. Fig. 22 shows the per-phase leg structure for a three-level Vienna rectifier. Some reduced-parts-count multilevel rectifiers for the number more than three levels have been proposed [65].

B. DC/DC Converters

The phase voltage of a multilevel diode-clamped or capacitor-clamped inverter resembles that of a full-bridge phase-shift-

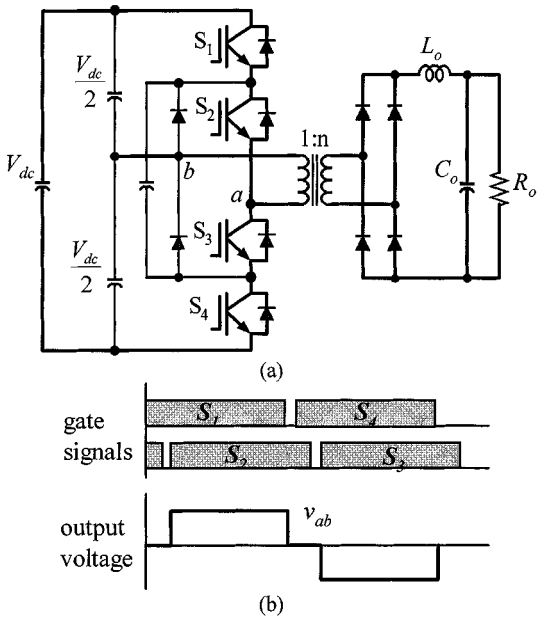

Fig. 23. Three-level capacitor-clamped inverter for dc–dc converter application. (a) Circuit diagram. (b) Gating and output waveforms.

modulated dc/dc converter [66]. Fig. 23(a) shows a three-level dc/dc converter based on a capacitor-clamped inverter circuit along with diode clamping to ensure neutral-point voltage balance [67], [68]. The same as the capacitor-clamped inverter, this converter only allows certain switch pairs to be turned on simultaneously. The switch pair $\{S_1, S_2\}$ yields $+V_{\rm dc}/2$, $\{S_3, S_4\}$ yields $-V_{\rm dc}/2$, and $\{S_1, S_3\}$ and $\{S_2, S_4\}$ yield zero output. By applying gate pulses sequentially, as shown in Fig. 23(b), a three-level output voltage across the transformer primary can be obtained. With phase-shift operation, this circuit operates inherently under the soft-switching condition.

C. Large Motor Drives With Nonregenerative Front Ends

Diode-clamped three-level inverters are now widely applied in medium-voltage (2.3, 3.3, 4.16, and even 6 kV) applications, using an IGBT with forced-air cooling. These applications cover a wide range of high-power loads including fans, pumps, blowers, compressors, and conveyors.

An important issue in the application of these inverters is the injection of current harmonics into the power supply due to both the high power of the drive and the capacitive filters in the dc link, which increase the distortion of the input current. A 12-pulse configuration of the input rectifier, as shown in Fig. 24, is a standard solution for reducing the input current harmonics. Some manufacturers include an 18-pulse and 24-pulse rectifier to improve the quality of the input current.

Fig. 25 presents a three-level inverter with capacitor-clamped topology and 18-pulse configuration of the input rectifier [69]. The secondary voltages are shifted by 20° from each other. With this type of input rectifier, the harmonics in the input currents are drastically reduced, achieving a THD of less than 1.55% [69].

Fig. 26 shows a seven-level cascade multicell inverter used in nonregenerative drives for 2.3-kV networks. This inverter uses three cells in each phase. The input part of each cell has a three-

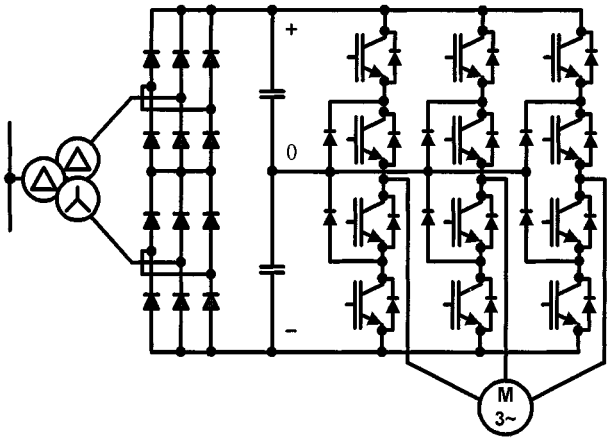

Fig. 24. Three-level diode-clamped inverter with 12-pulse input rectifier.

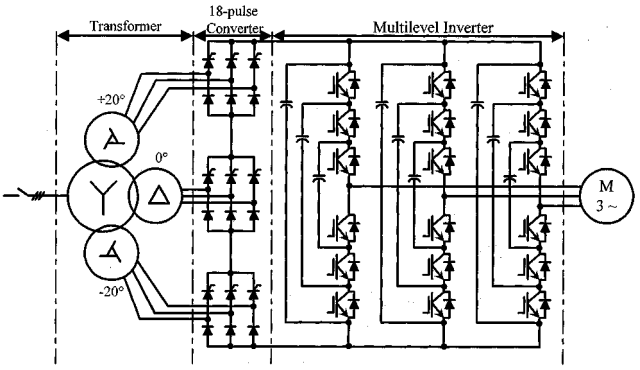

Fig. 25. Three-level capacitor-clamped inverter with 18-pulse input rectifier.

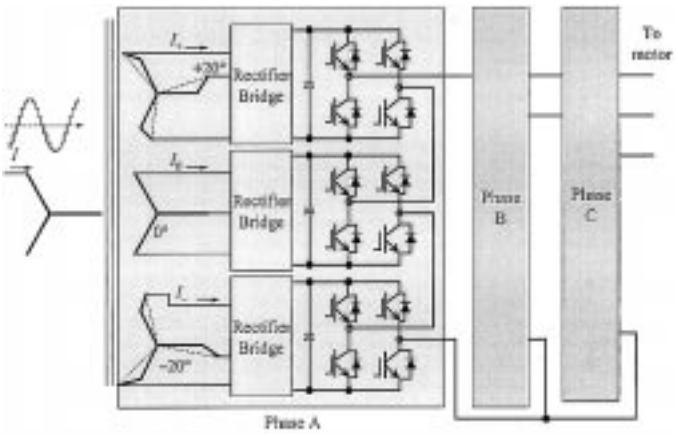

Fig. 26. Seven-level cascaded inverter with nonregenerative rectifier.

phase diode rectifier, which does not allow the regeneration of power. Table I presents the number of cells used in each phase for different motor voltages, as reported by one manufacturer [7].

The high quality of the input current assures compliance with IEEE Standard 519–1992. In the case of 4.16-kV inverters with five cells per phase, the quality of the output voltage is very high with a voltage distortion THD of $<$10%. In this 11-level inverter, the input current of the inverter has a 30-pulse waveform and a THD of $< 1\%$ [7].

TABLE I
CASCADED INVERTERS USED IN MEDIUM-VOLTAGE DRIVES [7]

Levels	Cells per phase	Output voltage (kV)	Pulses in input current	Displacement in secondaries [°]
7	3	2.3	18	20
9	4	3.3	24	15
11	5	4.16	30	12

D. Large Motor Drives With Regenerative Front Ends

The use of a three-level active front end (AFE) at the input side of a three-level diode-clamped inverter has become a very popular solution for high-power regenerative loads. This solution, presented in Fig. 27, allows the regeneration of full motor power with reduced harmonics and high power factor. Drives with three-level AFE are used in laminators [70], high-power downhill conveyors [71], and other regenerative high-power loads.

A very interesting application of this technology in which two three-level AFEs are used in a so-called tandem configuration is shown in Fig. 28 [71]. This drive uses GTO technology and, for this reason, an operation with low switching frequency is highly desirable. The selective harmonic-elimination method is used with three commutation angles (α_1, α_2, and α_3) in each AFE in order to eliminate harmonics 11 and 13. The equations to achieve this purpose are

$$V_1 = \frac{4 \cdot V_{\mathrm{dc}}}{\pi}\left[\cos(\alpha_1) - \cos(\alpha_2) + \cos(\alpha_3)\right] = \frac{4 \cdot V_{\mathrm{dc}}}{\pi} \cdot M \tag{6}$$

$$V_{11} = \frac{4 \cdot V_{\mathrm{dc}}}{\pi \cdot 11}\left[\cos(11\alpha_1) - \cos(11\alpha_2) + \cos(11\alpha_3)\right] = 0 \tag{7}$$

$$V_{13} = \frac{4 \cdot V_{\mathrm{dc}}}{\pi \cdot 13}\left[\cos(13\alpha_1) - \cos(13\alpha_2) + \cos(13\alpha_3)\right] = 0 \tag{8}$$

where M is the modulation index and V_{dc} is the voltage in each dc-link capacitor.

The wye–wye and wye–delta connection in the input transformers produces a 30° displacement in the input voltages of the AFEs, eliminating all harmonics of order $6 \cdot n \pm 1 (n = \text{odd})$: 5, 7, 17, 19, 29, and 31. In this way, the first harmonics are of the order 23 and 25. An important reduction of the input current harmonics, working with a very low switching frequency, is obtained with this method.

Although this multipulse transformer allows the phase-shifted currents to be summed together for a near sinusoidal input current, the major difficulty is the design of the transformer. With irrational turns ratios, it is possible to produce undesirable interharmonic contents. Fig. 29 shows a solution using an active filter circuit as the regenerative front end [14]. In this circuit, the transformer does not need to have irrational turns ratios because the secondary winding current is compensated by an active filter. The active filter also allows power flow to be reversed, which solves the problem found in Fig. 26.

The regenerative block shown in Fig. 29 has limited capability because the active filter is normally designed with a smaller power rating. In certain applications in which the regenerative block also needs rated capability, the circuit shown in Fig. 29 would not be applicable. A more general-purpose regenerative four-quadrant-type configuration is shown in Fig. 30 [16]. In this circuit, each power module contains an AFE converter and a full-bridge inverter. The AFE converter corrects the power factor and eliminates the harmonics, thus, the transformer can be designed in a conventional way, similar to the one shown in Fig. 29. It allows all the regenerative power to be pumped back to the source because the AFE converter needs to be designed with full power rating. The only drawback to this AFE-based cascaded inverter is that it requires high number of devices. The use of single-phase AFEs at the line side of each cell has been considered as an alternative to spare power semiconductors [72]. However, this circuit imposes restrictions to the number of cells that can be connected in series to eliminate low-frequency harmonics in the input current.

E. Applications in Power Systems

When the number of levels is greater than three, both the diode-clamped and cascaded multilevel inverters have equivalently separate dc sources for each level in order to enable power conversion involving real power such as in motor drives [11], [57]. However, as mentioned previously, both inverters have a perfect niche in harmonic and reactive power compensation [55], [62], [63]. The capacitor-clamped inverter cannot have balanced voltage for power conversion involving only reactive power [61], thus, it is not suited for reactive power compensation.

The first unified power-flow controller (UPFC) in the world was based on a diode-clamped three-level inverter [73]. The UPFC is comprised of the back-to-back connection of two identical GTO thyristor-based three-level converters, each rated at 160 MVA; it was commissioned in mid-1998 at the Inez Station of American Electric Power (AEP) in Kentucky for voltage support and power-flow control. Fig. 31 shows the system configuration.

On the other hand, the cascaded multilevel inverter is best suited for harmonic/reactive compensation and other utility applications [13], [62], [63], since each H-bridge inverter unit can balance its dc voltage without requiring additional isolated power sources. GEC Alsthom T&D has commercialized the cascaded multilevel inverter for reactive power compensation/generation (STATCOM) [74].

V. FUTURE TRENDS

By looking at the number of papers published in recent years, it is easy to conclude that multilevel inverter research and development activities are experiencing an explosive rate of growth. A trend of having more and more multilevel inverters is obvious. Although this paper has focused on multilevel inverter circuit topology, control, and applications, there is other research and development in related areas, such as high-voltage high-power semiconductor devices, sensors, high-speed DSPs, thermal management, and packaging. It is difficult to include

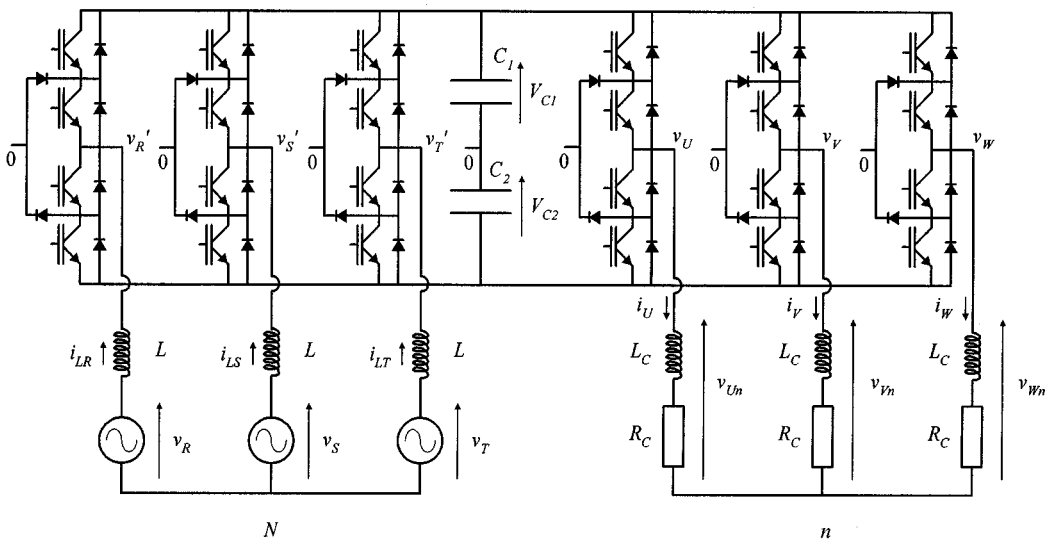

Fig. 27. Three-level AFE and inverter.

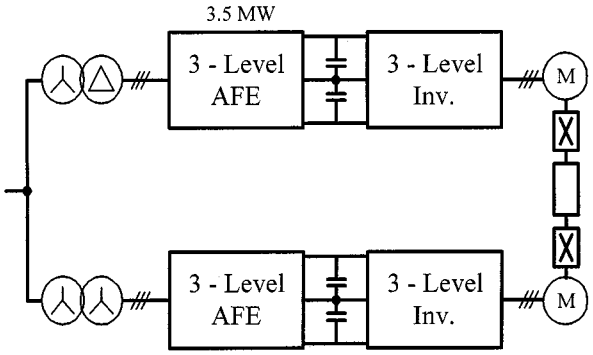

Fig. 28. Two parallel-connected three-level AFEs.

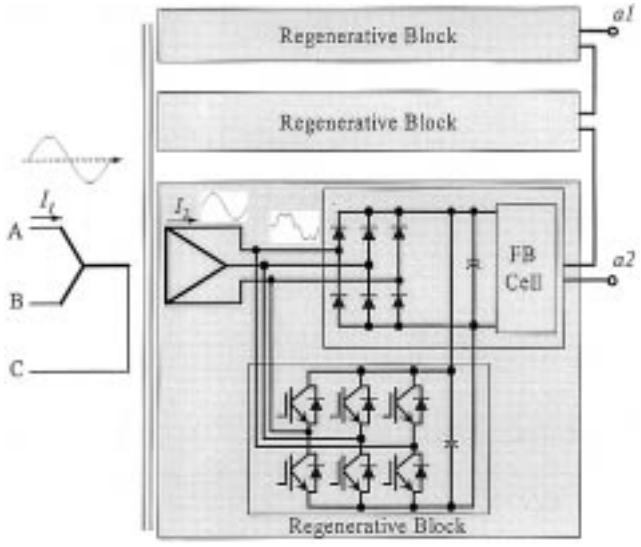

Fig. 29. Cascaded multicell inverter regenerative blocks.

all the related technologies in one paper; however, those technologies related to multilevel inverter development should not be neglected from the ongoing development. Based on the progress of semiconductor devices and advanced circuit topologies, future trends can be observed in the following areas.

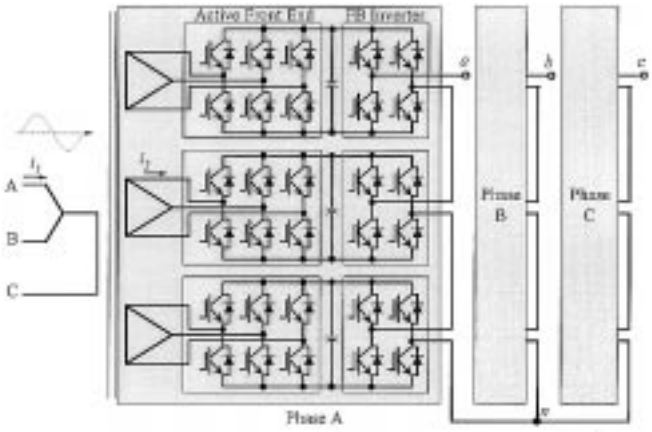

Fig. 30. Cascaded regenerative inverter with three-phase AFEs.

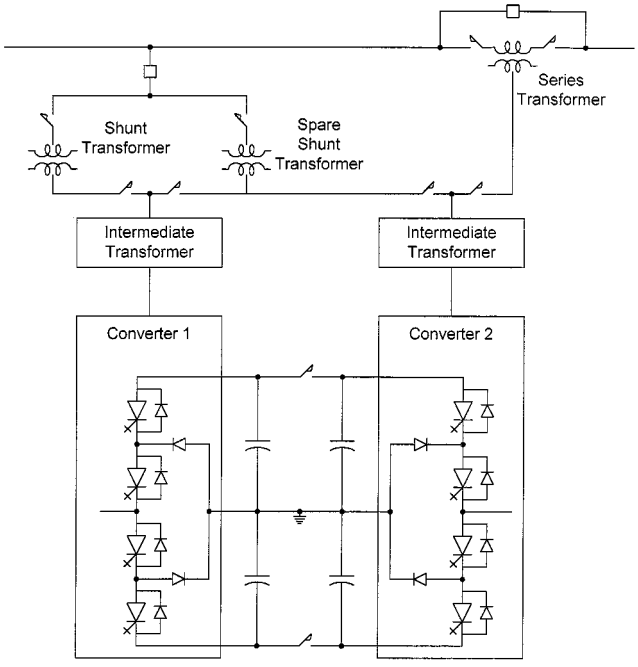

Fig. 31. System configuration of the UPFC installed at Inez.

A. Applications for Distribution Voltage Level

There is a strong demand to push voltage-source inverters (VSIs) into distribution voltage level, which is between 11–16 kV, or typically 13.8 kV. Currently, the power electronics for distribution and transmission voltage levels are mainly dominated by current source converters, which use thyristor devices with built-in reverse voltage blocking capability. The main problems with thyristors are their sluggish switching speeds and their inability to gate off. With the use of gate-turn-off high-voltage semiconductor devices in multilevel inverters, the widespread use of VSIs in distribution voltage level can be easily expected.

B. Advanced High-Voltage High-Power Semiconductor Devices

The availability of higher-voltage devices allows higher operating voltages with fewer inverter levels. The major contenders in the device arena are integrated-gate-commutated thyristor (IGCT) [75], [76], 3.3- and 6.5-kV high-voltage IGBT (HV-IGBT) [77], and emitter turn-off (ETO) thyristor [78]. As power level increased with new devices, the multilevel inverter power-handling capability is also proportionally increased. With the use of these high voltage devices, an inverter can easily achieve 5 MW with only three levels required. The application to the distribution voltage level can be achieved with less than five levels when the above-mentioned high-voltage devices are used.

C. Use of Optical Fibers for Sensors and Controls

For a scaled-down version multilevel inverter prototype and its control implementation, the wiring is short, the parasitic is minimum, and the isolation is not an issue. However, for a high-voltage system, the CM voltage level and the distance between power modules and the DSP controller become major problems in the inverter design. The CM voltage level can easily produce enough noise and upset the control circuit and gate drives. The wiring from controller to power modules for a multimegawatt inverter is also a problem, as it can be as long as tens of meters, which can either be the source of noise or be upset by noise. A future trend is to apply fiber-optic technologies for sensors, gate drive controllers, and communications.

D. Thermal Management

The conventional disc-type thyristors are typically cooled by circulating water through their clamping assemblies. This requires substantial effort to make sure that the water is deionized and well circulated with a sufficient flow rate. The water-cooled system is difficult to move around because the water can easily leak. For high-voltage systems, the insulation becomes a concern if the water deionizing system is not functioning. With the module-type package for high-voltage IGBTs, however, the cooling is much more flexible. Other cooling techniques, such as forced air and heat pipe, are gaining more acceptability in industry applications.

E. Distributed Energy Applications

Distributed energy systems, mostly those using alternative energies such as photovoltaic panels and fuel cells, can be easily configured with a separate source connected through the power conversion circuits used as an energy module or building block to provide individual output. A cascaded inverter can then be configured with multiple modules. Such a system does not need a transformer to provide isolation, and the system can be constructed in a cost effective manner.

VI. Conclusion

This paper has provided a brief summary of multilevel inverter circuit topologies and their control strategies. Different applications using different inverter circuits were also discussed. As mentioned in Section I, an early patent for the cascaded multilevel inverter can be traced back to 1975. However, the commercial products that utilize this superior circuit topology were not available until the mid-1990s. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. The intention of the authors was simply to provide groundwork to readers interested in looking back on the evolution of multilevel inverter technologies, and to consider where to go from here.

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José Rodríguez (M'81–SM'94) received the Engineer degree from the Universidad Técnica Federico Santa María, Valparaiso, Chile, in 1977 and the Dr.-Ing. degree from the University of Erlangen, Erlangen, Germany, in 1985, both in electrical engineering.

Since 1977, he has been with the University Técnica Federico Santa María, where he is currently a Professor and Head of the Department of Electronic Engineering. During his sabbatical leave in 1996, he was responsible for the Mining Division of Siemens Corporation in Chile. He has extensive consulting experience in the mining industry, especially in the application of large drives like cycloconverter-fed synchronous motors for SAG mills, high-power conveyors, controlled drives for shovels, and power quality issues. His research interests are mainly in the areas of power electronics and electrical drives. Recently, his main research interests have been multilevel inverters and new converter topologies. He has authored or coauthored more than 100 refereed journal and conference papers and contributed to one chapter in *Power Electronics Handbook* (New York: Academic, 2001).

Jih-Sheng (Jason) Lai (S'84–M'87–SM'93) received the M. S. and Ph.D. degrees in electrical engineering from the University of Tennessee, Knoxville, in 1985 and 1989, respectively.

From 1980 to 1983, he was the Head of the Electrical Engineering Department, Ming-Chi Institute of Technology, Taipei, Taiwan, R.O.C., where he initiated a power electronics program and received a grant from his college and a fellowship from the National Science Council to study abroad. In 1986, he became a staff member at the University of Tennessee, where he taught control systems and energy conversion courses. In 1989, he joined the Electric Power Research Institute (EPRI) Power Electronics Applications Center (PEAC), where he managed EPRI-sponsored power electronics research projects. In 1993, he joined Oak Ridge National Laboratory as the Power Electronics Lead Scientist, where he initiated a high-power electronics program and developed several novel high-power converters including multilevel converters and auxiliary-resonant-snubber-based soft-switching inverters. Since August 1996, he has been with Virginia Polytechnic Institute and State University, Blacksburg, as an Associate Professor. His main research areas are in high-power electronics converter topologies, motor drives, and utility power electronics interface and application issues. He has authored more than 100 published technical papers and two books. He is the holder of eight U.S. patents in the area of high power electronics and their applications. He chaired the Technical Committee for the 2001 DOE Future Energy Challenge.

Dr. Lai is the Chairman of the IEEE Power Electronics Society Standards Committee. He is a member of Phi Kappa Phi and Eta Kappa Nu. He was the recipient of several distinctive awards, including a Technical Achievement Award at Lockheed Martin Award Night, two Conference Paper Awards from the Industrial Power Converter Committee of the IEEE Industry Applications Society, one IEEE IECON Best Paper Award, and an Advanced Technology Award from the Inventors Clubs of America, Inc.

Fang Zheng Peng (M'93–SM'96) received the B.S. degree from Wuhan University, Wuhan, China, in 1983 and the M.S. and Ph.D. degrees from Nagaoka University of Technology, Nagaoka Japan, in 1987 and 1990, respectively, all in electrical engineering.

From 1990 to 1992, he was a Research Scientist with Toyo Electric Manufacturing Company, Ltd., where he was engaged in research and development of active power filters, flexible ac transmission systems (FACTS) applications, and motor drives. From 1992 to 1994, he was a Research Assistant Professor at Tokyo Institute of Technology, where initiated a multilevel inverter program for FACTS applications and a speed-sensorless vector control project. From 1994 to 1997, he was a Research Assistant Professor at the University of Tennessee, Knoxville, working for Oak Ridge National Laboratory (ORNL). From 1997 to 2000 he was a Senior Staff Member at ORNL and Lead (principal) Scientist of the Power Electronics and Electric Machinery Research Center. In 2000, he joined Michigan State University, East Lansing, as an Associate Professor in the Department of Electrical and Computer Engineering. He is the holder of ten patents.

Dr. Peng has received many awards, including the 1996 First Prize Paper Award and the 1995 Second Prize Paper Award from the Industrial Power Converter Committee at the IEEE Industry Applications Society Annual Meeting, the 1996 Advanced Technology Award of the Inventors Clubs of America, Inc., the International Hall of Fame, the 1991 First Prize Paper Award from the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the 1990 Best Paper Award from the *Transactions of the Institute of Electrical Engineers of Japan*, and the Promotion Award of the Electrical Academy. He has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS since 1997 and is currently the Chair of the Technical Committee for Rectifiers and Inverters of the IEEE Power Electronics Society.