

sysio::chain::webassembly
::interface::_sysio_f64_floor

sysio::chain::webassembly
::interface::_sysio_f64_gt

sysio::vm::binary_parser
::parse_function_body_code

f64_le

```
graph LR; A["sysio::chain::webassembly  
::interface::_sysio_f64_floor"] --> D[f64_le]; B["sysio::chain::webassembly  
::interface::_sysio_f64_gt"] --> D; C["sysio::vm::binary_parser  
::parse_function_body_code"] --> D;
```

The diagram illustrates three source components on the left, each enclosed in a white box with a black border. These components are connected by blue arrows to a single target component on the right, which is a gray box labeled 'f64_le'. The top source box contains the text 'sysio::chain::webassembly' followed by '::_interface::_sysio_f64_floor' on a new line. The middle source box contains 'sysio::chain::webassembly' followed by '::_interface::_sysio_f64_gt' on a new line. The bottom source box contains 'sysio::vm::binary_parser' followed by '::_parse_function_body_code' on a new line. Three blue arrows originate from the right side of these three boxes and point towards the left side of the 'f64_le' box.