

## 1. Description

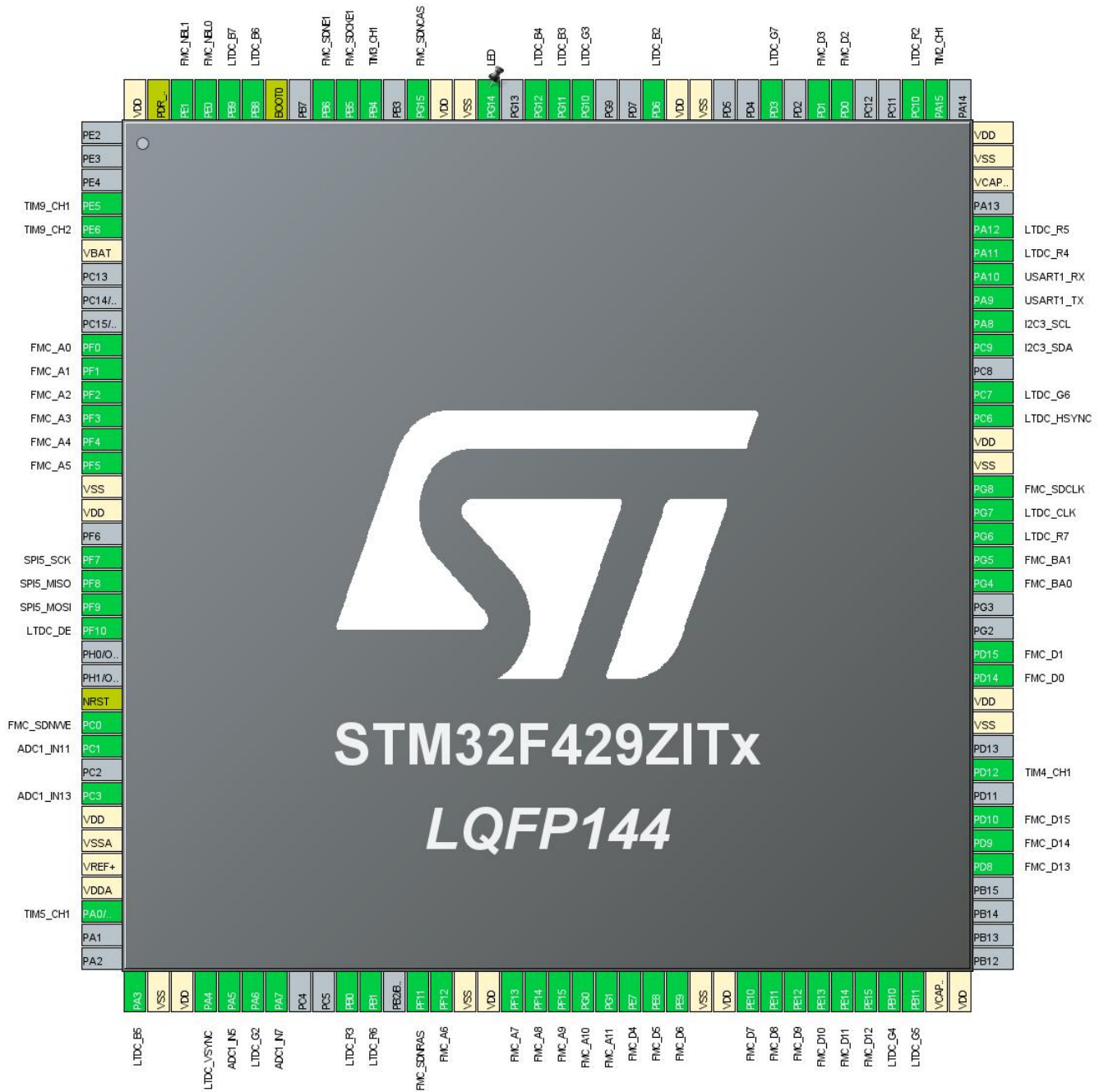
### 1.1. Project

Project Name	Micromouse Robot Wizualizer
Board Name	STM32F429I-DISC1
Generated with:	STM32CubeMX 5.6.0
Date	06/06/2020

### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429ZITx
MCU Package	LQFP144
MCU Pin number	144

## 2. Pinout Configuration



### 3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
4	PE5	I/O	TIM9_CH1	
5	PE6	I/O	TIM9_CH2	
6	VBAT	Power		
10	PF0	I/O	FMC_A0	
11	PF1	I/O	FMC_A1	
12	PF2	I/O	FMC_A2	
13	PF3	I/O	FMC_A3	
14	PF4	I/O	FMC_A4	
15	PF5	I/O	FMC_A5	
16	VSS	Power		
17	VDD	Power		
19	PF7	I/O	SPI5_SCK	
20	PF8	I/O	SPI5_MISO	
21	PF9	I/O	SPI5_MOSI	
22	PF10	I/O	LTDC_DE	
25	NRST	Reset		
26	PC0	I/O	FMC_SDNWE	
27	PC1	I/O	ADC1_IN11	
29	PC3	I/O	ADC1_IN13	
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP	I/O	TIM5_CH1	
37	PA3	I/O	LTDC_B5	
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	LTDC_VSYNC	
41	PA5	I/O	ADC1_IN5	
42	PA6	I/O	LTDC_G2	
43	PA7	I/O	ADC1_IN7	
46	PB0	I/O	LTDC_R3	
47	PB1	I/O	LTDC_R6	
49	PF11	I/O	FMC_SDNRAS	
50	PF12	I/O	FMC_A6	
51	VSS	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	VDD	Power		
53	PF13	I/O	FMC_A7	
54	PF14	I/O	FMC_A8	
55	PF15	I/O	FMC_A9	
56	PG0	I/O	FMC_A10	
57	PG1	I/O	FMC_A11	
58	PE7	I/O	FMC_D4	
59	PE8	I/O	FMC_D5	
60	PE9	I/O	FMC_D6	
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	FMC_D7	
64	PE11	I/O	FMC_D8	
65	PE12	I/O	FMC_D9	
66	PE13	I/O	FMC_D10	
67	PE14	I/O	FMC_D11	
68	PE15	I/O	FMC_D12	
69	PB10	I/O	LTDC_G4	
70	PB11	I/O	LTDC_G5	
71	VCAP_1	Power		
72	VDD	Power		
77	PD8	I/O	FMC_D13	
78	PD9	I/O	FMC_D14	
79	PD10	I/O	FMC_D15	
81	PD12	I/O	TIM4_CH1	
83	VSS	Power		
84	VDD	Power		
85	PD14	I/O	FMC_D0	
86	PD15	I/O	FMC_D1	
89	PG4	I/O	FMC_BA0	
90	PG5	I/O	FMC_BA1	
91	PG6	I/O	LTDC_R7	
92	PG7	I/O	LTDC_CLK	
93	PG8	I/O	FMC_SDCLK	
94	VSS	Power		
95	VDD	Power		
96	PC6	I/O	LTDC_HSYNC	
97	PC7	I/O	LTDC_G6	
99	PC9	I/O	I2C3_SDA	

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
100	PA8	I/O	I2C3_SCL	
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
103	PA11	I/O	LTDC_R4	
104	PA12	I/O	LTDC_R5	
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
110	PA15	I/O	TIM2_CH1	
111	PC10	I/O	LTDC_R2	
114	PD0	I/O	FMC_D2	
115	PD1	I/O	FMC_D3	
117	PD3	I/O	LTDC_G7	
120	VSS	Power		
121	VDD	Power		
122	PD6	I/O	LTDC_B2	
125	PG10	I/O	LTDC_G3	
126	PG11	I/O	LTDC_B3	
127	PG12	I/O	LTDC_B4	
129	PG14 *	I/O	GPIO_Output	LED
130	VSS	Power		
131	VDD	Power		
132	PG15	I/O	FMC_SDNCAS	
134	PB4	I/O	TIM3_CH1	
135	PB5	I/O	FMC_SDCKE1	
136	PB6	I/O	FMC_SDNE1	
138	BOOT0	Boot		
139	PB8	I/O	LTDC_B6	
140	PB9	I/O	LTDC_B7	
141	PE0	I/O	FMC_NBL0	
142	PE1	I/O	FMC_NBL1	
143	PDR_ON	Reset		
144	VDD	Power		

\* The pin is affected with an I/O function



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	Micromouse Robot Wizualizer
Project Folder	C:\Users\r0ck\Documents\STM32 Projects\Micromouse-Robot-Wizualizer
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.25.0

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	No
Set all free pins as analog (to optimize the power consumption)	No

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429ZITx
Datasheet	024030_Rev9

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

### 6.4. Sequence

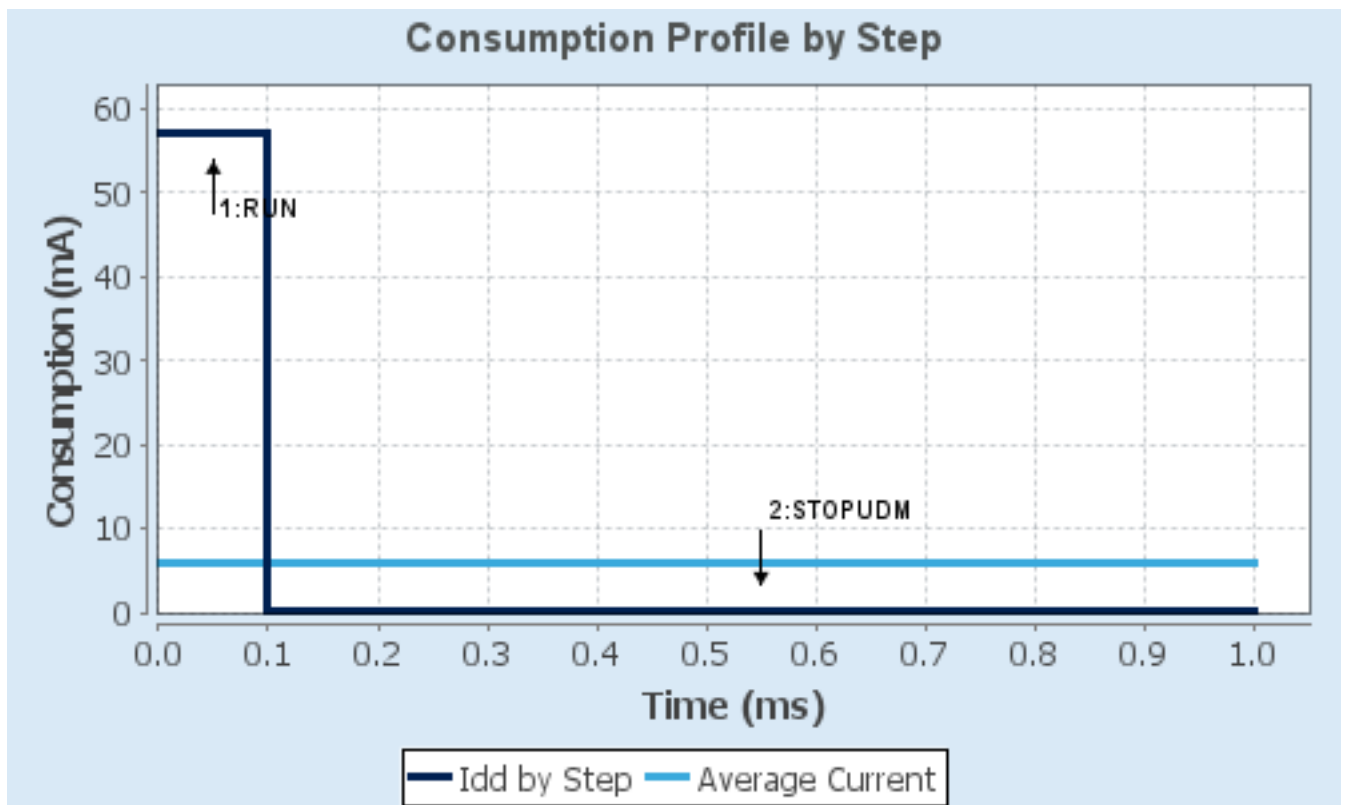


<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP UDM (Under Drive)
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	180 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	57 mA	100 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	225.0	0.0
<b>Ta Max</b>	97.48	104.99
<b>Category</b>	In DS Table	In DS Table

## 6.5. RESULTS

Sequence Time	1 ms	Average Current	5.79 mA
Battery Life	24 days, 10 hours	Average DMIPS	225.0 DMIPS

## 6.6. Chart



## 7. IPs and Middleware Configuration

### 7.1. ADC1

mode: IN5

mode: IN7

mode: IN11

mode: IN13

#### 7.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

##### ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel **Channel 11 \***

Sampling Time 3 Cycles

##### ADC\_Injected\_ConversionMode:

Number Of Conversions 0

##### WatchDog:

Enable Analog WatchDog Mode false

### 7.2. DMA2D

mode: Activated

#### 7.2.1. Parameter Settings:

##### Basic Parameters:

Transfer Mode Memory to Memory

Color Mode	RGB565 *
Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO
DMA2D Line Offset Mode	Line offsets expressed in pixels

**Foreground layer Configuration:**

DMA2D Input Color Mode	RGB565
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0

### 7.3. FMC

#### SDRAM 1

**Clock and chip enable: SDCKE1+SDNE1**

**Internal bank number: 4 banks**

**Address: 12 bits**

**Data: 16 bits**

**Byte enable: set**

#### **7.3.1. SDRAM 1:**

**SDRAM control:**

Bank	SDRAM bank 2
Number of column address bits	8 bits
Number of row address bits	12 bits
CAS latency	1 memory clock cycle
Write protection	Disabled
SDRAM common clock	Disabled
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

**SDRAM timing in memory clock cycles:**

Load mode register to active delay	16
Exit self-refresh delay	16
Self-refresh time	16
SDRAM common row cycle delay	16
Write recovery time	16
SDRAM common row precharge delay	16
Row to column delay	16

## 7.4. GPIO

## 7.5. I2C3

### I2C: I2C

#### 7.5.1. Parameter Settings:

##### Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

##### Timing configuration:

Coefficient of Digital Filter	0
Analog Filter	Enabled

##### Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

## 7.6. LTDC

### Display Type: RGB666 (18 bits)

#### 7.6.1. Parameter Settings:

##### Synchronization for Width:

Horizontal Synchronization Width	8
Horizontal Back Porch	7
Active Width	<b>320 *</b>
Horizontal Front Porch	6
HSync Width	7
Accumulated Horizontal Back Porch Width	14
Accumulated Active Width	334
Total Width	340

##### Synchronization for Height:

Vertical Synchronization Height	4
Vertical Back Porch	2
Active Height	<b>240 *</b>

Vertical Front Porch	2
VSynC Height	3
Accumulated Vertical Back Porch Height	5
Accumulated Active Height	245
Total Height	247

**Signal Polarity:**

Horizontal Synchronization Polarity	Active Low
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

**BackGround Color:**

Red	0
Green	0
Blue	0

## 7.6.2. Layer Settings:

**BackGround Color:**

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0
Layer 1 - Blue	0
Layer 1 - Green	0
Layer 1 - Red	0

**Number of Layers:**

Number of Layers	2 layers
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**Windows Position:**

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	0
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	0
Layer 1 - Window Horizontal Start	0
Layer 1 - Window Horizontal Stop	0
Layer 1 - Window Vertical Start	0
Layer 1 - Window Vertical Stop	0

**Pixel Parameters:**

Layer 0 - Pixel Format	ARGB8888
Layer 1 - Pixel Format	ARGB8888

**Blending:**

Layer 0 - Alpha constant for blending	0
Layer 0 - Default Alpha value	0

Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant
Layer 1 - Alpha constant for blending	0
Layer 1 - Default Alpha value	0
Layer 1 - Blending Factor1	Alpha constant
Layer 1 - Blending Factor2	Alpha constant

**Frame Buffer:**

Layer 0 - Color Frame Buffer Start Address	0
Layer 0 - Color Frame Buffer Line Length (Image Width)	0
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	0
Layer 1 - Color Frame Buffer Start Address	0
Layer 1 - Color Frame Buffer Line Length (Image Width)	0
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	0

## 7.7. RCC

### 7.7.1. Parameter Settings:

**System Parameters:**

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

**RCC Parameters:**

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

**Power Parameters:**

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

## 7.8. SPI5

## Mode: Full-Duplex Master

### 7.8.1. Parameter Settings:

#### Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

#### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>11.25 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

#### Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

## 7.9. SYS

Timebase Source: SysTick

## 7.10. TIM2

### Channel1: PWM Generation CH1

#### 7.10.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>44 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>999 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

##### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Output compare preload	Enable
Fast Mode	Disable



CH Polarity High

## 7.11. TIM3

### Slave Mode: External Clock Mode 1

#### Trigger Source: TI1FP1

##### 7.11.1. Parameter Settings:

###### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	0xFFFF *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

###### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

###### Trigger:

Trigger Polarity	Rising Edge
Trigger Filter (4 bits value)	0

## 7.12. TIM4

### Channel1: PWM Generation CH1

##### 7.12.1. Parameter Settings:

###### Counter Settings:

Prescaler (PSC - 16 bits value)	44 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

###### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

###### PWM Generation Channel 1:

Mode	PWM mode 1
------	------------

Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### 7.13. TIM5

#### Slave Mode: External Clock Mode 1

#### Trigger Source: TI1FP1

##### 7.13.1. Parameter Settings:

###### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	<b>0xFFFFFFFF *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	ETR mode 1

###### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

###### Trigger:

Trigger Polarity	Rising Edge
Trigger Filter (4 bits value)	0

### 7.14. TIM9

#### Channel1: PWM Generation CH1

#### Channel2: PWM Generation CH2

##### 7.14.1. Parameter Settings:

###### Counter Settings:

Prescaler (PSC - 16 bits value)	<b>44 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>999 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

###### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

#### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## **7.15. USART1**

### **Mode: Asynchronous**

#### **7.15.1. Parameter Settings:**

##### **Basic Parameters:**

Baud Rate	<b>9600 *</b>
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

**\* User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA7	ADC1_IN7	Analog mode	No pull-up and no pull-down	n/a	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC0	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

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Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB5	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PB6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	<b>Very High</b> *	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	<b>Very High</b> *	
LTDC	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA4	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB10	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC6	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC7	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA11	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC10	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High</b> *	
TIM2	PA15	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
TIM3	PB4	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PA0/WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM9	PE5	TIM9_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High *</b>	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	<b>Very High *</b>	
GPIO	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED

## 8.2. DMA configuration

nothing configured in DMA service

### 8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
FMC global interrupt	unused		
TIM5 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		
LTDC global interrupt	unused		
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		

\* User modified value

## 9. Predefined Views - Category view : Current

### Middleware

#### System Core

#### Analog

#### Timers

#### Connectivity

#### Multimedia

#### Security

#### Computing

DMA

ADC1 

TIM2 

FMC 

DMA2D 

GPIO 

TIM3 

I2C3 

LTDC 

NVIC 

TIM4 

SPI5 

RCC 

TIM5 

USART1 

SYS 

TIM9 



## ***10. Software Pack Report***