# CprE 3810, Computer Organization and

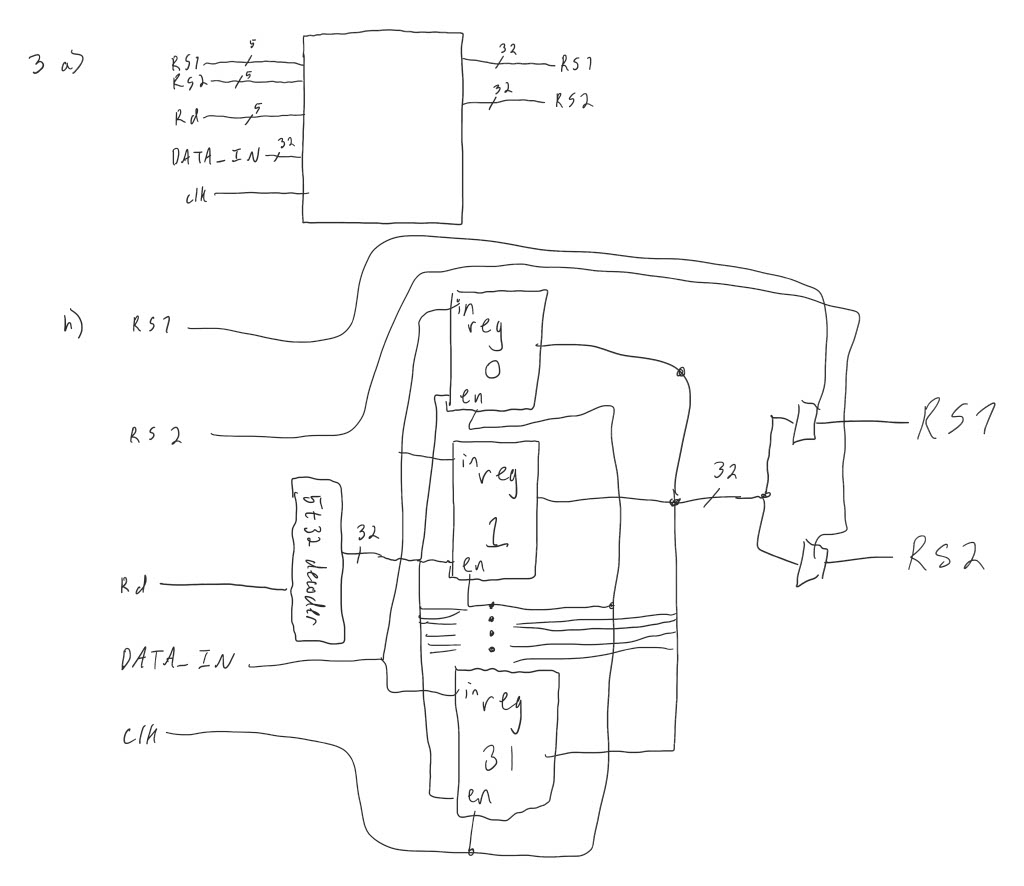
# Assembly-Level Programming

# Lab 2 Report

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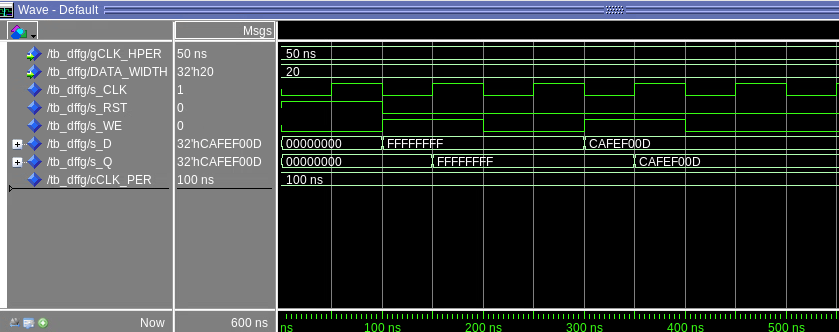
***Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the lab document for the context of the following questions****.*

[Part 3 (a)] Draw the interface description (i.e., the “symbol” or high-level blackbox) for the RISC-V register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?



[Part 3 (b)] Create an N-bit register using this flip-flop as your basis.

[Part 3 (c)] Waveform.



[Part 3 (d)] What type of decoder would be required by the RISC-V register file and why?

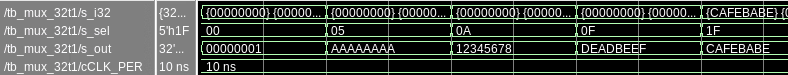
5 to 32 decoder because you need 32 inputs to enable writing to the 32 32-bit registers.

[Part 3 (e)] Waveform.

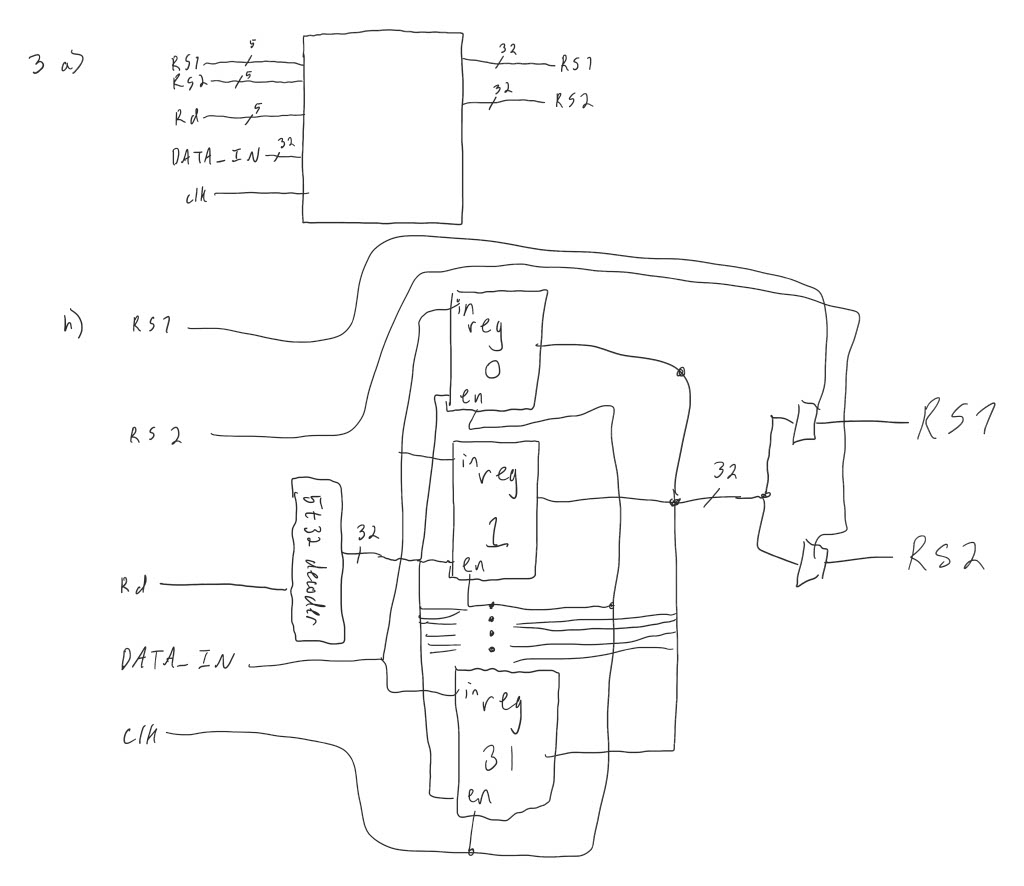


[Part 3 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

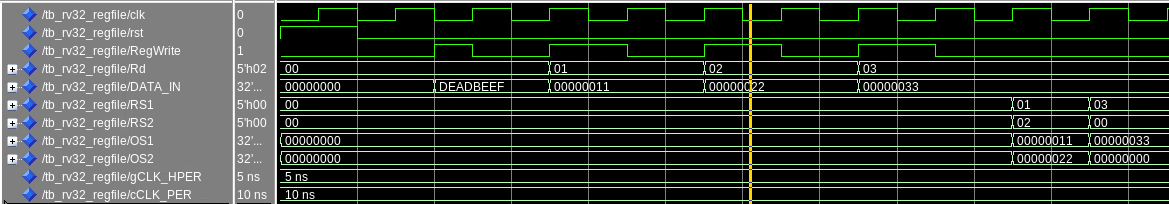
[Part 3 (g)] Waveform.



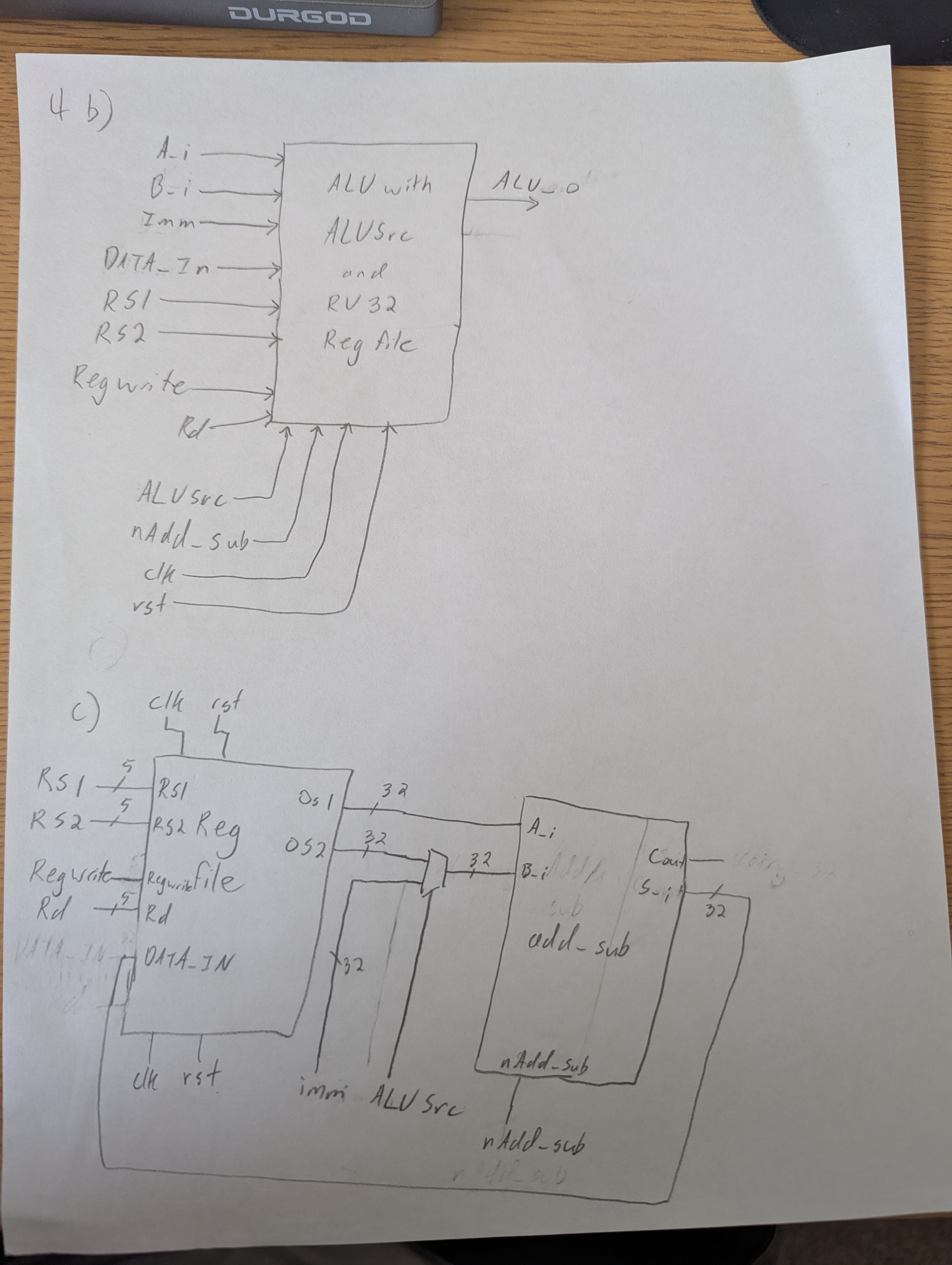
[Part 3 (h)] Draw a (simplified) schematic (i.e., components within the high-level blackbox) for the RISC-V register file, using the same top-level interface ports as in your solution describe above and using only the register, decoder, and mux VHDL components you have created.



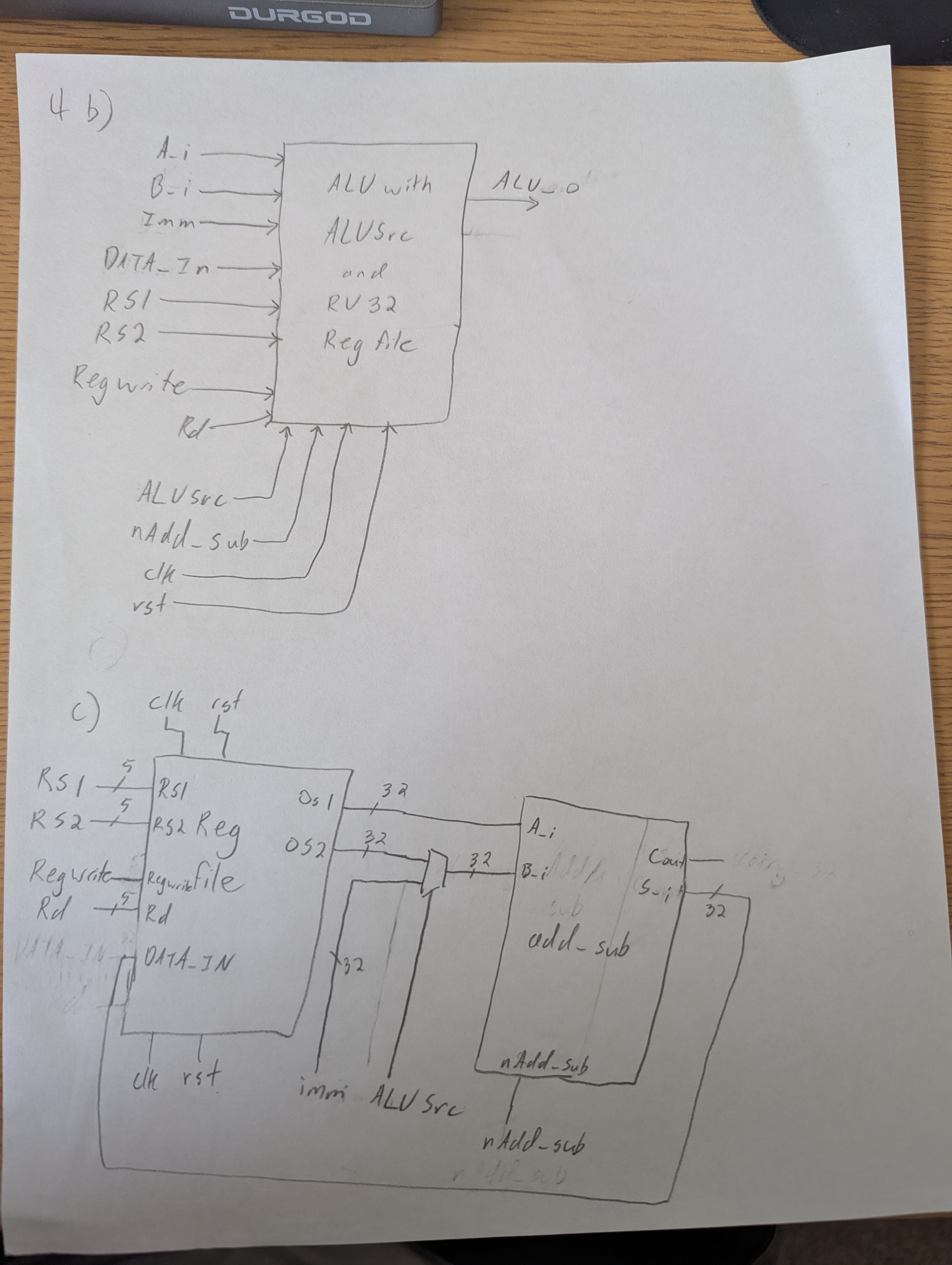
[Part 3 (i)] Waveform.



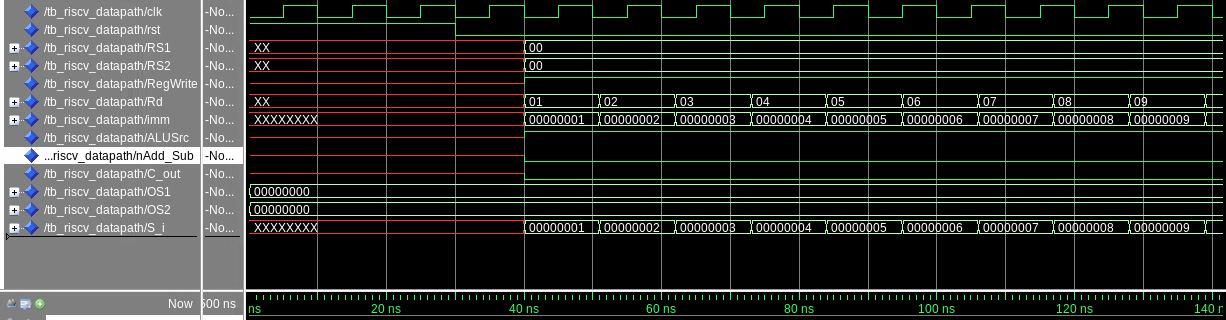
[Part 4 (b)] Draw a symbol for this RISC-V-like datapath.

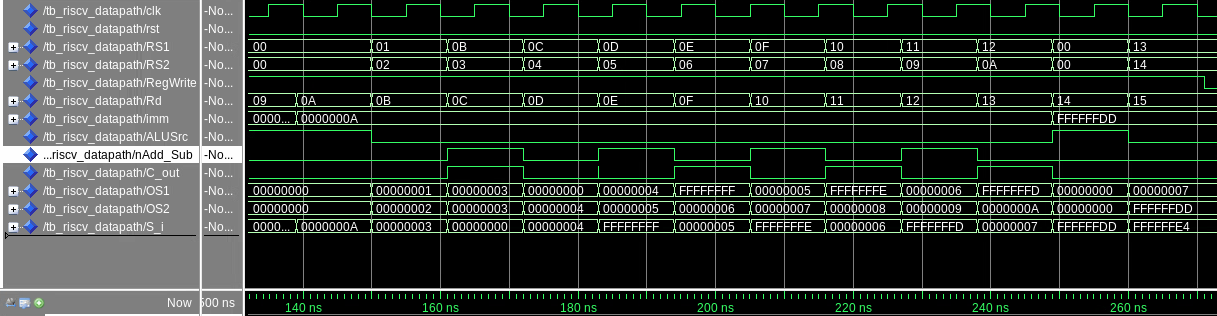


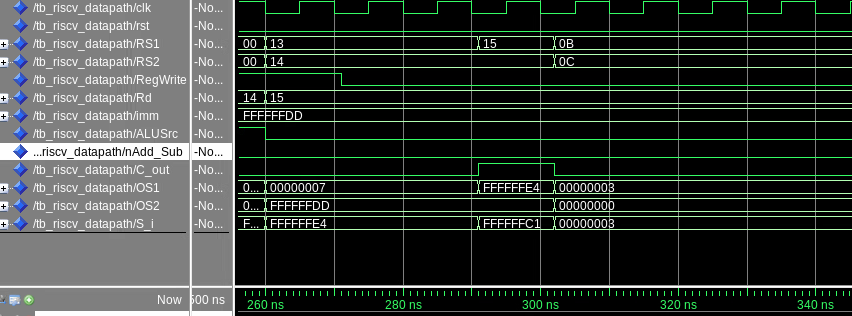
[Part 4 (c)] Draw a schematic of the simplified RISC-V processor datapath consisting only of the component described in part (a) and the register file from problem (1).



[Part 4 (d)] Include in your report waveform screenshots that demonstrate your properly functioning design. Annotate what the final register file state should be.







Register mapping

| Reg # | Name | ABI role |
| --- | --- | --- |
| x0 | zero | Constant 0 |
| x1 | ra | Return address |
| x2 | sp | Stack pointer |
| x3 | gp | Global pointer |
| x4 | tp | Thread pointer |
| x5 | t0 | Temp 0 |
| x6 | t1 | Temp 1 |
| x7 | t2 | Temp 2 |
| x8 | s0/fp | Saved/frame |
| x9 | s1 | Saved |
| x10 | a0 | Arg 0 / ret 0 |
| x11 | a1 | Arg 1 / ret 1 |
| x12 | a2 | Arg 2 |
| x13 | a3 | Arg 3 |
| x14 | a4 | Arg 4 |
| x15 | a5 | Arg 5 |
| x16 | a6 | Arg 6 |
| x17 | a7 | Arg 7 |
| x18 | s2 | Saved |
| x19 | s3 | Saved |
| x20 | s4 | Saved |
| x21 | s5 | Saved |
| … | … | (x22–x31 continue) |

Final state

| Reg | Name | Final Value |
| --- | --- | --- |
| x0 | zero | 0 (always) |
| x1 | ra | 1 |
| x2 | sp | 2 |
| x3 | gp | 3 |
| x4 | tp | 4 |
| x5 | t0 | 5 |
| x6 | t1 | 6 |
| x7 | t2 | 7 |
| x8 | s0 | 8 |
| x9 | s1 | 9 |
| x10 | a0 | 10 |
| x11 | a1 | 3 |
| x12 | a2 | 0 |
| x13 | a3 | 4 |
| x14 | a4 | -1 |
| x15 | a5 | 5 |
| x16 | a6 | -2 |
| x17 | a7 | 6 |
| x18 | s2 | -3 |
| x19 | s3 | 7 |
| x20 | s4 | -35 |
| x21 | s5 | -28 |
| x22–x31 | — | unchanged / undefined |

[Part 5 (a)] Read through the mem.vhd file, and based on your understanding of the VHDL implementation, provide a 2-3 sentence description of each of the individual ports (both generic and regular).

DATA\_WIDTH is the size of the data that can be store in the registers. It is set to 32, the same size as a word, by default.

ADDR\_WIDTH is the size of the memory addresses for the register. Since this is set to 10 by default, that means that there are 2^10 registers or 1024 words.

Clk is the clock, it is required for updating the registers.

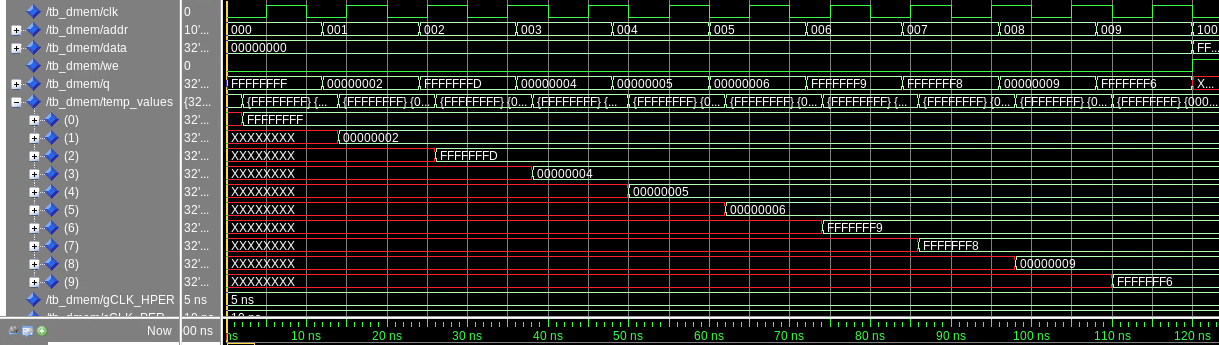
Addr is the address selector. It selects with word in memory we want to write to.

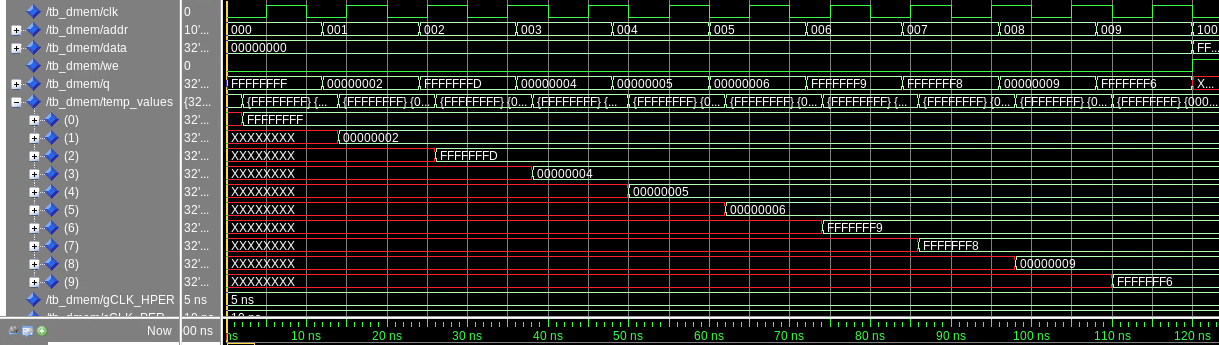
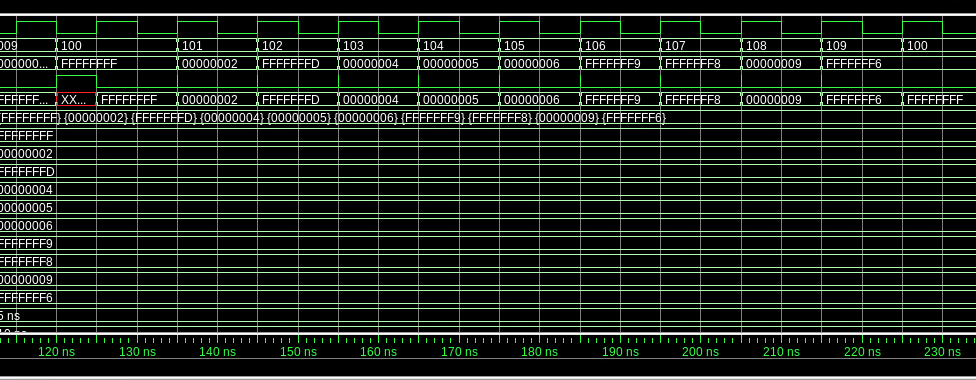
Data is the input bus of what we want to write to the word in memory.

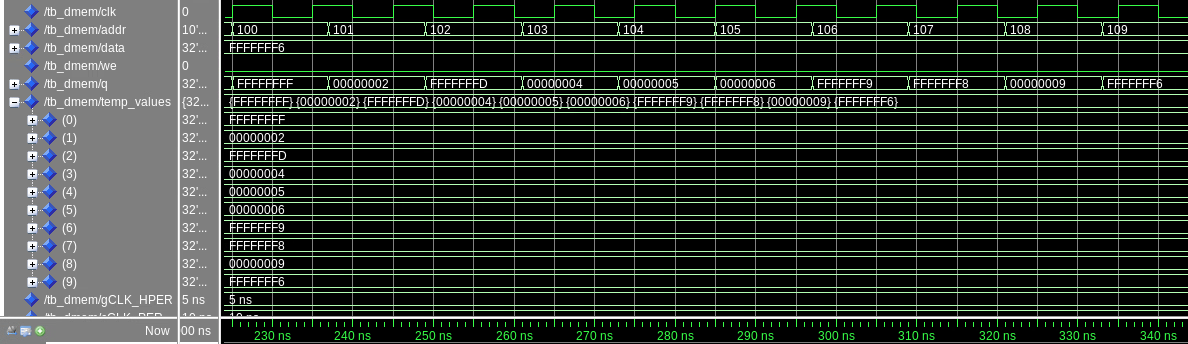
We is the write enable signal. It allows the memory to be changed.

Q is the output databus, it selected what is to be read from memory.

[Part 5 (c)] Waveforms.







[Part 6 (a)] What are the RISC-V instructions that require some value to be sign extended? What are the RISC-V instructions that require some value to be zero extended?

The RISC-V instructions that need to be sign extended are arithmetic immediates, loads, stores, branches, jump and links, and upper immediates. The instructions that require some values to be zero extended are unsinged ones like shift imeediate instructions and unsinged loads.

[Part 6 (b)] what are the different 12-bit to 32-bit “extender” components that would be required by a RISC-V processor implementation?

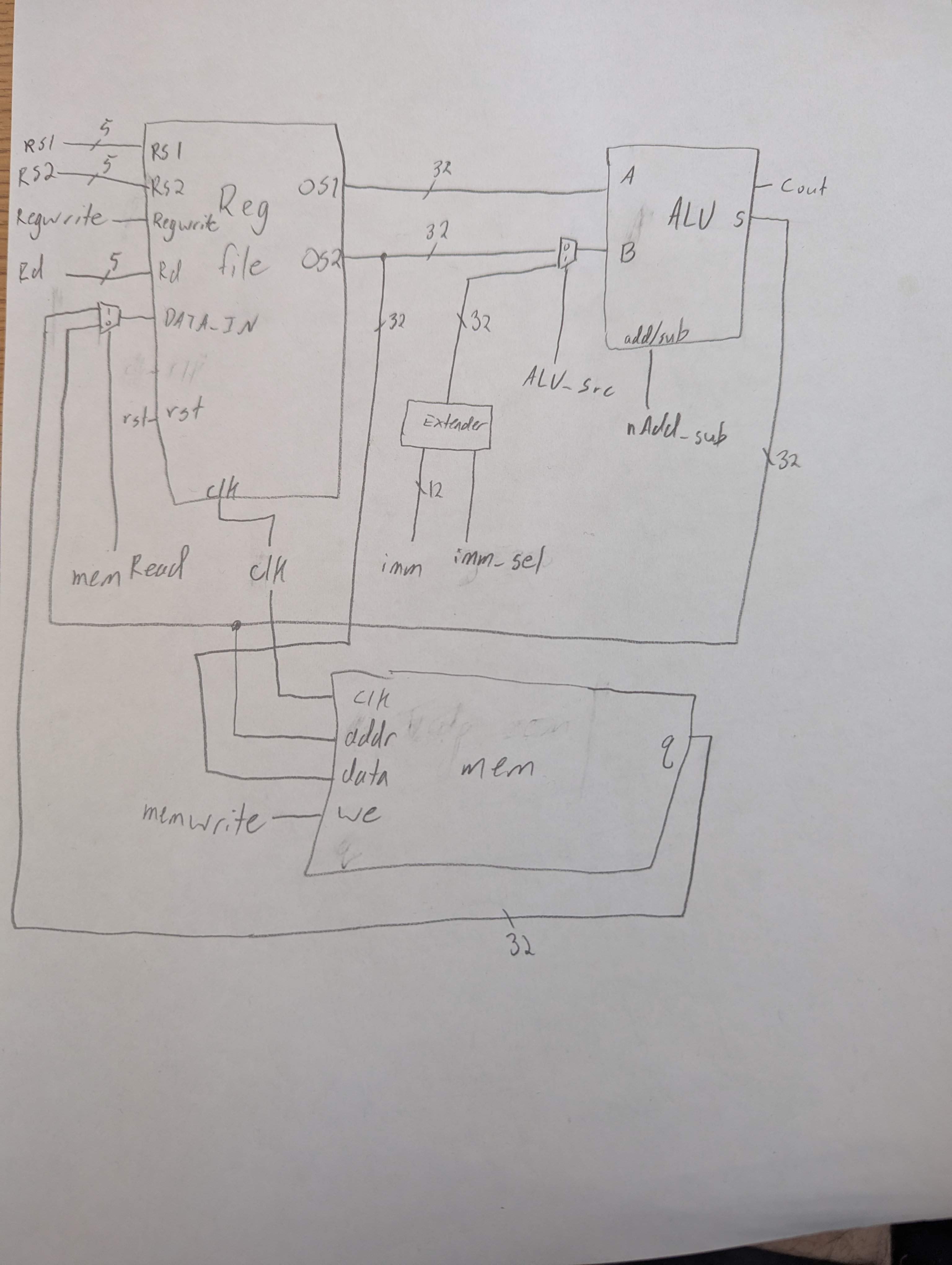
The different 12-bit to 32-bit extender components depend on the how the 12-bit immediate field is interpreted. The first component would be the sign extended that in the 12-bit immediate, would take the most significant digit and repeat it until you get 32 bits. This would be for I-type immediates and S-type offsets. Then the next component would be a zero extender component. This component would take the zero extended instructions mentioned in part a and add zeroes to the front.

[Part 6 (d)] Waveform.

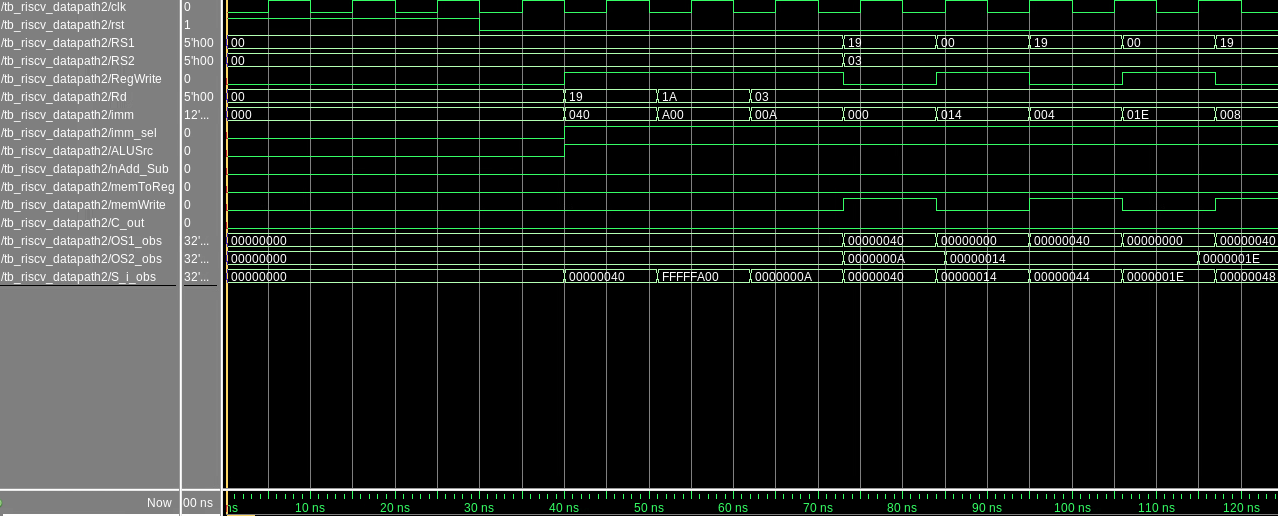


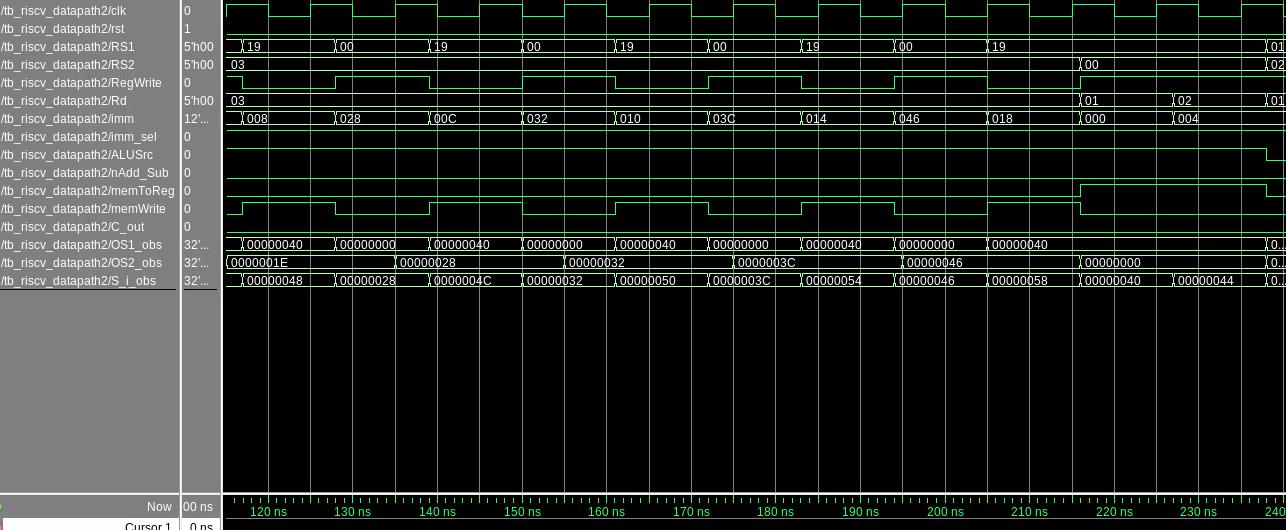
[Part 7 (a)] what control signals will need to be added to the simple processor from part 3? How do these control signals correspond to the ports on the mem.vhd component analyzed in part 4?

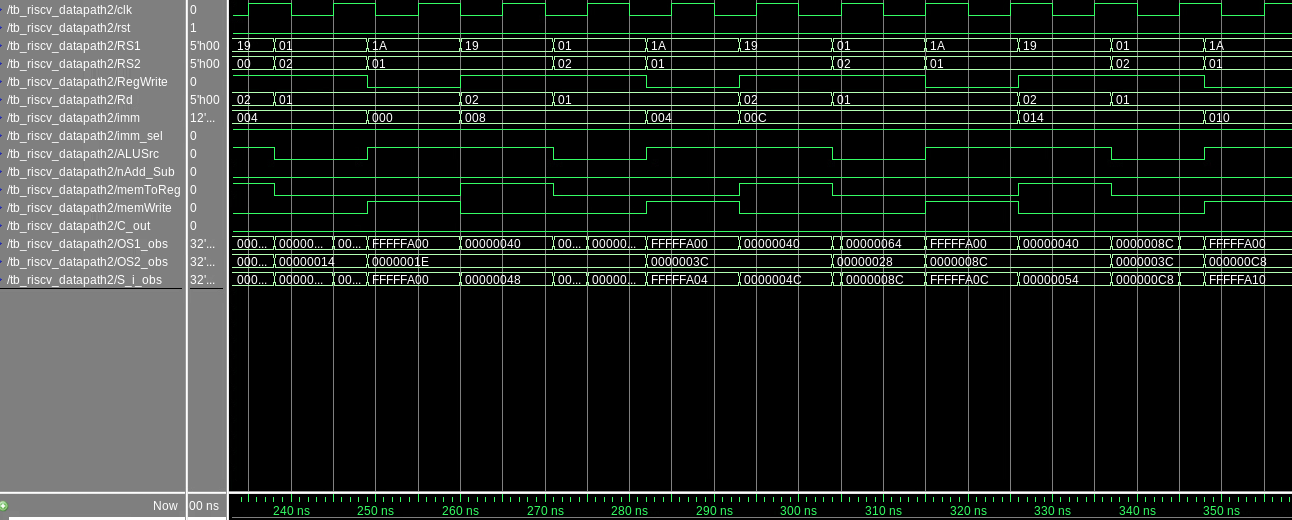
You would need to be a control signal for both the load and store controls, which would likely be hooked to a mux to control if the writing goes to the memory or registers. These correspond to the we and q prorts in part 4. Specifically, we controls store and q controls load. Although, q always loads to the given address.

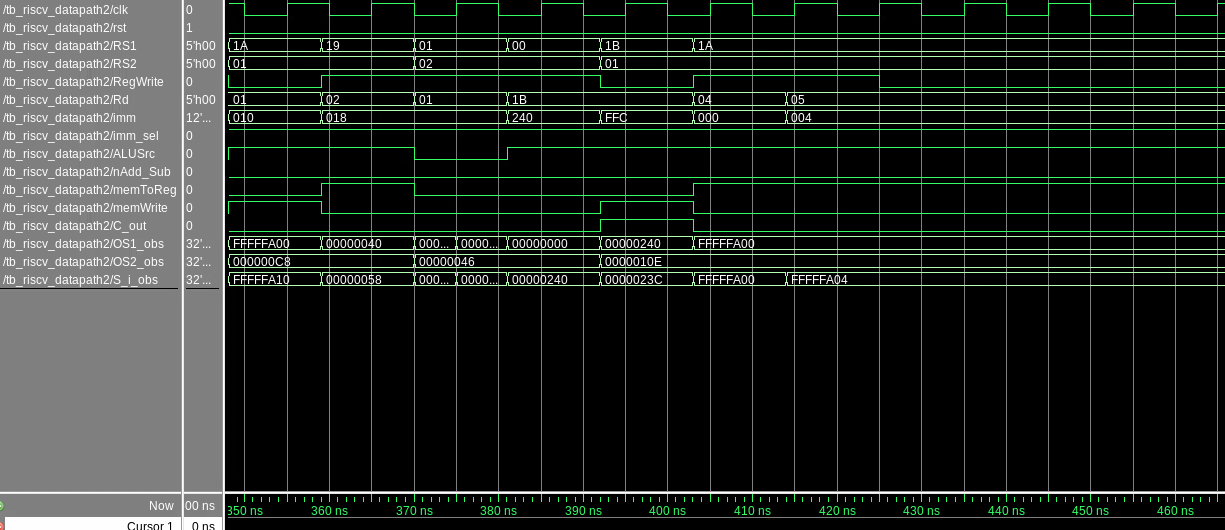
[Part 7 (b)] Draw a schematic of a simplified RISC-V processor consisting only of the base components used in part 2, the extender component described in part 4, and the data memory from part 3.

[Part 7 (c)] Waveform.









Final registers state

| Reg | Name | Final Value |
| --- | --- | --- |
| x0 | zero | 0 |
| x1 | ra | 230 |
| x2 | sp | 70 (last value loaded from A[6]) |
| x3 | gp | last imm written in preload loop = 70 |
| x4 | tp | 30 (B[0]) |
| x5 | t0 | 60 (B[1]) |
| x25 | s9 | 64 (base of A) |
| x26 | s10 | 320 (base of B) |
| x27 | s11 | 576 (base of B+64) |

Other registers are 0/undef