# CprE 3810, Computer Organization and

# Assembly-Level Programming

# Lab 2 Report

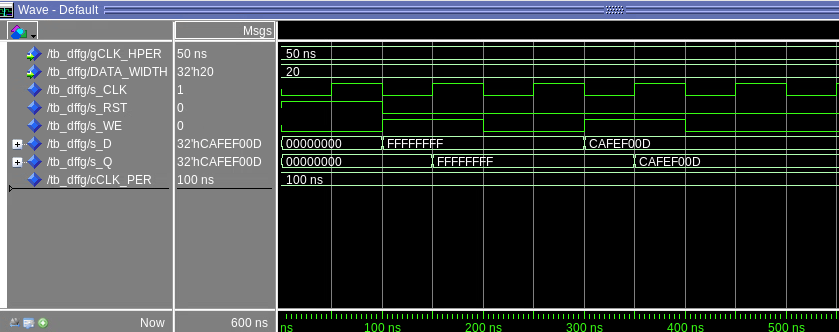
Student Name \_\_\_\_Zephaniah Gustafson\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

***Submit a typeset pdf version of this on Canvas by the due date. Refer to the highlighted language in the lab document for the context of the following questions****.*

[Part 3 (a)] Draw the interface description (i.e., the “symbol” or high-level blackbox) for the RISC-V register file. Which ports do you think are necessary, and how wide (in bits) do they need to be?

[Part 3 (b)] Create an N-bit register using this flip-flop as your basis.

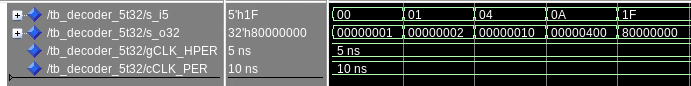
[Part 3 (c)] Waveform.



[Part 3 (d)] What type of decoder would be required by the RISC-V register file and why?

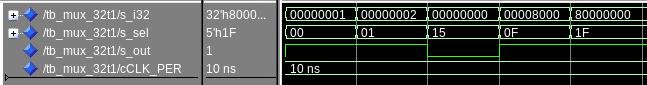
5 to 32 decoder because you need 32 inputs to enable writing to the 32 32-bit registers.

[Part 3 (e)] Waveform.



[Part 3 (f)] In your write-up, describe and defend the design you intend on implementing for the next part.

[Part 3 (g)] Waveform.



[Part 3 (h)] Draw a (simplified) schematic (i.e., components within the high-level blackbox) for the RISC-V register file, using the same top-level interface ports as in your solution describe above and using only the register, decoder, and mux VHDL components you have created.

[Part 3 (i)] Waveform.

[Part 4 (b)] Draw a symbol for this RISC-V-like datapath.

[Part 4 (c)] Draw a schematic of the simplified RISC-V processor datapath consisting only of the component described in part (a) and the register file from problem (1).

[Part 4 (d)] Include in your report waveform screenshots that demonstrate your properly functioning design. Annotate what the final register file state should be.

[Part 5 (a)] Read through the mem.vhd file, and based on your understanding of the VHDL implementation, provide a 2-3 sentence description of each of the individual ports (both generic and regular).

[Part 5 (c)] Waveforms.

[Part 6 (a)] What are the RISC-V instructions that require some value to be sign extended? What are the RISC-V instructions that require some value to be zero extended?

[Part 6 (b)] what are the different 16-bit to 32-bit “extender” components that would be required by a RISC-V processor implementation?

[Part 6 (d)] Waveform.

[Part 7 (a)] what control signals will need to be added to the simple processor from part 2? How do these control signals correspond to the ports on the mem.vhd component analyzed in part 3?

[Part 7 (b)] Draw a schematic of a simplified RISC-V processor consisting only of the base components used in part 2, the extender component described in part 4, and the data memory from part 3.

[Part 7 (c)] Waveform.