

Features:

- 64-bit timer with 12-bit prescaler and 8-bit step register
- Compliant with RISC-V privileged specification v1.11
- Configurable number of timers per hart and number of harts
- Can be used with APB (Advanced Peripheral Bus) or TL-UL (Tile link).

Block Diagram:

Hardware interface

Signal Name	Width	Direction	Description
clk_i	1 bit	input	Primary clock
rst_ni	1 bit	input	Active low asynchronous reset
reg_we	1 bit	input	Write enable signal
reg_re	1 bit	input	Read enable signal
reg_addr	9 bit	input	Address for read/write
reg_wdata	32 bit	input	Register write data
reg_be	4 bit	input	Byte selection bits for Write
reg_rdata	32 bit	output	Read data
reg_error	1 bit	output	Error indication
intr_timer_expired_0_0_o	1 bit	output	Interrupt signal

Programmers Guide:

Initialization

The software should configure the step and prescaler bits before enabling the timer control in order to correctly increment the timer value. If software wants to change step or prescaler it should first disable the timer by writing 0x0 to CTRL register and then it can change the step and prescaler by changing the CFG register. The first step should always be to disable the timer by writing 0x0 to the timer CTRL register. Secondly the CFG register should be modified to the desired prescaler and step value. Now the timer compare value should be written to the CMP_LOWER as well as CMP_UPPER if UPPER. If a programmer needs to use only the first 32 bits then you must set the upper 32 bits of the CMP register to 0x0. Moving forward now the CTRL register needs to be written 0x1 in order to activate the timer to start the counter. Now if the programmer needs to reset the timer can do it by activating the hardware reset pin. If there

<p align="center">rv_timer.INTR_TEST0 @0x11c</p> <p align="center">Interrupt test register</p> <p align="center">Reset Default = 0x0,mask 0x1</p>															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															T_0
Bits	Type	Reset	Name			Description									
0	wo	x	T_0			Interrupt test for timer									

rv_timer.INTR_ENABLE0 @0x114															
Interrupt Enable															
Reset Default = 0x0,mask 0x1															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															IE_0
Bits	Type	Reset	Name			Description									
0	rw	0x0	IE_0			Interrupt Enable for timer									

rv_timer.COMPARE_UPPER_0 @0x110															
Timer Value Upper															
Reset Default = 0xffffffff,mask 0xffffffff															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
upper compare value															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
upper compare value															
Bits	Type	Reset	Name	Description											
31:0	rw	0xffffffff	value	Timer compare value[63:32]											

rv_timer.COMPARE_LOWER_0 @0x10c Timer Value lower Reset Default = 0xffffffff,mask 0xffffffff															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
lower compare value															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
lower compare value															
Bits	Type	Reset	Name				Description								
31:0	rw	0xffffffff	value				Timer compare value[31:0]								

