Timer

Registers

- Timer register
- Compare register
- Prescaler / Control Register

Timer Register

- It is basically a counter register which is provided the clk generated by prescaler. if prescaler is enabled with some value otherwise direct PCLK is connected to it.

Compare register

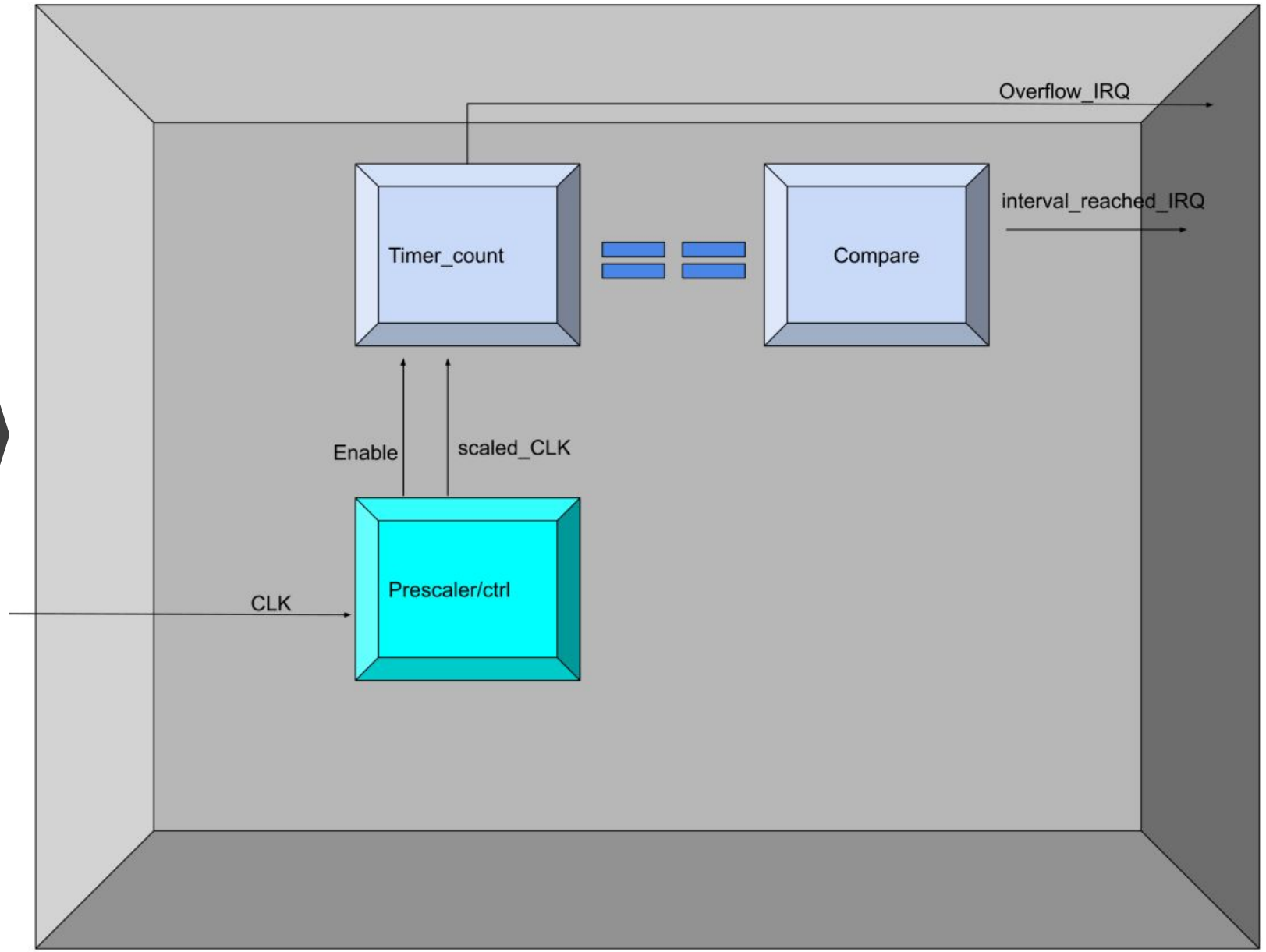
- It contains the value which will be compared with timer register if both are equal then an interrupt will be generated.

Prescaler / Control register

- It is a register which contains some prescaler bits as well as an enable bit. It simply enable / disable the timer based on the value of zeroth bit. ctrl_reg[0] = 0 or ctrl_reg[0] = 1. 0 = disable , 1 = enable.

- In this timer the prescaler_value = ctrl_reg[5:3].
- This value is used to divide the clk frequency.
- For this timer if prescaler is 1 and enable bit is also 1 so the clk provided to timer register will be 10 times slower than the PCLK.

BLOCK DIAGRAM



Address and prescaler format

- REG_TIMER 0
- REG_TIMER_CTRL /Prsecaler 1
- REG_CMP 2
- format of :PADDR = {7'd0,index[2:0],2’d0}
- addr => ctrl = 12'd4
- addr => cmp = 12'd8
- addr => timer = 12’d0
- PRESCALER_STARTBIT 3 of reg_timer_ctrl
- PRESCALER_STOPBIT 5 of reg_timer_ctrl
- prescaler format: WDATA = {26'd0,presc_bit[5:3],3’d0}

Prescaler Values

- ctrl = 32'd0 disabled timer no prescaler
- ctrl = 32'd1 enabled timer no prescaler
- ctrl = 32'd8 disabled timer prescaler 1 i.e 10 times larger delay
- ctrl = 32'd9 enabled timer prescaler 1 i.e 10 times lager delay
- ctrl = 32'd16 disabled timer prescaler 2 i.e 20 times greater delay
- ctrl = 32'd17 enabled timer prescaler 2 i.e 20 times greater delay
- ctrl = 32'd24 disabled timer prescaler 3 i.e 30 times greater delay
- ctrl = 32'd25 enabled timer prescaler 3 i.e 30 times greater delay
- ctrl = 32'd32 disabled timer prescaler 4 i.e 40 times greater delay
- ctrl = 32'd33 enabled timer prescaler 4 i.e 40 times greater delay
- ctrl = 32'd40 disabled timer prescaler 5 i.e 50 times greater delay
- ctrl = 32'd41 enabled timer prescaler 5 i.e 50 times greater delay
- ctrl = 32'd48 disabled timer prescaler 6 i.e 60 times greater delay
- ctrl = 32'd49 enabled timer prescaler 6 i.e 60 times greater delay
- ctrl = 32'd56 disabled timer prescaler 7 i.e 70 times greater delay
- ctrl = 32'd57 enabled timer prescaler 7 i.e 70 times greater delay

Specs

- to set prescaler we have to write on REG_TIMER_CTRL
- to set timer we have to write on REG_CMP
- irq_o[0] == overflow interrupt when REG_Timer == 32’hFFFF_FFFF
- irq_o[1] == time reached interrupt
- zeroth bit of reg timer ctrl is ENABLE BIT
- if you set value 1 in cmp register then you will receive interrupt after every clock cycle
- if you set value 1 in cmp register and 1 value in prescaler bits then you will receive interrupt after every 10 clock cycles
- Conclusion prescaler value 1 will slow down the clock ten times and normal number of cycle-based delay will be given by value of compare register you set.

Delay time calculation

- max value through cmp register = 4294967295 clks
- delay_time = time_of_one_clk*(cmp value * prescaler_value)
- Max delay_time = time_of_one_clk*(4294967295*70)
- = time_of_one_clk*(300647710650)

Ports

- input HCLK 1 bit
- input HRESETn 1 bit
- input PADDR 12 bits
- input PWDATA 32 bits
- input PWRITE 1 bit
- input PSEL 1 bit
- input PENABLE 1 bit
- output PRDATA 32 bits
- output PREADY 1 bit
- output PSLVERR 1 bit
- output irq_o 2 bits

Thank you