PWM peripheral IP

Features:

- Pulse-width modulated (PWM) with adjustable duty cycle.
- Suitable for general-purpose use.
- Two Independent pwm channels and registers.
- Programmable resolution.
- Different frequency configurations for both PWM outputs.
- All duty cycle settings are independently programmable.
- Both APB and TL-UL interfaces are available.

PROGRAMMER'S GUIDE:

Configurations for using IP:

- In order to use this IP you need to set four configuration parameters through separate write transactions which include. Period, Divisor , Duty Cycle and Control.
- The preferred sequence should be Divisor, Period, Duty Cycle and Control at the end.
- Firstly set the value of the Divisor register by writing @ address 0x4 any number by which you want to divide the input clk and want your PWM from that clk

  Note: if you set the Divisor 2 the effective clk frequency will be

  $F_{effclk} = F_{inclk} / 2.$

  Where,

  F_{effclk} is an effective clk which will be responsible for generation of PWM.

  F_{inclk} is input clk frequency.

- Now set the Period of PWM by writing @ address 0x8

  Note: if you set period 2 the frequency of PWM will be

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$$F_{pwm} = F_{effclk} / 2$$

Where,

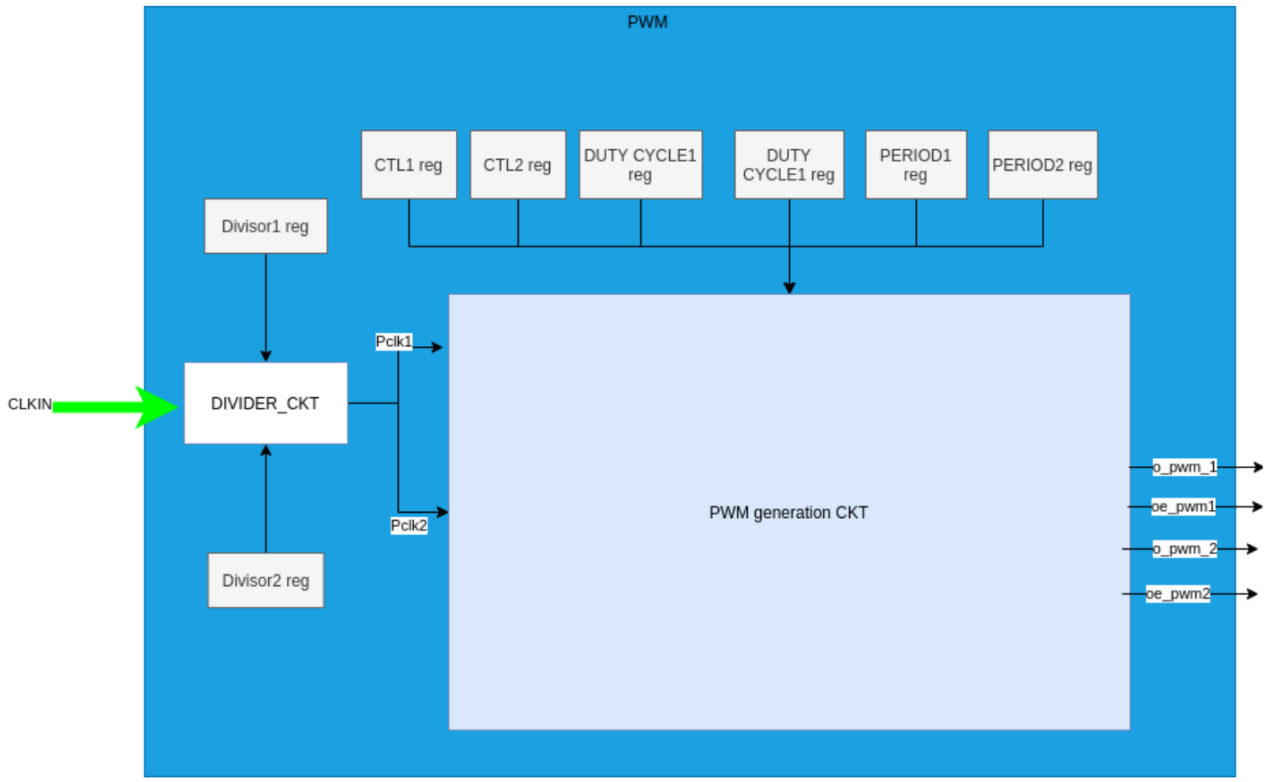
Fpwm is the frequency of pwm output signal.

- Now set the duty cycle by writing @ address 0xC

  Note: for example if period is 100 and duty cycle is 20 so the PWM output will be high for 20 cycles of F_{effclk} will be low for 80 cycles of F_{effclk}.

- At the end when all other parameters are set its time to enable the control so that the PWM signal can be enabled on the output. To enable control write value 0x7 (Binary form 111) @ address 0x0.

BLOCK DIAGRAM:



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PORTS:

Signal Name	Direction	Width	Description
Clk_i	input	1	Input clk
rst_n1	input	1	Active low reset
w_en	input	1	Write enable
rd_en	input	1	Read enable
addr_i	input	ADDR_WIDTH=8	Address input
wdata_i	input	DATA_WIDTH=32	Write data
rdata_o	output	DATA_WIDTH=32	Read data
o_pwm_1	output	1	PWM output 1
o_pwm_2	output	1	PWM output 2
oe_pwm1	output	1	Output valid signal for PWM 1
oe_pwm2	output	1	Output valid signal for PWM 2