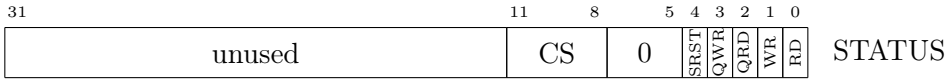
SPI Master

Signal	Direction	Description
`spi_clk`	**output**	Master Clock
`spi_csn0`	**output**	Chip Select 0
`spi_csn1`	**output**	Chip Select 1
`spi_csn2`	**output**	Chip Select 2
`spi_csn3`	**output**	Chip Select 3
`spi_mode[1:0]`	**output**	SPI Mode
`spi_sdo0`	**output**	Output Line 0
`spi_sdo1`	**output**	Output Line 1
`spi_sdo2`	**output**	Output Line 2
`spi_sdo3`	**output**	Output Line 3
`spi_sdi0`	**input**	Input Line 0
`spi_sdi1`	**input**	Input Line 1
`spi_sdi2`	**input**	Input Line 2
`spi_sdi3`	**input**	Input Line 3
`events_o[1:0]`	**output**	Event/Interrupt

STATUS (Status Register)

Address: `0x1A10_2000`
Reset Value: `0x0000_0000`



`Bit 11:8` **CS**: Chip Select.
Specify the chip select signal that should be used for the next transfer.

`Bit 4` **SRST**: Software Reset.
Clear FIFOs and abort active transfers.

`Bit 3` **QWR**: Quad Write Command.
Perform a write using Quad SPI mode.

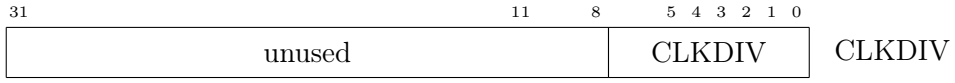
`Bit 2` **QRD**: Quad Read Command.
Perform a read using Quad SPI mode.

`Bit 1` **WR**: Write Command.
Perform a write using standard SPI mode.

`Bit 0` **RD**: Read Command.
Perform a read using standard SPI mode.

CLKDIV (Clock Divider)

Address: `0x1A10_2004`
Reset Value: `0x0000_0000`



`Bit 7:0` **CLKDIV**: Clock Divider.
Clock divider value used to divide the SoC clock for the SPI transfers. This register should not be modified while a transfer is in progress.

SPICMD (SPI Command)

Address: `0x1A10_2008`
Reset Value: `0x0000_0000`

`Bit 31:0` **SPICMD**: SPI Command.
When performing a read or write transfer the SPI command is sent first before any data is read or written. The length of the SPI command can be controlled with the `SPILEN` register.

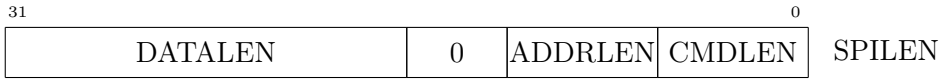
SPIADR (SPI Address)

Address: `0x1A10_200C`
Reset Value: `0x0000_0000`

`Bit 31:0` **SPIADR**: SPI Address.
When performing a read or write transfer the SPI command is sent first before any data is read or written, after this the SPI address is sent. The length of the SPI address can be controlled with the `SPILEN` register.

SPILEN (SPI Transfer Length)

Address: `0x1A10_2010`
Reset Value: `0x0000_0000`



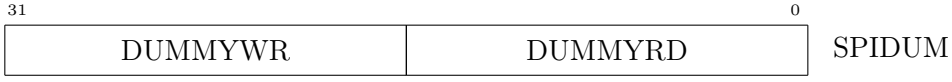
`Bit 31:16` **DATALEN**: SPI Data Length.
The number of bits read or written. Note that first the SPI command and address are written to an SPI slave device.

`Bit 13:8` **ADDRLEN**: SPI Address Length.
The number of bits of the SPI address that should be sent.

`Bit 5:0` **CMDLEN**: SPI Command Length.
The number of bits of the SPI command that should be sent.

SPIDUM (SPI Dummy Cycles)

Address: `0x1A10_2014`
Reset Value: `0x0000_0000`

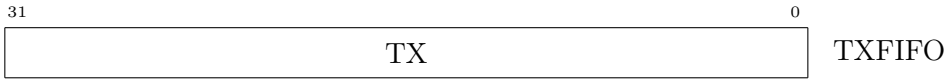


`Bit 31:16` **DUMMYWR**: Write Dummy Cycles.
Dummy cycles (nothing being written or read) between sending the SPI command + SPI address and writing the data.

`Bit 15:0` **DUMMYRD**: Read Dummy Cycles.
Dummy cycles (nothing being written or read) between sending the SPI command + SPI address and reading the data.

TXFIFO (SPI Transmit FIFO)

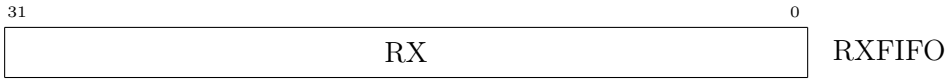
Address: `0x1A10_2018`
Reset Value: `0x0000_0000`



`Bit 31:0` **TX**: Transmit Data.
Write data into the FIFO.

RXFIFO (SPI Receive FIFO)

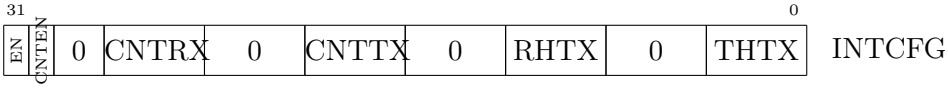
Address: `0x1A10_2020`
Reset Value: `0x0000_0000`



`Bit 31:0` **RX**: Receive Data.
Read data from the FIFO.

INTCFG (Interrupt Configuration)

Address: `0x1A10_2024`
Reset Value: `0x0000_0000`



`Bit 31` **EN**: Interrupt Enable.
Enable interrupts