DS - SLP - 2021 - 2022

10 pts

Exercice 2 (03 → 35)

décompteur modulo 6 :

1)

Clk	Q_2	Q_1	Q_0	D_2	D_1	D_0
↑	0	0	0	1	0	1
	0	0	1	0	0	0
	0	1	0	0	0	1
	0	1	1	0	1	0
	1	0	0	0	1	1
	1	0	1	1	0	0

1 pt

Q_2Q_1 \ Q_0	0	1
00	1	0
01	1	0
11	–	–
10	1	0

$D_0 = \overline{Q_0}$ (0,5)

Q_2Q_1 \ Q_0	0	1
00	0	0
01	0	1
11	–	–
10	1	0

$D_1 = Q_2\overline{Q_0} + Q_1Q_0$ (0,5)

Q_2Q_1 \ Q_0	0	1
00	1	0
01	0	0
11	–	–
10	0	1

$D_2 = Q_2Q_1 + \overline{Q_2}Q_1\overline{Q_0}$ (0,5)

2)

Q_2	Q_1	Q_0	S_5	S_4	S_3	S_2	S_1	S_0
0	0	0					1	
0	0	1				1		
0	1	0			1			
0	1	1		1				
1	0	0	1					
1	0	1		1				

1

$S_0 = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}$

$S_1 = Q_0\,\overline{Q_1}\,\overline{Q_2}$

$S_2 = \overline{Q_0}\,Q_1\,\overline{Q_2} = \overline{Q_0}\,\overline{Q_1 + Q_2}$

$S_3 = Q_0Q_1\,\overline{Q_2}$

$S_4 = \overline{Q_0}\,Q_1Q_2$

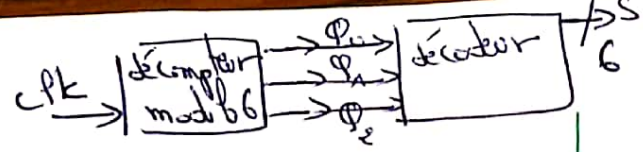
$S_5 = Q_0\,\overline{Q_1}\,Q_2$

1,5

GAL22V10 : GAL 22V10

circuit generic array logic contenant 22E/S dont 10 sorties versatiles basé sur la technologie CMOS effaçable (0,5)

combinatoire (1,5) + 1 pts séq / + croix 1 pt (1)



- library ieee;
use ieee.std_logic_1164.all;
entity decomp_deco is
port(clk : in std_logic;
S : out std_logic_vector(5 downto 0));
end decomp_deco;
architecture arch_decomp_deco of
decomp_deco is
signal Q : std_logic_vector(2 downto 0);
begin
Q <= "000";
Process(clk)
begin
if rising_edge(clk) and Q <= "10" then
Q <= Q - 1;
end if;
end process;
S(0) <= not(Q(0)) and not(Q(1)) and not(Q(2));
S(1) <= Q(0) and not(Q(1)) and not(Q(2));
S(2) <= not(Q(0)) and Q(1) and not(Q(2));
S(3) <= Q(0) and Q(1) and not(Q(2));
S(4) <= not(Q(0)) and not(Q(1)) and Q(2);
S(5) <= Q(0) and not(Q(1)) and Q(2);
end arch_decomp_deco_comp;

1)

V	r_{i-1}	b_i	a_i	S_i	r_i	
0	0	0	0	0	0	Additionneur
0	0	0	1	1	0	
0	0	1	0	1	0	
0	0	1	1	0	1	
0	1	0	0	1	0	
0	1	0	1	0	1	
0	1	1	0	0	1	
0	1	1	1	1	1	
1	0	0	0	0	0	Soustracteur
1	0	0	1	1	0	
1	0	1	0	1	1	
1	0	1	1	0	0	
1	1	0	0	1	1	
1	1	0	1	0	0	
1	1	1	0	0	1	
1	1	1	1	1	1	

2pt

2)