Start & Stop

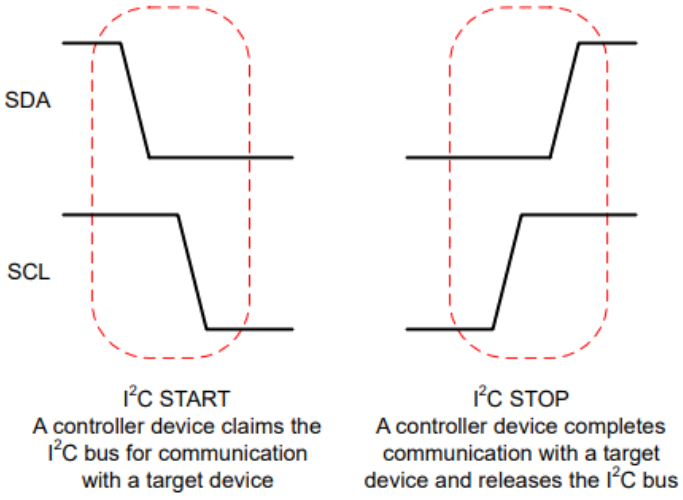
Saturday, November 15, 2025 4:08 PM

Start

- Controllers claim the bus by sending an "I2C Start." The controller pulls SDA low, THEN SCL low.

Stop

- With communication over, SCL is released, THEN SDA.



I²C START
A controller device claims the I²C bus for communication with a target device

I²C STOP
A controller device completes communication with a target device and releases the I²C bus

Interpreting Data Bits

- Logical one happens when SDA is high (released) and SCL is high.
  Logical zero happens when SDA is low (pulled) and SCL is high.

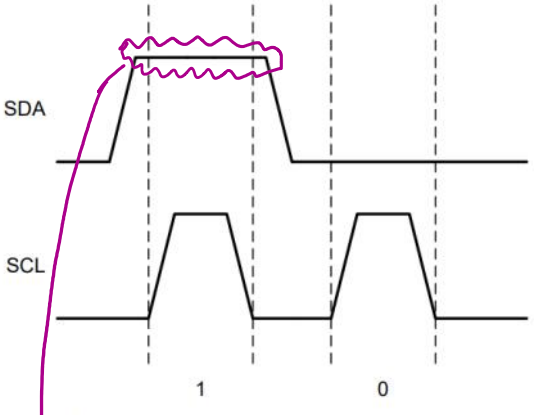


Figure 3-2. I²C Digital One and Zero Representations

If this changes while SCL is high, that's an invalid bit and might even be perceived as a START or STOP condition.