Communication Frames

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- After a controller initiates START, communication begins with the controller sending an address frame. From there, data frames can now be sent.

- Each data frame also has an acknowledge bit which is how the slave tells the controller that the message has been received.

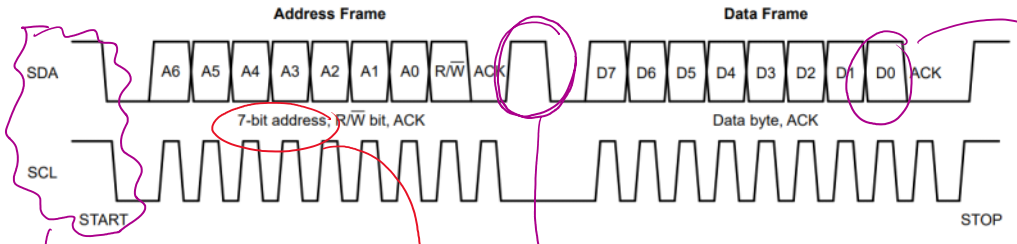

Figure 3-3. I²C Address and Data Frames

It's simultaneously low and high to indicate it can be 0 or 1.

Controller claims bus

Remember controller releases SDA during Ack to let the slave pull it down, so after slave releases, no one's pulling it LOW so it goes high

Every I2C device has a unique address and consists of 7-bits.

Address Frames

- 7 bits implies 128 unique addresses, but there are reserved addresses.

- If the Read-Write (R/$\overline{W}$) bit is 1, the controller wants to read data from the target. If 0, the controller wants to write to the target.

- The acknowledge bit is used to verify successful communication. The target pulls SDA down to GND (0) while SCL is high to indicate the message was received.
  - Thus if SDA is still high, communicate was unsuccessful (NACK – no acknowledgement).

Data Frames

- Data is sent one byte at a time with each byte having an ACK bit.

* If the controller is reading (R/$\overline{W}$ = 1), the controller pulls SDA low to acknowledge data has been received. If 0, the target pulls SDA low.

Acknowledge Bit

Completion

- When finished, the controller issues an I2C STOP → SCL released, then SDA released

Reserved Addresses

Table 5-1. List of Reserved I²C Addresses

Target Address	R/$\overline{W}$ Bit	Description
000 0000	0	General call address
000 0000	1	START byte
000 0001	X	C-Bus address
000 0010	X	Reserved for different bus format
000 0011	X	Reserved for future purposes
000 01XX	X	Hs-mode controller code
111 11XX	1	Device ID
111 10XX	X	10-bit target address

General Call

- Addresses all devices connected to the bus.