Tackling Bus Capacitance

Saturday, November 15, 2025 4:08 PM

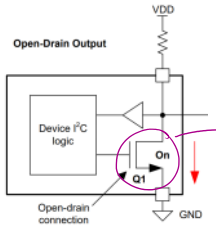
How can we tackle bus capacitance and the slow passive rise-time it causes?

Adjusting Pullup Resistance ($\tau = RC$)

- As mentioned in the "Bus Capacitance" notes, reducing the size of the pullup resistor will reduce τ, and thus the line rise time at the expense of higher power consumption.

* There is one other consideration to make besides higher power consumption. If we have a lower pullup resistance, we must also be capable of sinking that larger current to ground.

  - Recall the diagram from the "Connection" notes which depicted an NMOS connecting the I2C device to SDA and SCL:



More important for small pullup resistances because now there's a smaller drop across the resistor, so V_{DS} of the NMOS higher which increases pinchoff

This transistor has limits on what current it can sink because of (pinchoff) limited gate voltage from the I2C controller, small FETs are chosen to make the I2C package smaller thus the substrate is physically smaller in width and limits current. The NMOS also has thermal limits.

Using I2C Buffers/Repeaters

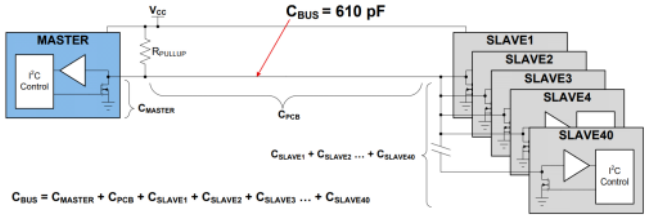


Figure 8. Example I²C System that Includes Capacitance on the Bus due to Master, PCB, and all the Slaves on the Bus

- Say we have a lot of I2C devices connected (40) and a master where each device has 10 pF of capacitance, and our PCB trace has 200 pF of capacitance.

  Since all the slaves and the master are connected in parallel with each other (they all have one node connected to the bus and another connected to GND), their capacitances all add:

  $200\text{ pF} + 41(10\text{ pF}) = 610\text{ pF}$

- The I2C fast-mode spec has a max bus capacitance ($C_{Bus,Max}$) of 400 pF.

- To get around this, we can use a buffer/repeater that splits the capacitance of our devices so that the bus sees 2 separate capacitances that are both lower than the original.

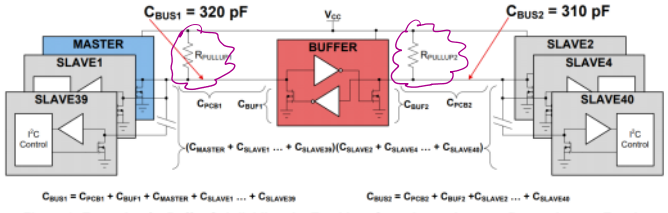


Figure 9. Example of a Buffer Subdividing the Total bus Capacitance into two Buses that are Evenly Distributed

Note: This bus example also accounts for the capacitance of the buffer itself by adding 10 pF to each bus.

- Note we now have 2 separate pullup resistors, one for each bus.

Using I2C Accelerators

- They inject current during rising edges which rapidly charges the capacitance.

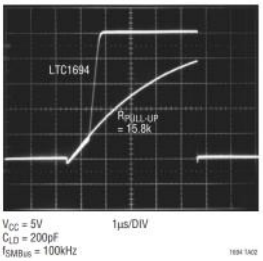
$$I = C\frac{dV}{dt} \rightarrow dV = \frac{1}{C}I\,dt \rightarrow \int dV = \frac{1}{C}\int I\,dt \rightarrow V = \frac{1}{C}I\,\Delta t$$

Quasi-static current assumption (I remember it's used in E&M from Physics of EE)

- They detect the rising edge by first detecting that the bus is LOW, then they monitor the slew rate (dV/dt) to sense a rising edge.
- They stop injecting current when bus voltage reaches some middle-range threshold.

Timing is important, otherwise they might create contention.

Comparison of SMBus Waveforms for the LTC1694 vs Resistor Pull-Up



Reduce Physical Bus Length
- This would reduce any parasitic capacitance from the traces.

Reduce Number of Devices (self-explanatory)