

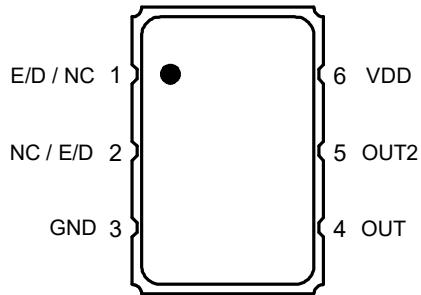
Description

The XU devices are low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types. These devices are designed to operate at three different power supplies and are available in multiple package sizes as well as temperature grades.

With a patented one-time program (OTP) allowing for infinite memory shelf life, the XU devices can be programmed to generate an output frequency from 16kHz to 1500MHz with a resolution as low as 1Hz accuracy. The configuration capability of this family of devices allows for fast delivery times for both sample and large production orders.

Pin Assignments

Note: To minimize power supply line noise, a 0.01 μ F bypass capacitor should be placed between V_{DD} (Pin 6) and GND (Pin 3).



Features

- Frequency range: 0.016MHz to 1500MHz^[1]
- Output types: LVDS, LVPECL, HCSL, LVCMS
- Supply voltage options: 1.8V, 2.5V, or 3.3V
- Phase jitter (1.875MHz to 20MHz): 100fs typical
- Phase jitter (12kHz to 20MHz): 300fs typical
- Package options:
 - 5.0 × 3.2 × 1.2 mm
 - 7.0 × 5.0 × 1.3 mm
- Operating temperature: -20°C to +70°C
 - Frequency stability options: ±20, ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +85°C
 - Frequency stability options: ±25, ±50, or ±100 ppm
- Operating temperature: -40°C to +105°C
 - Frequency stability options: ±50 or ±100 ppm

Table 1. Pin Description

Pin #	Name	Description
1	E/D NC	Enable/Disable ^{[a][b]} No connect
2	NC E/D	No connect Enable/Disable ^{[a][b]}
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output ^[c]
6	V _{DD}	Supply voltage

[a] Pulled high internally = output enabled.

[b] Low = output disabled.

[c] Do not connect for LVCMS. For XLVCMS both OUT and OUT2 are ON and in opposite phase.

See [Ordering Information](#) for more details.

[1] There is a dead zone between 1037.5MHz to 1300MHz.
Contact [support](#) for frequencies above 1300MHz.

Ordering Information

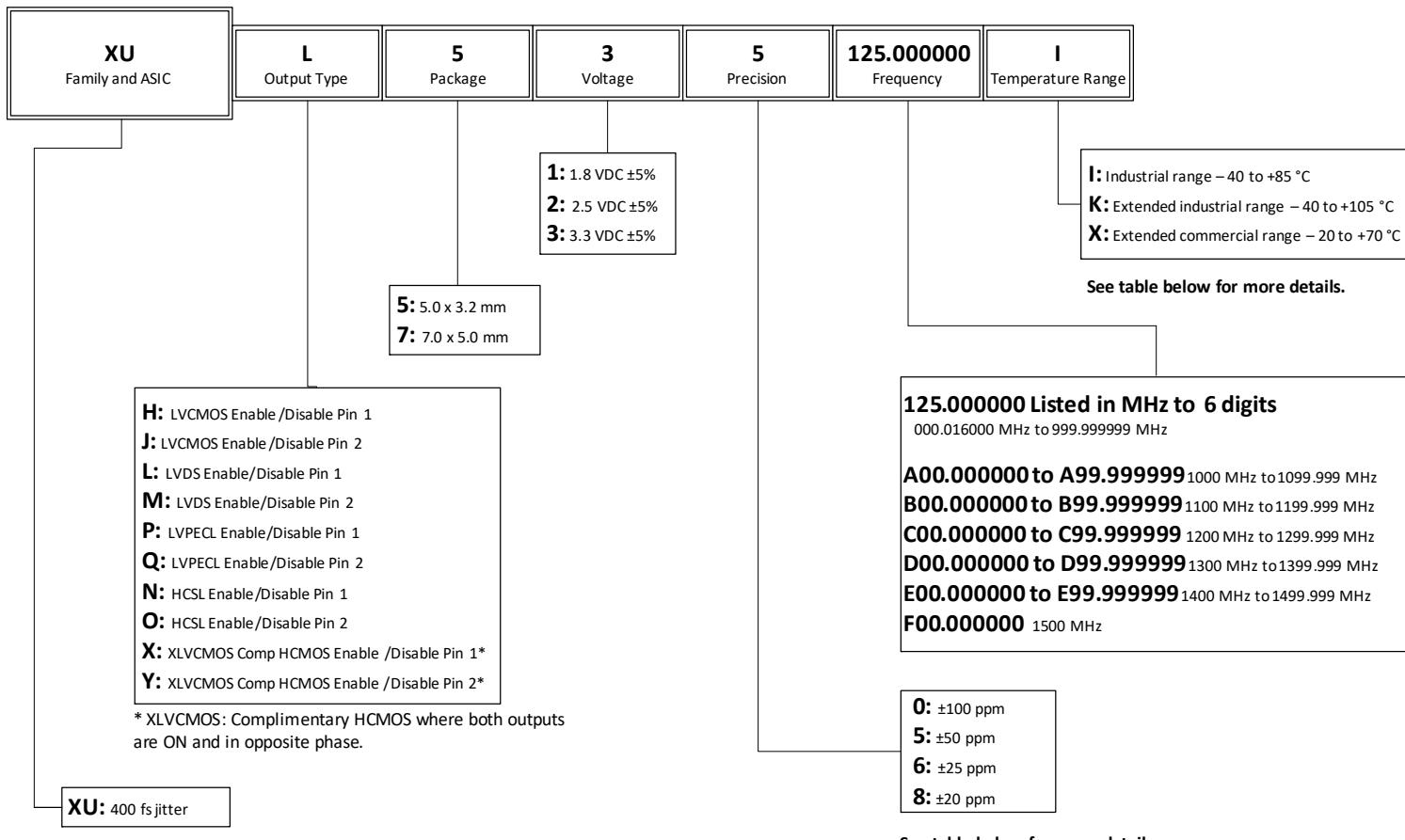


Table 2. Frequency Stability and Operating Temperature Decoder

“Precision” and “Temperature Range” Codes	Operating Temperature	Frequency Stability		
		Minimum	Maximum	Unit
“8” and “X”	-20°C to +70°C	-20	+20	ppm
“6” and “X”	-20°C to +70°C	-25	+25	ppm
“5” and “X”	-20°C to +70°C	-50	+50	ppm
“0” and “X”	-20°C to +70°C	-100	+100	ppm
“6” and “I”	-40°C to +85°C	-25	+25	ppm
“5” and “I”	-40°C to +85°C	-50	+50	ppm
“0” and “I”	-40°C to +85°C	-100	+100	ppm
“5” and “K”	-40° to +105°C	-50	+50	ppm
“0” and “K”	-40° to +105°C	-100	+100	ppm

Contents

Description	1
Pin Assignments	1
Features	1
Ordering Information	2
Absolute Maximum Ratings	4
Mechanical Testing	4
Solder Reflow Profile	4
DC Electrical Characteristics	5
AC Electrical Characteristics	8
Output Waveforms	12
Package Outline Drawings	14
Marking Diagrams	14
Revision History	15

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. The ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings

Item	Rating			
V _{DD}	-0.5 to +5.0V			
E/D	-0.5V to V _{DD} + 0.5V			
OUT	-0.5V to V _{DD} + 0.5V			
Storage Temperature	-55°C to 125°C			
Maximum Junction Temperature	125°C			
Core Current	65mA maximum			
Theta J _A	JU6	75.9 °C/W	JS6	89.6 °C/W
Theta J _B		48.6°C/W		54.3 °C/W
ESD Rating—Human Body Model	1000V			

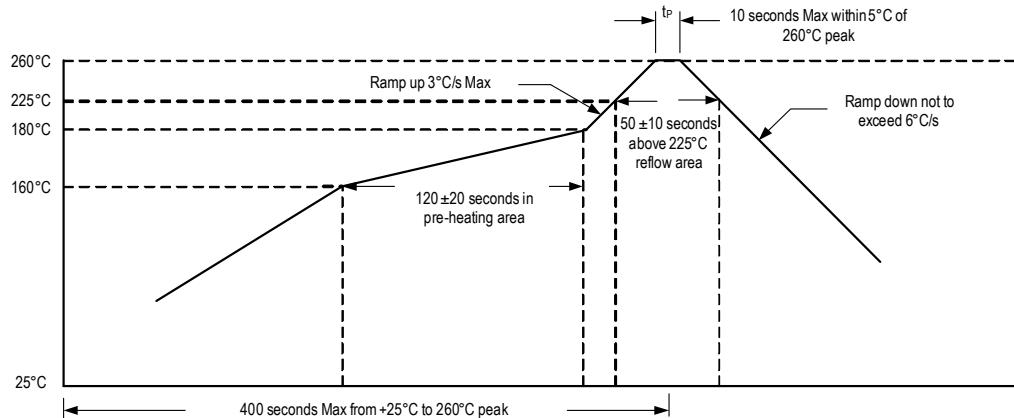
Mechanical Testing

Table 4. Mechanical Testing *

Parameter	Test Method
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.
Mechanical Vibration	Frequency: 10 – 55MHz amplitude: 1.5mm. Frequency: 55 – 2000Hz peak value: 20G. Duration time: 4H for each X,Y,Z axis; total 12hours.
High Temp Operating Life (HTOL)	2000 hours at 125°C (under power).
Hermetic Seal	Gross leak (air leak test). Fine leak (Helium leak test) He-pressure: 6kgf/cm ² 2 hours.

* MSL level does not apply.

Solder Reflow Profile



DC Electrical Characteristics

Note for all DC Electrical Characteristics tables: A pull-up resistor from V_{DD} to E/D enables output when pin 1 is left open.

Table 5. 3.3V IDD DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Unit
I_{DD}	Current Consumption	LVDS	0.016MHz to 400MHz.	-	-	97	mA
			400.000+MHz to 1.5GHz.	-	-	122	
		LVPECL	0.016MHz to 212.5MHz.	-	-	115	
			212.5+MHz to 400MHz.	-	-	128	
			400+MHz to 670MHz.	-	-	142	
			HCSL	0.016MHz to 670MHz.	-	145	
		LVC MOS	0.016MHz to 62.5MHz.	-	-	98	
			62.5+MHz to 167MHz.	-	-	108	

Table 6. 2.5V IDD DC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Unit
I_{DD}	Current Consumption	LVDS	0.016MHz to 400MHz.	-	-	90	mA
			400.000+MHz to 1.35GHz.	-	-	103	
		LVPECL	0.016MHz to 156.25MHz.	-	-	102	
			156.25+MHz to 400MHz.	-	-	112	
			400+MHz to 670MHz.	-	-	118	
		HCSL	0.016MHz to 400MHz.	-	-	102	
			400.000+MHz to 670MHz.	-	-	112	
		LVC MOS	0.016MHz to 62.5MHz.	-	-	80	
			62.5+MHz to 125MHz.	-	-	85	
			125+MHz to 167MHz.	-	-	92	

Table 7. 1.8V IDD DC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Unit
I_{DD}	Current Consumption	LVDS	0.016MHz to 400MHz.	-	-	65	mA
			400.000+MHz to 1.0GHz.	-	-	72	
		LVPECL	0.016MHz to 250MHz.	-	-	75	
			250.000+MHz to 670MHz.	-	-	97	
		HCSL	0.016MHz to 400MHz.	-	-	68	
			400.000+MHz to 670MHz.	-	-	77	
		LVCMOS	0.016MHz to 125MHz.	-	-	58	

Table 8. LVDS DC Electrical Characteristics

$V_{DD} = 3.3V$, $2.5V$, $1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OD}	Differential Output Voltage	-	0.25	0.4	0.5	V
V_{OS}	Output Offset Voltage	-	1	1.17	1.375	
V_{IH}	Enable/Disable Input High Voltage	-	$70\%V_{DD}$	-	-	
V_{IL}	Enable/Disable Input Low Voltage	-	-	-	$30\%V_{DD}$	

Table 9. LVPECL DC Electrical Characteristics

$V_{DD} = 3.3V$, $2.5V$, $1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	$V_{DD} = 3.3V \pm 5\%$.	1.85	-	2.3	V
		$V_{DD} = 2.5V \pm 5\%$.	1.1	-	1.45	
		$V_{DD} = 1.8V \pm 5\%$.	0.5	-	0.8	
V_{OL}	Output Low Voltage	$V_{DD} = 3.3V \pm 5\%$.	1.1	-	1.65	
		$V_{DD} = 2.5V \pm 5\%$.	0.35	-	0.85	
		$V_{DD} = 1.8V \pm 5\%$.	0	-	0.25	
V_{IH}	Enable/Disable Input High Voltage	-	$70\%V_{DD}$	-	-	
V_{IL}	Enable/Disable Input Low Voltage	-		-	$30\%V_{DD}$	

Table 10. HCSL DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	$V_{DD} = 3.3V \pm 5\%$.	0.6	-	1.1	V
		$V_{DD} = 2.5V \pm 5\%$.	0.55	-	0.95	
		$V_{DD} = 1.8V \pm 5\%$.	0.45	-	0.7	
V_{OL}	Output Low Voltage	-	0	-	0.2	
V_{IH}	Enable/Disable Input High Voltage	-	$70\%V_{DD}$	-	-	
V_{IL}	Enable/Disable Input Low Voltage	-		-	$30\%V_{DD}$	

Table 11. LVC MOS DC Electrical Characteristics

$V_{DD} = 3.3V, 2.5V, 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	-	$90\%V_{DD}$	-	-	V
V_{OL}	Output Low Voltage	-	-	-	$10\%V_{DD}$	
V_{IH}	Enable/Disable Input High Voltage	-	$70\%V_{DD}$	-	-	
V_{IL}	Enable/Disable Input Low Voltage	-	-	-	$30\%V_{DD}$	

AC Electrical Characteristics

Table 12. 3.3V AC Electrical Characteristics

$V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit		
F	Output Frequency Range	LVDS.		0.016	-	1500	MHz		
		LVPECL, HCSL.		0.016	-	670			
		LVC MOS.		0.016	-	167			
Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$.	-20		-	+20	+20	ppm		
		-25				+25			
		-50				+50			
		-100				+100			
	Temperature = $-40^\circ C$ to $+85^\circ C$.	-25		-	+25	+50	ppm		
		-50				+50			
		-100				+100			
	Temperature = $-40^\circ C$ to $+105^\circ C$.	-50		-	+50	+100	ppm		
		-100							
Output Load	LVDS.	Differential.	-	100	-	-	Ω		
		LVPECL.	$V_{DD} - 2.0V$.	-	50	-			
		HCSL.	To GND.	-	50	-			
		LVC MOS.	To GND.	-	15	-	pF		
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		-	-	10	ms		
t_R	Output Rise Time	LVDS.	20% to 80% Vpk-pk.	-	275	380	ps		
		LVPECL.		-	-	400			
		HCSL.		-	-	330			
		LVC MOS.	10% to 90% V_{DD} .	-	-	3	ns		
t_F	Output Fall Time	LVDS.	80% to 20% Vpk-pk.	-	275	380	ps		
		LVPECL.		-	-	400			
		HCSL.		-	-	330			
		LVC MOS.	90% to 10% V_{DD} .	-	-	3	ns		
O_{DC}	Output Clock Duty Cycle	LVDS.		45	-	55	%		
		LVPECL.	$F_{OUT} \leq 312.5\text{MHz}$.	45	-	55			
			$F_{OUT} > 312.5\text{MHz}$.	40	-	60			
		HCSL.		45	-	55			
		LVC MOS.	$F_{OUT} \leq 62.5\text{MHz}$.	45	-	55			
			$F_{OUT} > 62.5\text{MHz}$.	40	-	60			
T_{OE}	Output Enable/ Disable Time			-	-	100	ns		

Table 12. 3.3V AC Electrical Characteristics (Cont.)

$V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.	-	300	400	fsec
		LVPECL.	-	300	400	
		HCSL.	-	300	400	
		LVCMOS.	$F_{OUT} = 100MHz$.	-	300	400

Table 13. 2.5V AC Electrical Characteristics

$V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
F	Output Frequency Range	LVDS.		0.016	-	1350	MHz
		LVPECL.		0.016	-	670	
		HCSL.		0.016	-	670	
		LVCMOS.		0.016	-	167	
	Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$.		-20 -25 -50 -100	-	+20 +25 +50 +100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$.		-25 -50 -100	-	+25 +50 +100	
		Temperature = $-40^\circ C$ to $+105^\circ C$.		-50 -100	-	+50 +100	
	Output Load	LVDS.	Differential.	-	100	-	Ω
		LVPECL.	$V_{DD} - 2.0V$.	-	50	-	
		HCSL.	To GND.	-	50	-	
		LVCMOS.	To GND.	-	15	-	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		-	-	10	ms
t_R	Output Rise Time	LVDS.	20% to 80% Vpk-pk.	-	300	400	ps
		LVPECL.		-	250	630	
		HCSL.		-	-	315	
		LVCMOS.	10% to 90% V_{DD} .	-	-	3	ns
t_F	Output Fall Time	LVDS.	80% to 20% Vpk-pk.	-	300	400	ps
		LVPECL.		-	360	630	
		HCSL.		-	-	315	
		LVCMOS.	90% to 10% V_{DD} .	-	-	3	ns

Table 13. 2.5V AC Electrical Characteristics (Cont.)

$V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
O_{DC}	Output Clock Duty Cycle	LVDS.	45	-	55	%
		LVPECL.	$F_{OUT} \leq 156.25MHz$.	45	-	
			$F_{OUT} \leq 156.25MHz$.	40	-	
		HCSL.	45	-	55	
		LVC MOS.	$F_{OUT} \leq 62.5MHz$.	45	-	
			$F_{OUT} > 62.5MHz$.	40	-	
T_{OE}	Output Enable/ Disable Time		-	-	100	ns
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.	-	400	500	fsec
		LVPECL.	-	350	500	
		HCSL.	-	350	500	
		LVC MOS.	$F_{OUT} = 100MHz$.	-	350	

Table 14. 1.8V AC Electrical Characteristics

$V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
F	Output Frequency Range	LVDS.	0.016	-	1000	MHz
		LVPECL, HCSL.	0.016	-	670	
		LVC MOS.	0.016	-	125	
	Frequency Stability	Temperature = $-20^\circ C$ to $+70^\circ C$.		-20	-25	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$.		-50		
		Temperature = $-40^\circ C$ to $+105^\circ C$.		-100		
	Output Load	-25		-	+25	ppm
		-50		-	+50	
		-100		-	+100	ppm
		-50		-	+50	ppm
		-100		-	+100	
				-	-	pF
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.	-	-	10	ms
t_R	Output Rise Time	LVDS.	-	250	315	ps
		LVPECL.	20% to 80% V _{pk-pk} .	250	350	
		HCSL.		-	320	
		LVC MOS.	10% to 90% V_{DD} .	5	-	ns

Table 14. 1.8V AC Electrical Characteristics (Cont.)

$V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; $-40^\circ C$ to $+85^\circ C$, $-40^\circ C$ to $+105^\circ C$.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
t_F	Output Fall Time	LVDS.	80% to 20% Vpk-pk.	-	250	315	ps
		LVPECL.		-	250	350	
		HCSL.		-	-	320	
		LVC MOS.	90% to 10% V_{DD} .	-	5	-	ns
O_{DC}	Output Clock Duty Cycle	LVDS.	$F_{OUT} \leq 156.25MHz$.	45	-	55	%
			$F_{OUT} \leq 156.25MHz$.	40	-	60	
		LVPECL.	$F_{OUT} \leq 312.5MHz$.	45	-	55	
			$F_{OUT} > 312.5MHz$.	40	-	60	
		HCSL.		40	-	60	
			$F_{OUT} \leq 62.5MHz$.	45	-	55	
		LVC MOS.	$F_{OUT} > 62.5MHz$.	40	-	60	
T_{OE}	Output Enable/ Disable Time			-	-	100	ns
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.		-	800	1200	fsec
		LVPECL.		-	750	1200	
		HCSL.		-	100	1200	
		LVC MOS.	$F_{OUT} = 100MHz$.	-	800	1200	

Notes for all AC Electrical Characteristics tables:

¹ A pull-up resistor from V_{DD} to E/D enables output when pin 1 is left open.

² Installation should include a 0.01 μ F bypass capacitor placed between V_{DD} and GND to minimize power supply line noise.

³ Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

⁴ Standard LVC MOS frequencies include 10MHz, 12MHz, 12.288MHz, 16MHz, 20MHz, 24MHz, 24.576MHz, 25MHz, 33.333MHz, 40MHz, 48MHz, 50MHz, 100MHz, 125MHz and 156.25MHz.

⁵ Standard differential frequencies include 100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz and 400MHz.

Output Waveforms

Figure 1. LVDS Output Waveforms

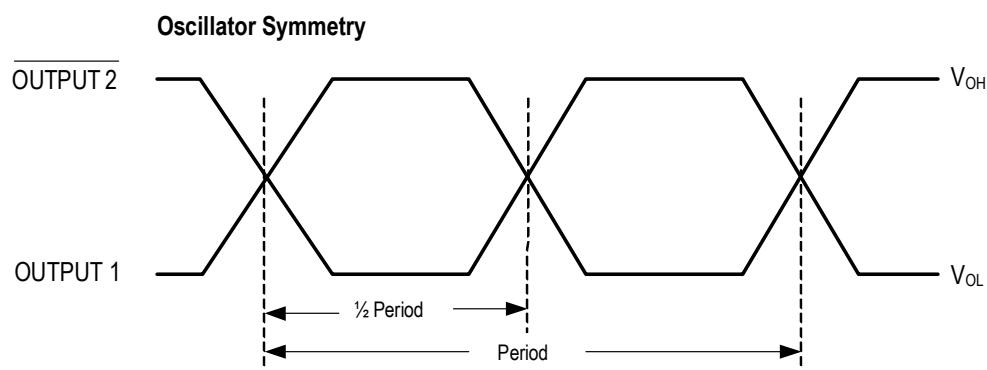
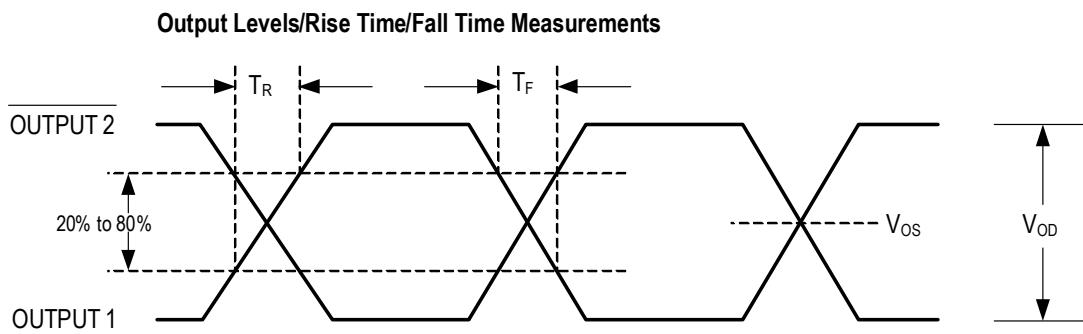


Figure 2. LVPECL Output Waveforms

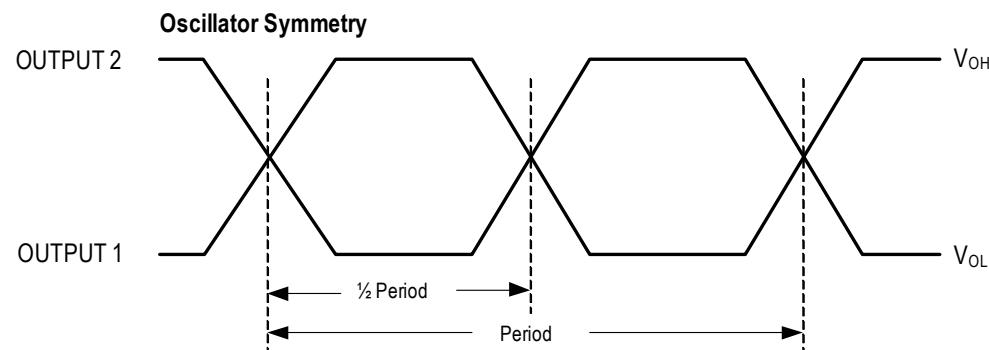
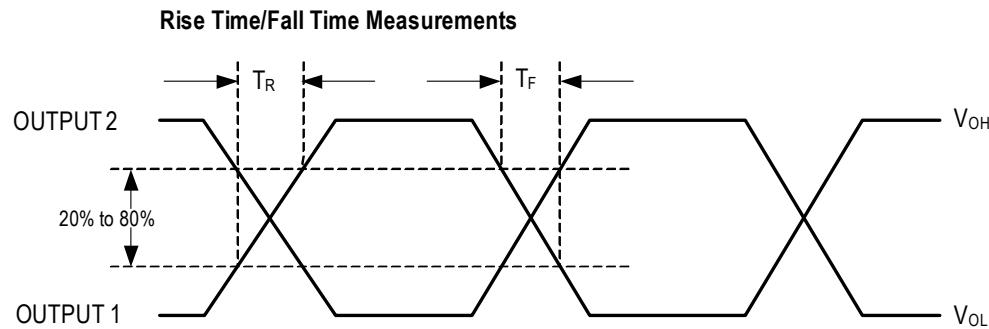
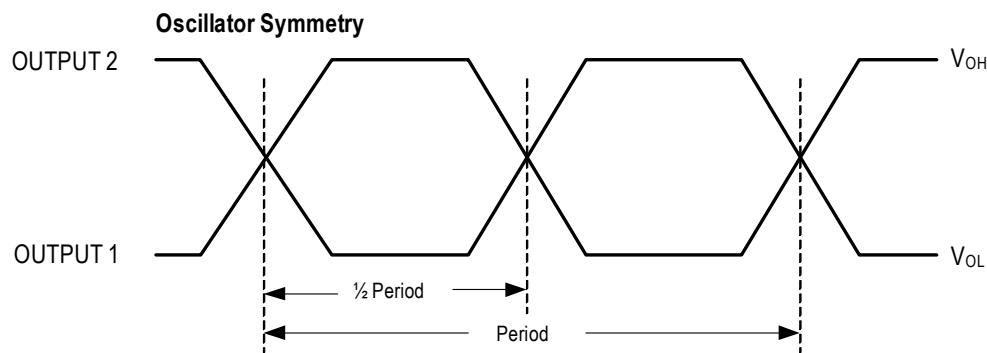
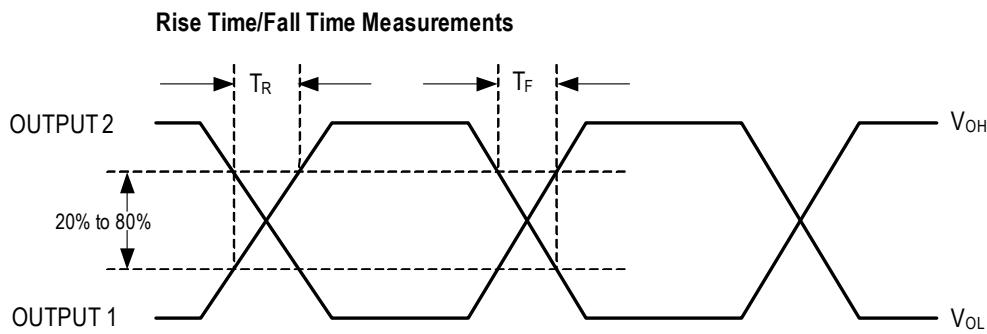
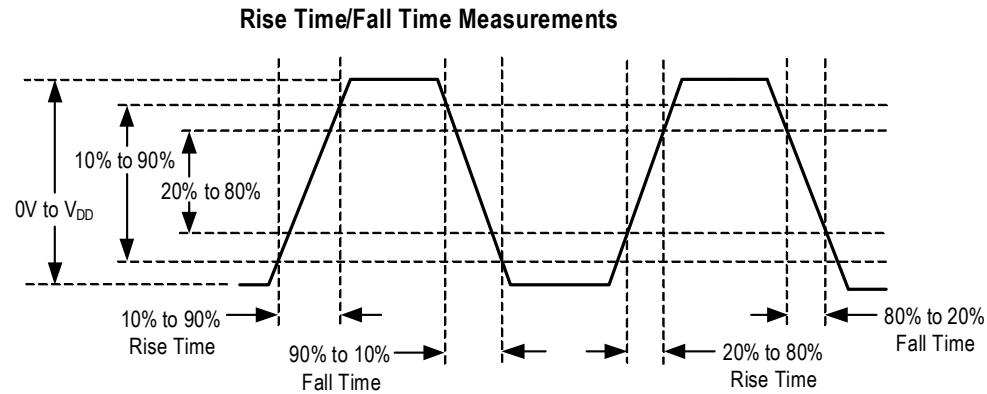


Figure 3. HCSL Output Waveforms**Figure 4. LVC MOS Output Waveforms****Oscillator Symmetry**

On Time $\frac{1}{2}$ Period

Off Time $\frac{1}{2}$ Period

50% V_{DD}

Period

©2016-2024 Renesas Electronics Corporation

13

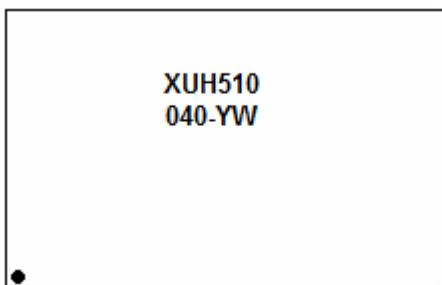
November 21, 2024

Package Outline Drawings

The package outline drawings ([JS6](#), [JU6](#)) are appended at the end of this document. The package information is the most current data available.

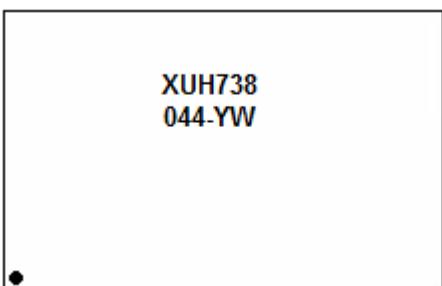
Marking Diagrams

JS6 5.0 × 3.2 mm Package Option (example based on XUH510040.000000I)



- Line 1:
 - "XU" = family; "H" = output type; "5" = package size; "1" = voltage; "0" = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
 - "040" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
 - "YW" denotes the last digit of the year and work week the part was assembled.

JU6 7.0 × 5.0 mm Package Option (example based on XUH738044.736000X)

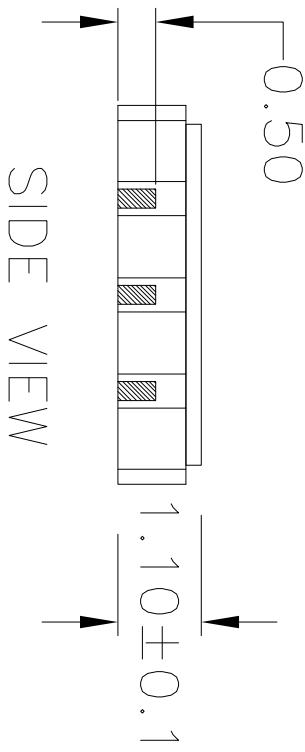
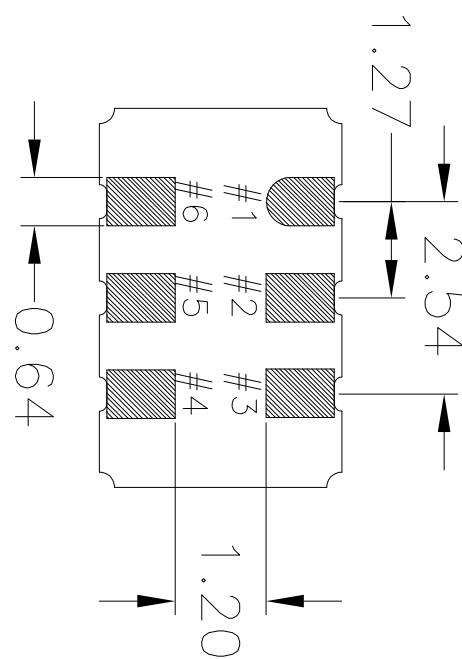
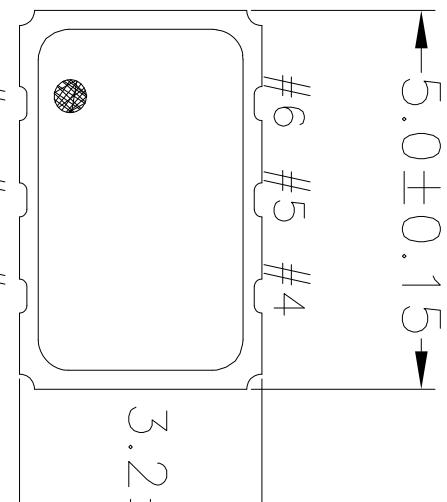


- Line 1:
 - "XU" = family; "H" = output type; "7" = package size; "3" = voltage; "8" = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
 - "044" denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
 - "YW" denotes the last digit of the year and work week the part was assembled.

Revision History

Revision Date	Description of Change
November 21, 2024	Updated Table 11 .
November 1, 2023	Updated values in Table 11 .
January 11, 2022	<ul style="list-style-type: none">▪ Updated Frequency Stability values in Table 14.▪ Removed Aging parameters in Table 12, Table 13 and Table 14.
December 7, 2021	<ul style="list-style-type: none">▪ Updated Frequency Stability values in Table 12 and Table 13.▪ Removed I2C section.
November 23, 2021	Added Frequency Stability and Operating Temperature Decoder table after Ordering Information.
August 18, 2021	Moved Ordering Information table to just after Pin Descriptions.
January 19, 2021	<ul style="list-style-type: none">▪ Removed 4-pin package description table, figure, and package drawing references.▪ Added footnote for pin 5 in Table 1.▪ Added footnote under "Output Type" in Ordering Information.
January 12, 2021	Added Marking Diagrams section and updated Package Outline Drawings links.
February 11, 2020	Added I2C Bus Characteristics tables.
June 28, 2019	<ul style="list-style-type: none">▪ Added footnote to frequency range bullet under front page Features.
June 25, 2018	<ul style="list-style-type: none">▪ Updated Package Outline Drawings section.
November 22, 2017	<ul style="list-style-type: none">▪ Updated Theta JA and JB in Absolute Maximum Ratings table.▪ Added MSL statement under Mechanical Testing table.▪ Updated ordering information.
October 19, 2017	<ul style="list-style-type: none">▪ Updated document title.▪ Updated Features bullets.▪ Updated Absolute Maximum Ratings and ESD Compliance tables.▪ Added -40°C to +105°C rating to all electrical tables.▪ Removed phase noise charts.▪ Updated Ordering Information table.
May 12, 2017	<ul style="list-style-type: none">▪ Reformatted embedded tables.▪ Removed "Jitter Performance" tables and moved the "Phase Jitter (12kHz–20MHz)" parameter to its respective AC Electrical Characteristics table.▪ Updated all Output Waveform drawings.
December 1, 2016	Initial release.

REVISONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



NOTES:

1. ALL DIMENSIONS IN MM.

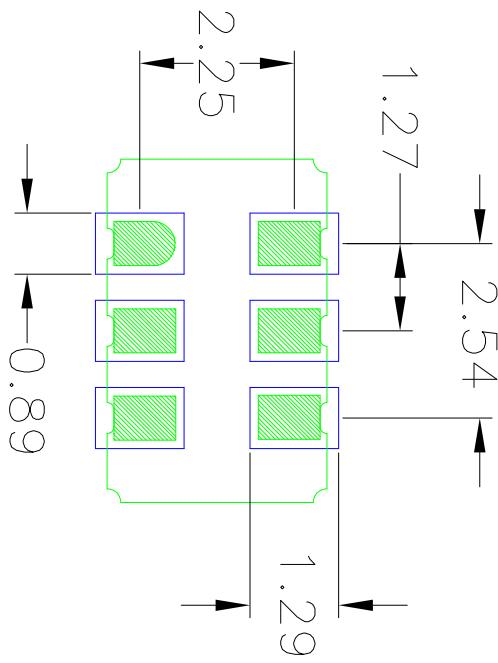
TOLERANCES UNLESS SPECIFIED	5024, Silver Creek Valley Rd
DECIMAL	San Jose, CA 95138
XX±	PHONE: (408) 727-6116
XXXX±	FAX: (408) 492-8674
APPROVALS	TITLE JS6 PACKAGE OUTLINE
DRAWN <i>DB&C</i>	5.0 x 3.2 mm BODY
CHECKED	1.1 mm Thick
	SIZE DRAWING No. REV
	C PSC-4411 03
DO NOT SCALE DRAWING	SHEET 1 OF 2



IDT™

www.IDT.com

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHUA



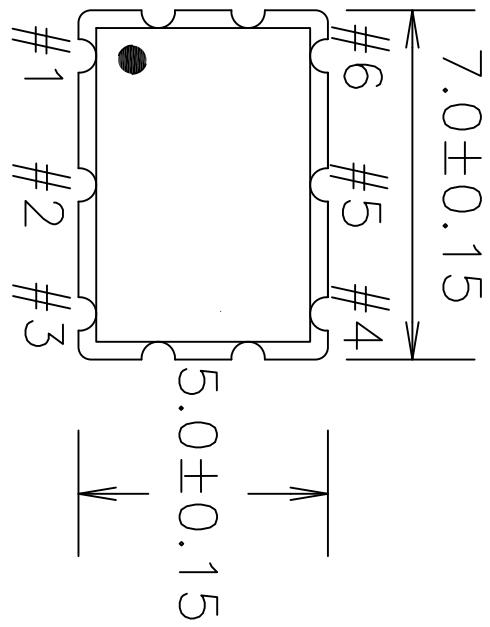
RECOMMENDED LAND PATTERN

NOTES:

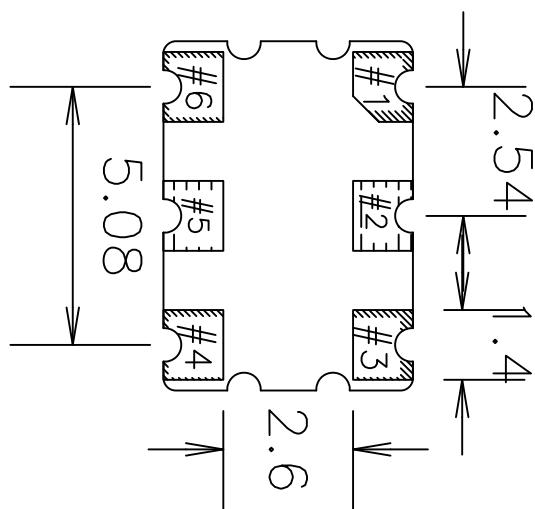
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL \pm ANGULAR XXXX± XXXX±		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674	
APPROVALS	DATE	TITLE: J36 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick	
DRAWN BY & C 04/2/12	CHECKED	SHEET C DRAWING No. PSC-4411	SIZE REV 03
		DO NOT SCALE DRAWING	
		SHEET 2 OF 2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRAWING	8/12/14	JHUA



TOP VIEW

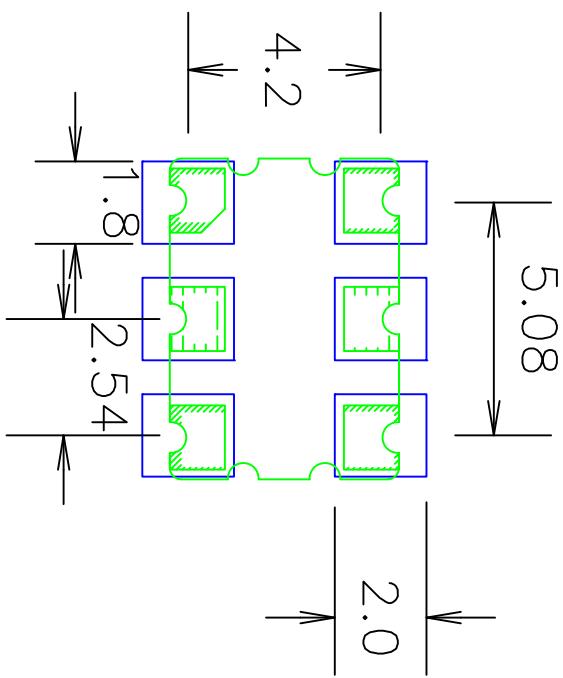


BOTTOM VIEW

- NOTES:
- ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED	DECIMAL ±	ANGULAR ±	IDT™	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.COM
XXX±				
APPROVALS	DATE		TITLE	JU6 PACKAGE OUTLINE
DRAWN BY	10/03/12		7.0 x 5.0 mm BODY	1.3 mm Thick
CHECKED			SIZE	DRAWING No.
			C	PSC-4430
				DO NOT SCALE DRAWING
				SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	K.S.
01	UPDATE PACKAGE DRAWING	8/12/14	J.HUA



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
 2. TOP DOWN VIEW AS VIEWED ON PCB.
 3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
 4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
 5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
- FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR \pm \pm	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-5116 FAX: (408) 492-8874
WWW.IDT.COM	WWW.IDT.COM
APPROVALS	DATE
DRAWN 3/25	10/03/12
CHECKED	
	SHEET 2 OF 2
	SIZE C
	DRAWING NO. PSC-4430
	REV 01
DO NOT SCALE DRAWING	

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.