MT25QL512ABB8ESF-0SIT

https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/7161/MT25QL512ABB8ESF-0SIT.pdf

As far as PCB design goes, not everything in the datasheet matters to us like extended addressing, security registers, programming, etc. because that'll be handled by the bitstream generated in Vivado.

Basic Info:

- 2.7-3.6 V operating range
- 512 MegaBit density -> 64 MB per chip

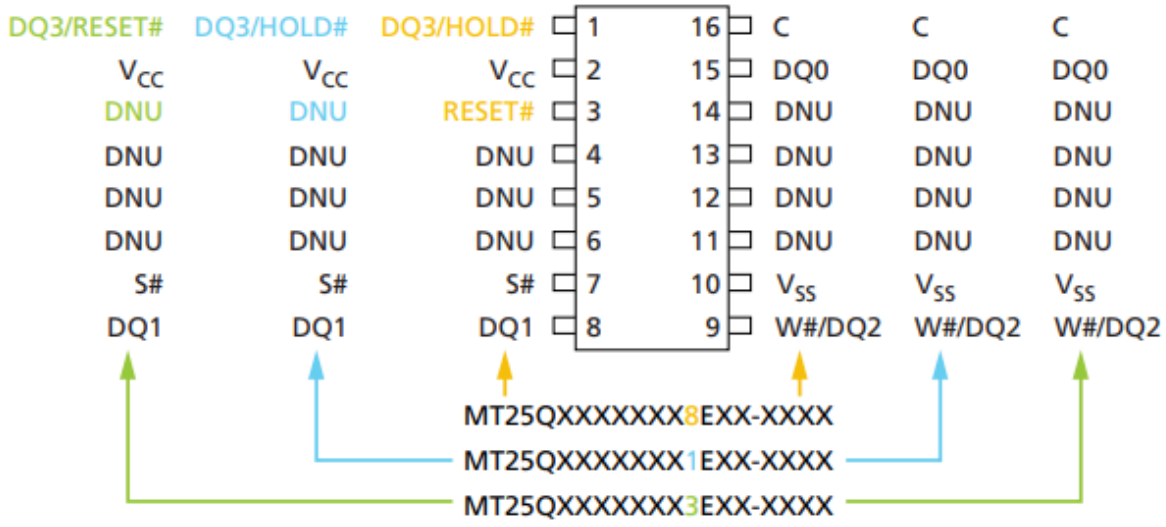
Signal Assignments:

Our package code is SF (...8ESF-0SIT), so we'll use the pinout on **Page 13.**

Notice that 7 pins are marked as DNU (Do Not Use). That explains why the IC has 16 pins, but the schematic in Altium only uses 9 pins.

Signal Assignments – Package Code: SF

Figure 5: 16-Pin, Plastic Small Outline – SO16 (Top View)



Notes:
1. RESET# or HOLD# signals can share Pin 1 with DQ3, depending on the selected device (see Part Numbering Ordering Information). When using single and dual I/O commands on these parts, DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.
2. Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pull-up resistor and may be left unconnected if not used.

Signal Descriptions:

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- **S# (Input):** Chip select, active low.
    - Running it high puts the device in standby mode and tri-states all output pins and input pins (besides RESET) are ignored.
    - Driving it low enables the device (active mode).
    - After power up, there has to be a falling edge on S# before any commands are sent. That means you can't just keep S# low during activation as well as when you want to use the flash.
- **C (Input):** Clock. This device is CPOL = 0 (polarity = 0) meaning clock idles low.
    - Therefore the device looks at inputs on the rising edge of the clock, and data is outputted on the falling edge.
- **RESET# (Input):** Active low reset.
    - When driven low, device is reset and outputs are tri-stated. Data may be lost if a reset happens while the FLASH is doing some operation (WRITE, PROGRAM, ERASE, etc).
- **HOLD# (Input):** Pauses communication.
    - For my IC, HOLD# and DQ3 share the same pin.
    - It's only used in regular SPI mode, not in QSPI. In QSPI, HOLD# functionality is disabled so that the pin can be used as a 3rd data line.
- **W# (Input):** Freezes the status register from getting modified. The status register holds flags which gives information about the operations that are happening, and firmware you write can read or modify the status register.
    - W# is write protection to prevent firmware from modifying the status register.
    - It shares a pin with DQ2.
    - In QSPI mode, the pin is used for input/output as DQ2.
- ****DQ[3:0] (Input/Output):** Bidirectional DQ signals for address, command, and data.
    - In regular SPI mode, DQ0 and DQ1 are for MISO and MOSI. DQ2 and DQ3 are used for HOLD# and RESET as mentioned earlier.
- **VCC (Supply):** Supply voltage.
- **VSS (Supply):** Ground connection.

Supported Clock Frequencies (STR Mode):

Page 28, Table 10 (IT Parts)

For QAD I/O Fast Read (MHz):

- 39
- 48
- 58
- 69
- 78

- 86
- 97
- 106
- 115
- 125
- 133

Power Up/Power Down:

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Use a decoupling capacitor of 100 nF.

Important: During power up/power down, **the device MUST NOT be selected (S# != 0).** S# must follow the voltage applied on VCC until VCC reaches the correct values. Only after VCC reaches 3.3 V (in my case) can S# be toggled to 0 to enable the device.

- That's why S# has a pull up resistor. The FCS_B pin on the FPGA is likely an open drain connection that can go high-Z during startup to avoid enabling the FLASH and having it read garbage addresses/commands from the database (which are also open drain and probably floating at this point).