ISL8014A

https://www.renesas.com/en/document/dst/isl8014a-datasheet

Basics:

- **SMPS ->** More efficient than if I went with a LVPS which matters since the 1 V rail draws a large amount of current
- Up to 4 A continuous output
    - Less than 0.4 V dropout at 4 A current draw
- 2.8 V to 5.5 V input
- Fast transient response
- **Discontinuous operation** at light load provides higher efficiency by reducing switching losses
- **Forced continuous operation** at light load reduces noise and RF interference
- Power good signal for when output is in regulation

Pin Descriptions:

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- **VIN (Pins 1 and 2 to split the current between pins for lower resistance)**
    - Input supply. **Use a 10 uF ceramic cap** to ground.
- **VDD**
    - Input supply for the **analog switching circuitry** in the IC, tied to V_{IN}. Probably should add some isolation to ensure none of the switching noise gets on V_{IN}.
        - I can create an RC lowpass filter using 22 ohms and 1 uF that has a cutoff of 7 kHz.
- **EN**
    - Active high enable.
    - It's **recommended** that EN should be kept below 0.4 V until V_{IN} reaches 2.5 V.
- **PG**
    - Power good signal. It's delayed by 1 ms after output voltage has stabilized.
    - Needs a pull-up resistor to VIN. Used a 100k in the example application.
- **SYNCH**
    - Mode selection pin
    - HIGH (Connect to VDD, must be higher than 2.5 V): PWM mode, more efficient at high load
    - LOW (Connect to GND, must be less than 0.4 V): PFM mode, more efficient at light load
    - Or connect to external function generator.

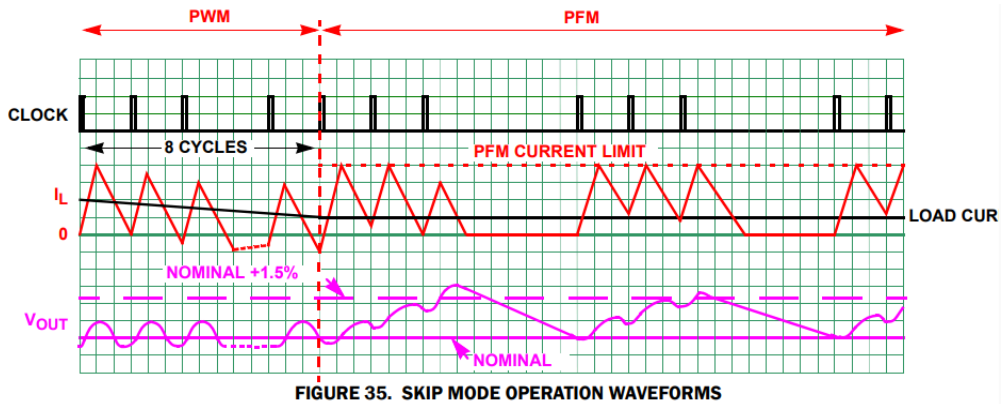

FIGURE 35. SKIP MODE OPERATION WAVEFORMS

- **LX (2 of them to handle high current, so tie their outputs together)**
    - Switching node output, connect to a series inductor.
- **PGND**
    - Power ground
- **SGND**
    - Signal ground
- **VFB**
    - Output feedback. Connect to the output of the inductor at LX through a resistor divider for adjustable output.
    - For 0.8 V output, connect to the output of the inductor with no resistor divider.
- **Exposed Pad**
    - Must be connected to SGND pin.
    - **Place as many thermal vias as possible under this pad for optimal thermals.**

Example Implementation

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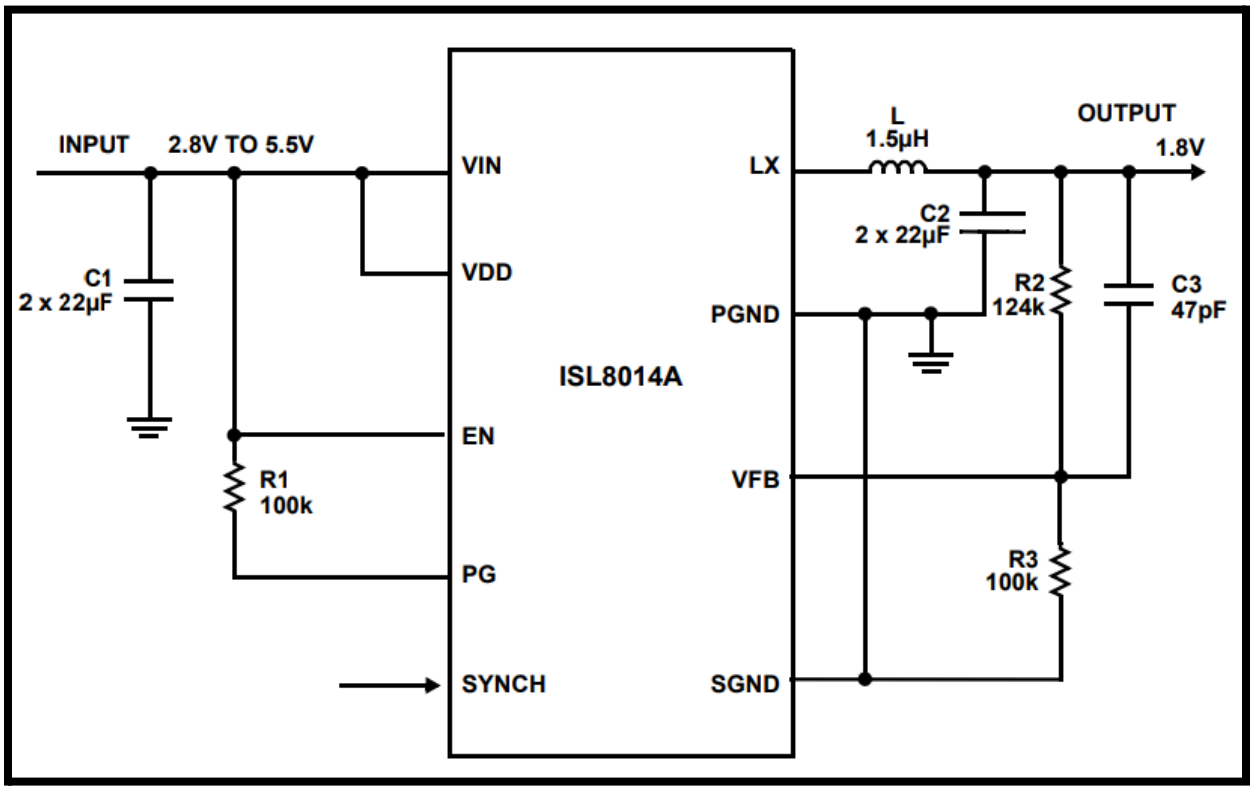

Typical Operating Performance

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- Based on Figure 1, PWM mode with 3.3 V input at 2 A and 1.2 V output is about **85% efficiency**. At 1 V, that's probably even lower because of the lower duty cycle.

Enable Signal Ramp Up:

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It's **recommended** that the EN voltage be less than 0.4 V until V_{IN} reaches 2.5 V.
The datasheet recommends using a voltage divider so that EN tracks V_{IN}, but at a lower rate:

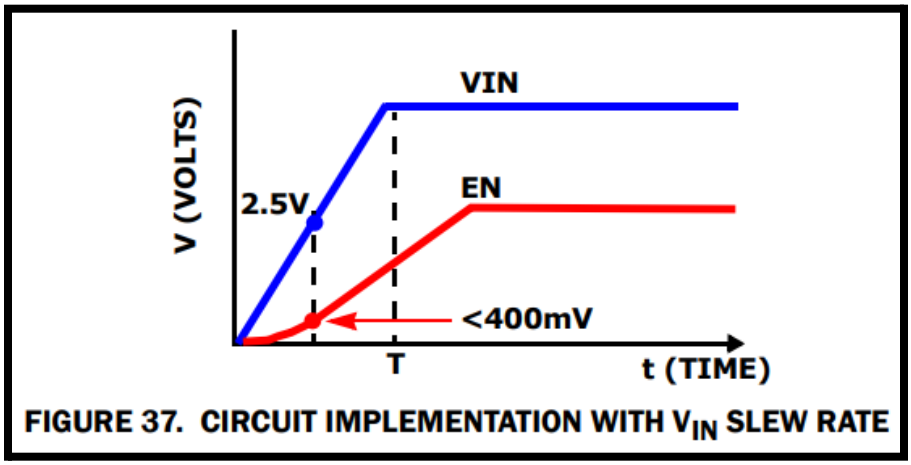

FIGURE 37. CIRCUIT IMPLEMENTATION WITH V_{IN} SLEW RATE

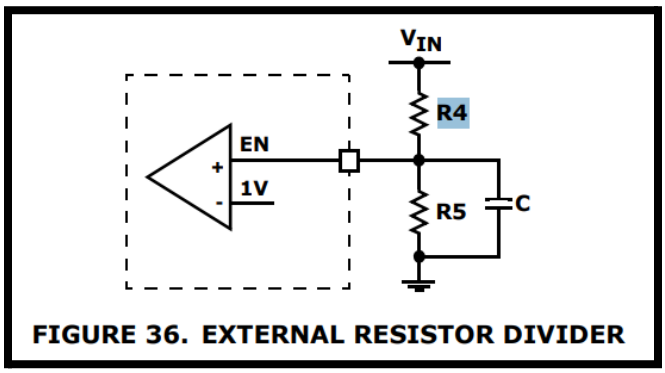

FIGURE 36. EXTERNAL RESISTOR DIVIDER

The datasheet provides an equation for calculating R_4 based on R_5 and V_{IN}.

We need to select the ratio such that EN is 1.4 V (minimum to enable logic high) when V_{IN} is equal to or greater than 2.5 V (for me, I'll probably make that 2.9 V or 3 V).

Set R_5 between 10k and 100k.

$R_4 = \frac{R5 * (Vin - 1.4\,V)}{1.4\,V}$, I'll go with R_4 = 100k and R_5 = 75k

Then we can select the capacitance such that the time constant is at least twice the rise time because that'll allow the delay to EN to be high enough such that EN is still less than 0.4 V by the time V_{IN} reaches 2.5 V (2.9 or 3 V for me).

T = rise time of V_{IN}, I couldn't find any values for this for M.2 M-key, so I'll just shoot in the dark with 5 ms, but I'll double that to 10 ms for safety

C >= $\frac{2T}{R4 \,||\, R5}$ -> $\frac{2 * 0.01\,s}{100k \,||\, 75k}$ = 4.7 * 10^{-7}

Output Inductor and Capacitor Selection

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For higher output voltages (like 3.3 V), a higher inductance can be used to reduce current and voltage ripple on the output.

It's **recommended** that inductor ripple current is 30% of the maximum output current for best performance.

Ripple Current (ΔI) = $\frac{VO * (1 - \frac{VO}{Vin})}{L * fs}$

- V_O = output voltage
- V_{IN} = input voltage
- f_s = switching frequency of the PMIC

From my estimates using the Xilinx Power Estimator, my peak current on the 1 V rail is about 2.3 A. 30% of that would be 0.69 A.

0.69 A = $\frac{1.004\,V * (1 - \frac{1.004\,V}{3.3\,V})}{L * 1\,MHz}$, solving we get L = 1.01 uH

The equation above can be rearranged to help me find the inductance to use, **BUT** Renesas also recommends the inductor have a saturation current over 7 A since the regulator can spike to 6 A under heavy load.

TABLE 1. OUTPUT CAPACITOR VALUE vs V_{OUT}

V_{OUT} (V)	C_{OUT} (µF)	L (µH)
0.8	2 x 22	1.0~2.2
1.2	2 x 22	1.0~2.2
1.5	2 x 22	1.5~3.3
1.8	2 x 22	1.5~3.3
2.5	2 x 22	1.5~3.3
3.3	2 x 22	2.2~4.7
3.6	2 x 22	2.2~4.7

Additional output capacitances should be added when high load transients or low output ripple is required. -> I already added the decoupling caps that Xilinx recommended on the FPGA side for the 1 V rail, so I'll just add a 4.7 uF here for some bulk.

Output Voltage Resistor Divide

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Feedback resistor is typically between 10k and 100k

$R_3 = \frac{R2 * 0.8\,V}{Vout - 0.8\,V}$

If you want the output to be 0.8 V, then you don't need R_3 and R_2 is shorted.

For my implementation, I'll go with R_2 = 12k and R_3 = 47k which yields about 1.004 V on the output. I want resistors on the lower end so I have a low impedance network which is less susceptible to interference.

For better performance, add 47 pF in parallel with R2 (100k).

- This 47 pF cap is what's called a **"feedforward capacitor"** which improves transient response. Basically if the FPGA load increases suddenly, output voltage will dip. The 47 pF cap couples this change to the feedback pin on the PMIC, and it bypasses the resistor network to tell the PMIC to immediately boost output.
- In terms of control theory, the 47 pF cap adds a zero and pole to the open loop transfer function, which when placed properly will provide a phase boost.