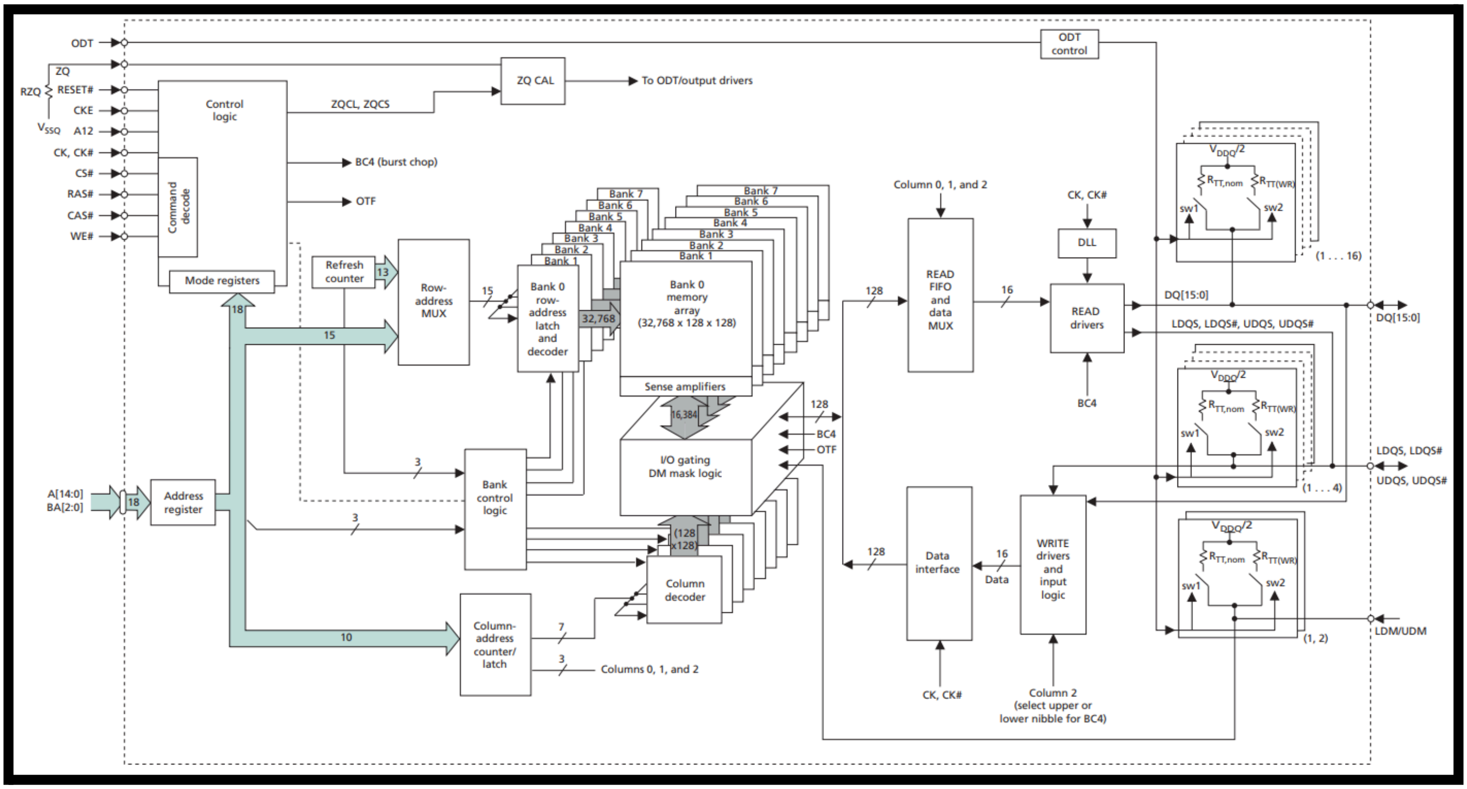
MT41K256M16TW-107:P

https://mm.digikey.com/Volume0/opasdata/d220001/medias/docus/6128/MT41K1G4_MT41K512M8_MT41K256M16_RevR_Sep2018.pdf?_gl=1*cem9st*_up*MQ..*_gs*MQ..&gclid=Cj0KCQiApL7KBhC7ARIsAD2Xq3BgY-IWL3f4dasmx9KOrNK8YfDGwEREzaznlQ7BKzRcOb5HQ3cNZQYaAnjMEALw_wcB&gclsrc=aw.ds&gbraid=0AAAAADrbLlhuIhfoUkRWjDnrL4PqzKPWi

I’ve chosen a 256x16 configuration. A[14:0] are used for row addresses, A[9:0] are for column addresses, and BA[2:0] are for bank selection.

- 2^{15} = 32768
- 2^{10} = 1024
- 2^{3} = 8
- 32768 * 1024 = 33,554,432
    - That means we have 33,554,432 UNIQUE addresses.
    - Each address contains 1 word, which in our case is 16 bits.
    - Thus each of our 8 banks hold 33,554,432 * 16 = 536,870,912 bits
- 536,870,912 * 8 = 4,294,967,296 bits = 4 Gigabits = 512 Megabytes

An FBD (Figure 5) is provided on Page 16 for the 256x16 version.



BGA arrangement is provided on Page 18 for the 256x16.

Pin Descriptions

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- **A[14:0]:** Address inputs.
    - Provides the row address for **ACTIVATE** commands.
        - Because of the way DRAM works, it's "destructive" by nature. Memory cells contain a capacitor and transistor.
        - Reading data from memory cells causes the capacitor to lose its charge because that charge is drained onto the bitline.
        - Sense amplifiers can see the data/charge that's drained onto a bitline, convert that into a logic value (1/0), and write that back to the original memory cell to avoid destruction of data.
        - The ACTIVATE command basically opens a specific row in a specific memory bank, and does what I mentioned above with transferring that data into sense amplifiers.
    - During **READ/WRITE** commands, A[9:0] provide the column address.
        - **When not in ACTIVATE mode,** some of the address pins are used for another purpose like A10 and A12:
            - A10 is used as a PRECHARGE signal.
                - If high, the row will be closed when the READ/WRITE operation is finished.
                - If low, the row will stay open for another command which is more efficient than rerunning ACTIVATE.
            - A12 is used as a "Burst Chop/BC" signal. This controls how much data comes out.
                - If high, you get 8 bytes of data from a row.
                - If low, that's chopped and you get 4 which is useful if you want to save time and don't need 8 bytes.
                -
    - The **PRECHARGE** command is used to close a row manually.
        - It's done after a READ/WRITE operations or when we're switching between rows in a bank.
        - A10 is used as a bank selector.
            - If high, precharge is applied to all banks.
            - If low, precharge is only applied to the bank selected by the Bank Address (BA[2:0]) pins.
- **BA[2:0]:** Bank address inputs.
    - Recall from the FBD above that there's 8 banks that can be selected.
    - BA[2:0] define which bank an ACTIVATE, READ/WRITE, or PRECHARGE command is applied to.

    - During **LOAD MODE**, BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded. You can see the mode registers in the FBD above. They're on the bottom of the "Control logic" block.
        - Mode registers control functionality like ODT (on die termination), refresh settings, burst length, write leveling, etc.
- **CK/CK#:** Differential pair of clock inputs.
    - Differential pairs help with combatting EMI.
    - All control/address signals are sampled when CK is on its positive edge and CK# is on its negative edge.
- **CKE:** Clock enable, active high.
    - When high it enables, and when low it disables, internal circuitry and clocks.
- **CS#:** Chip select, active low.
- **LDM:** Input data mask.
    - Lower byte, input mask signal for write data.
        - Because I chose 256x16 RAM, our word size is 16 bits.
        - Sometimes computers only need to modify 8 bits of data from RAM instead of 16 bits.
        - The lower byte mask allows us to leave the lower 8 bits unchanged during a WRITE.
    - When LDM is high, the lower byte is masked.
    - When LDM is low, the lower byte is modifiable during a WRITE.
- **UDM:** Upper byte input data mask.
    - Same principle as LDM.
- **ODT:** On-die termination, active high.
    - ODT are resistors on the die that can be activated to help with impedance matching and reduce reflections.
    - When high, termination resistance is enabled.
        - It applies to DQ[15:0], LDQS, LDQS#, UDQS, LDM, and UDM.
            - These signals were chosen because they operate at a higher speed and are more prone to transmission line effects.
- **RAS#, CAS#, WE#:** Define the command being entered. You can think of the 3 bits together as being opcodes.
    - RAS = Row Access Strobe, when low the DRAM will latch the row address pins (lock them) and send them to row decoders to trigger the appropriate sense amplifiers.
    - CAS = Column Access Strobe, when low the DRAM will latch the address pins and send them to column decoders to pick a specific piece of data from an already open row.
    - WE = Write Enable, determines direction of data (in/out).
- **RESET#:** Active low asynchronous reset.
- **DQ[7:0]**: Data output AND input (if we want to read or write data to RAM).
    - The lower byte.

- **DQ[15:8]:** Upper byte for data input/output.
- **LDQS/LDQS#:** Basically a differential pair for a local clock for the lower bits (DQ[7:0]).
    - There's a global clock that originates from the CPU/FPGA, and that's used for determining when to sample the address lines and when to check for commands.
    - This global clock has to travel to every DRAM chip, so it takes a long and complex path, but at high speed, that makes transmission line effects more important so **it can't be used to precisely time data bits** on DQ[15:0].
    - The memory controller also has local data clocks called "Local Strobe" (DQS) that travel simpler paths alongside the data bits, so they experience the same delay. Thus they are better synchronized.
    - During memory training for boot up, the memory controller will send test patterns on the DQS to see which timing is best synchronized.

- There's also some relevant information about reads and writes relating to this data clock:
    - Just a notices, READs and WRITEs are from the perspective of the CPU/FPGA, so a WRITE is the CPU/FPGA sending data to DRAM.
    - **Center-Aligned WRITES**
        - When the CPU/FPGA memory controller is writing data to RAM, it will send the data bits, then wait 90* (quarter cycle) before sending the data clock strobe (DQS). It controls both data and DQS.
            - This is similar to what I do with SDA and SCL in I2C to ensure SDA is sampled only when it has stabilized.
        - Thus the DQS edge arrives in the middle of the data window, thus that data line is stabilized when DRAM samples it.
    - **Edge-Aligned READS**
        - DRAM is simpler for costs, so it doesn't add a shift to DQS like the memory controller does.
        - Instead DRAM will send DQ and DQS at the same time so that their edges are aligned. DRAM controls both data and DQS for reads.
        - From there, the memory controller on the CPU/FPGA (which is smarter) will shift the DQS to sample the data at the correct time.
    - It gets more complex when you consider Double Data Rate where we sample on rising and falling edges, but the concept is the same. We still have a 90* delay before sampling after a rising edge, and a falling edge.
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- **UDQS/UDQS#:** Differential clock for the upper byte (DQ[15:8]).
    - We have this separation for local clocks between upper and lower bytes because those bytes are pretty independent. We can read/write to just an upper byte or lower byte if we want.

- **V_{DD}:** Input power (1.35 V)
- **V_{DDQ}:** DQ power supply used for output signals. When signals are going out, they feed directly from V_{DDQ} and draw more power.
- **V_{REFCA}:** Reference voltage for control, command, and address. Must be maintained at all times.
- **V_{REFDQ}:** Reference voltage for data, must be maintained at all times.
- **V_{SS}:** Ground.
- **V_{SSQ}:** Isolated from normal V_{SS} for better noise immunity.
- **ZQ:** Calibration to ensure the strength of the signals of the signals leaving DRAM is right and that ODT resistance is right. **Use a HIGH PRECISION 240 ohm resistor.**

Electrical Specifications

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IMPORTANT: Micron hasn't provided any decoupling capacitor specifications. Probably because single DRAM chips are expected to go onto a larger DIMM.