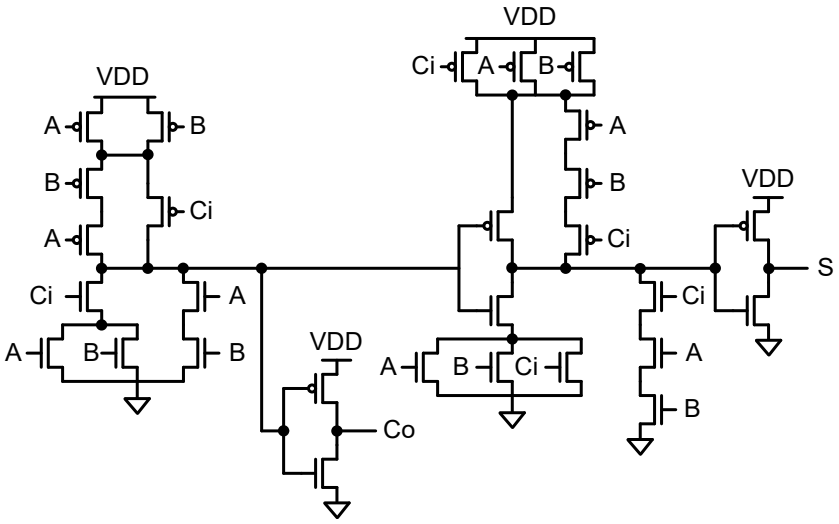
LAB 3 Performance Analysis for Adders

1. ***Sizing issue for Carry Propagation***
2. ***Delay Vs. Voltage***
3. ***Find out Critical Path***

Truth Table for Full adder：

Input(A，B，Ci)	output(Co)	output(S)
000	0	0
001	0	1
010	0	1
100	0	1
011	1	0
101	1	0
110	1	0
111	1	1

Full adder Schematic：



Input pattern：

```
VA    A    0    pulse(1.8    0    1n    0.1n    0.1n    19.9n    40n)
VB    B    0    pulse(1.8    0    1n    0.1n    0.1n    39.9n    80n)
VC    C    0    pulse(1.8    0    1n    0.1n    0.1n    79.9n    160n)
.tran    0.05n    200n
```

LAB 6-1 $^{1bit}/_{8bits}$ Full Adder under Regular Voltage

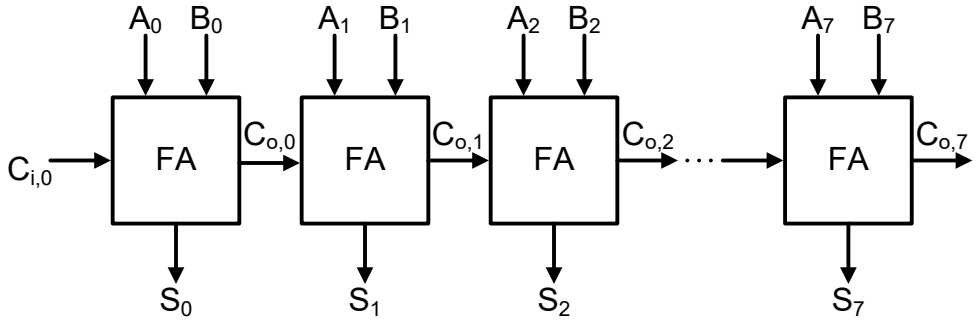
6-1-a：(1bit)

Write down a full adder SPICE，Loading 0.1p(for S、C_{out}), Observe Waveform, Delay time, and Power consumption。(Practice Sizing to let **Delay smaller than 0.3ns。)**

6-1-b：(8bits)

Try to connect full adder to be 8-bit carry-ripple adder，Loading 0.1p (for S_0~S_7, C_{o7}), observe waveform, Delay time and Power consumption。(Practice Sizing to let **Delay smaller than 0.3ns**。

8-bit carry-ripple adder：



LAB 6-2 $^{1bit}/_{8bits}$ full adder Under Various Supply Voltage

6-2-a：(1bit)

VDD=1.6V,1.4V, 1.2V, 1.0V, 0.8V, 0.6V，to measure Delay time, Power consumption, and PDP under various supply voltage. (Once **0.2V lower, your input pattern should 10 times slower.**)