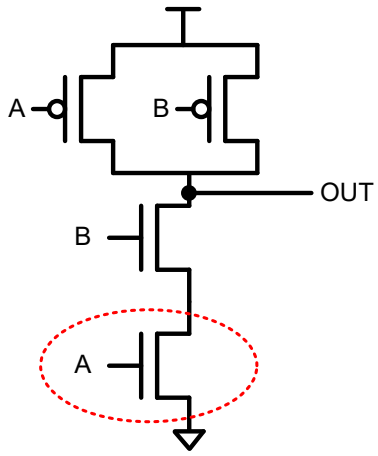
LAB-2 Scaling Property

1. Discuss how do fan-in, fan-out, and cascade stage affect delay and power?

*The Pattern you need:

Please test with the following pattern:
(To see how many patterns you need, ex: two inputs with va and vb, four inputs with va, vb, vc, and vd.)

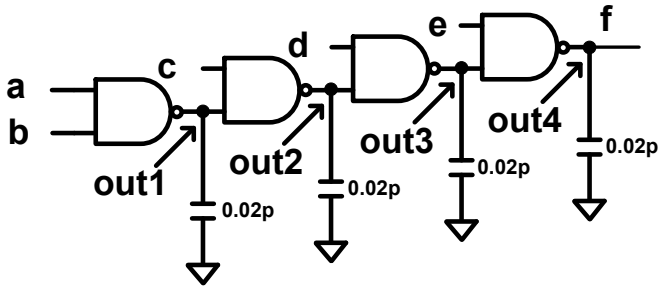
Note: Please put input A to the MOS transistor most near VDD or GND.




```
VA      A       0    pulse( 1.8   0   0.1n      0.1n      0.1n      9.9n      20n )
VB      B       0    1.8
VC      C       0    1.8
VD      D       0    1.8
VE      E       0    1.8
VF      F       0    1.8
VG      G       0    1.8
VH      H       0    1.8
.tran     0.1n     80n
```

Analysis of NAND fan-in, fan-out, and cascade-stage

1. Please Analysis and compare the 2-input NAND, 4-input NAND, 6-input NAND, 8-input NAND circuits under various fan-in with the same ***loading c=0.02p***. Please measure Delay time and Power consumption with transistor Size using PMOS W/L=1u/0.18u, NMOS W/L=1u/0.18u。(Using EXCEL to record Delay and Power according to various fan-in change.)
2. Please Analysis and compare the 4-input NAND, under various fan-out with ***loading c=0.05p, 0.1p, 0.15p, 0.2p, 0.25p, ...1p,*** . Please measure Delay time and Power consumption with transistor Size using PMOS W/L=1u/0.18u, NMOS W/L=1u/0.18u。(Using EXCEL to record Delay and Power according to various fan-out change.)
3. Please cascade the 2-input NAND as following, with fan-out loading c=0.02p.， Please measure Delay time and Power consumption with transistor Size using PMOS W/L=1u/0.18u, NMOS W/L=1u/0.18u。(Using EXCEL to record Delay and Power according to various cascade stage change.)



2-input NAND Cascade