

## PRE-LAB QUESTIONS OR EXERCISES

N/A

## PROBLEMS ENCOUNTERED

N/A

## REQUIREMENTS NOT MET

N/A

## FUTURE WORK/APPLICATIONS

This lab gave me a better understanding of how somewhat more complex circuit and logic designs can be made and implemented. In this lab we created a decoder that converted a binary number into HEX of an LED display. This is valuable because it gives insight as to how basic conversion works, even if this is at a really low level.

## PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

### Part A

$S_0$	$S_1$	$D_3(L)$	$D_2(H)$	$D_1(L)$	$D_0(H)$	$Y(L)$	$S_0$	$S_1$	$D_3(L)$	$D_2(H)$	$D_1(L)$	$D_0(H)$	$Y(L)$
0	0	-	-	-	0	0	L	L	-	-	-	L	H
0	0	-	-	-	1	1	L	L	-	-	-	H	L
0	1	-	-	0	-	0	L	H	-	-	L	-	L
0	1	-	-	1	-	1	L	H	-	-	H	-	H
1	0	-	0	-	-	0	H	L	-	L	-	-	H
1	0	-	1	-	-	1	H	L	-	H	-	-	L
1	1	0	-	-	-	0	H	H	L	-	-	-	L
1	1	1	-	-	-	1	H	H	H	-	-	-	H

Figure 1: Truth and voltage table for MUX

$$SOP = \bar{S}_0 \bar{S}_1 D_0 + \bar{S}_0 S_1 D_1 + S_0 \bar{S}_1 D_2 + S_0 S_1 D_3$$

$$POS = (S_0 + S_1 + D_0)(S_0 + \bar{S}_1 + D_1)(\bar{S}_0 + S_1 + D_2)(\bar{S}_0 + \bar{S}_1 + D_3)$$

Figure 2: Logic equations for MUX

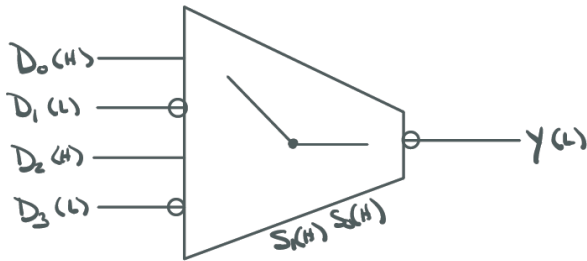


Figure 3: Functional Block Diagram for MUX

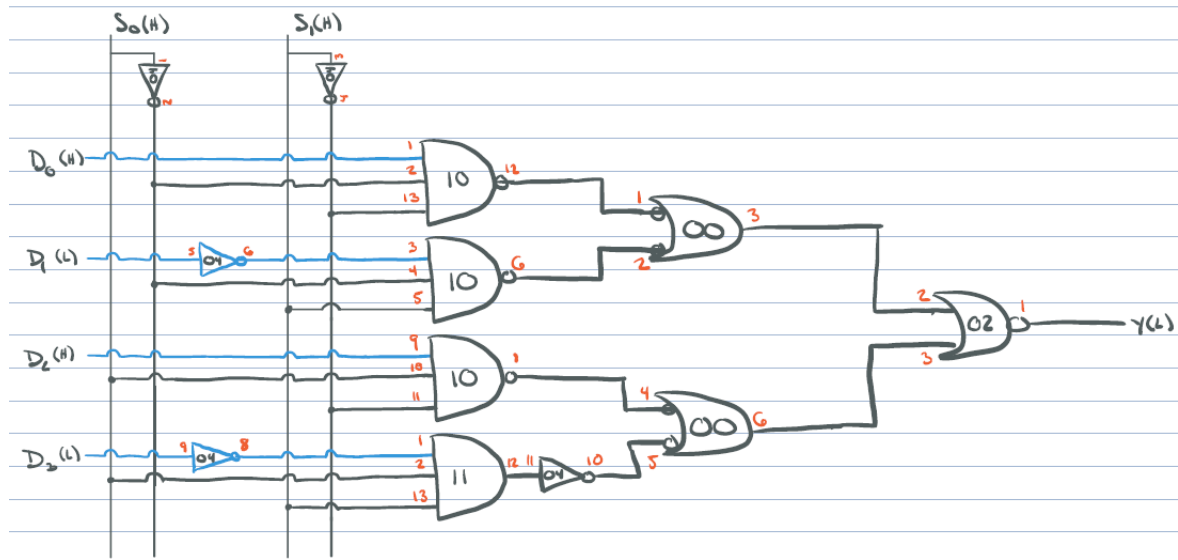


Figure 4: Circuit design for MUX

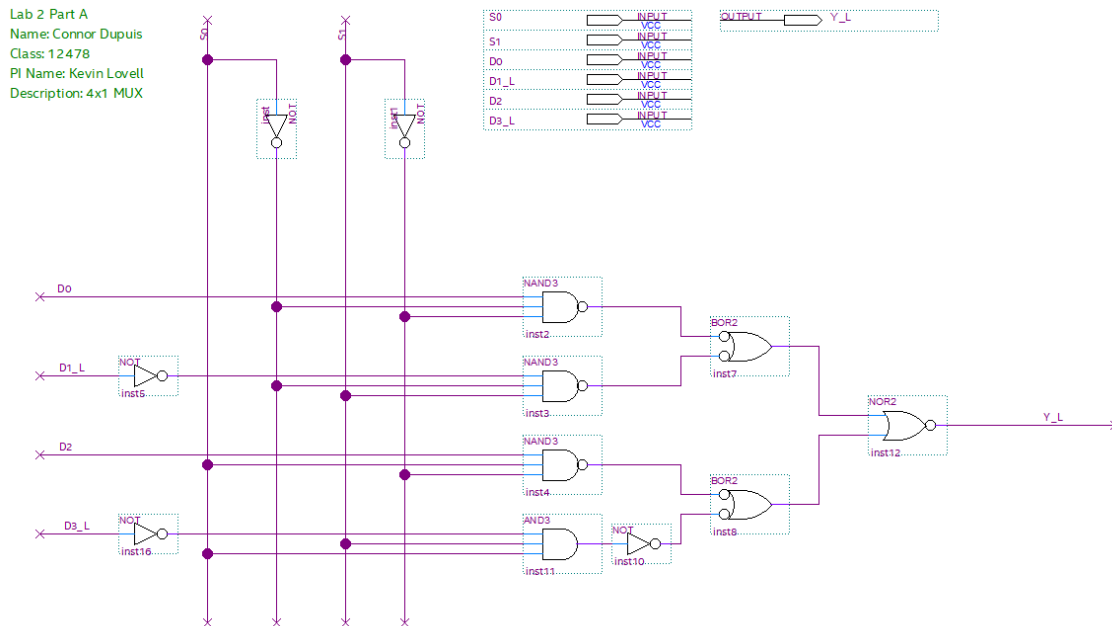
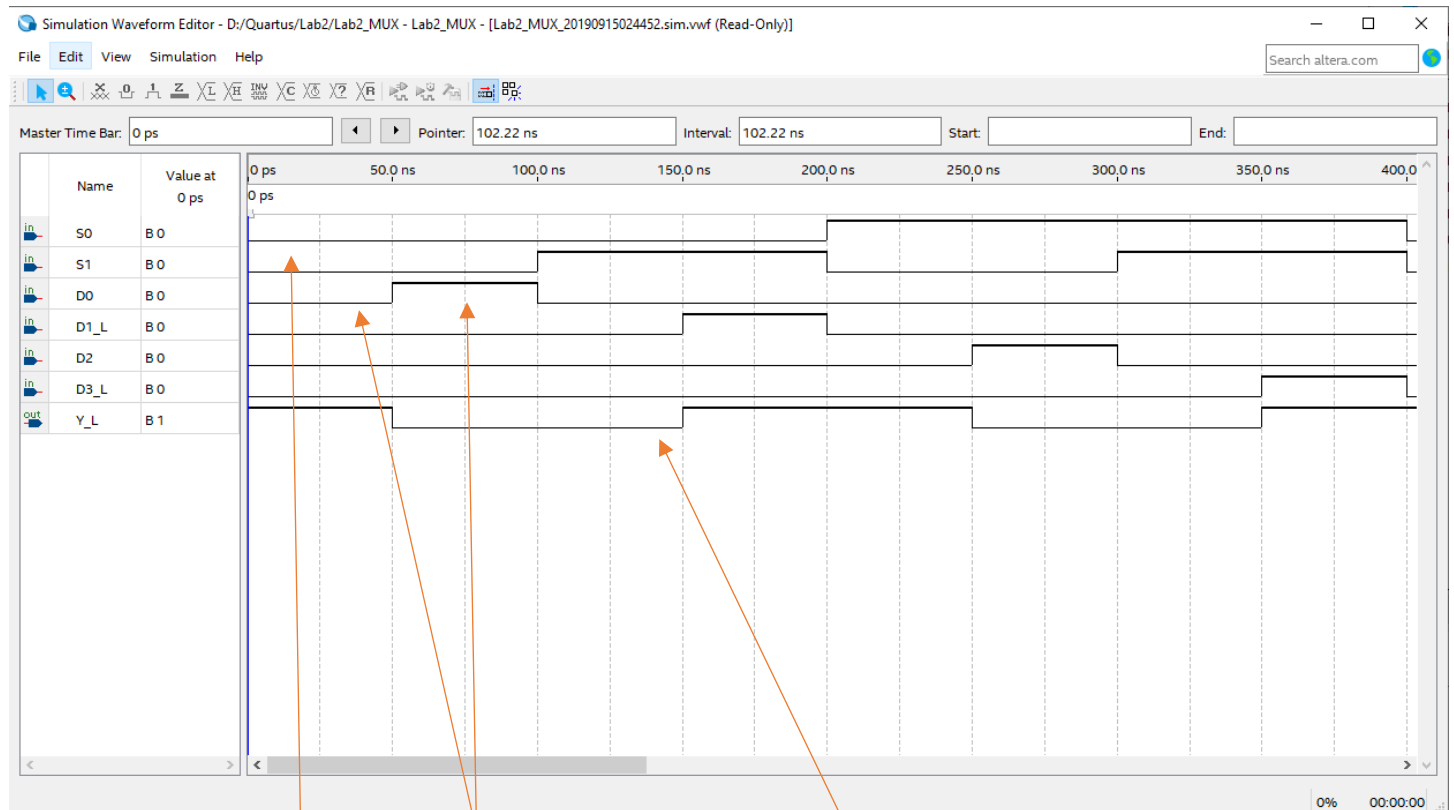


Figure 5: Quartus circuit design for MUX



S0 and S1 corresponds to which input it is directing to. 00 goes to D0, 01 goes to D1\_L, 10 goes to D2, and 11 goes to D3\_L.

When being directed to, all the inputs have a 0 and a 1. The arrow is pointing to when S0 and S1 are 00, then D0 is 0 then 1.

The final output of the MUX.

## Part B

T(L)	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	A	B	C	D	E	F	G	
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	1	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	1	0	1	1	9
1	1	0	1	0	1	1	1	0	1	1	1	A
1	1	0	1	1	0	0	1	1	1	1	1	B
1	1	1	0	0	1	0	0	1	1	1	0	C
1	1	1	0	1	0	1	1	1	1	0	1	D
1	1	1	1	0	1	0	0	1	1	1	1	E
1	1	1	1	1	1	0	0	0	1	1	1	F
0	-	-	-	-	1	1	1	1	1	1	1	G

Figure 6: Truth table for 7-segment LED

$$A \text{ POS : } (X_3 + X_2 + X_1 + \bar{X}_0)(X_3 + \bar{X}_2 + X_1 + X_0)(\bar{X}_3 + X_2 + \bar{X}_1 + \bar{X}_0)(\bar{X}_3 + \bar{X}_2 + X_1 + \bar{X}_0)$$

$$B \text{ POS : } (X_3 + \bar{X}_2 + X_1 + \bar{X}_0)(\bar{X}_3 + X_2 + X_1 + \bar{X}_0)(\bar{X}_3 + X_2 + \bar{X}_1 + \bar{X}_0)(\bar{X}_3 + \bar{X}_2 + X_1 + X_0)(\bar{X}_3 + \bar{X}_2 + \bar{X}_1 + X_0)(\bar{X}_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)$$

$$C \text{ POS : } (X_3 + X_2 + \bar{X}_1 + X_0)(\bar{X}_3 + \bar{X}_2 + X_1 + X_0)(\bar{X}_3 + \bar{X}_2 + \bar{X}_1 + X_0)(\bar{X}_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)$$

$$D \text{ POS : } (X_3 + X_2 + X_1 + \bar{X}_0)(X_3 + \bar{X}_2 + X_1 + X_0)(X_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)(\bar{X}_3 + X_2 + \bar{X}_1 + X_0)(\bar{X}_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)$$

$$E \text{ POS : } (X_3 + X_2 + X_1 + \bar{X}_0)(X_3 + X_2 + \bar{X}_1 + \bar{X}_0)(X_3 + \bar{X}_2 + X_1 + X_0)(X_3 + \bar{X}_2 + X_1 + \bar{X}_0)(X_3 + \bar{X}_2 + \bar{X}_1 + X_0)(X_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)$$

$$F \text{ POS : } (X_3 + X_2 + X_1 + \bar{X}_0)(X_3 + \bar{X}_2 + X_1 + X_0)(X_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)(X_3 + \bar{X}_2 + \bar{X}_1 + X_0)(\bar{X}_3 + X_2 + X_1 + \bar{X}_0)$$

$$G \text{ POS : } (X_3 + X_2 + X_1 + X_0)(X_3 + X_2 + X_1 + \bar{X}_0)(X_3 + \bar{X}_2 + \bar{X}_1 + \bar{X}_0)(\bar{X}_3 + \bar{X}_2 + X_1 + X_0)$$

Figure 7: Logic equations for 7-segment LED

T(L)	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	A	B	C	D	E	F	G	
H	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	H	H	H	H	H	H	L	L	H	3
H	L	H	L	L	L	H	H	L	L	H	H	4
H	L	H	L	H	H	L	H	H	L	H	H	5
H	L	H	H	L	H	L	H	H	H	H	H	6
H	L	H	H	H	H	H	H	L	L	L	L	7
H	H	L	L	L	H	H	H	H	H	H	H	8
H	H	L	L	H	H	H	H	H	L	H	H	9
H	H	L	H	L	H	H	H	L	H	H	H	A
H	H	L	H	H	L	L	H	H	H	H	H	B
H	H	H	L	L	H	L	L	H	H	H	L	C
H	H	H	L	H	L	H	H	H	H	L	H	D
H	H	H	H	L	H	L	L	H	H	H	H	E
H	H	H	H	H	H	L	L	L	H	H	H	F
L	-	-	-	-	H	H	H	H	H	H	H	G

Figure 8: Voltage table for 7-segment LED

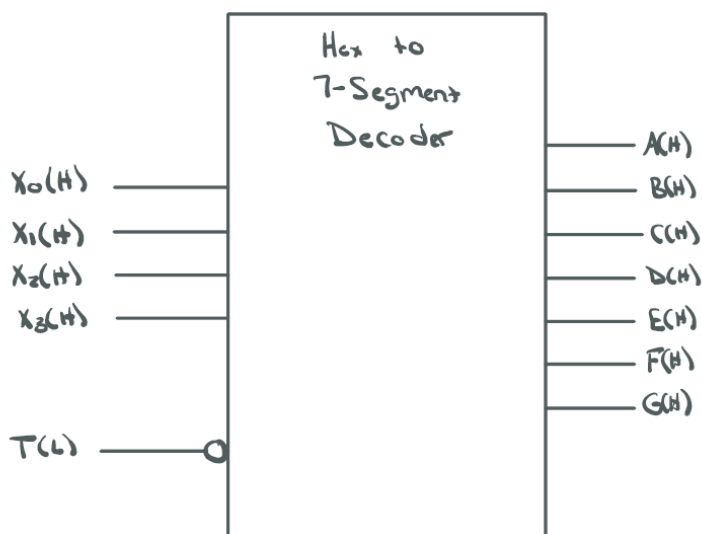


Figure 9: Functional block diagram for 7-segment LED

Lab 2 Part 8

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Description 7 Segment decoder

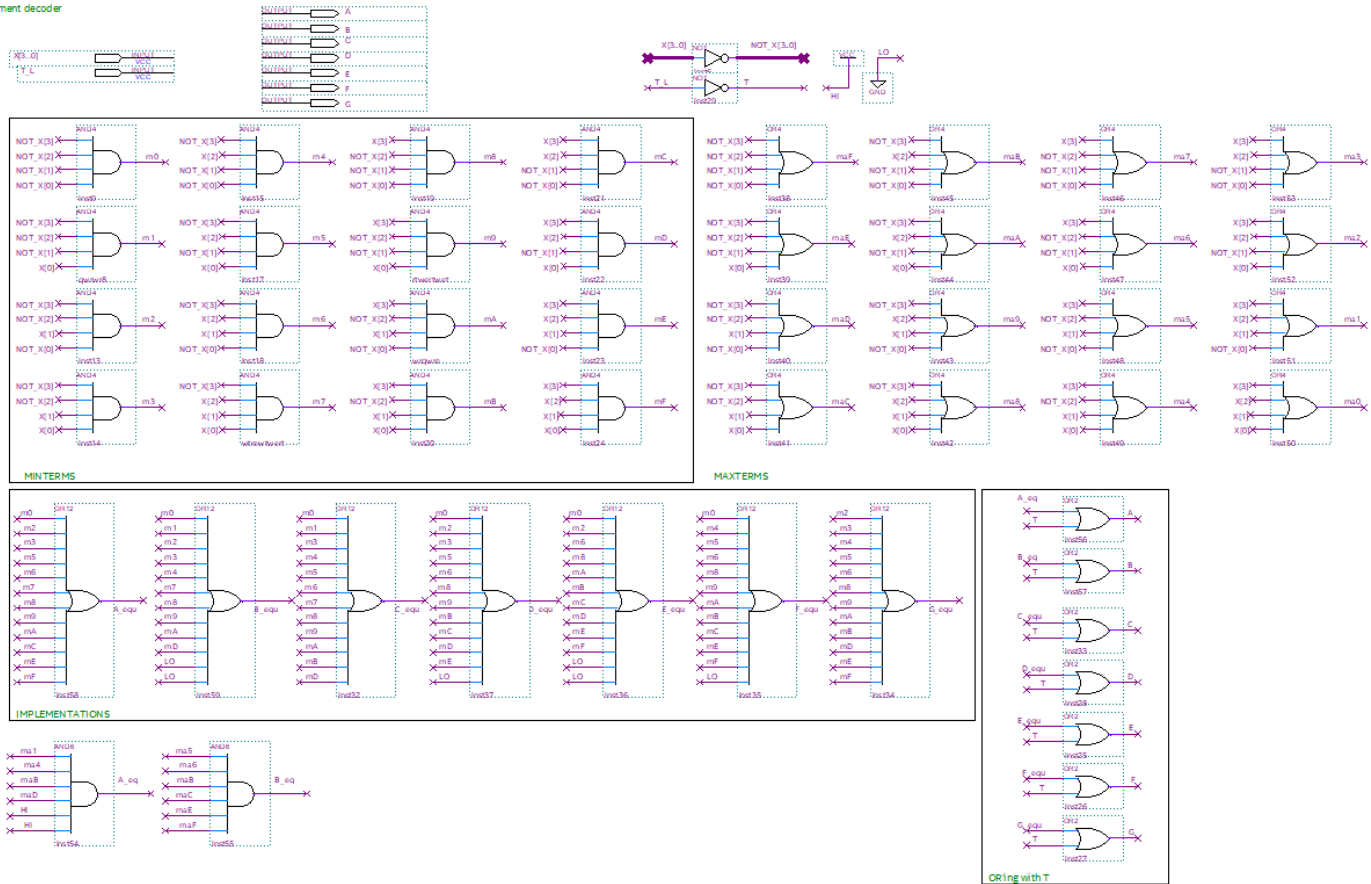
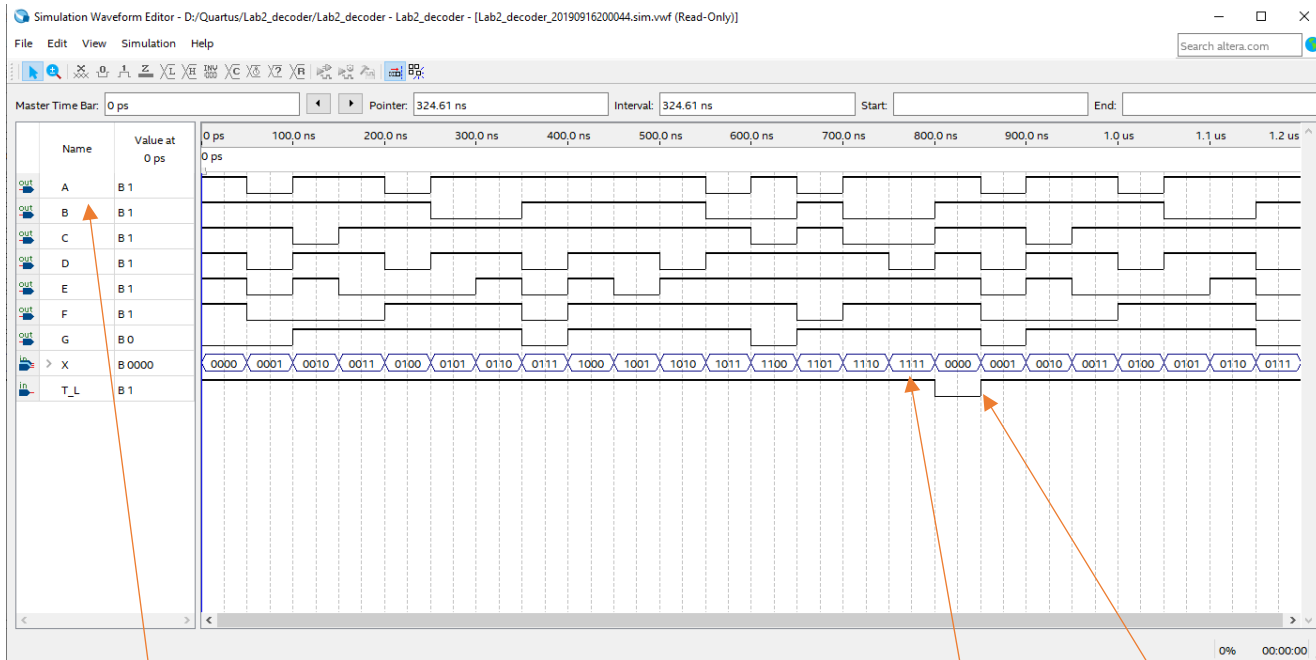


Figure 10: Quartus circuit design for 7-segment LED



The letter determines whether not that respective LED segment is on. High is on and Low is off

The inputs represent a binary number which is then translated into the hex via the LED segments previously described. IE. 1111 = 15 = F

T is a test input which if it is Low, then all the LED segments should turn on.