EEL 3701 — Digital Logic & Computer Systems
Revision **1**

Lab **4** Report: **ALU and CPU**

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

PRE-LAB QUESTIONS OR EXERCISES

Part 1 Questions:

1. If you were to make a complete (un-abbreviated) truth table for your ALU, how many rows would it need? (The answer should tell you why I did not want a simulation including ALL input combinations.)
   a. It Would take 2048 rows because there are 11 inputs.
2. What changes would be necessary to the design already made if you wanted to add two more functions, F=A NOR B and F=A XOR B, where XOR is exclusive or?
   a. You would need 6 input Mux's instead of the 4 input ones we are using to accommodate the added inputs.

Part 2 Questions:

1. Draw the single simple device that can be added to your circuit design to "remember" the last carry output. Specify the inputs and outputs for this device.
   a.
2. Will a divide by two work for all 4-bit 2's complement numbers? Explain.
   a. No, if you try to divide 7, you ill get 3.
3. Describe how you can take the 2's complement of a number, i.e., if A is loaded with a number, get the 2's complement of A into B.
   a. You can complement and add 0001 to that number.
4. Describe how you subtract with your CPU. Hint: See above question.
   a. Take the 2's complement and add that to the number you re trying to subtract from.
5. Suppose you're not allowed to use a flip-flop that has an asynchronous CLR or SET, how can you add a function that clears the contents of either A or B?
   a. Set all values of the inputs to 0, this will set REGA and REGB to all zeroes.

PROBLEMS ENCOUNTERED

N/A

REQUIREMENTS NOT MET

N/A

FUTURE WORK/APPLICATIONS

In this lab we learned how to make a simple CPU, which on itself can be applied ad used for various functions. By learning using this basic design we can build on it and if we wanted, add even ore functions, applications and abilities. CPUs are staples in almost every electronic device, and it is valuable to understand how one works and operates.

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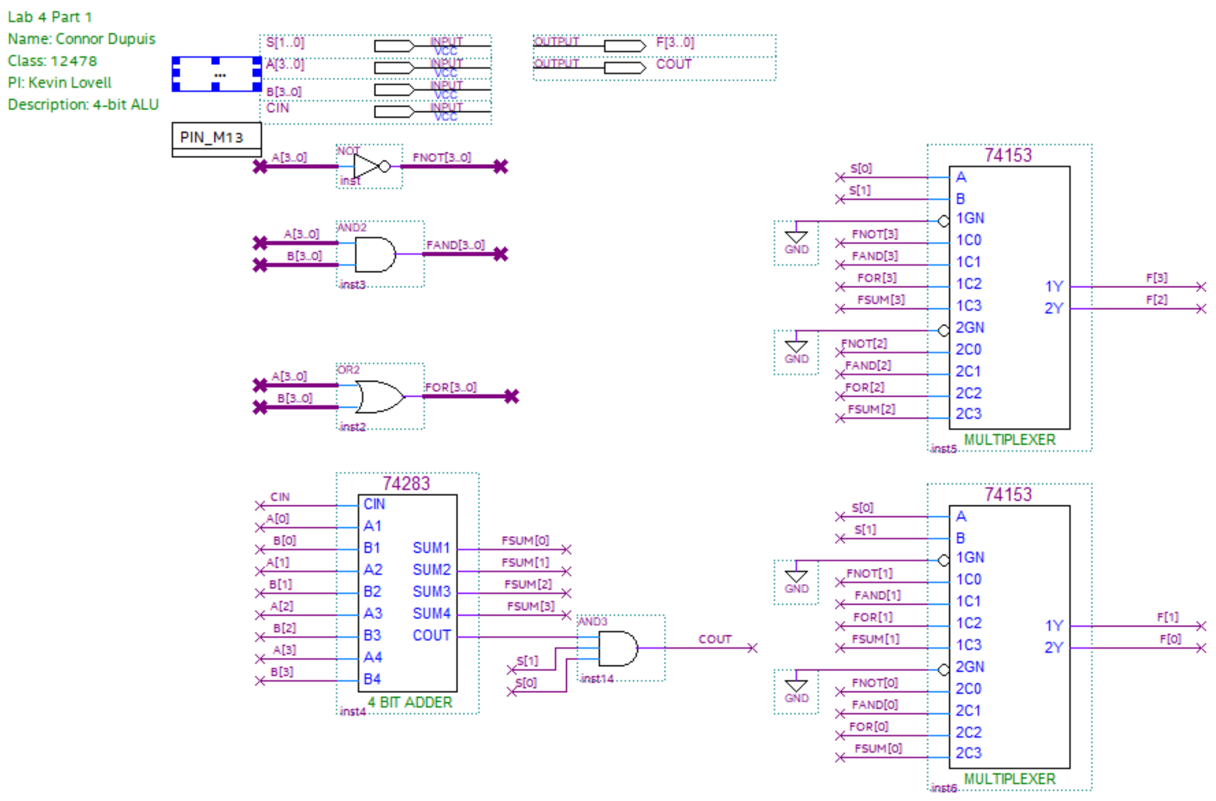
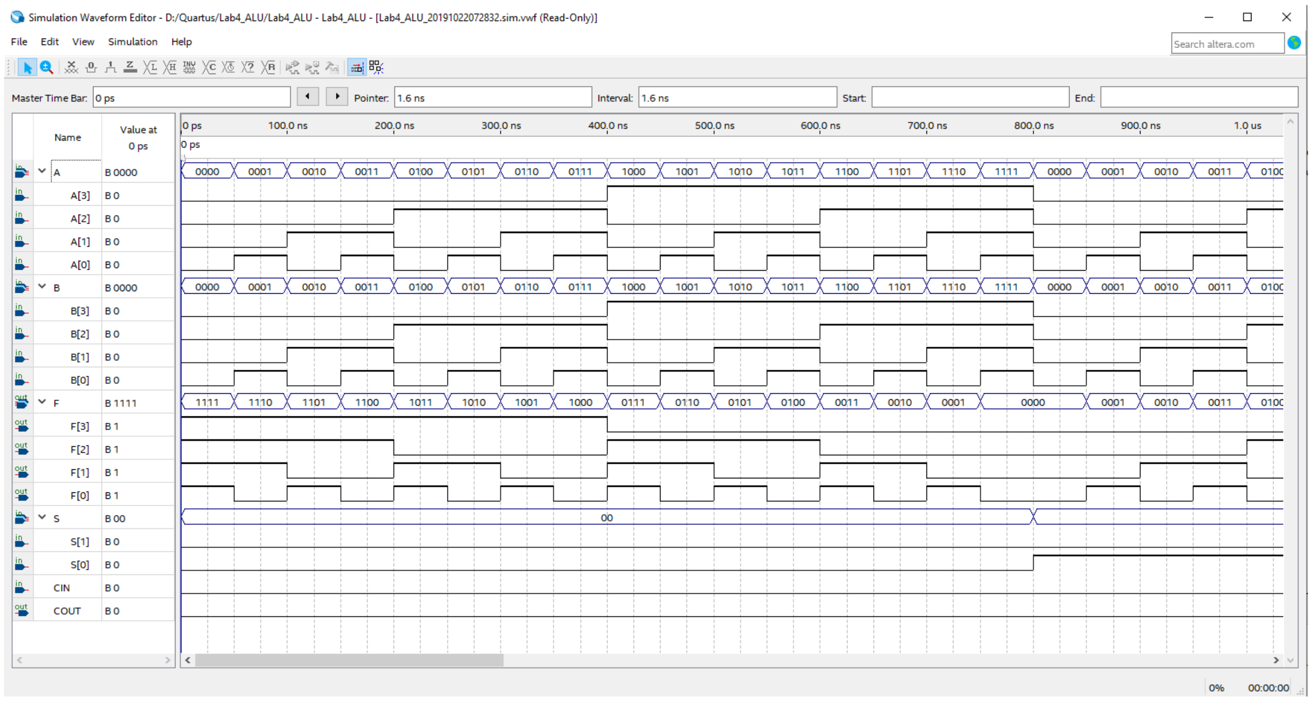
PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Part 1:




Simulation Waveform Editor - D:/Quartus/Lab4_ALU/Lab4_ALU - Lab4_ALU - [Lab4_ALU_20191022072832.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 1.6 ns
Interval: 1.6 ns
Start:
End:
Name
Value at 0 ps
0 ps
100.0 ns
200.0 ns
300.0 ns
400.0 ns
500.0 ns
600.0 ns
700.0 ns
800.0 ns
900.0 ns
1.0 us
A B 0000
A[3] B 0
A[2] B 0
A[1] B 0
A[0] B 0
B B 0000
B[3] B 0
B[2] B 0
B[1] B 0
B[0] B 0
F B 1111
F[3] B 1
F[2] B 1
F[1] B 1
F[0] B 1
S B 00
S[1] B 0
S[0] B 0
CIN B 0
COUT B 0
A: 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100
B: 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100
F: 1111 1110 1101 1100 1011 1010 1001 1000 0111 0110 0101 0100 0011 0010 0001 0000 0001 0010 0011 0100
S: 00
0%
00:00:00

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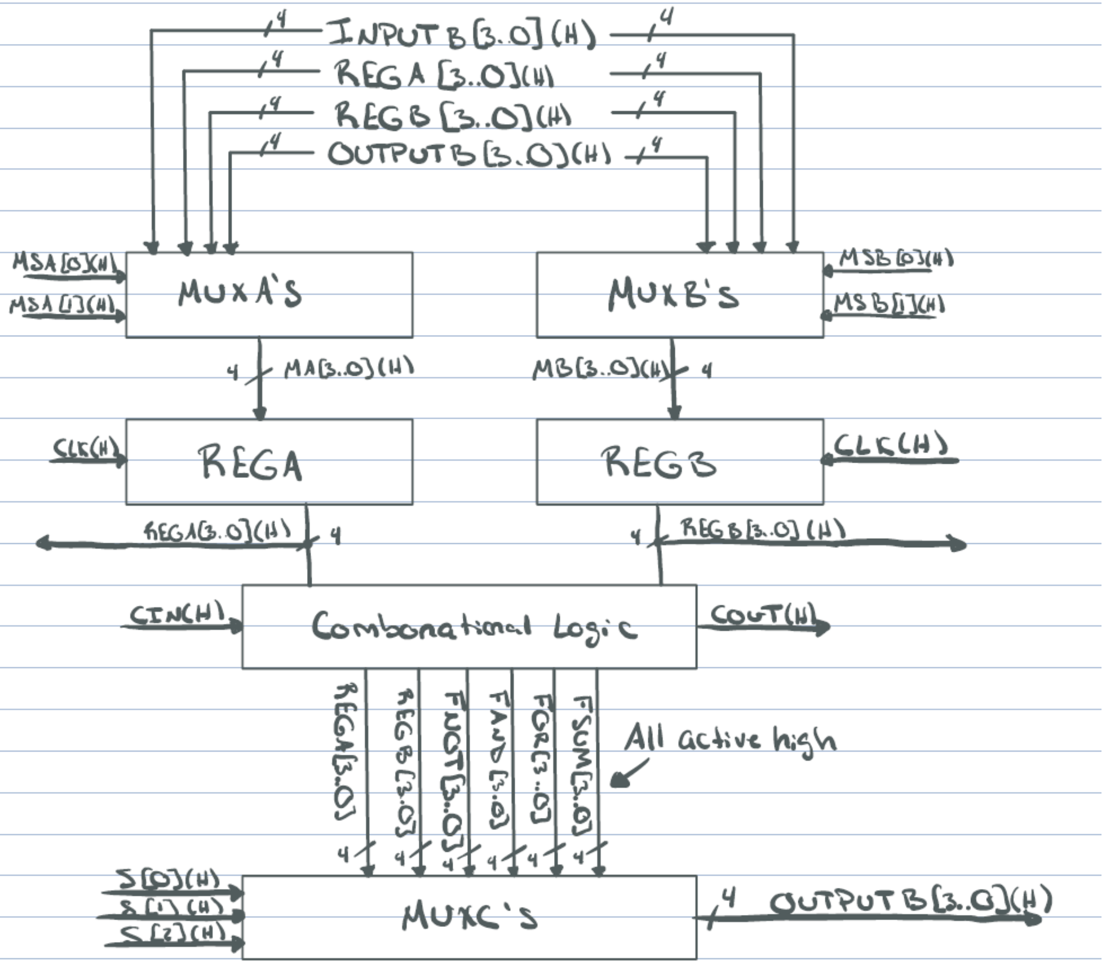
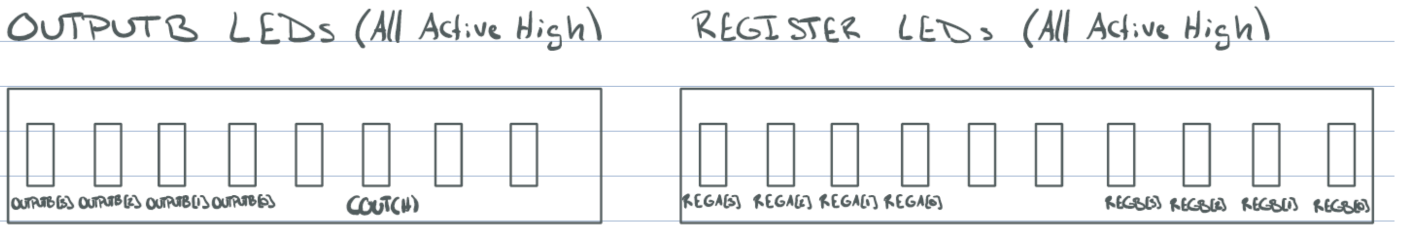
Part 2:





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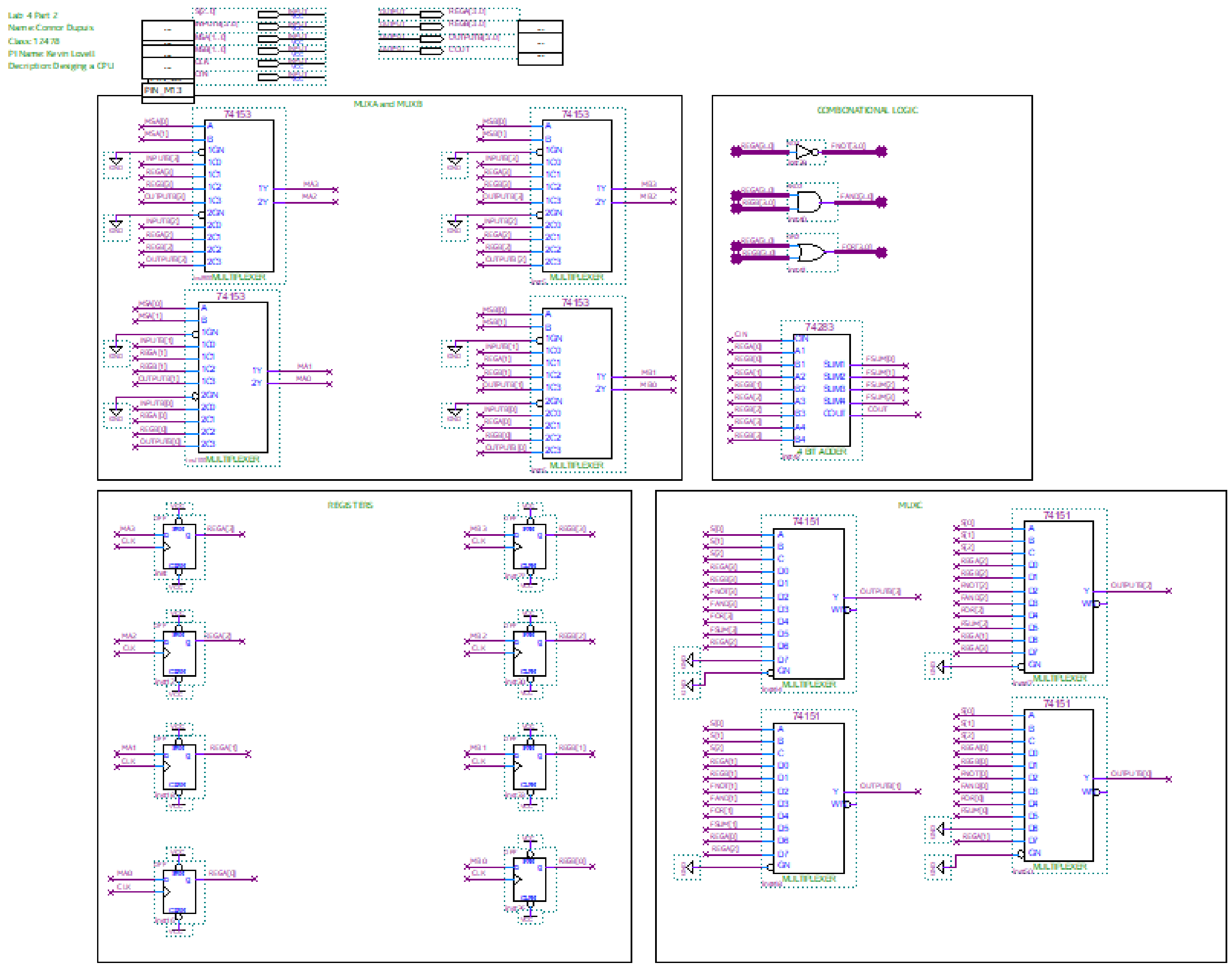
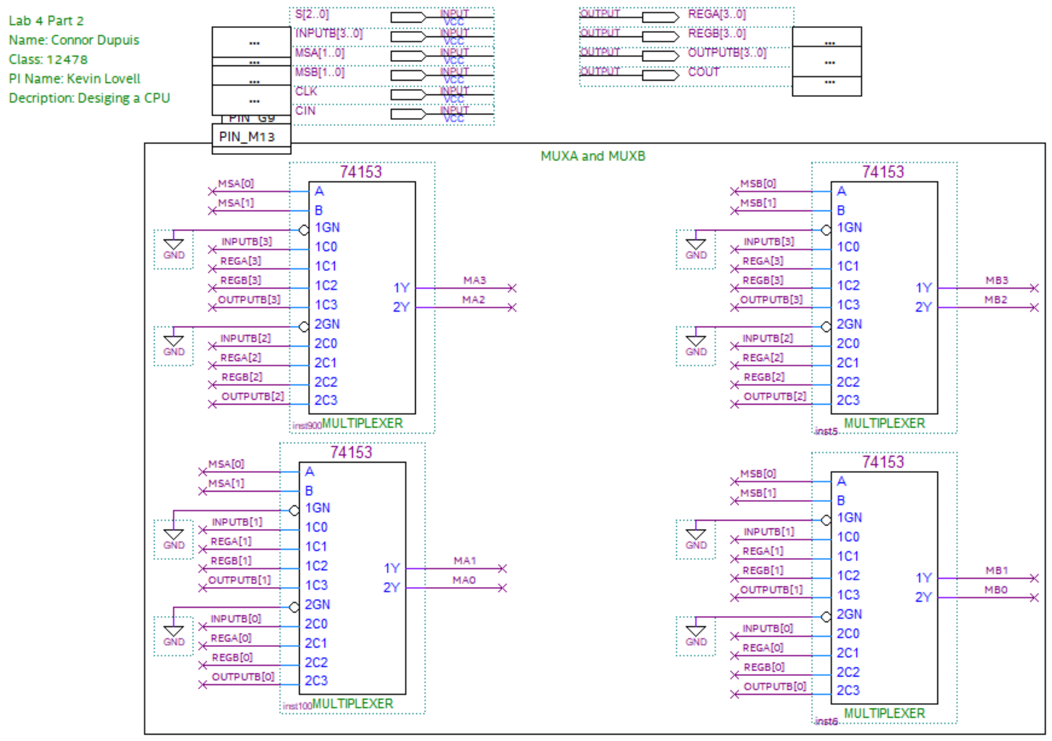
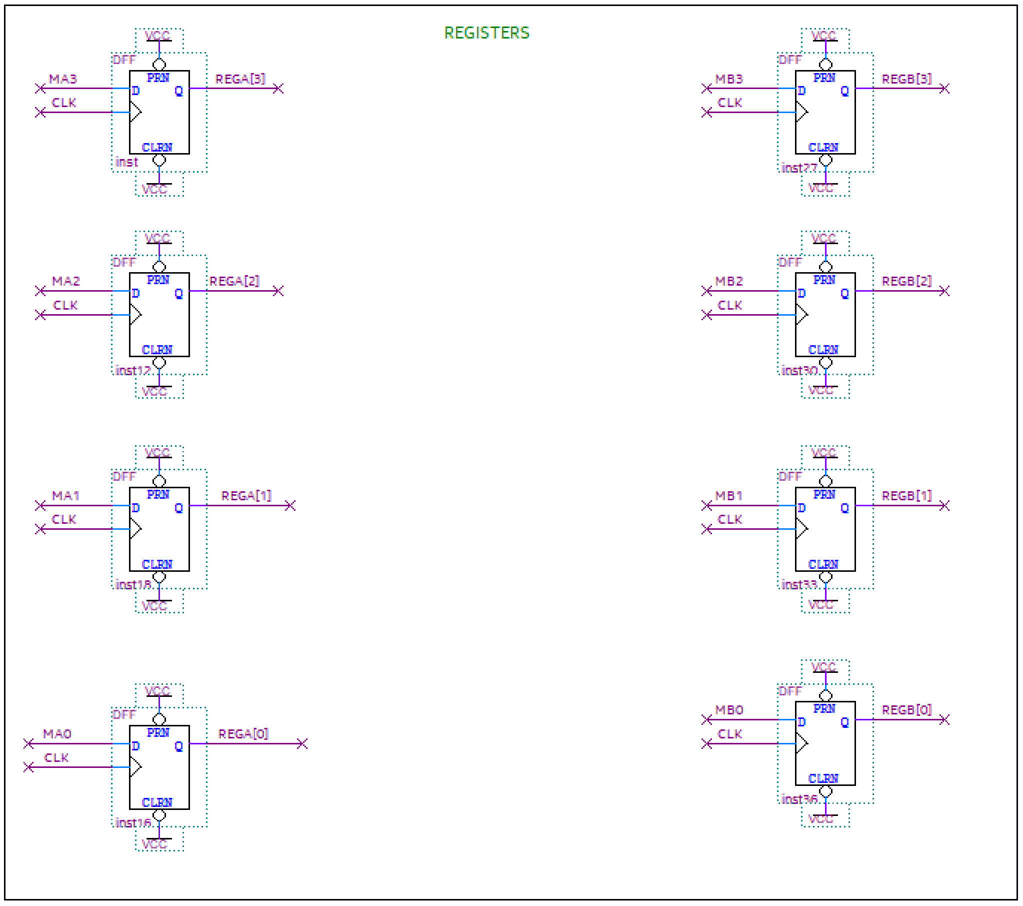
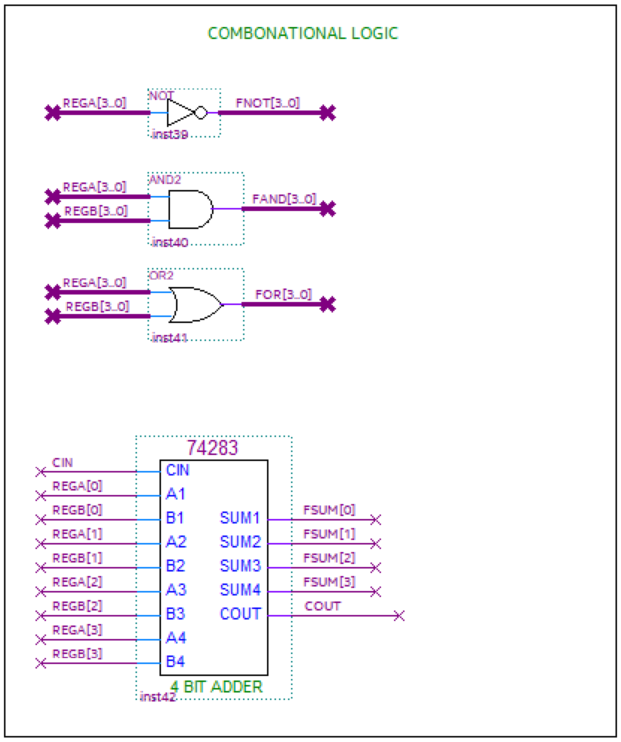
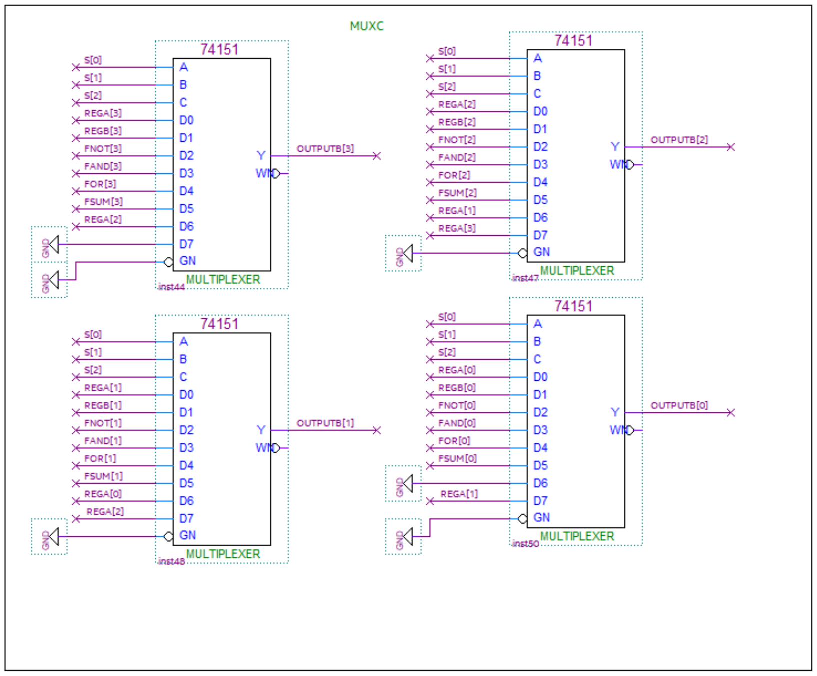


Individual Pictures Below:






COMBONATIONAL LOGIC
REGA[3..0]
NOT
FNOT[3..0]
inst39
AND2
REGB[3..0]
FAND[3..0]
inst40
OR2
FOR[3..0]
inst41
74283
CIN
A1
B1
A2
B2
A3
B3
A4
B4
SUM1
SUM2
SUM3
SUM4
COUT
FSUM[0]
FSUM[1]
FSUM[2]
FSUM[3]
4 BIT ADDER
inst42


MUXC
74151
MULTIPLEXER
S[0]
S[1]
S[2]
OUTPUTB[3]
OUTPUTB[2]
OUTPUTB[1]
OUTPUTB[0]
GND
inst44
inst47
inst48
inst50

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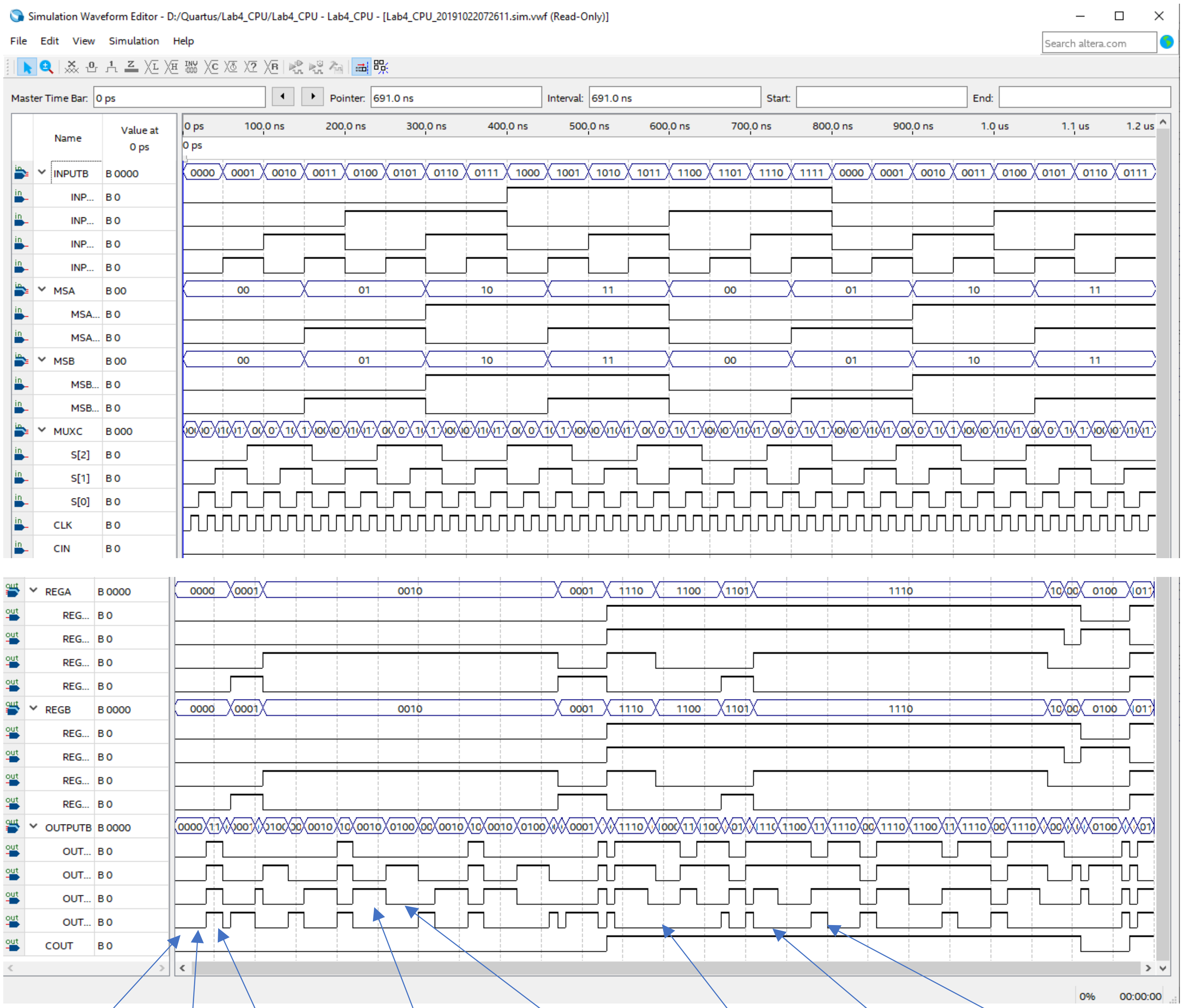

Simulation Waveform Editor - D:/Quartus/Lab4_CPU/Lab4_CPU - Lab4_CPU - [Lab4_CPU_20191022072611.sim.vwf (Read-Only)]

Master Time Bar: 0 ps   Pointer: 691.0 ns   Interval: 691.0 ns   Start: End:

Displays the REGA to the output	Displays the REGB to the output	Displays the complement of REGA to the output	Displays (REGA and REGB) to the output	Displays (REGA or REGB) to the output	Displays (REGA + REGB) to the output	Displays REGA shifted left one bit to the output	Displays the REGA shifted right one bit to the output

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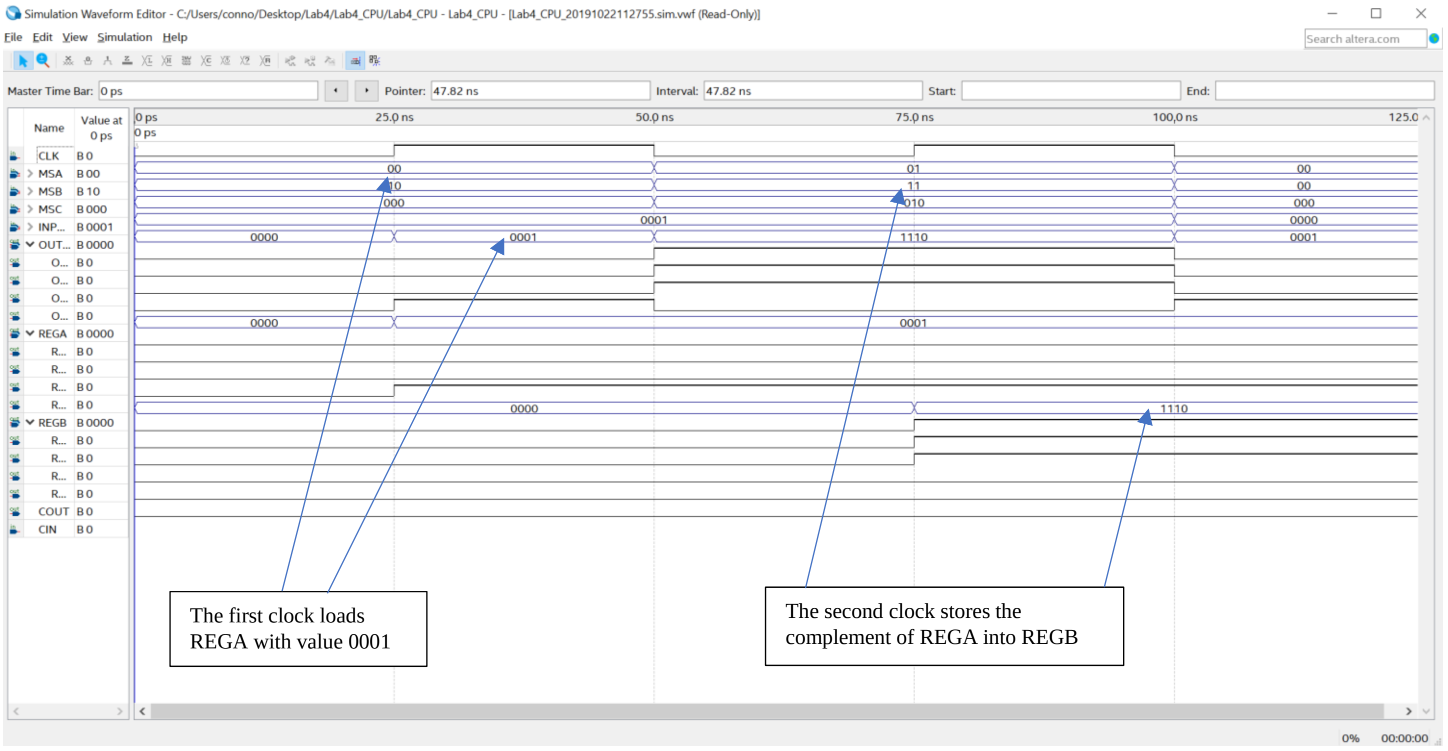
Table 4: Sample table for Pre-lab Requirement 4.

	MSA	MSB	MSC	Input	Cin	RegA	RegB	Output	RegA+	RegB+	Output+	Cout+	Description
a.	00	10	000	0001	0	?	?	?	0001	?	0001	0	Loads REGA with 0001
	01	11	010	0001	0	0001	?	1110	0001	1110	1110	0	Stores the Complement of A into B
	00	10	000	0110	0	?	?	?	0110	?	0110	0	Loads REGA with 0110
b.	01	00	001	1001	0	0110	?	0000	0110	1001	1001	0	Loads REGB with 1001
	11	10	011	1001	0	0110	1001	0000	0000	1001	0000	0	ANDs AB and Stores it in A
	00	10	000	0110	0	?	?	?	0110	?	0110	0	Loads REGA with 0110
c.	01	00	001	1001	0	0110	?	0000	0110	1001	1001	0	Loads REGB with 1001
	01	11	100	1001	0	0110	1001	1111	0110	1111	1111	0	ORs AB and Stores it in B
d.	00	00	000	0001	0	?	?	?	0001	0001	0001	0	Loads REGA and REGB with 0001
	11	10	101	0001	0	0001	0001	0010	0010	0001	0011	0	Sums A+B and Stores it in A
e.	00	10	000	1101	0	?	?	?	1101	?	1101	0	Loads REGA with 1101
	01	11	110	1101	0	1101	?	1010	1101	1010	1010	0	Shifts A Left and Stores it in B
	00	10	000	0011	0	?	?	?	0011	?	0011	0	Load REGA with 0011 (3)
	01	00	001	0111	0	0011	?	0000	0011	0111	0111	0	Load REGB with 0111 (7)
	11	10	101	0111	0	0011	0111	1010	1010	0111	0001	1	Sum A+B and Store it in A
	01	00	001	0100	0	1010	0111	0111	1010	0100	0100	1	Load REGB with 0100 (4)
	11	10	100	0100	0	1010	0100	1110	1110	0100	1110	1	Stores A OR B in A
	11	10	111	0100	0	1110	0100	0111	1110	0100	0011	0	Shifts A right and Stores it in A
f.	11	10	111	0100	0	0111	0100	0011	0011	0100	0001	0	Shifts A right and Stores it in A
	11	10	010	0100	0	0011	0100	1100	1100	0100	0011	1	Complements A and Stores it in A
	01	00	001	0011	0	1100	0100	0100	1100	0011	0011	1	Loads REGB with 0011 (3)
	11	10	011	0011	0	1100	0011	0000	0000	0011	0000	0	ANDs AB and Stores it in A
	11	10	110	0011	0	0000	0011	0000	0000	0011	0000	0	Shifts A Left and Stores it in A

Simple Functions:

A.



Simulation Waveform Editor - C:/Users/conno/Desktop/Lab4/Lab4_CPU/Lab4_CPU - Lab4_CPU - [Lab4_CPU_20191022112755.sim.vwf (Read-Only)]

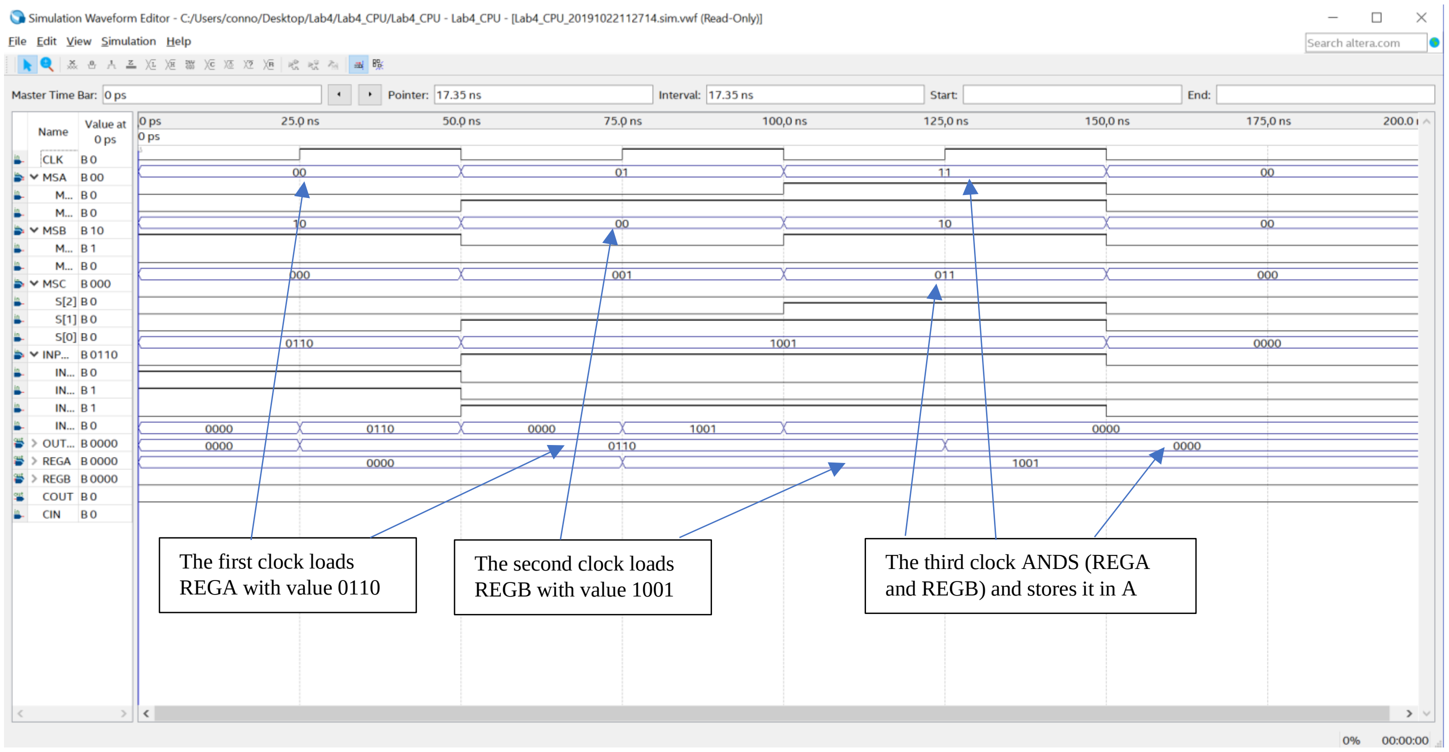
Master Time Bar: 0 ps Pointer: 47.82 ns Interval: 47.82 ns Start: End:

Name	Value at 0 ps	Waveform
CLK	B 0	
MSA	B 00	00, 01, 00
MSB	B 10	10, 11, 00
MSC	B 000	000, 010, 000
INP...	B 0001	0001, 0000
OUT...	B 0000	0000, 0001, 1110, 0001
REGA	B 0000	0000, 0001
REGB	B 0000	0000, 1110
COUT	B 0	
CIN	B 0	

The first clock loads REGA with value 0001

The second clock stores the complement of REGA into REGB

B.


Simulation Waveform Editor - C:/Users/conno/Desktop/Lab4/Lab4_CPU/Lab4_CPU - Lab4_CPU - [Lab4_CPU_20191022112714.sim.vwf (Read-Only)]

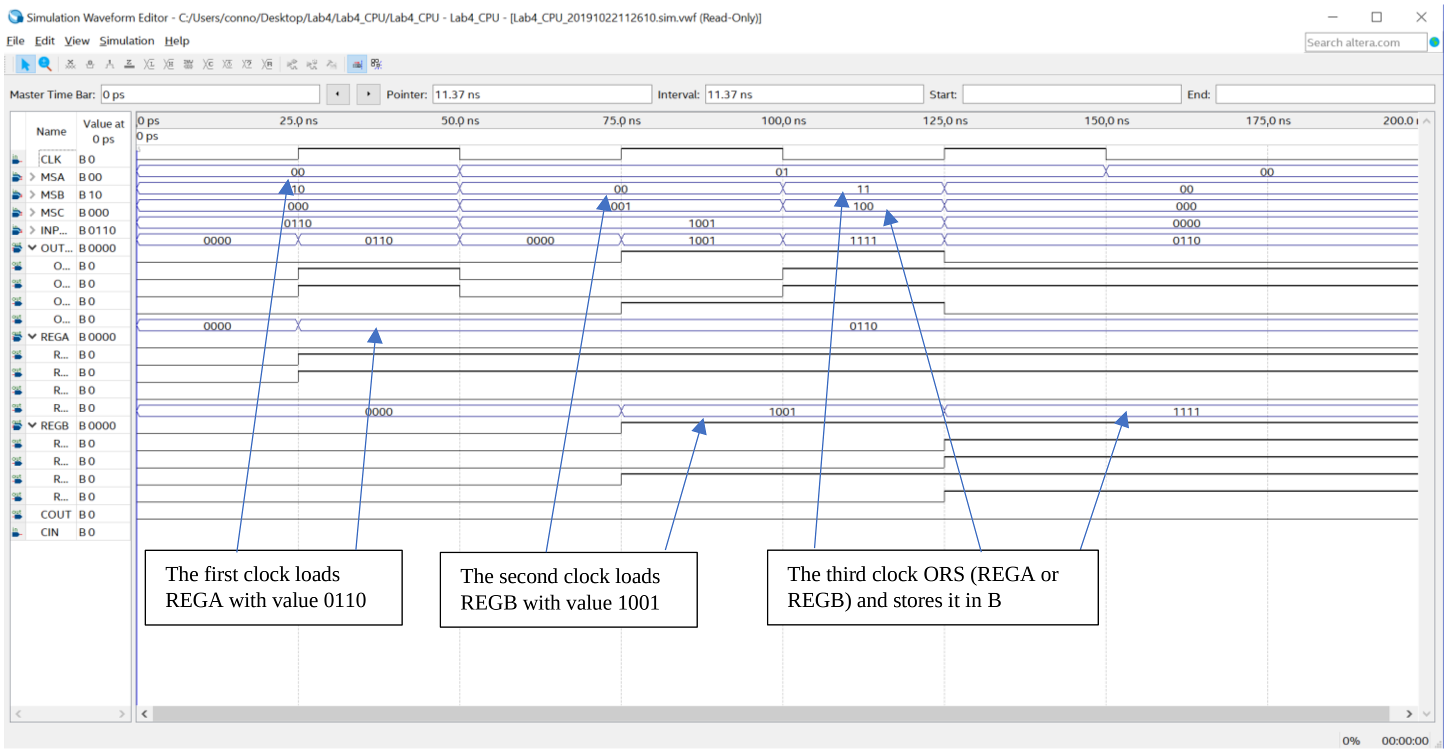
Master Time Bar: 0 ps Pointer: 17.35 ns Interval: 17.35 ns Start: End:

The first clock loads REGA with value 0110

The second clock loads REGB with value 1001

The third clock ANDS (REGA and REGB) and stores it in A

C.


Simulation Waveform Editor - C:/Users/conno/Desktop/Lab4/Lab4_CPU/Lab4_CPU - Lab4_CPU - [Lab4_CPU_20191022112610.sim.vwf (Read-Only)]

Master Time Bar: 0 ps Pointer: 11.37 ns Interval: 11.37 ns Start: End:

The first clock loads REGA with value 0110

The second clock loads REGB with value 1001

The third clock ORS (REGA or REGB) and stores it in B

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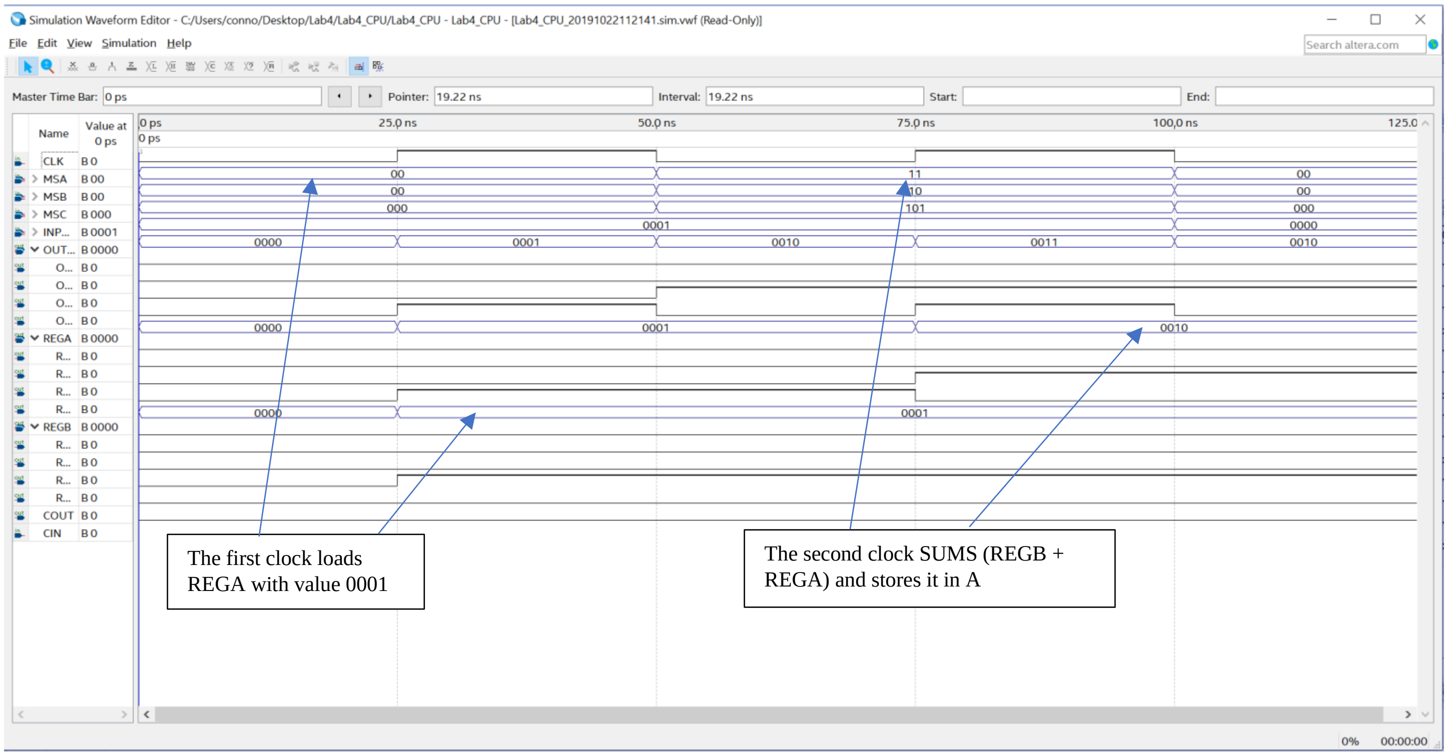
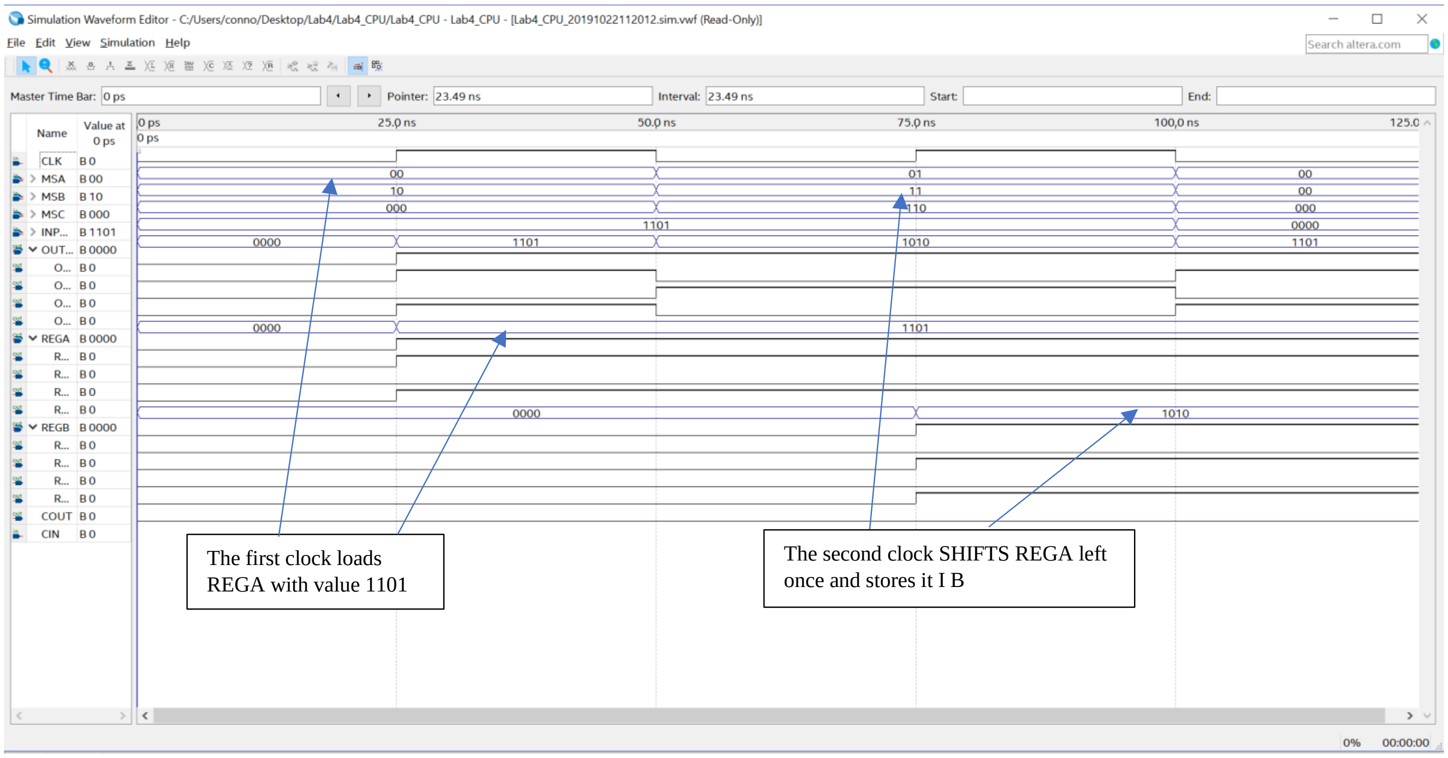
D.



The first clock loads REGA with value 0001

The second clock SUMS (REGB + REGA) and stores it in A

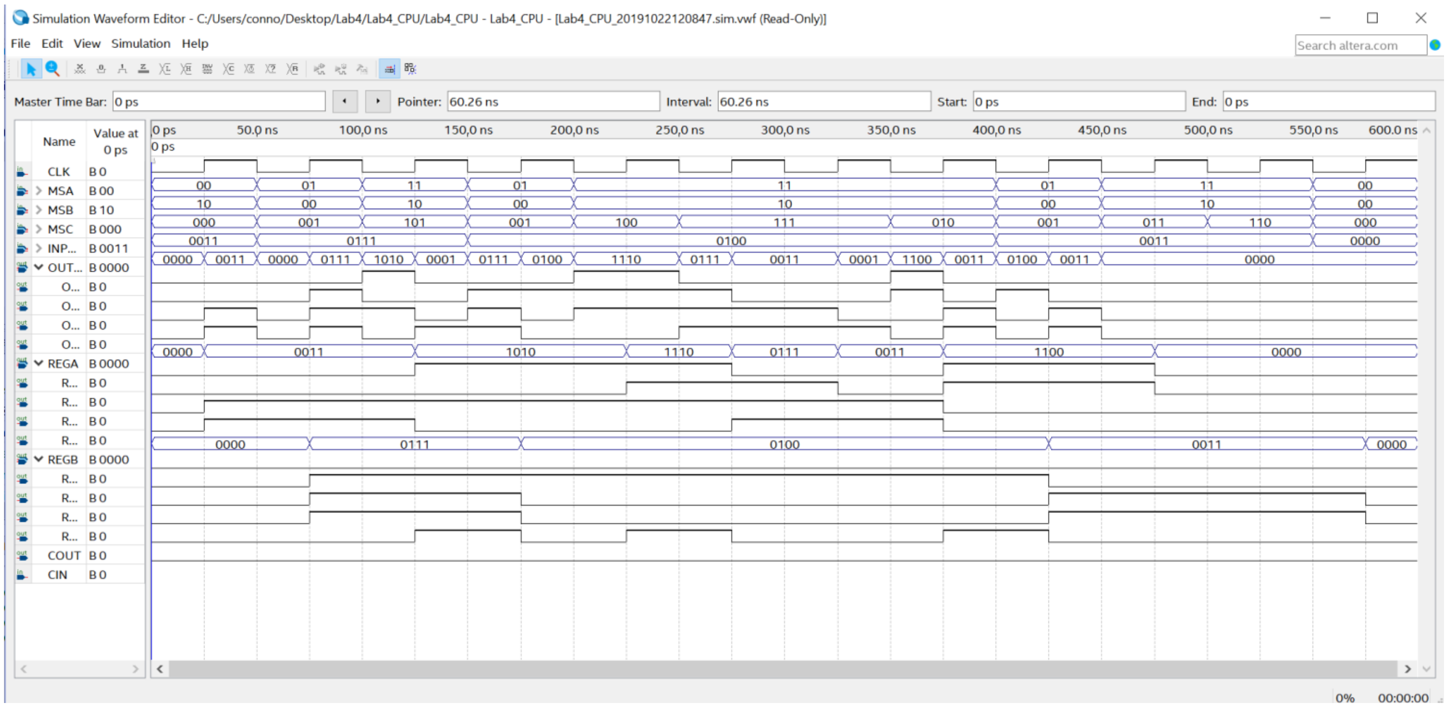
E.



The first clock loads REGA with value 1101

The second clock SHIFTS REGA left once and stores it I B

F.


Simulation Waveform Editor - C:/Users/conno/Desktop/Lab4/Lab4_CPU/Lab4_CPU - Lab4_CPU - [Lab4_CPU_20191022120847.sim.vwf (Read-Only)]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 60.26 ns
Interval: 60.26 ns
Start: 0 ps
End: 0 ps
Name
Value at 0 ps
0 ps
50.0 ns
100.0 ns
150.0 ns
200.0 ns
250.0 ns
300.0 ns
350.0 ns
400.0 ns
450.0 ns
500.0 ns
550.0 ns
600.0 ns
CLK B 0
MSA B 00
MSB B 10
MSC B 000
INP... B 0011
OUT... B 0000
O... B 0
REGA B 0000
R... B 0
REGB B 0000
COUT B 0
CIN B 0
00 01 11 01 11 01 11 00
10 00 10 00 10 00 10 00
000 001 101 001 100 111 010 001 011 110 000
0011 0111 0100 0011 0000
0000 0011 0000 0111 1010 0001 0111 0100 1110 0111 0011 0001 1100 0011 0100 0011 0000
0000 0011 1010 1110 0111 0011 1100 0000
0000 0111 0100 0011 0000
0%
00:00:00