EEL 3701 — Digital Logic & Computer Systems
Revision 1
Lab 3 Report: A Debounced Switch and Counters

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

PRE-LAB QUESTIONS OR EXERCISES

N/A

PROBLEMS ENCOUNTERED

N/A

REQUIREMENTS NOT MET

N/A

FUTURE WORK/APPLICATIONS

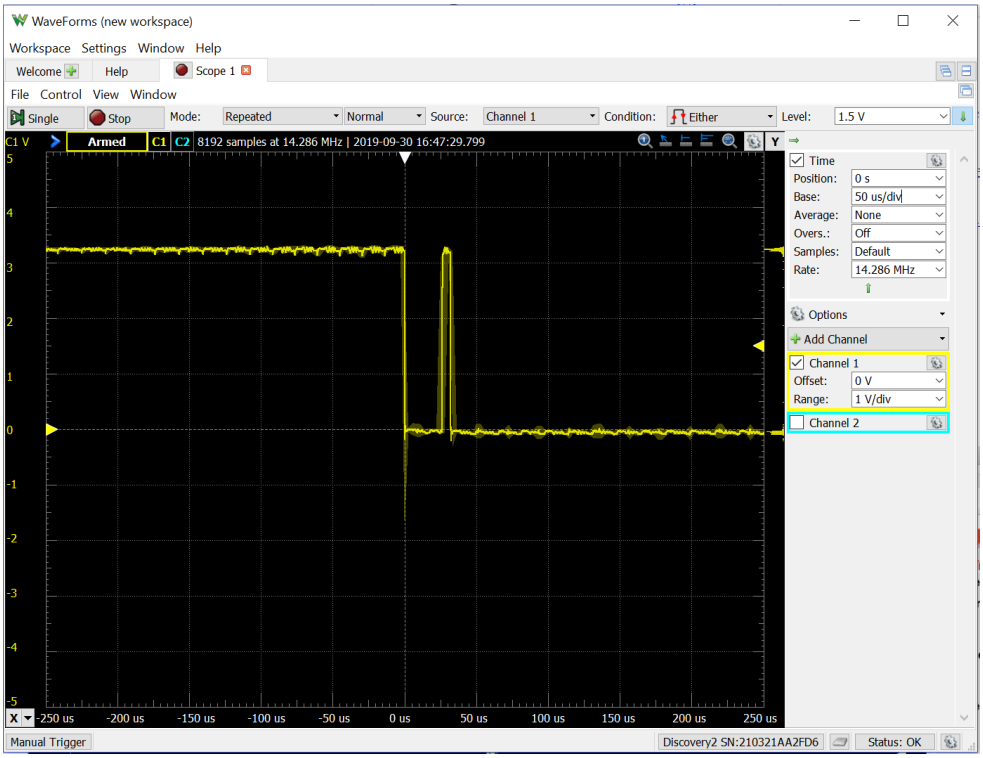
In this lab we use debouncing switch circuit with SPDT switch to act our input for our counters. We also use flip-flops and implement them to create our counter. This understanding of these circuit designs leads to further implementation such as more complex state machines and counters that are even more complex.

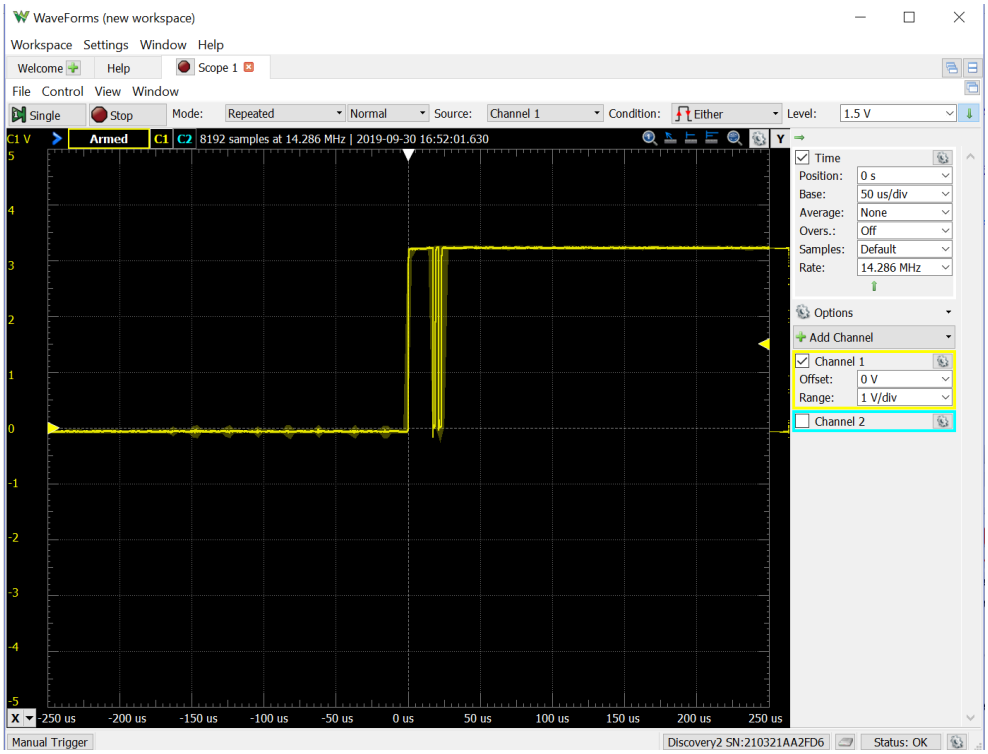
EEL 3701 — Digital Logic & Computer Systems
Revision 1
Lab 3 Report: A Debounced Switch and Counters

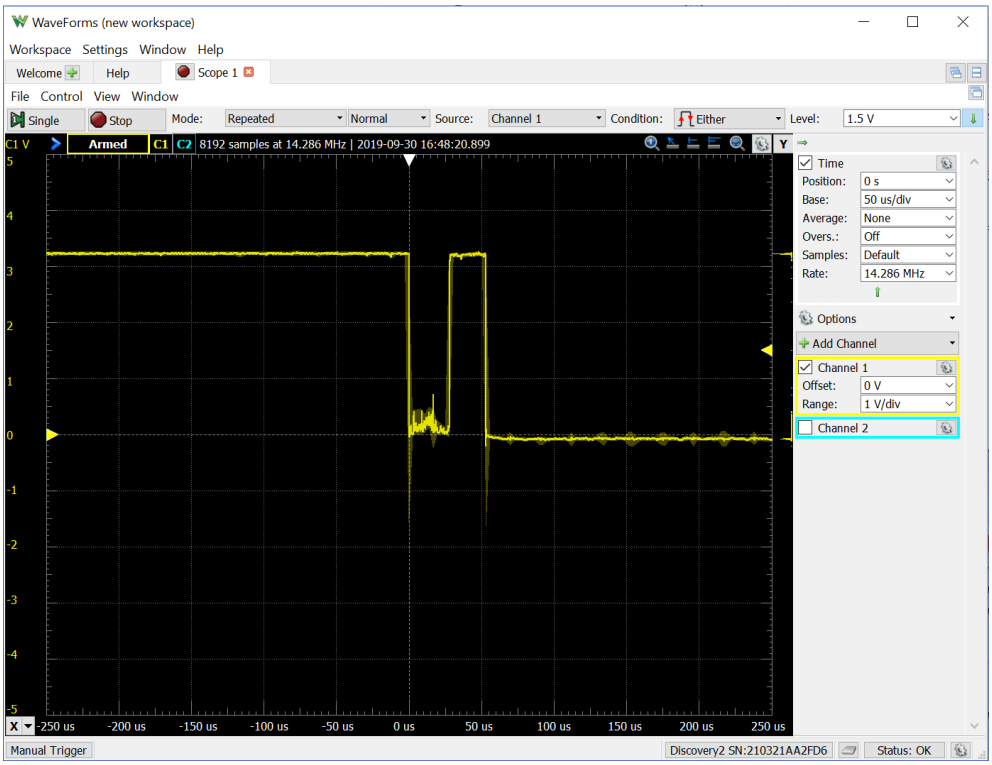
Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Bouncing SPST Circuit

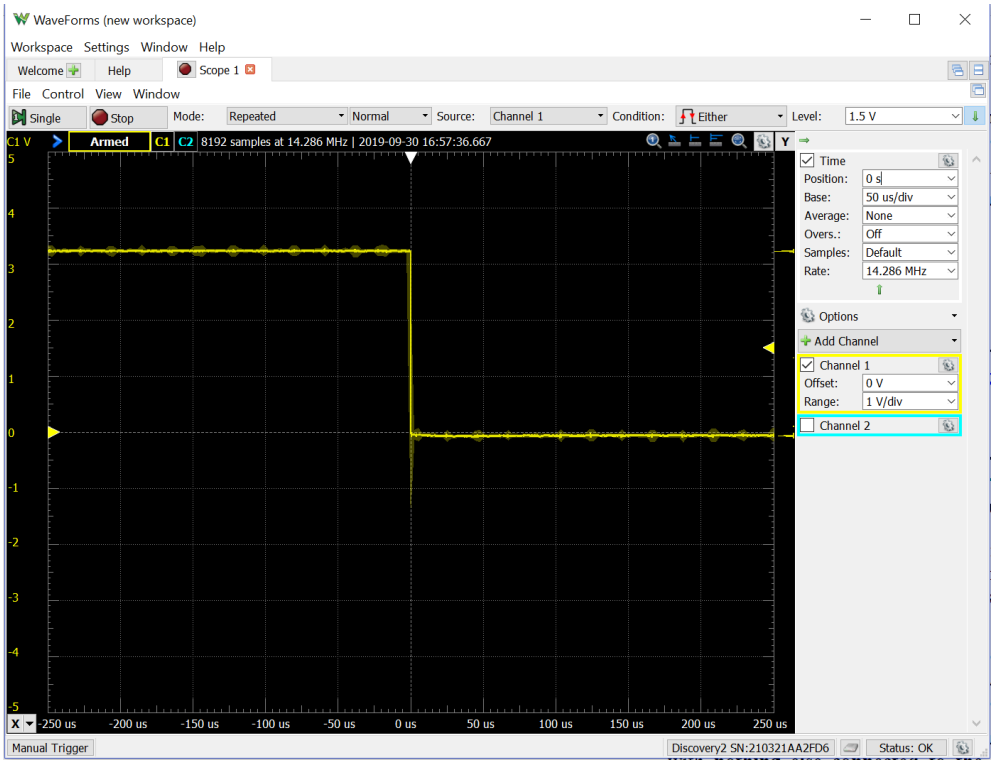


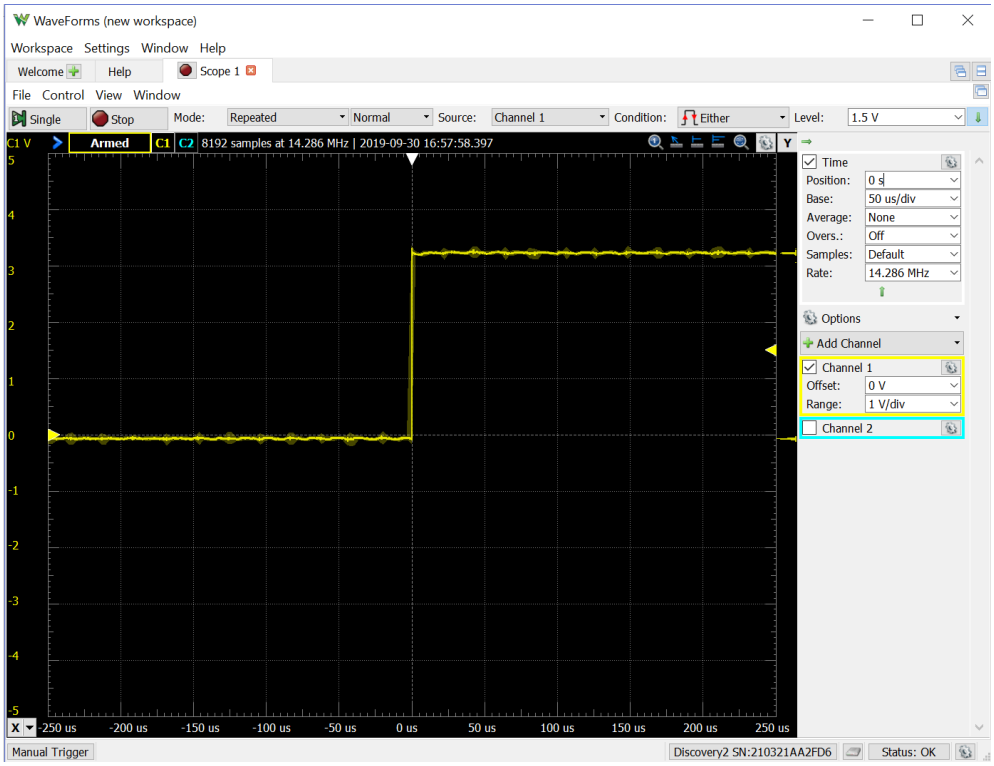




The clocks that would occur would be the number of times it bounced. In this case it bounced 5 times total so it would be 5 clocks assuming forward.

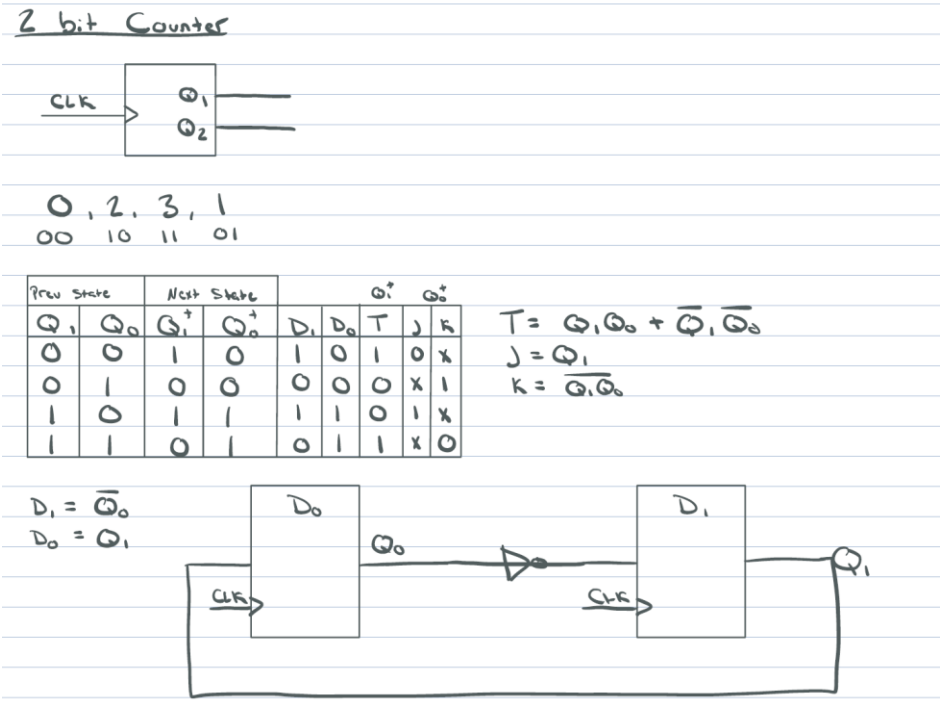
Debounce SPDT Circuit





This switch would only bounces once, so only one clock is recorded.

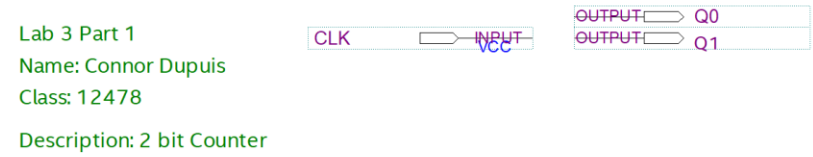
2-bit Counter

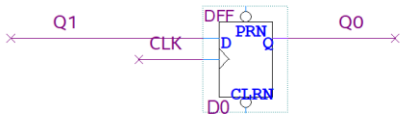


EEL 3701 — Digital Logic & Computer Systems
Revision 1

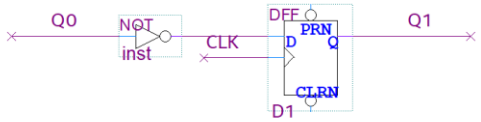
Lab 3 Report: A Debounced Switch and Counters

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

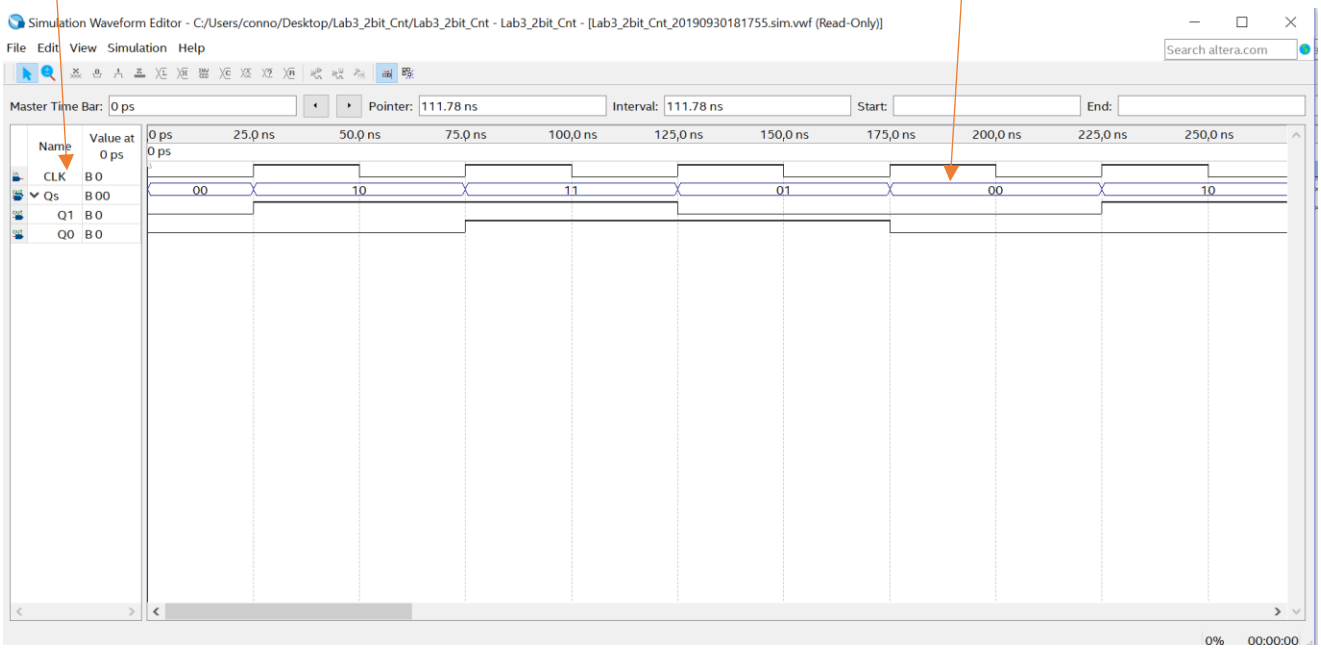




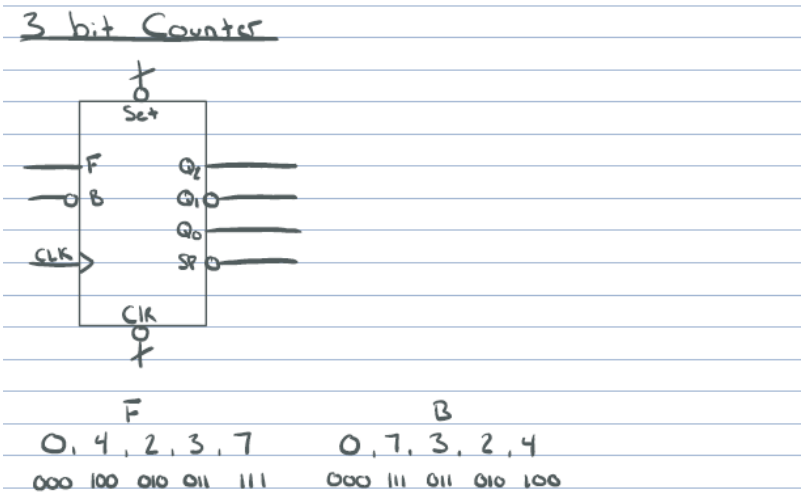
Clock is rising, meaning the count is increasing.



The counting number in binary. 0-2-3-1.



3-bit Counter



EEL 3701 — Digital Logic & Computer Systems
Revision 1
Lab 3 Report: **A Debounced Switch and Counters**

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

		Prev State			Next State					
F	B	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
1	0	0	0	0	1	0	0	1	0	0
1	0	0	0	1	X	X	X	X	X	X
1	0	0	1	0	0	1	1	0	1	1
1	0	0	1	1	1	1	1	1	1	1
1	0	1	0	0	0	1	0	0	1	0
1	0	1	0	1	X	X	X	X	X	X
1	0	1	1	0	X	X	X	X	X	X
1	0	1	1	1	0	0	0	0	0	X
0	1	0	0	0	1	1	1	1	1	1
0	1	0	0	1	X	X	X	X	X	X
0	1	0	1	0	1	0	0	1	0	0
0	1	0	1	1	0	1	0	0	1	0
0	1	1	0	0	0	0	0	0	0	0
0	1	1	0	1	X	X	X	X	X	X
0	1	1	1	0	X	X	X	X	X	X
0	1	1	1	1	0	1	1	0	1	1
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	X	X	X	X	X	X
0	0	0	1	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1	0	1	1
0	0	1	0	0	1	0	0	1	0	0
0	0	1	0	1	X	X	X	X	X	X
0	0	1	1	0	X	X	X	X	X	X
0	0	1	1	1	1	1	1	1	1	1

$D_2 = \bar{F}B\bar{Q}_2 + \bar{F}B\bar{Q}_2\bar{Q}_0 + F\bar{B}\bar{Q}_2\bar{Q}_1 + F\bar{B}\bar{Q}_2Q_0$

$D_1 = \bar{F}B\bar{Q}_2\bar{Q}_1 + \bar{F}Q_1Q_0 + FQ_2\bar{Q}_1 + F\bar{B}\bar{Q}_2Q_1 + \bar{F}\bar{B}Q_1$

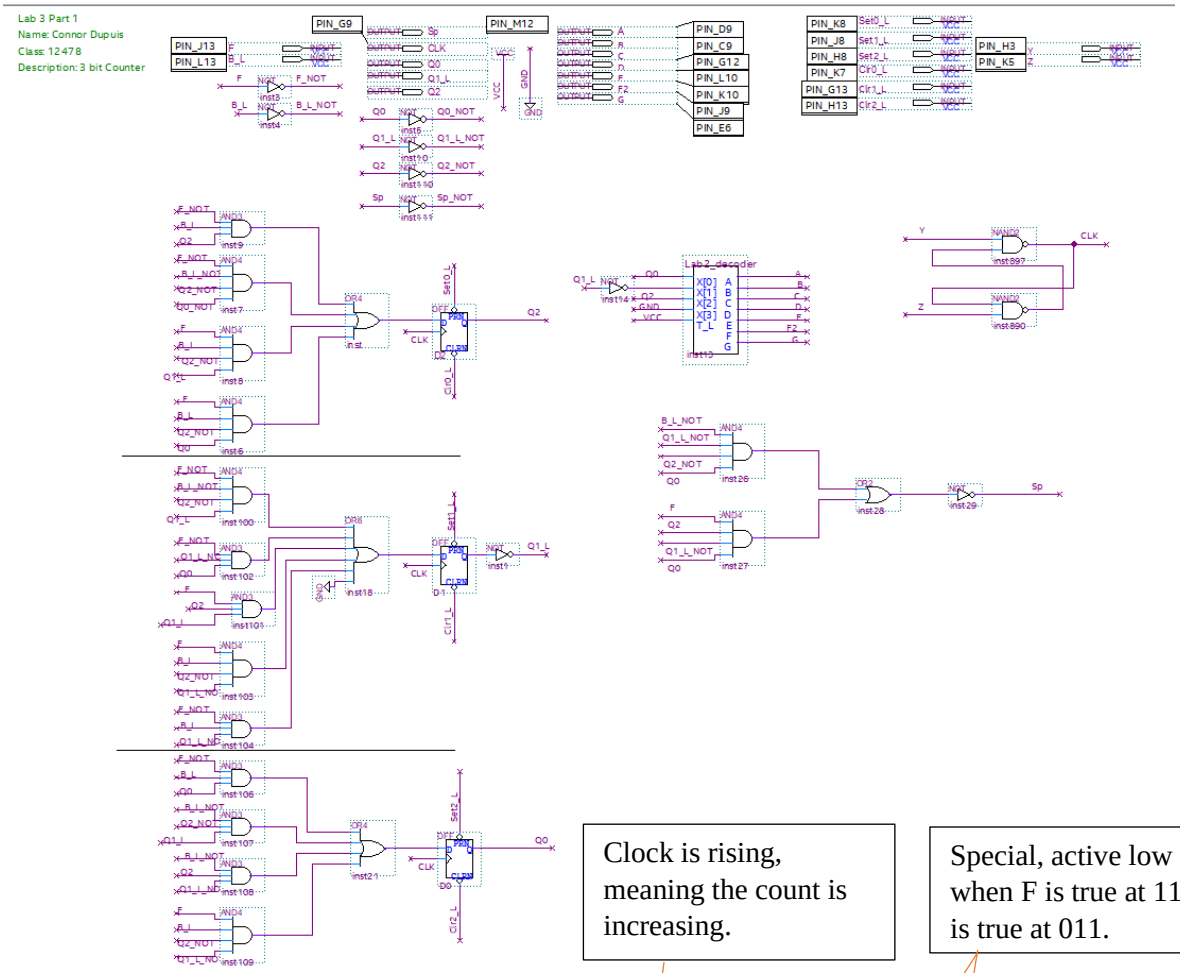
$D_0 = \bar{F}\bar{B}Q_0 + B\bar{Q}_2\bar{Q}_1 + BQ_2Q_1 + F\bar{B}\bar{Q}_2Q_1$

$S_P = Q_1B\bar{Q}_2Q_0 + FQ_2Q_1Q_0$

EEL 3701 — Digital Logic & Computer Systems
Revision 1

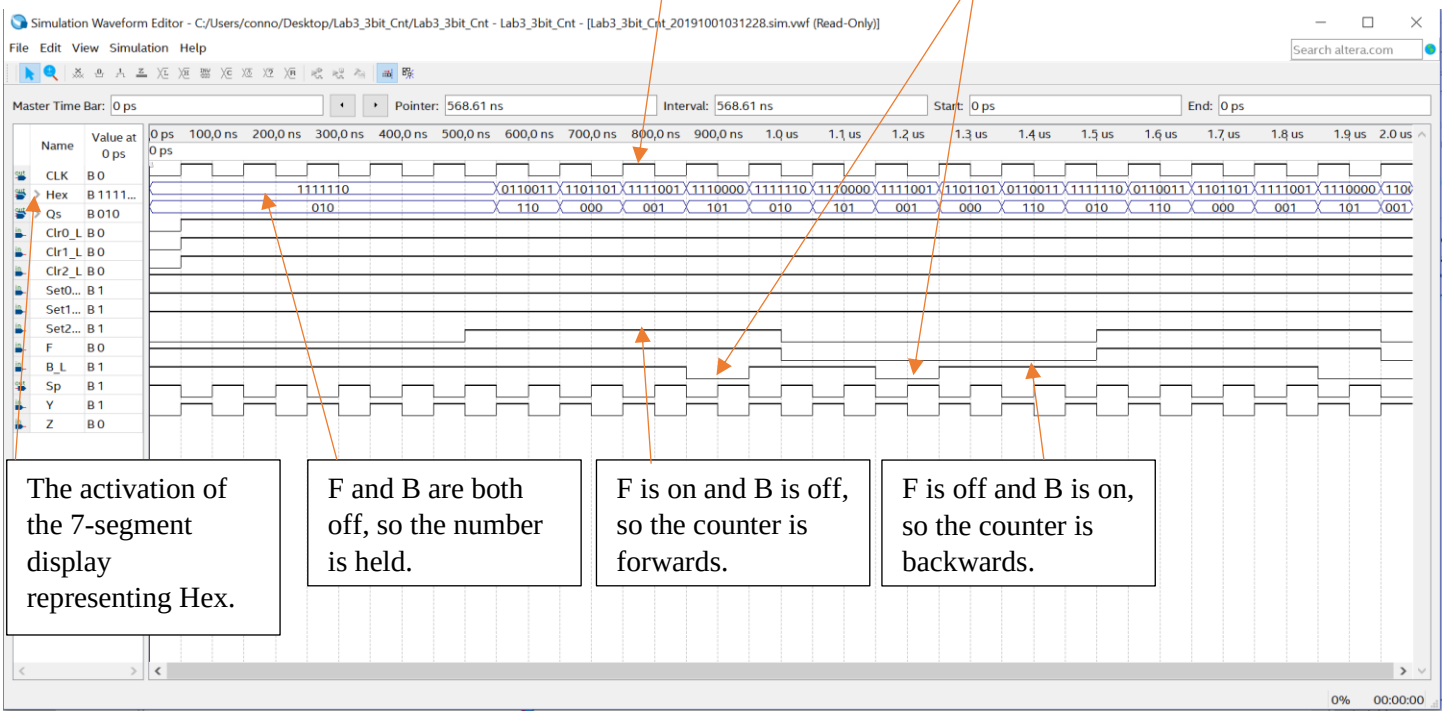
Lab 3 Report: A Debounced Switch and Counters

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year



Clock is rising, meaning the count is increasing.

Special, active low only turns on when F is true at 111, and when B is true at 011.



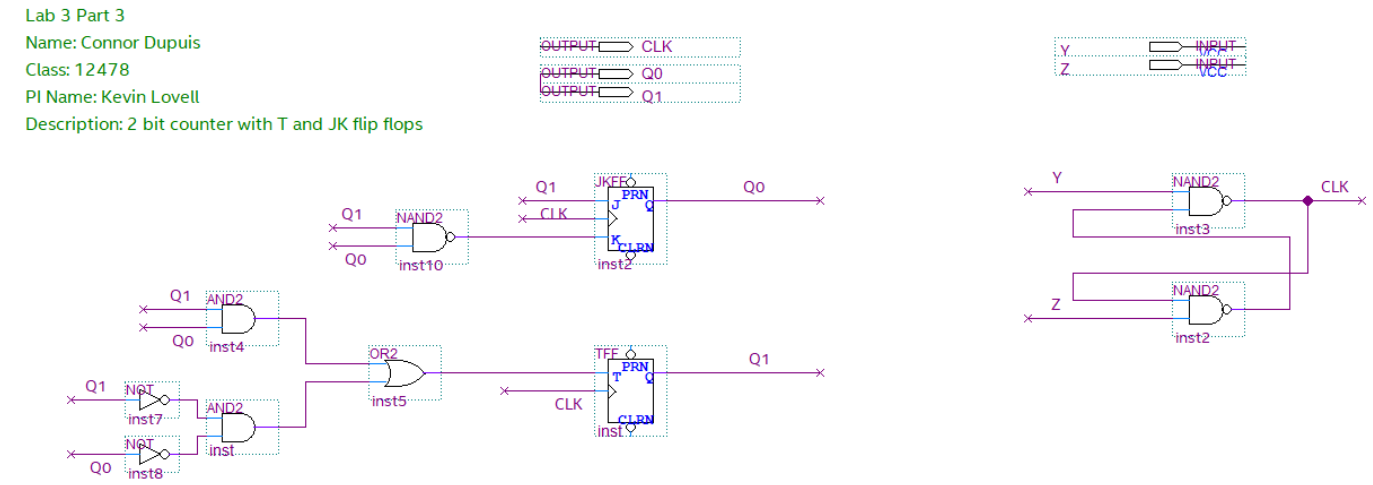
The activation of the 7-segment display representing Hex.

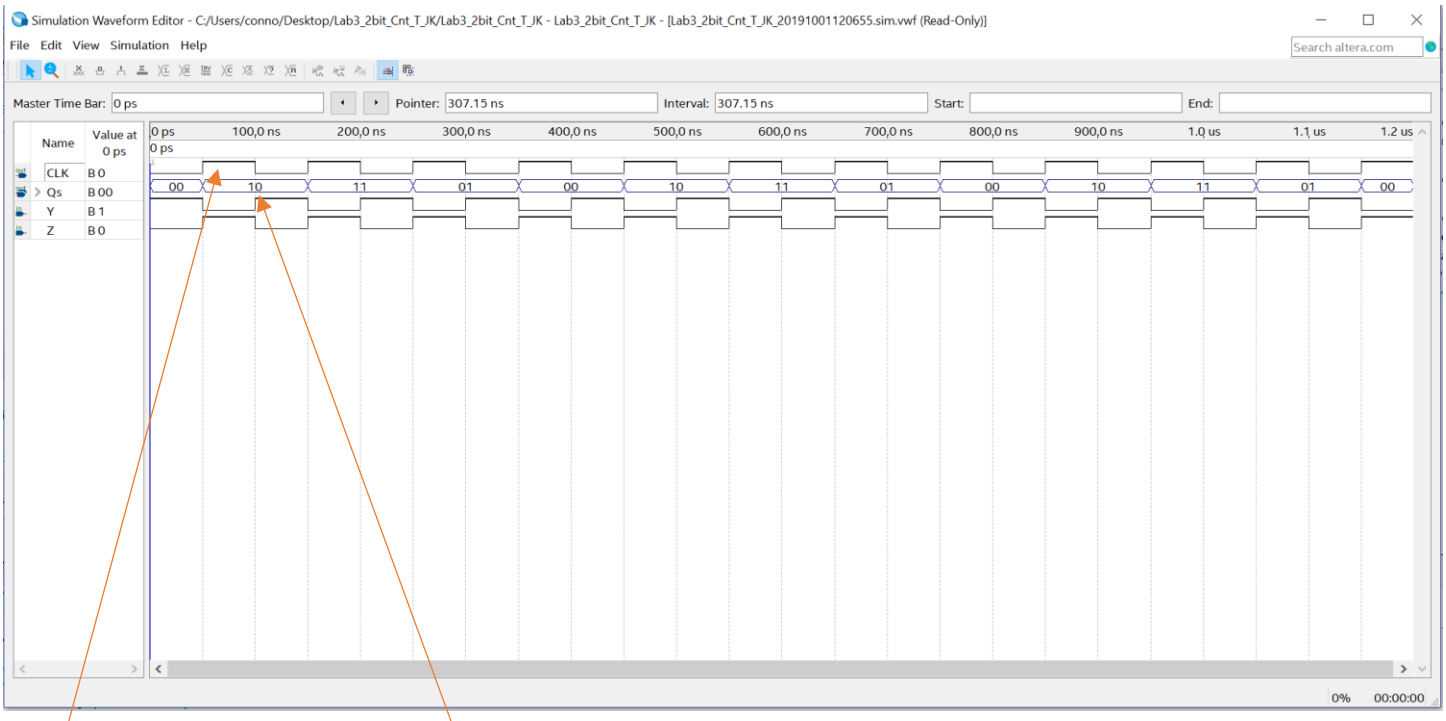
F and B are both off, so the number is held.

F is on and B is off, so the counter is forwards.

F is off and B is on, so the counter is backwards.

2-bit Counter T and JK Redesign





Clock is rising, meaning the count is increasing.

The counting number in binary. 0-2-3-1.