LAB 1: Mixed-Logic Design and Quartus

OBJECTIVES

- To understand the operation of Altera's Quartus as a digital design and simulation tool.
- To learn how to realize (construct) mixed-logic circuit designs using descrete components (IC's, LED's, switches, and resistors).

MATERIALS

- Printouts (required) of the below documents:
  - Your *Summary* file
  - *Pinouts* of our 74'xxx parts (keep in your toolbox)
- **Your** pre-lab designs and simulations
  - Your *Summary* document and **all** designs and simulations done in pre-lab must uploaded through Canvas (for this lab and **every** lab) **before** the start of your lab period. You may want to print some of the design and simulation material (**not** required) for your **own** use during your lab.
- Download onto your laptop (not just links):
  - The lab assignment (this document)
  - *Quartus 18.1 Tutorial*
  - *Quartus Display Issues (for high resolution laptop monitors)*
  - Instruction on using the *Out of the Box PLD Programmer*
- Bring your laptop with Quartus installed and the above documents already downloaded.
- Bring your USB-Blaster [**REQUIRED**]
  - Your toolbox. (In lab 0 you constructed your *OOTB 3701 CPLD Board*. This must be complete prior to your Lab 1.)
  - Prototyping bread board, wires, IC's, multi-meter, DAD/NAD, and chip extractor
  - IC components, resistors, LEDs, and switches

TOTALLY OPTIONAL PRE-PRE-LAB

This section is for your eyes only, i.e., it will **not** be turned in; it **will** help you understand the big picture, so I **strongly** recommend that you do it!

With A, B, and C all active-high, make a truth table and a voltage table for C = /A*B. Design the circuit in Quartus and verify that the Quartus voltage simulation matches the voltage table. Now change A to active-low in Quartus by just changing the name of the signal from A to A_L. Do not change the circuit design in Quartus. Does the voltage simulation change? How about the truth table and voltage table? What is the equation of this "new" circuit?

See also the hint that corresponds to the above at www.mil.ufl.edu/3701/labs/quartus_mixed-logic.html.

PRE-LAB REQUIREMENTS

As stated in the *Lab Rules & Policies* document that you "signed" previously, submit through Canvas your *Pre-Lab Report* (a pdf file which includes your Truth and Voltage Tables, circuit designs, and annotated simulations, etc.), and **all** pre-lab design and simulation files (using the Quartus' archive feature) **BEFORE** the start of your lab.

You must do the following **before** lab and submit your design and simulation work **through Canvas BEFORE** entering the lab. (A printed copy of each of your designs is advised for **your own use**, but is **not** required.)

- Re-read the relevant part of lecture that shows switch circuit and LED circuit designs and layouts.
- Read all the required documents **before your lab.**
- Read the below **Review from Lab 0** section. Make sure you understand all of its parts.
- Create your *Pre-Lab Report* document. Bring a print out of the first page (as described in *Lab Rules and Policies*) and the pinouts of our 74'xxx parts.
- Complete the *Quartus Tutorial* and Homework 2.
- Complete the designs and simulations in the below sections and submit this through Canvas as a Quartus archive files (called **Lab1XXX.qar**). Also, include the designs and simulations in your lab document file. (I will **NOT** continue to remind you of this in future labs.)

Review From Lab 0

Your lab PI demonstrated the functioning of some of the components in your toolbox during your Lab 0, including SPST (switches), LEDs, SIP resistor packs, DIP resistor packs, and breadboards. Before Lab 1, verify that you can repeat what your PI demonstrated in Lab 0 (and then do this again before Lab 2). If you are uncomfortable with any of these parts, reread the relevant class notes and *Hardware: Getting Started* document. You can also go to any office hour to get additional help. You are expected to know how to do all of the following (from Lab 0).

1. Know how to use your multimeter to verify the voltage suppied from your PLD board.
2. Know how to use your multimeter to verify electrical node connectivity of your breadboards (also known as prototyping boards). This includes the power/ground buses and the general signals.
3. Know how to place an IC (integrated circuit) device on the breadboard, where power/ground are located, and how power/ground are connected . You should be able to find pin 1 on all their 74'xxx ICs. You should understand how to read your pin-outs.
4. Know how DIP and SIP resistors work and how to use them. You should also be able to sketch the internal resistor circuit for each.

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5. Know how to construct switch circuits using a SIP resistor. You should also be able to sketch a switch circuit diagram. Only use the SIP as pull-up resistors in your switch circuits. (Switch circuits can be made with pull-down resistors, but these circuits should use different value resistor values than circuits with pull-up resistors. Since you only have single value SIP resistor packs, do **NOT** use switch circuits with pull-down resistors in EEL 3701 during the entire semester.)

6. Know how to construct active-low and active-high LED circuits using DIP resistors. The LED in each of these circuits should be lit (on) when the relevant signal is true, i.e., an active-low LED circuit should light up when the signal is low (ground) and an active-high LED circuit should light up when the signal is high (Vcc). You should also be able to sketch an LED circuit diagram.

7. Know how to construct a 2-input AND-gate circuit (using a 74HC08) on your breadboard (implementing the equation Y = A * B), with all signals active-high, with two input switch circuits, and an output LED circuit.

PRE-LAB REQUIREMENTS

1. Using only AND gates with **NO** bubbles, OR with **NO** bubbles, and NOT gates, design and draw the circuit for the following logic equation.

   V = /[(A * /B) + /(C + /D)] (1)

   Do **NOT** simplify the equation: (For this part only, do **not** use the alternative way to draw the AND and OR gates.) The output and all the inputs are active-high. Do this by hand, i.e., without Quartus. Write the equations for intermediate inputs next to the input pins of each gate.

   Since you will not build this circuit, you are not limited (in this section) to parts in your lab kit.

2. Most of the world uses positive-logic only; and so will you in this section (and in the previous section). Draw the circuit for the equation below by hand and then with Quartus **using only the positive-logic logic gates** (i.e., AND, OR, NAND, NOR, and NOT gates) and **active-high** inputs and output. Use a project and filename of **`Lab1a`**. (Positive-logic gates do **not** have bubbles at input pins.)

   W = /[(A * /B) + /(C + /D)] (2)

   Note that this equation has the same right-hand side as the equation (1). Do **not** simplify or otherwise manipulate the equation, i.e., do **not** use BAND2 instead of NOR2 even when you want an AND function.. **Always add your name on each schematic using the Quartus package** (as described in the *Lab Rules and Policies*).

3. Generate a truth (logic) table (using 0's and 1's) for equation (2) and then make a voltage table (using L's and H's) for this logic diagram. Both tables **MUST** be in counting order. Generate a complete simulation (timing diagram) for this circuit (using Quartus) and verify that it matches the **voltage** table.

   Note: Voltage tables are helpful in verifying simulation outputs (since Quartus simulations display voltages, not logic values). Unfortunately, in Quartus simulation a "0" represents a low voltage and a "1" represents a high voltage.

   Compare the voltage table to the Quartus simulation to verify that the circuit does indeed implement the equation given.

   Take a screenshot of the simulated results. Annotate the simulation copied to your Word file (or equivent), i.e., add notes with arrows pointing to important results. You can **not** annotate by hand. (If you would rather, you can use tools such as Snip Tool or Paint to create your annotations.) **Every simulation** that you turn in this semester **must** be annotated. Annotations are meant as a guide to help you and others reading your Pre-Lab document (like your PI) understand the simulation. It should help explain what is going on and prove that your circuit works. Simple circuits may need only a few (2 or 3 annoations) while more complicated circuits (like those that you will design later in the semester) may need many more.

4. **Submit** (through Canvas) the archive file (use filename `Lab1a.qar`) with both the design and the simulation (with annotation), and also submit the two tables.

5. Again draw (by hand and then with Quartus, using project and filename `Lab1b`) a circuit design for equation (3). Note that this equation has the same right-hand side as the equations (1) and (2). In this design you are not limited in your gate selection (except that the gates should be available in the chips of your lab kit).

   X = /[(A * /B) + /(C + /D)] (3)

   Choose activation-levels for the inputs and outputs that will allow you to **minimize** the number of **gates** necessary. Do **NOT** simplify the equation: Draw the gates in such a way that the logic of the equation is apparent in the circuit, e.g., if you need a 2-input AND gate with bubbles at the inputs (a BAND2 in Quartus), draw the gate this way instead of as a NOR gate. Show intermediate inputs as in part 1. Unless otherwise stated, all **hand-drawn** and Quartus-generated circuits this semester must be drawn as described above.

   Note that Quartus includes only some of the mixed-logic circuit elements in its libraries. For instance,

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Quartus does not have a level-shifter with the bubble on the input side.

Generate a voltage table for this design. (Hint: The truth table should be the same as the one made in the previous section. Truth tables depend only on the logic equations, not on the logic design. Note that the voltage table and the simulation for this design may **NOT** match the voltage table and the simulation for the design of parts 1-4.) **Submit** (through Canvas) the archive file with your design and simulation, named `Lab1b.qar`. Remember to put the design, annotated simulation, and the truth and voltage tables in your document file. **For this entire semester, when using Quartus to draw a circuit, label all active-low inputs or outputs with _L at the end, since .L and (L) will not work, e.g., R(L) will be written as R_L. All active-high signals will end in _H or have no special ending (your choice), e.g., S(H) will either be written as S_H or S.**

6. Make a new project and filename `Lab1c`. Copy the logic diagrams in Quartus for equations (2) and (3) and place them in a single new file, i.e., this file will have circuits for both W and X. Generate a complete Quartus simulation timing diagram for these two circuits and verify that the voltage tables for the two circuits match the simulation outputs. Since all of the inputs for the positive-logic circuit are active-high and some of the inputs for the mixed-logic solution are probably active-low, if you just copy the two files you will have eight inputs. In order to directly compare the outputs, use the four inputs for **either** W or X and **create the other necessary inputs (with opposite activation-levels) using level-shifters** as shown in Figure 1. For example, using the signals name in Figure 1, you can **not** have a switch for G(H) **and another** switch from G(L); you can have one switch for either G(H) **or** G(L), and you will get the other signal with a level shifter. **Submit** (through Canvas) the archive file (including the design and simulation, with filename `Lab1c.qar`).

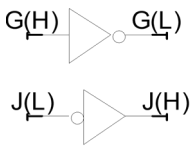

Figure 1: Use only four inputs. Create alternate activation-level inputs with level-shifters.

7. Make a new project and filename `Lab1d`. Design mixed-logic implementations of the equations for Y and Z in equations (4) and (5) below. The goal in this part is to choose input and output activation-levels to minimize the **total number gates and chips** used in the overall design of these two circuits. Choose only one of the two possible activation-levels for each of the inputs, i.e., A(H), B(L), etc. [but not A(H) for one and A(L) for the other]. (If you need both A(H) and A(L), that will cost one gate, a level-shifter or its equivalent, as shown in Figure 1.) Create the design by hand and then do it with Quartus in a single file. Do **not** simplify. (Hint: No more than two chips are needed.) **Add pin number and chip labels to each gate** to change this schematic into a wiring diagram.

$$Y = /[\ (A * /B) + /(C + /D)\ ] \quad (4)$$

$$Z = [\ (A + /B) * /(C * D)\ ] \quad (5)$$

Submit (through Canvas) the archive file (with design and simulation, named `Lab1d.qar`).

8. Create a **truth** table for equations (4) and (5). Note: Activation-levels have **no** effect when constructing a truth table from a logic equation.

9. Create a **voltage** table for equations (4) and (5).

10. Add pin numbers and chip labels to your design in part 7. While looking at your pinout sheet, label the inputs and outpus of your gates using the text tool with the pin numbers of the corresponding IC chips (For example, if using an AND gate from a 74'08 chip, you could use pins 1 and 2 for inputs and pin 3 for the output.) You should also use the text tool to add the chip number, e.g., lable the gate **08** for the 7'C08 chip. If there are multiples of the same part needed, i.e., if you need five 2-input AND gates when the 74'08 only has four gates per chip, then label the two 74'08's diffenently, e..g., **08_A** and **08_B**.

11. **For this lab only**, you will also draw a layout of your circuit as it would appear on your breadboard. A layout shows each of the parts (ICs, switches, LEDs, SIP and DIP resistor packs) as they appear on the breadtype board. Include the needed switches, resistors (SIP and/or DIP), and LED's. Generally, we will not draw a layout in this course, but instead just place pin numbers and labels on a schematic diagram. (You should use one of the posted files: `protoboard_for_layout.ppt` [a PowerPoint file] or `protoboard_for_layout.pdf` [an Acrobat file] to draw your layout.)

    Draw a layout of the circuit you designed in parts 7 and 10 of the Pre-Lab (above). Include these layout diagrams in your lab document.

    In future labs you will **ONLY** draw logic circuit diagrams (also known as schematic circuit diagrams) with pin numbers added as you did in part 10 above, but you will **NOT** draw layout diagrams.

    Note: You are asked to construct these circuits below in the next section.

12. Implement the pre-lab's wiring diagrams for both circuits in part 7 on your own breadboard. You must

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wire your breadboard with your own wires **at home**, i.e., **before** your lab. All inputs must come from switches and all outputs must go to LED's (as described in class notes and in the *Hardware: Getting Started* document).

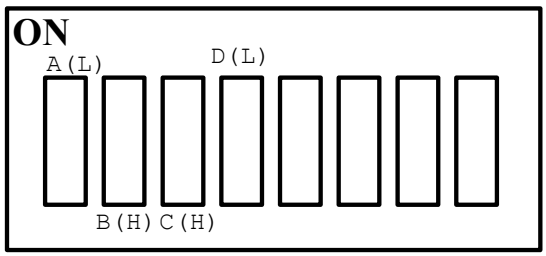

Figure 2: Switch layout (legend) with true switch positions labeled. A and D are active-low signals; B and C are active-high signals.

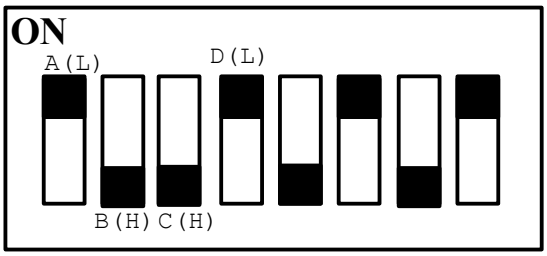

Figure 3: Switch layout (legend) with true switch positions labeled. A and D are active-low signals; B and C are active-high signals. All switches are shown in their true positions.

The activation-level of each input must be obvious for each of the inputs, i.e., labeled as active-high or active-low. Make **a legend on your logic circuit diagram** that indicates the switch position for each input signal when it is true (as shown in Figures 2 and 3). For every circuit diagram that you build in lab this semester you are **REQUIRED** to draw a legend on your logic circuit design, like the one shown in Figure 2. Be sure to include the word ON. Figure 3 shows each of the switches in their true position.

All output LED circuits should match the activation-level of the corresponding output. An LED should be on (lit) when the corresponding output is true. Make **a legend on your logic circuit diagram** that indicates the location of each LED on an LED dip chip (as shown in Figure 5).

IN-LAB PROCEDURE

1. Complete the lab quiz.
2. Demonstrate the operation of the circuits you built in the pre-lab, part 7, by switching through various inputs and comparing the output LED results to those obtained in the pre-lab simulation.

SPECIAL NOTES

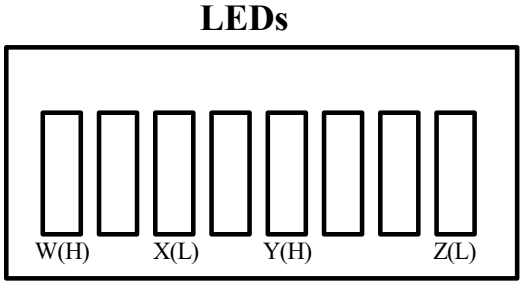

Figure 4: LED layout (legend). Note that each LED should be on (lit) when the corresponding signal is true.

- **Note: For the remainder of the semester, all circuits should be simulated and the simulation output should be compared to the voltage table to verify that the circuit performs the required function(s). In every lab, part of the pre-lab requirments is to submit (through Canvas) your lab document that contains truth tables, voltage tables, design files, simulation files, etc. All Quartus archive files (containing the designs and simulations) must also be submitted. Lab submissions must be submitted as described in the** *Lab Rules and Policies* document**, i.e., at least 15 minutes PRIOR to the start of your lab.**
- If you need help with this lab, don't hesitate to ask questions in class, visit Dr. Schwartz, or visit a PI during office hours.
- There will be a 30-minute to 1.25 hour quiz relating to Lab 0 and Lab 1's pre-lab at the beginning of this lab. Quizzes will happen at the beginning of every lab. In general, lab quizzes will relate to present or previous labs, but may also cover homework and in-class material.

    1) In this lab you will be given a new equation (similar to the two given in the pre-lab section).
        a) Draw the logic diagram by hand, using appropriate mixed-logic notation.
        b) Draw the circuit (in Quartus).
        c) Draw a truth table for the equation.
        d) Draw a voltage table for the equation.
        e) Verify the correct operation of the circuit using Quartus simulation and comparing this to your voltage table.
        f) Build the circuit and demonstrate its correct operation.

Tips for building and debugging circuits

In your future breadboard designs, your circuit will probably not work the very first time you build it. Therefore, trouble-shooting is a basic skill that you will have to learn. The followings are some helpful suggestions. Please feel free to ask your PI any questions

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you may have on this subject. Keep this handout available for use in future labs.

- Come prepared with a large, neat Pre-Lab schematic diagram. **REQUIRED**. (I suggest that you print this and bring it to your lab, with room for notes and corrections., but this is **not** required.)
- When creating a large circuit, you should identify, build, and debug small portions of the circuit, one at a time, to isolate potential problems. In other words, decompose your design and your construction. (Be the Tortoise and not the Hare!) Several links to versions of the story are available below.
  - http://www.storyit.com/Classics/Stories/tortoisehare.htm
  - Video: https://youtu.be/MeZe2qPLPh0

- Start trouble-shooting at the point at which the voltage value is wrong; continue to check your circuit backward, making sure that at each point the value agrees with your prediction.
- Construct your circuit neatly. Use appropriate length wires for connections; i.e., use short wires for short distance connections. Your circuit should not look like a bowl of spaghetti or a bird's nest.
- Use your multi-meter or an LED circuit with a long wire as a logic probe. Ask your PI to demonstrate this if you do not understand.
- Check IC insertion to make sure all the pins are in the correct holes and that the IC does not have any missing or bent legs.
- Check power and ground connections (and other connections) **before** applying power to the circuit.
- Make sure that the power and the ground are properly connected to all IC's before applying power to the circuits.
- **DO NOT** short (connect) the power supply outputs (Vcc and GND) together, i.e., do not allow the exposed wires to touch each other. This will cause permanent damage to the power supply. If the green light on your PLD board does not turn on when you connect your PLD board to power, there is most likely a short.
- **DO NOT** connect the power supply to the breadboard with reverse polarity. This could cause permanent chip damage.
- **DO NOT** connect an output of any gate to the output of another gate, to a switch circuit output, to Vcc, or to GND. These situations will cause excessive currents and result in permanent damage to the chip or chips involved.