Lab 4: ALU and CPU

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Lab Section: 1491

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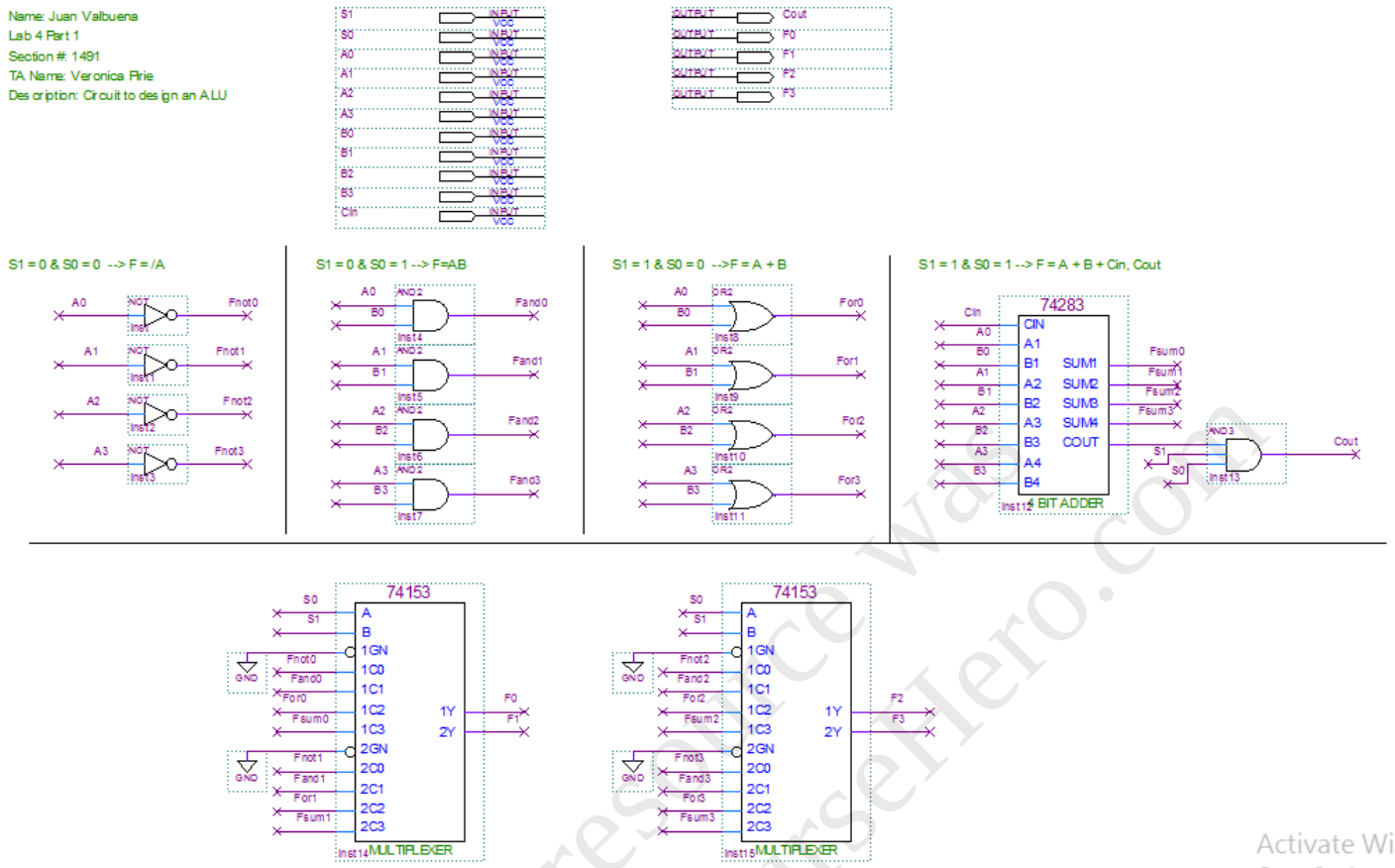
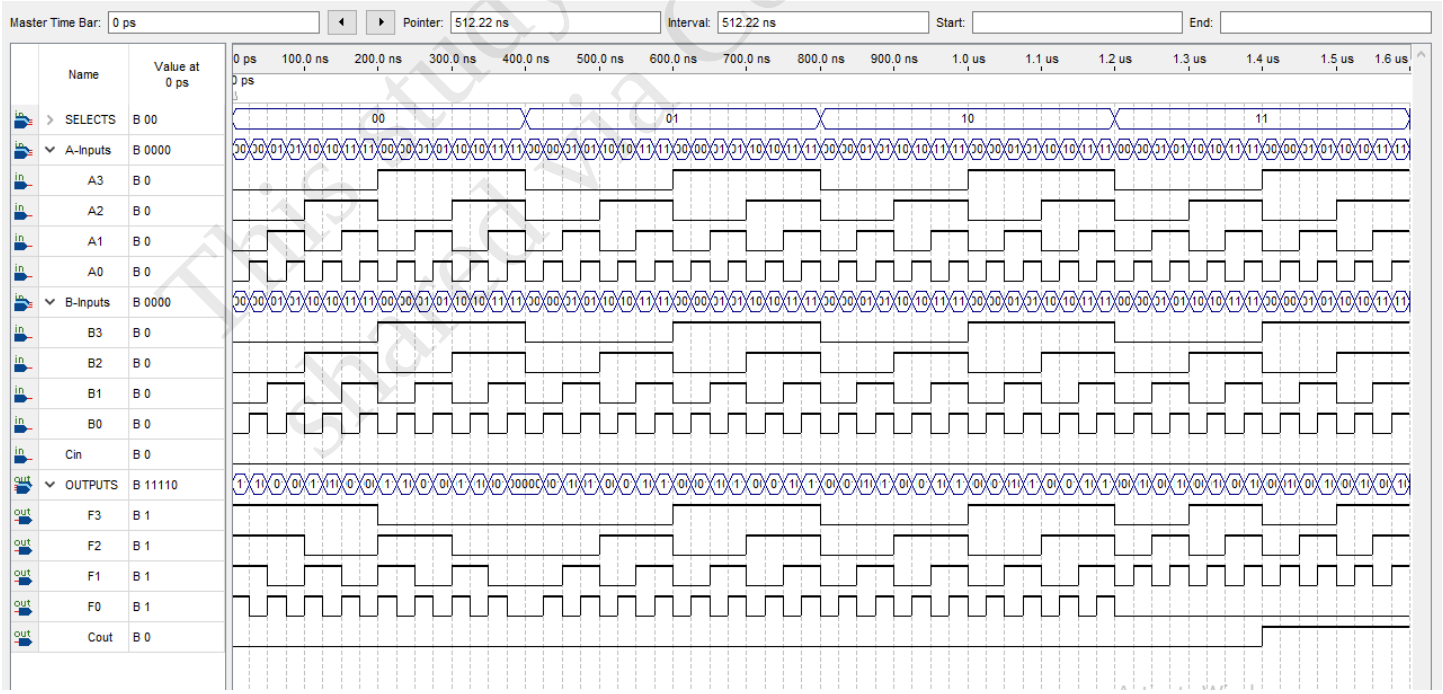
Part 1: ALU

ALU Schematic



ALU Simulation



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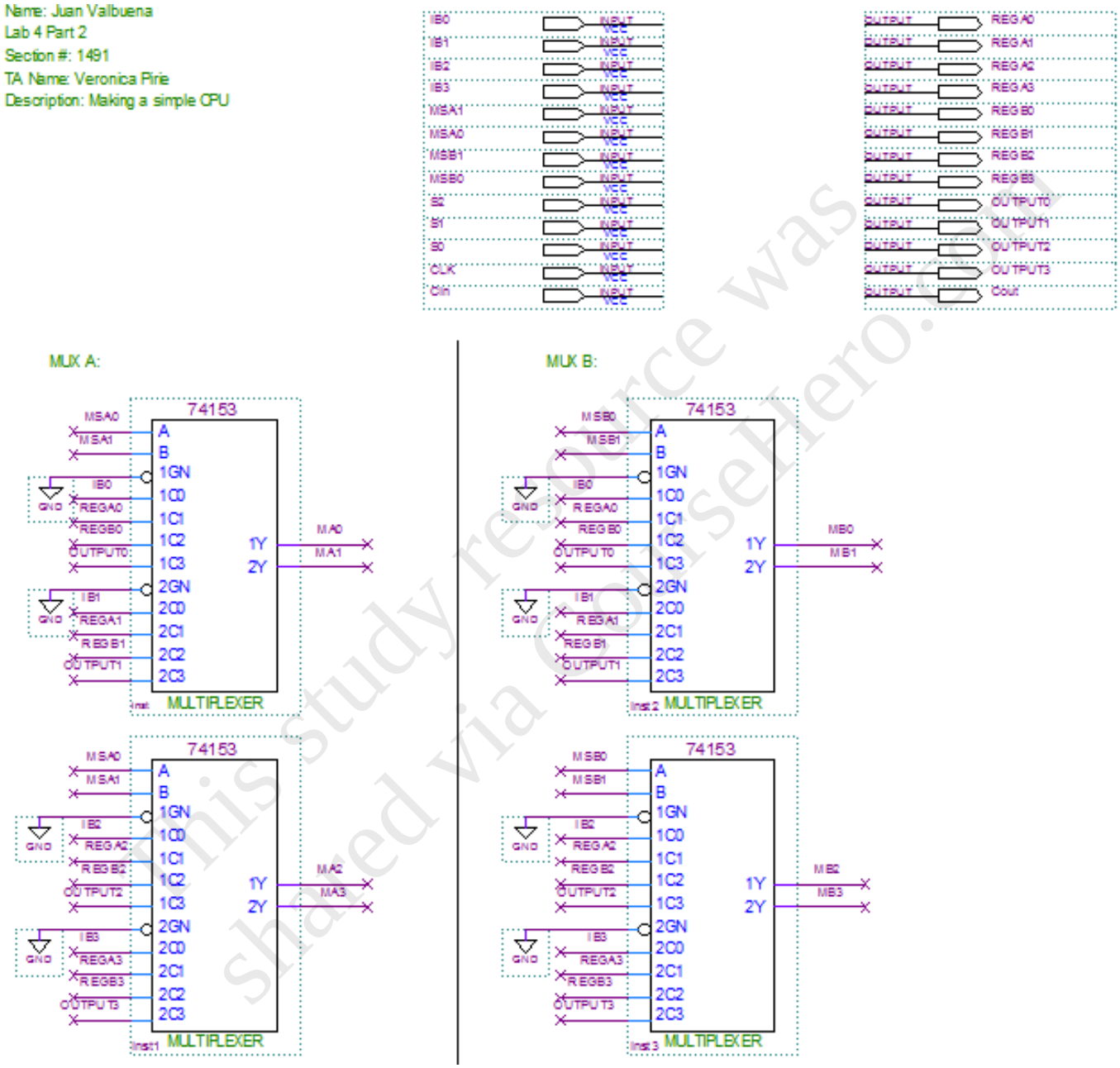
Activate Wir

ALU Pre-Lab Questions

1. Making a complete truth table for the ALU will result in 2048 rows since there's 11 inputs.
2. Since there's two additional functions and we're using a 4-bit mux an additional 2 lines needs to be added making it into a 6-bit mux. Can be done by using a 4 bit and a 2-bit mux.

PART 2: CPU

CPU SCHEMATIC



This includes my inputs and outputs as well as MUX A and MUX B

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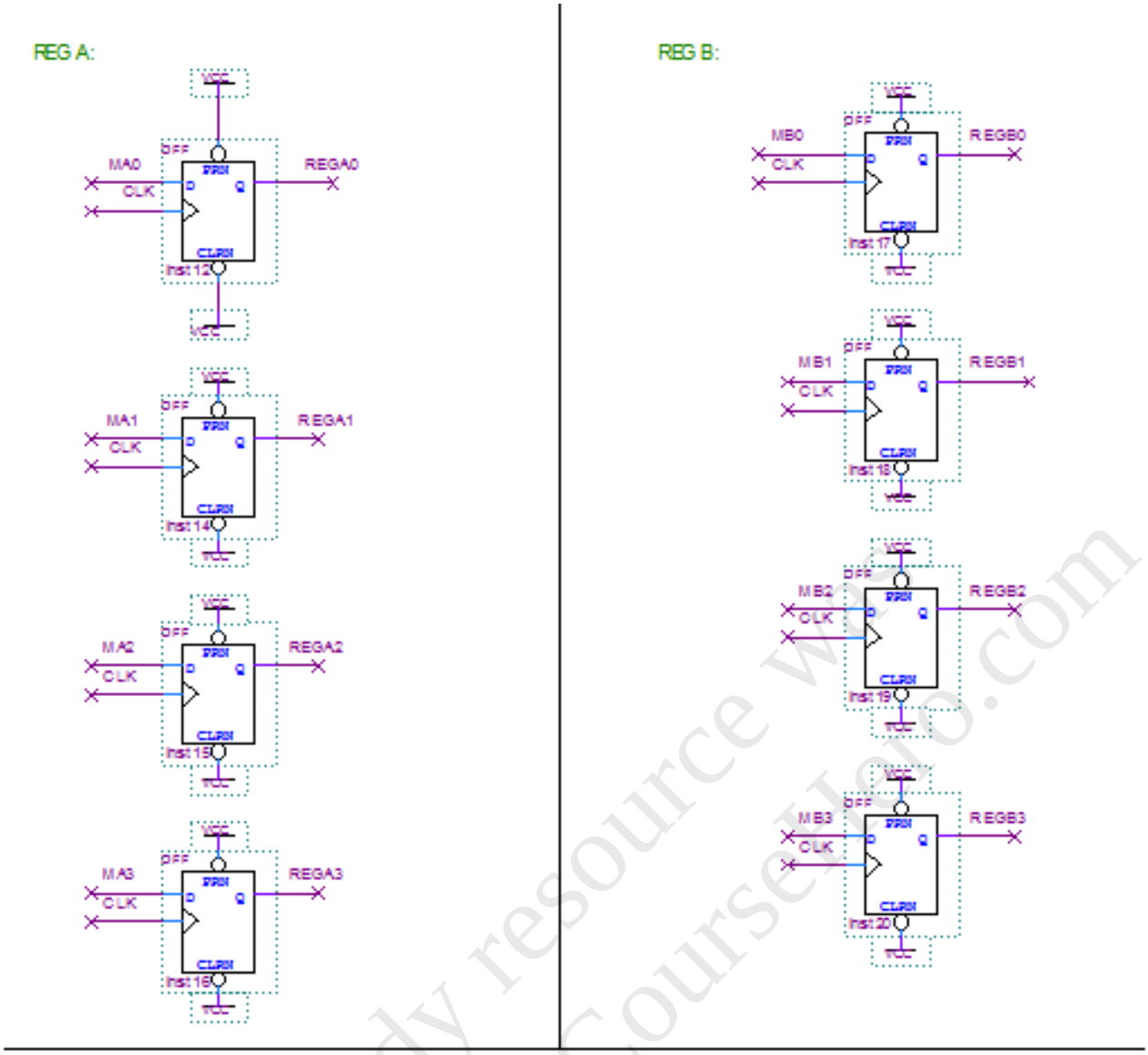

These are both my register A and register B respectively

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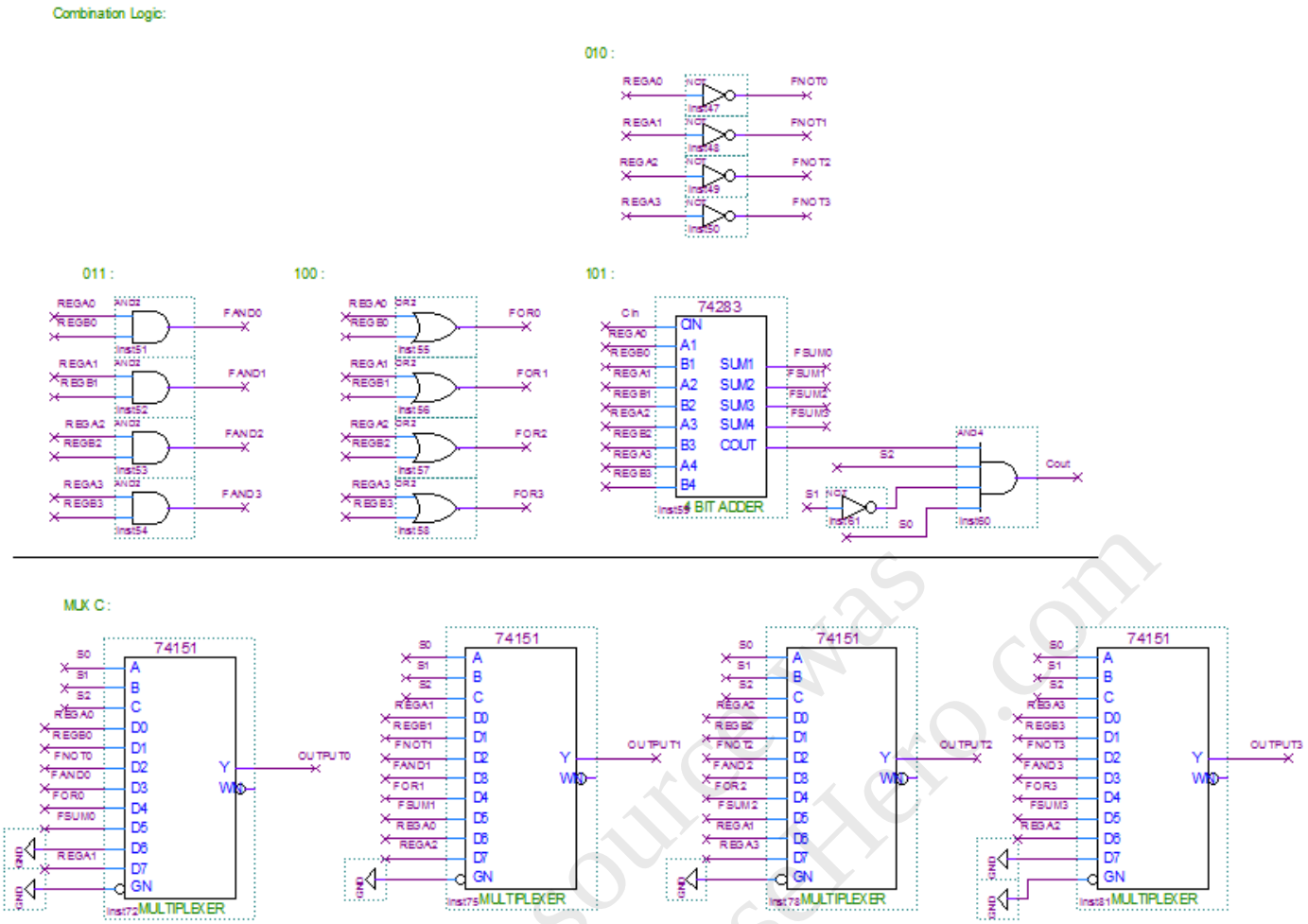
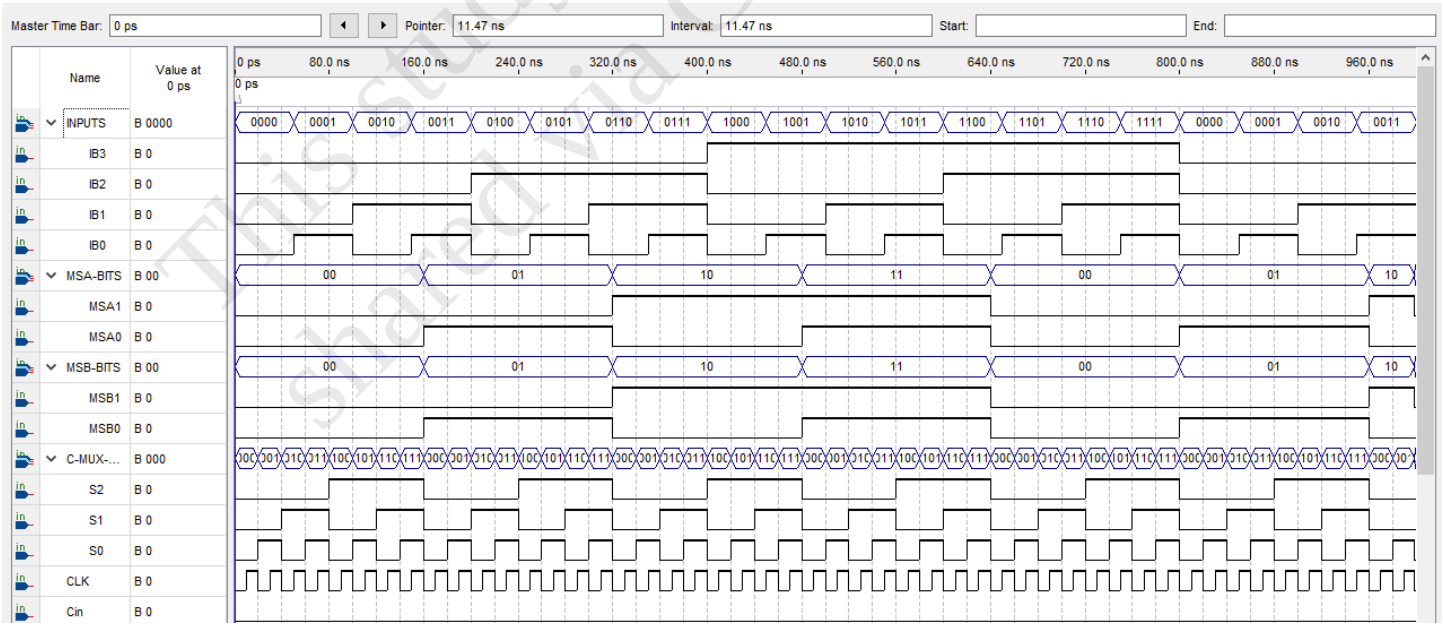


This includes my combinational logic and my 4 8 bit muxes to create my C-Mux.

CPU Simulation:



These are all the inputs for my CPU

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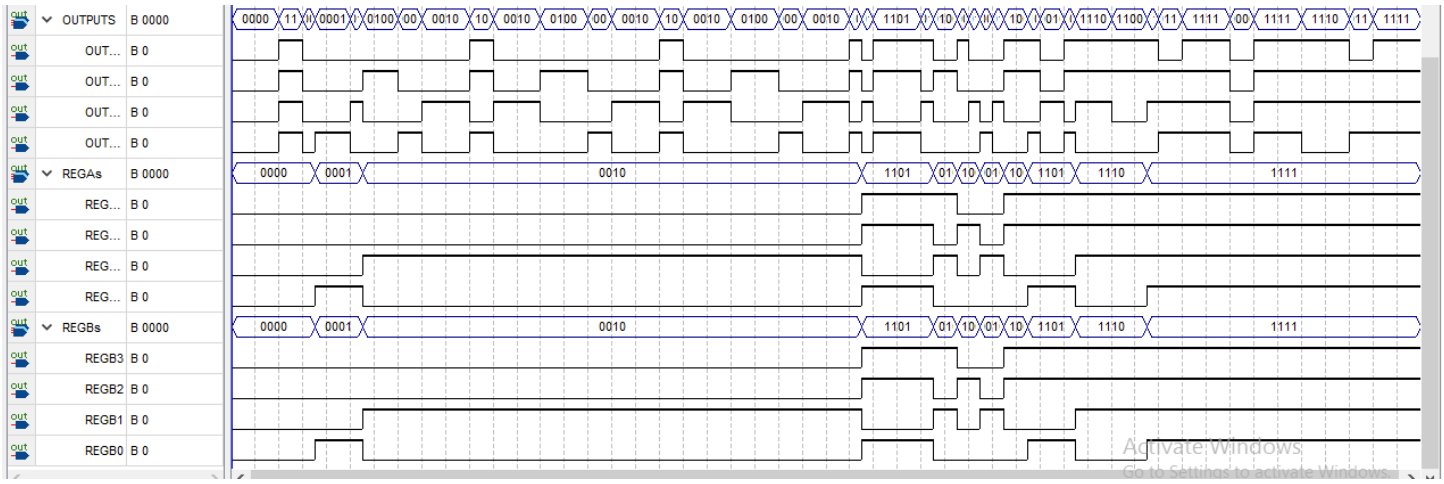
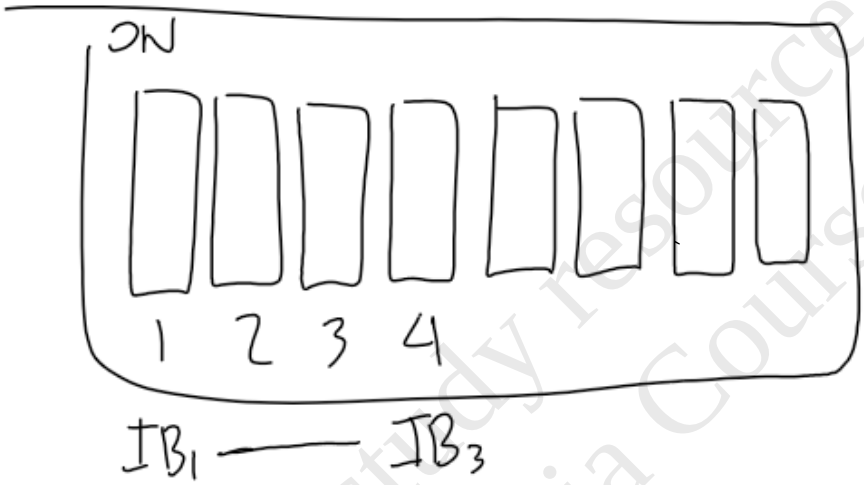


This are all the outputs for the CPU simulation

The inputs I did in counting order and

counting every 50 ns and my C-Mux bits are counting every 20 ns

LEGEND



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