EEL 3701 — Digital Logic & Computer Systems
Revision 1
Lab 1 Report: **Mixed-Logic Design and Quartus**

Dupuis, Connor
Class #: 12478
Kevin Lovell
Month Day, Year

PRE-LAB QUESTIONS OR EXERCISES

N/A

PROBLEMS ENCOUNTERED

N/A

REQUIREMENTS NOT MET

N/A

FUTURE WORK/APPLICATIONS

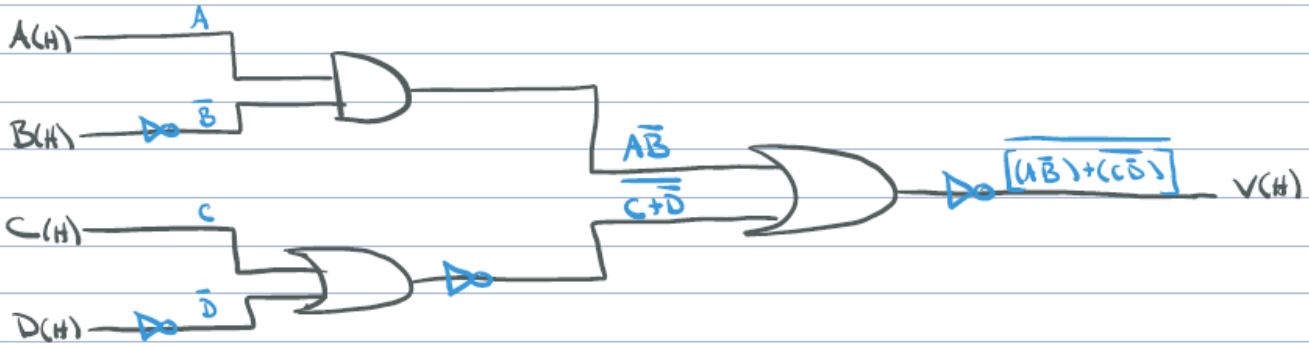
In this lab I learned how to build basic circuits involving inputs, gate to manipulate the inputs, and outputs that show the result. This lab is the building block for the labs to come as it introduced me to some fundamental concepts such as active high/low, pull-up/down resistors for switches, and other basic knowledge that will help me in the future of this class.

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

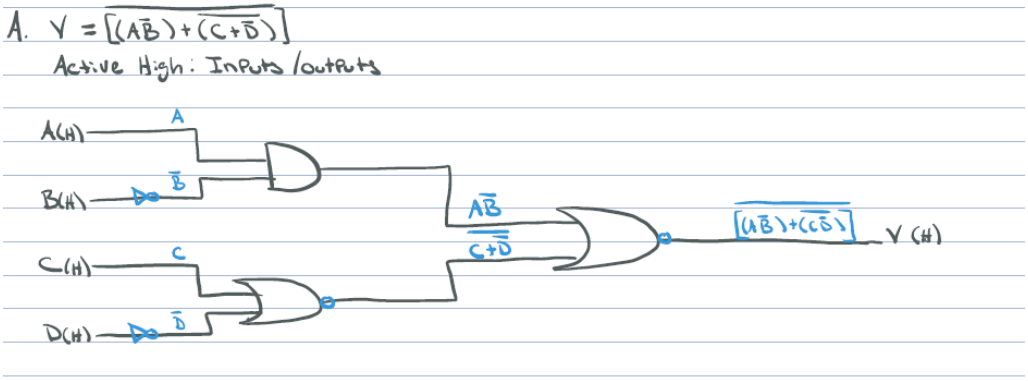
Introduction Question

1. $Y = \overline{[(A\bar{B}) + \overline{(C+\bar{D})}]}$

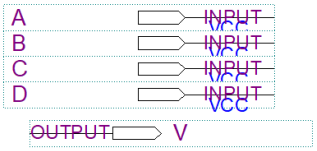
Active High: Inputs / outputs

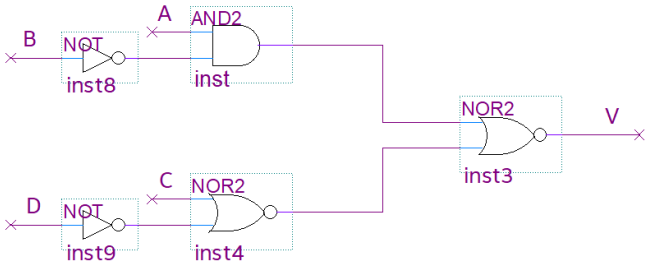


Part A

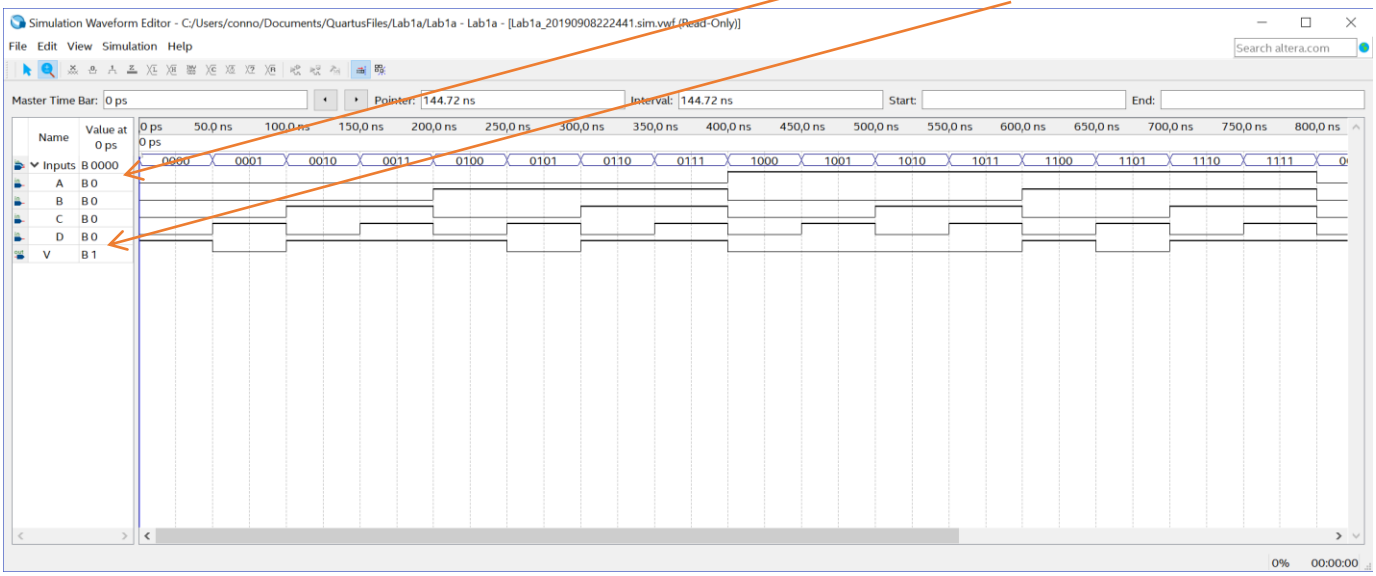


Lab 1 Part A
Name: Connor Dupuis
Class: 12478
PI Name: Kevin Lovell
Description: V = /[(A * /B) + /(C + /D)]





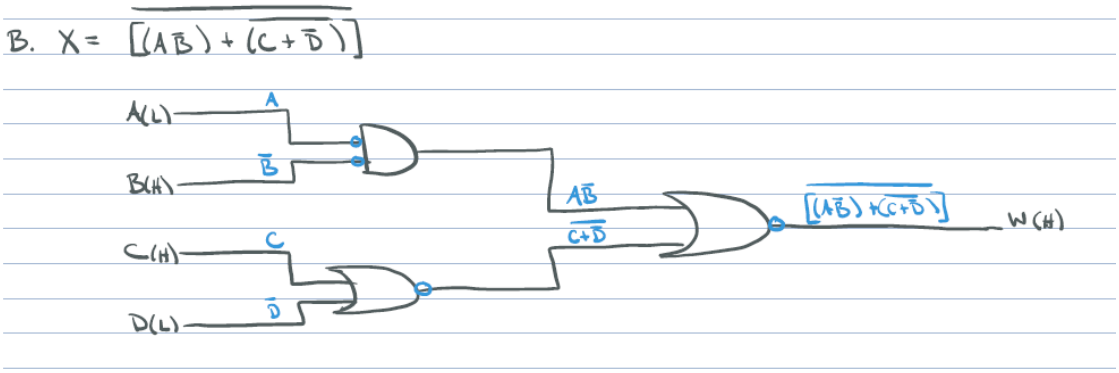
The respective inputs and outputs of the design above. All input and output signals are active high.



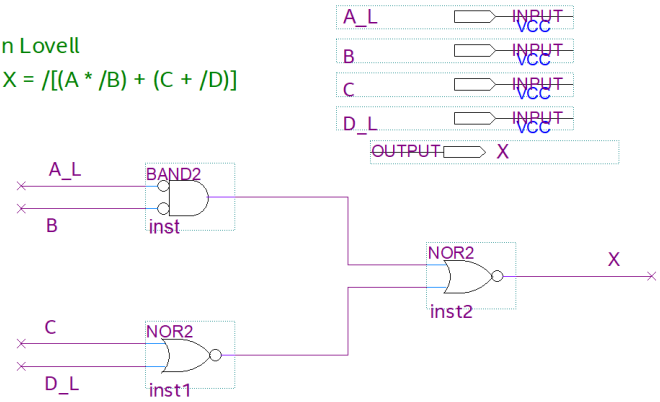
Truth Table								
A	B	C	D	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]
0	0	0	0	1	1	0	0	1
0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	0	1
0	1	0	0	0	1	0	0	1
0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	1	1	1	0	0
1	0	1	1	1	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	0	1	0	0	0	1	0
1	1	1	0	0	1	0	0	1
1	1	1	1	0	0	0	0	1

Voltage Table								
A	B	C	D	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]
L	L	L	L	H	H	L	L	H
L	L	L	H	H	L	L	H	L
L	L	H	L	H	H	L	L	H
L	L	H	H	H	L	L	L	H
L	H	L	L	L	H	L	L	H
L	H	L	H	L	L	L	H	L
L	H	H	L	L	H	L	L	H
L	H	H	H	L	L	L	L	H
H	L	L	L	H	H	H	L	L
H	L	L	H	H	L	H	H	L
H	L	H	L	H	H	H	L	L
H	L	H	H	H	L	H	L	L
H	H	L	L	L	H	L	L	H
H	H	L	H	L	L	L	H	L
H	H	H	L	L	H	L	L	H
H	H	H	H	L	L	L	L	H

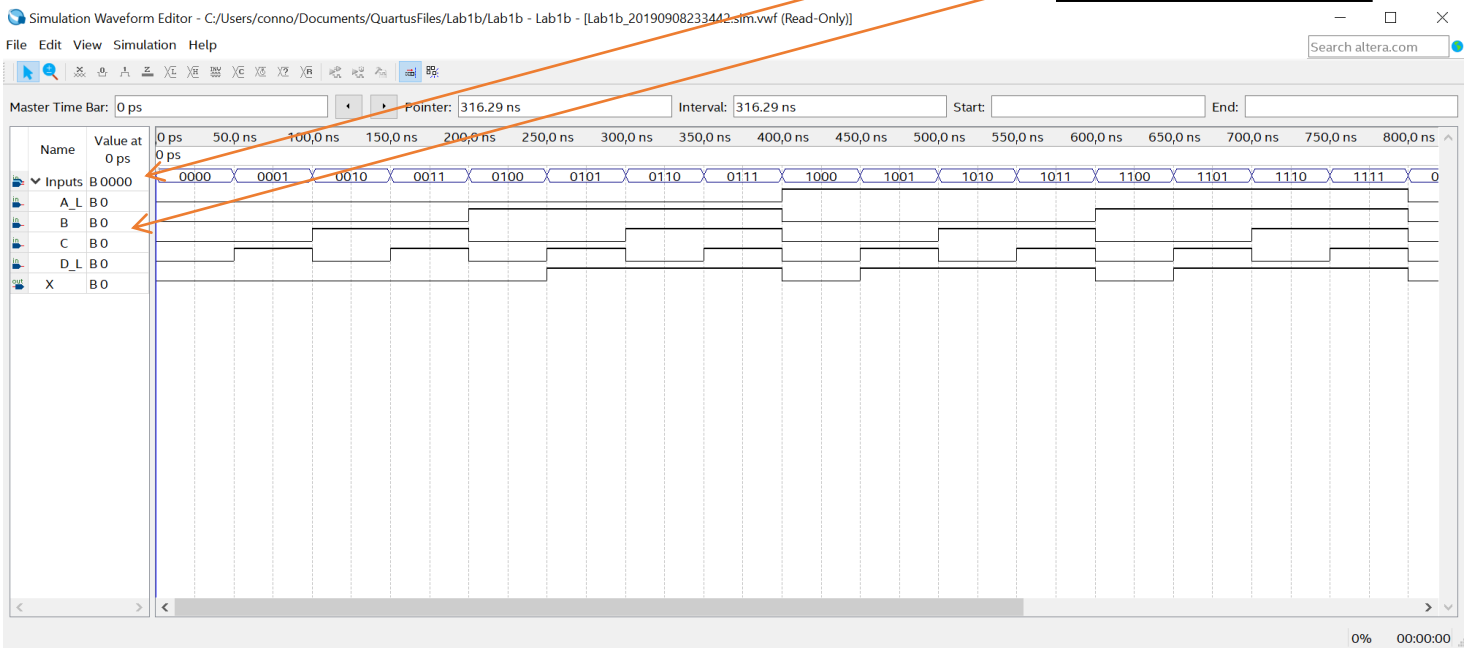
Part B



Lab 1 Part B
Name: Connor Dupuis
Class: 12478
PI Name: Kevin Lovell
Description: X = /[(A * /B) + (C + /D)]



The respective inputs and outputs of the design above. With inputs A and D being active low; and B and C being active high. The output signal is active high.

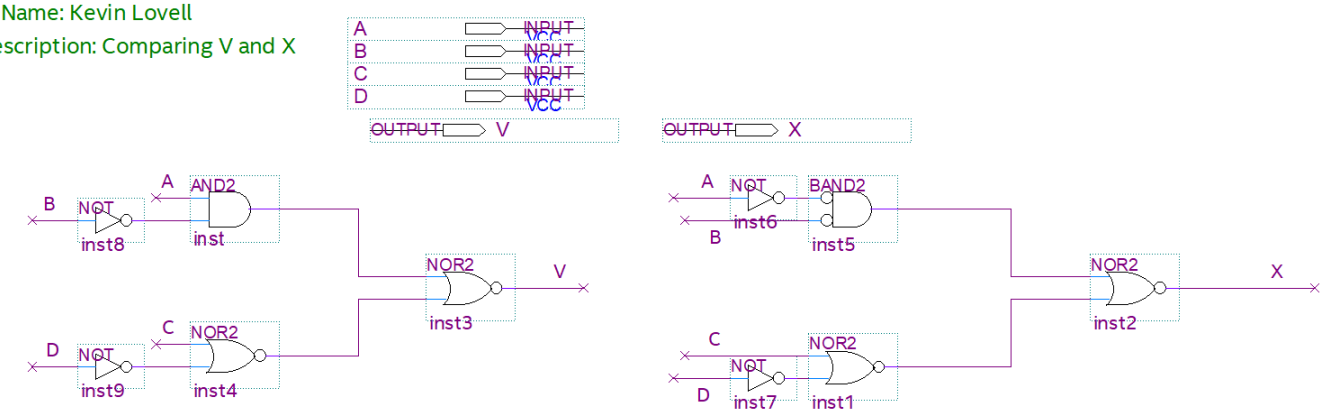


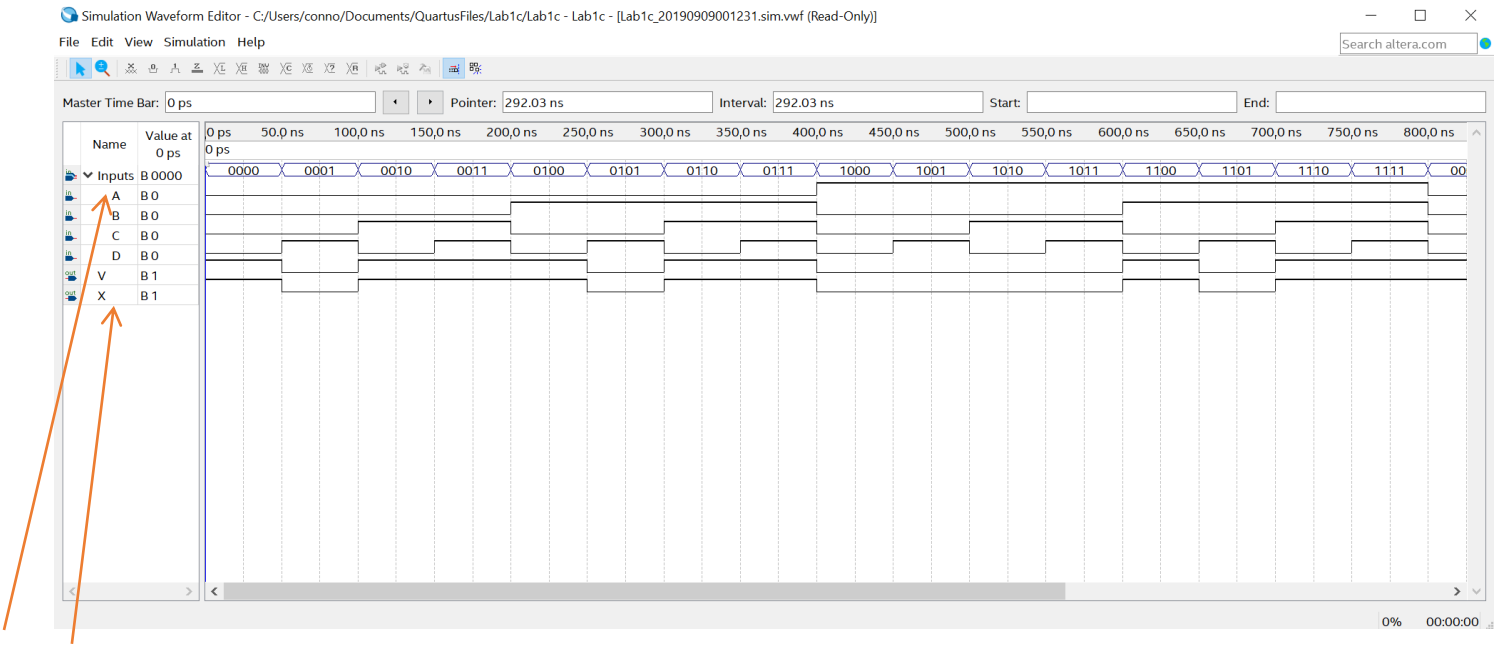
Truth Table								
A_L	B	C	D_L	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]
0	0	0	0	1	1	0	0	1
0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	0	1
0	1	0	0	0	1	0	0	1
0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	1	1	1	0	0
1	0	1	1	1	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	0	1	0	0	0	1	0
1	1	1	0	0	1	0	0	1
1	1	1	1	0	0	0	0	1

Voltage Table								
A_L	B	C	D_L	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]
L	L	L	L	H	H	L	L	L
L	L	L	H	H	L	L	H	L
L	L	H	L	H	H	L	L	L
L	L	H	H	H	L	L	L	L
L	H	L	L	L	H	L	L	L
L	H	L	H	L	L	L	H	H
L	H	H	L	L	H	L	L	H
L	H	H	H	L	L	L	L	H
H	L	L	L	H	H	H	L	L
H	L	L	H	H	L	H	H	H
H	L	H	L	H	H	H	L	H
H	L	H	H	H	L	H	L	H
H	H	L	L	L	H	L	L	L
H	H	L	H	L	L	L	H	H
H	H	H	L	L	H	L	L	H
H	H	H	H	L	L	L	L	H

Part C

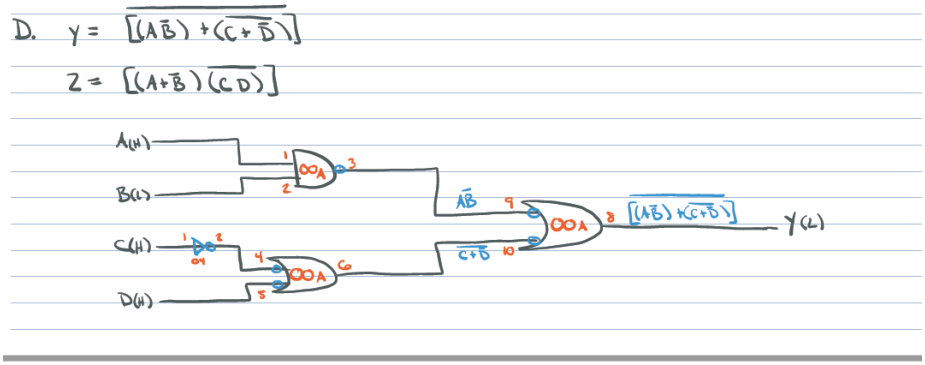
Lab 1 Part C
Name: Connor Dupuis
Class: 12478
PI Name: Kevin Lovell
Description: Comparing V and X

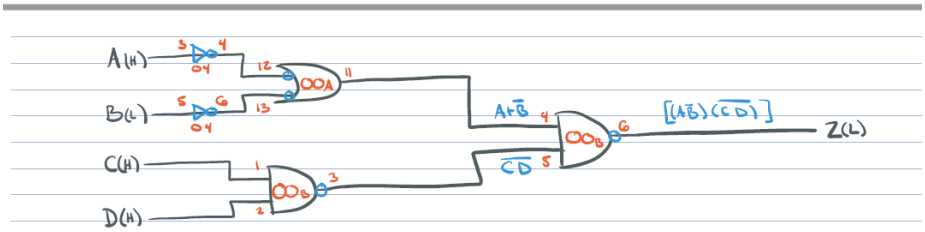


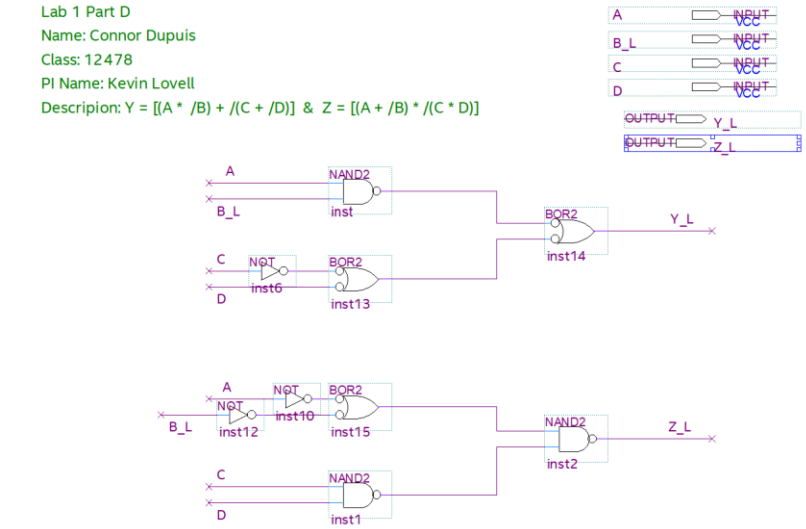


The respective inputs and outputs of the design above. With all input and output signals are active high.

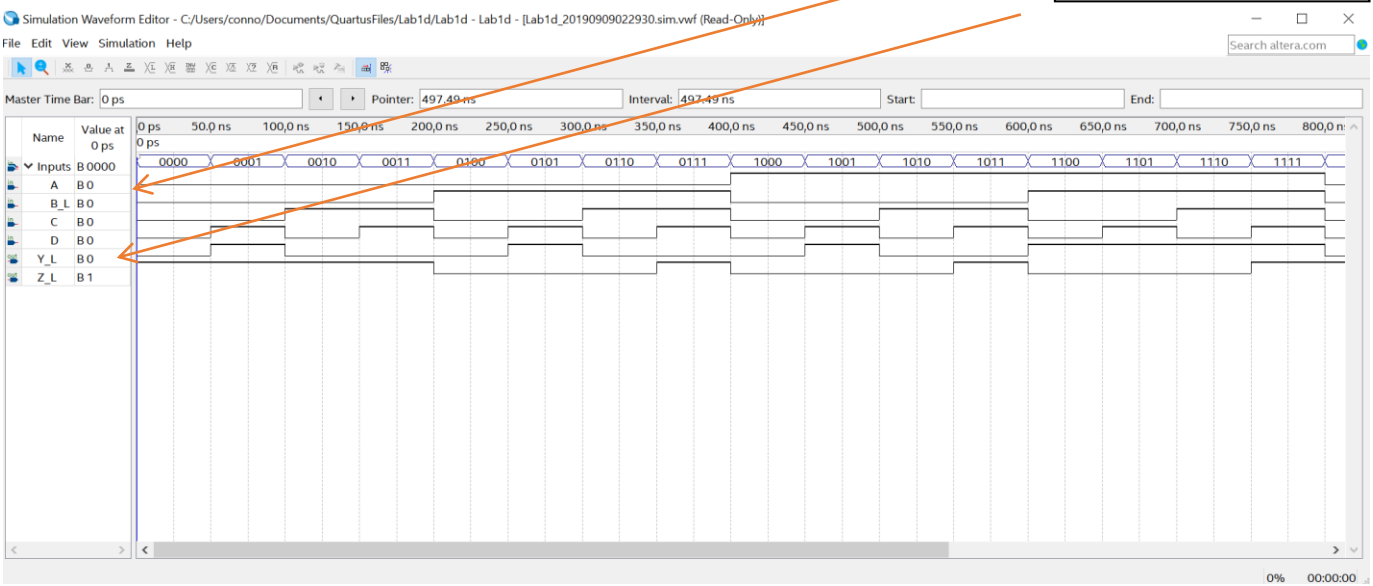
Part D







The respective inputs and outputs of the design above. With input signals A, C, and D being active high and input B being active low. Both output signals are active low.

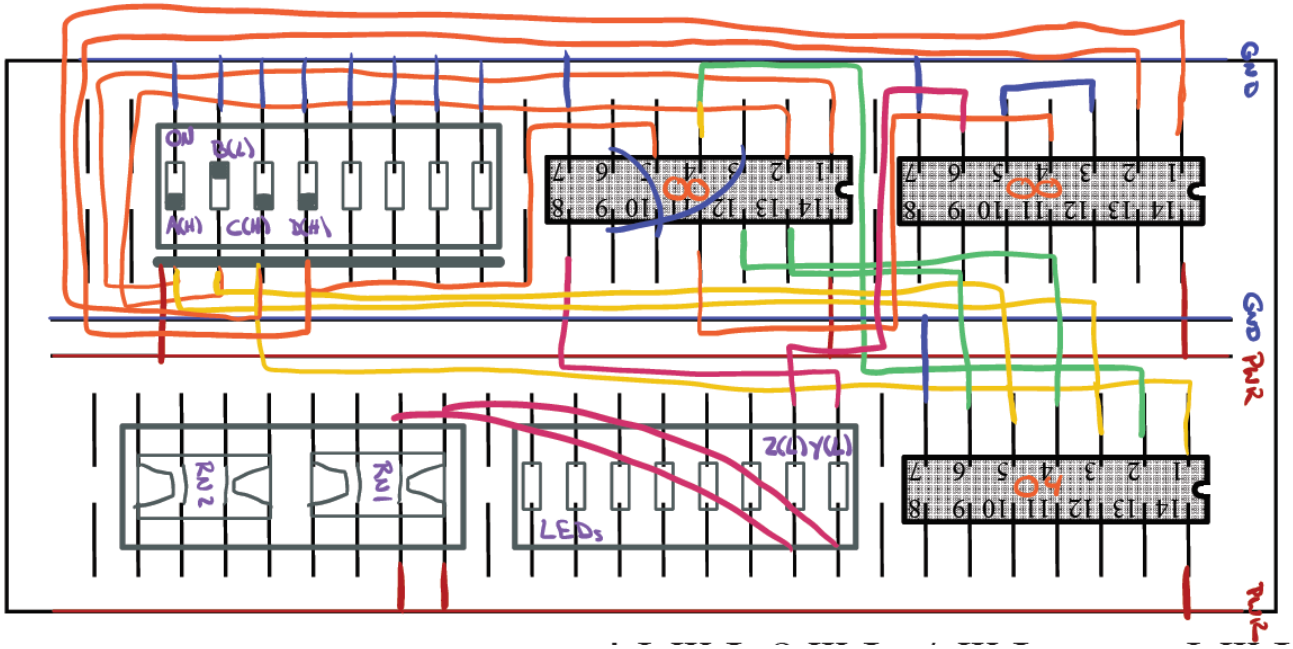


Truth Table (Y)								
A	B_L	C	D	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]_L
0	0	0	0	1	1	0	0	1
0	0	0	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	0	1
0	1	0	0	0	1	0	0	1
0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	1
0	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	0	0
1	0	0	1	1	0	1	1	0
1	0	1	0	1	1	1	0	0
1	0	1	1	1	0	1	0	0
1	1	0	0	0	1	0	0	1
1	1	0	1	0	0	0	1	0
1	1	1	0	0	1	0	0	1
1	1	1	1	0	0	0	0	1

Voltage Table (Y)								
A	B_L	C	D	/B	/D	(A*/B)	/(C + /D)	/[(A*/B)+(C+/D)]_L
L	L	L	L	H	H	L	L	L
L	L	L	H	H	L	L	H	H
L	L	H	L	H	H	L	L	L
L	L	H	H	H	L	L	L	L
L	H	L	L	L	H	L	L	L
L	H	L	H	L	L	L	H	H
L	H	H	L	L	H	L	L	L
L	H	H	H	L	L	L	L	L
H	L	L	L	H	H	H	L	L
H	L	L	H	H	L	H	H	H
H	L	H	L	H	H	H	L	L
H	L	H	H	H	L	H	L	L
H	H	L	L	L	H	L	L	H
H	H	L	H	L	L	L	H	H
H	H	H	L	L	H	L	L	H
H	H	H	H	L	L	L	L	H

Truth Table (Z)							
A	B_L	C	D	/B	(A + /B)	/(C*D)	[(A+/B)*/(C*D)]_L
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	1
0	0	1	0	1	1	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	0
0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	1
1	1	0	1	0	1	1	1
1	1	1	0	0	1	1	1
1	1	1	1	0	1	0	0

Voltage Table (Z)							
A	B_L	C	D	/B	(A + /B)	/(C*D)	[(A+/B)*/(C*D)]_L
L	L	L	L	H	H	H	H
L	L	L	H	H	H	H	H
L	L	H	L	H	H	H	H
L	L	H	H	H	H	L	H
L	H	L	L	L	L	H	L
L	H	L	H	L	L	H	L
L	H	H	L	L	L	H	L
L	H	H	H	L	L	L	H
H	L	L	L	H	H	H	L
H	L	L	H	H	H	H	L
H	L	H	L	H	H	H	L
H	L	H	H	H	H	L	H
H	H	L	L	L	H	H	L
H	H	L	H	L	H	H	L
H	H	H	L	L	H	H	L
H	H	H	H	L	H	L	H


GND
GND PWR
PWR
RN2
RN1
LEDs