**PRE-LAB QUESTIONS OR EXERCISES**

N/A

**PROBLEMS ENCOUNTERED**

N/A

**REQUIREMENTS NOT MET**

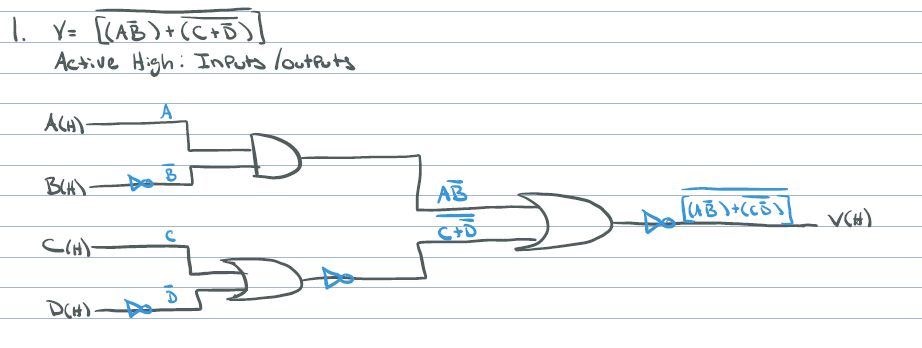
N/A

**FUTURE WORK/APPLICATIONS**

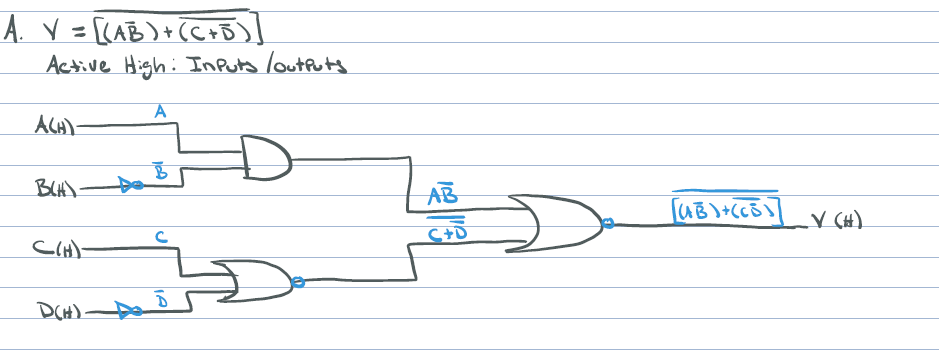
In this lab I learned how to build basic circuits involving inputs, gate to manipulate the inputs, and outputs that show the result. This lab is the building block for the labs to come as it introduced me to some fundamental concepts such as active high/low, pull-up/down resistors for switches, and other basic knowledge that will help me in the future of this class.

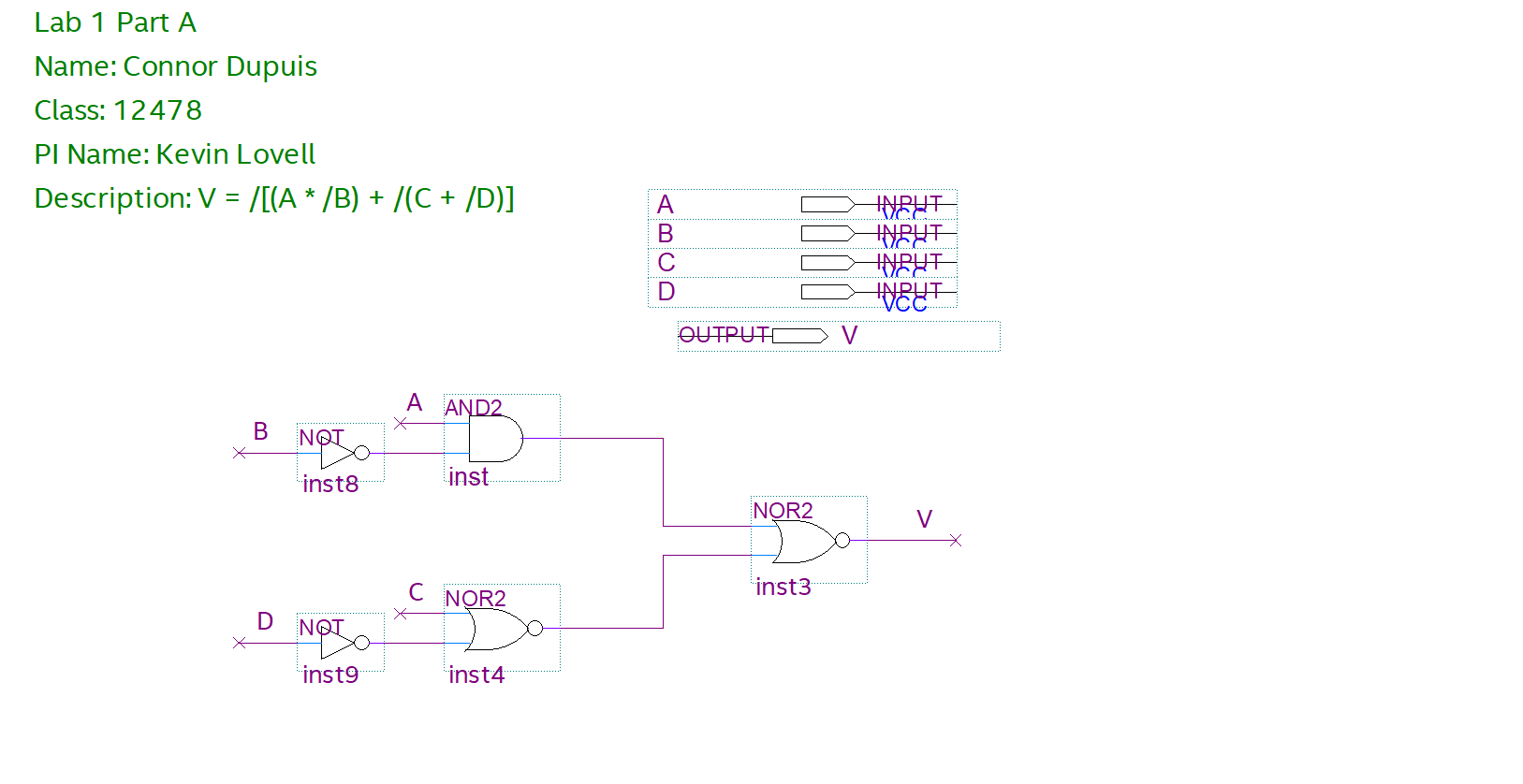
**PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)**

**Introduction Question**

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**Part A**

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The respective inputs and outputs of the design above. All input and output signals are active high.

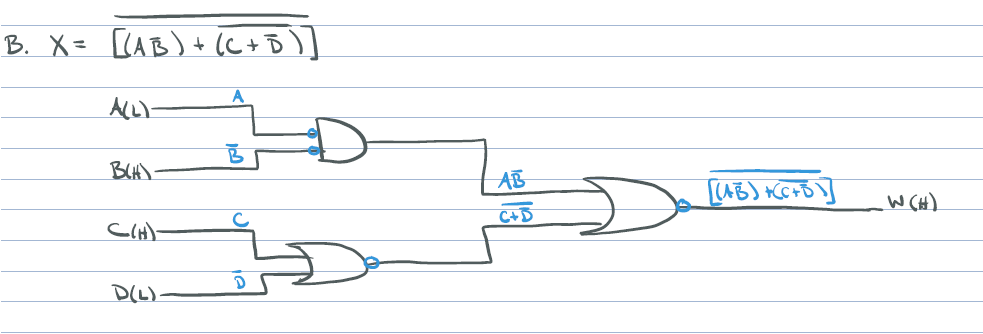
A screenshot of a social media post

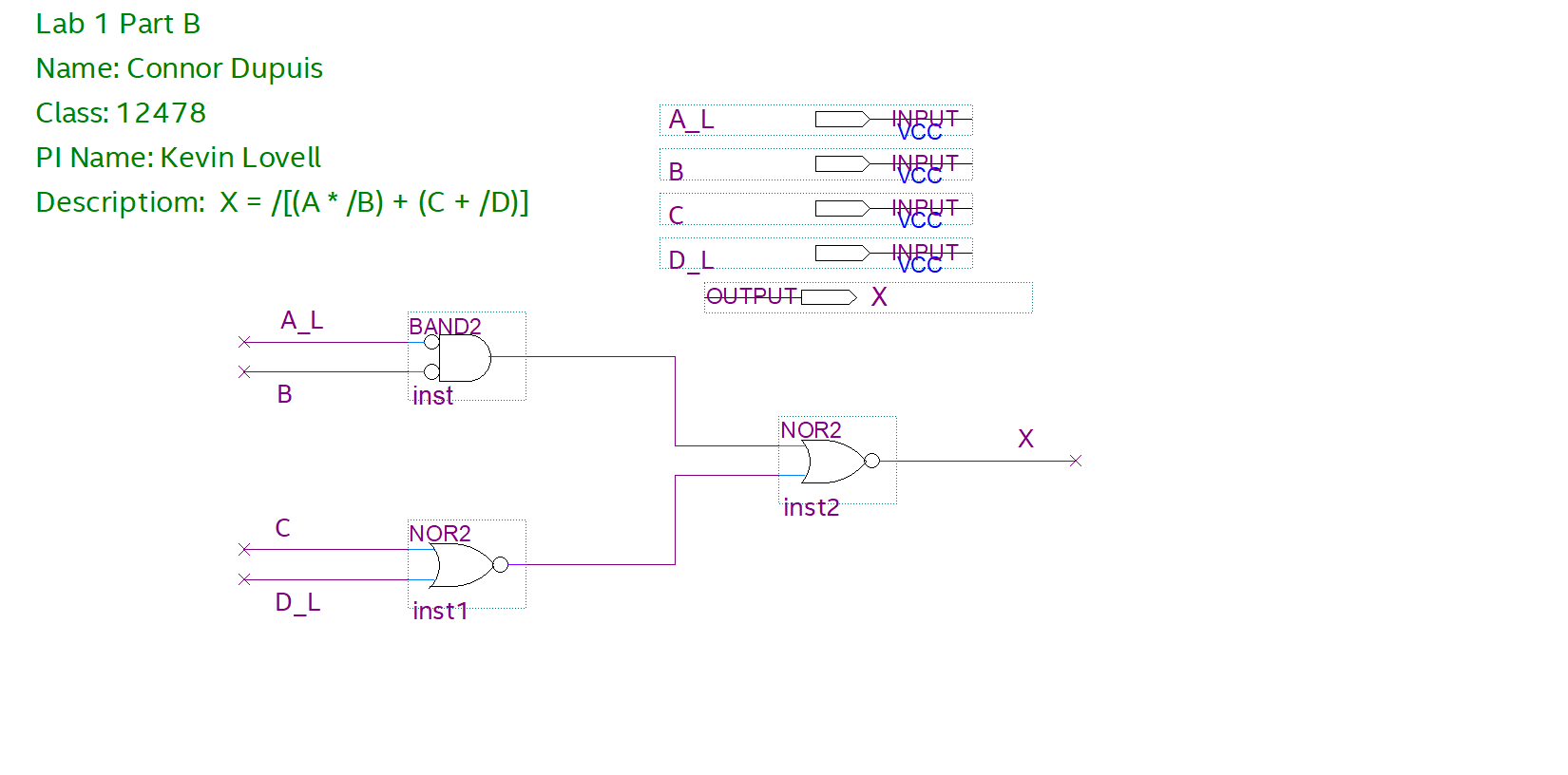
Description automatically generated

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Truth Table | | | | | | | | |
| A | B | C | D | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)] |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Voltage Table | | | | | | | | |
| A | B | C | D | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)] |
| L | L | L | L | H | H | L | L | H |
| L | L | L | H | H | L | L | H | L |
| L | L | H | L | H | H | L | L | H |
| L | L | H | H | H | L | L | L | H |
| L | H | L | L | L | H | L | L | H |
| L | H | L | H | L | L | L | H | L |
| L | H | H | L | L | H | L | L | H |
| L | H | H | H | L | L | L | L | H |
| H | L | L | L | H | H | H | L | L |
| H | L | L | H | H | L | H | H | L |
| H | L | H | L | H | H | H | L | L |
| H | L | H | H | H | L | H | L | L |
| H | H | L | L | L | H | L | L | H |
| H | H | L | H | L | L | L | H | L |
| H | H | H | L | L | H | L | L | H |
| H | H | H | H | L | L | L | L | H |

**Part B**

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The respective inputs and outputs of the design above. With inputs A and D being active low; and B and C being active high. The output signal is active high.

A picture containing screenshot

Description automatically generated

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Truth Table | | | | | | | | |
| A\_L | B | C | D\_L | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)] |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

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| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Voltage Table | | | | | | | | |
| A\_L | B | C | D\_L | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)] |
| L | L | L | L | H | H | L | L | L |
| L | L | L | H | H | L | L | H | L |
| L | L | H | L | H | H | L | L | L |
| L | L | H | H | H | L | L | L | L |
| L | H | L | L | L | H | L | L | L |
| L | H | L | H | L | L | L | H | H |
| L | H | H | L | L | H | L | L | H |
| L | H | H | H | L | L | L | L | H |
| H | L | L | L | H | H | H | L | L |
| H | L | L | H | H | L | H | H | H |
| H | L | H | L | H | H | H | L | H |
| H | L | H | H | H | L | H | L | H |
| H | H | L | L | L | H | L | L | L |
| H | H | L | H | L | L | L | H | H |
| H | H | H | L | L | H | L | L | H |
| H | H | H | H | L | L | L | L | H |

**Part C**

**A screenshot of a cell phone

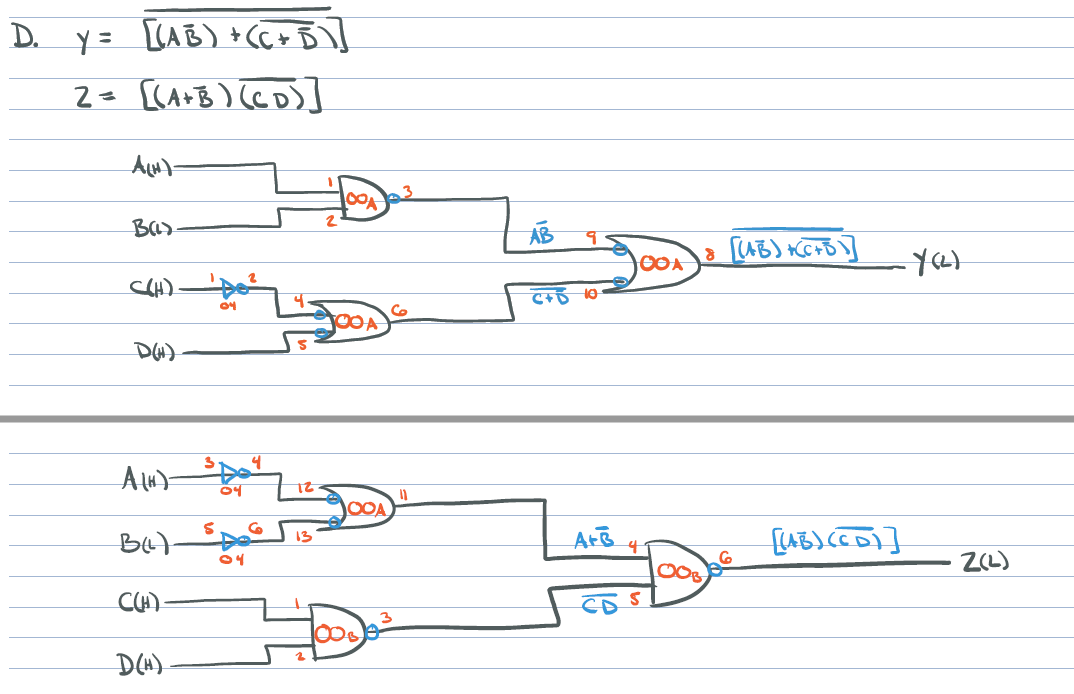
Description automatically generated**

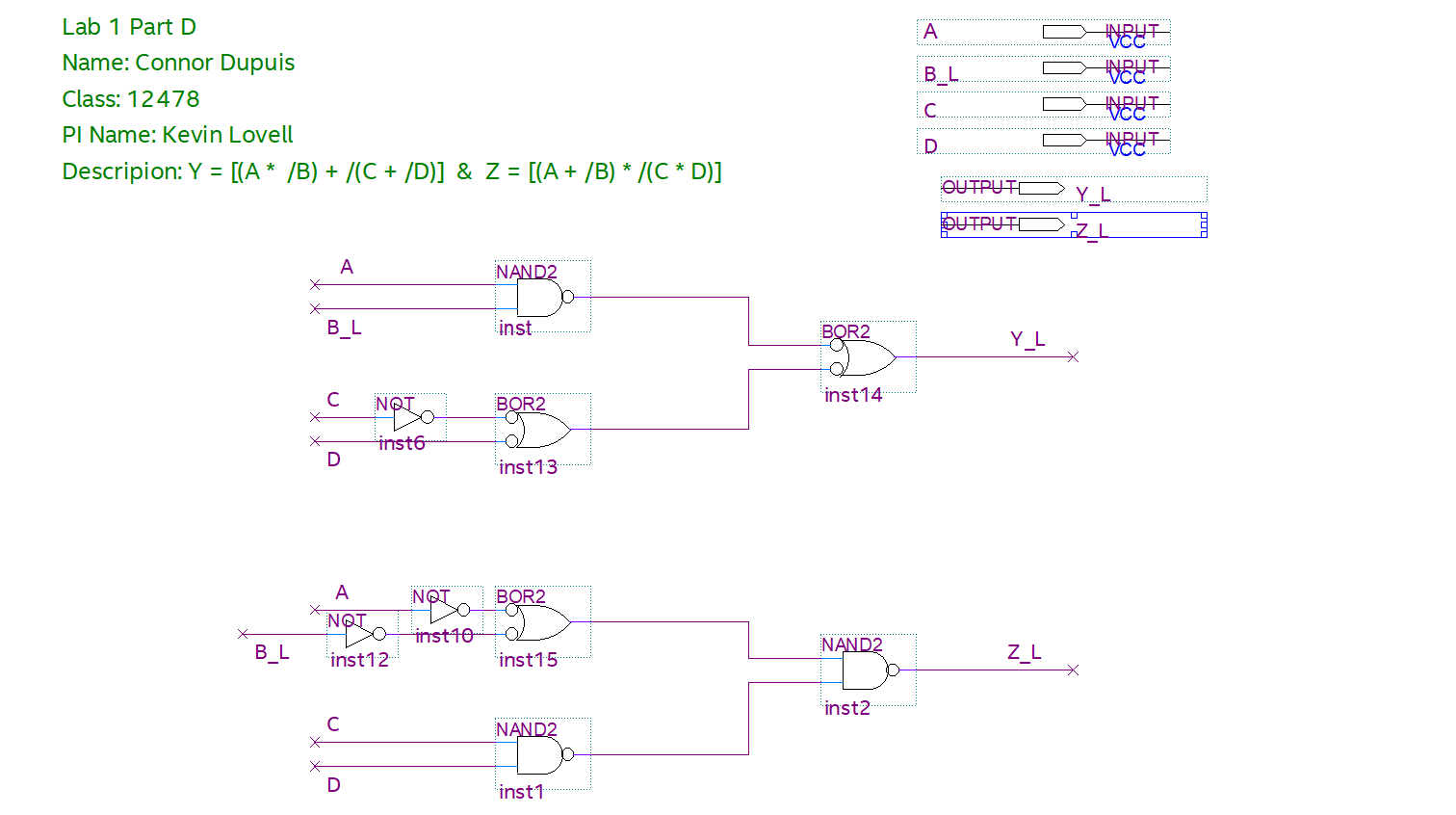
**A screenshot of a computer

Description automatically generated**

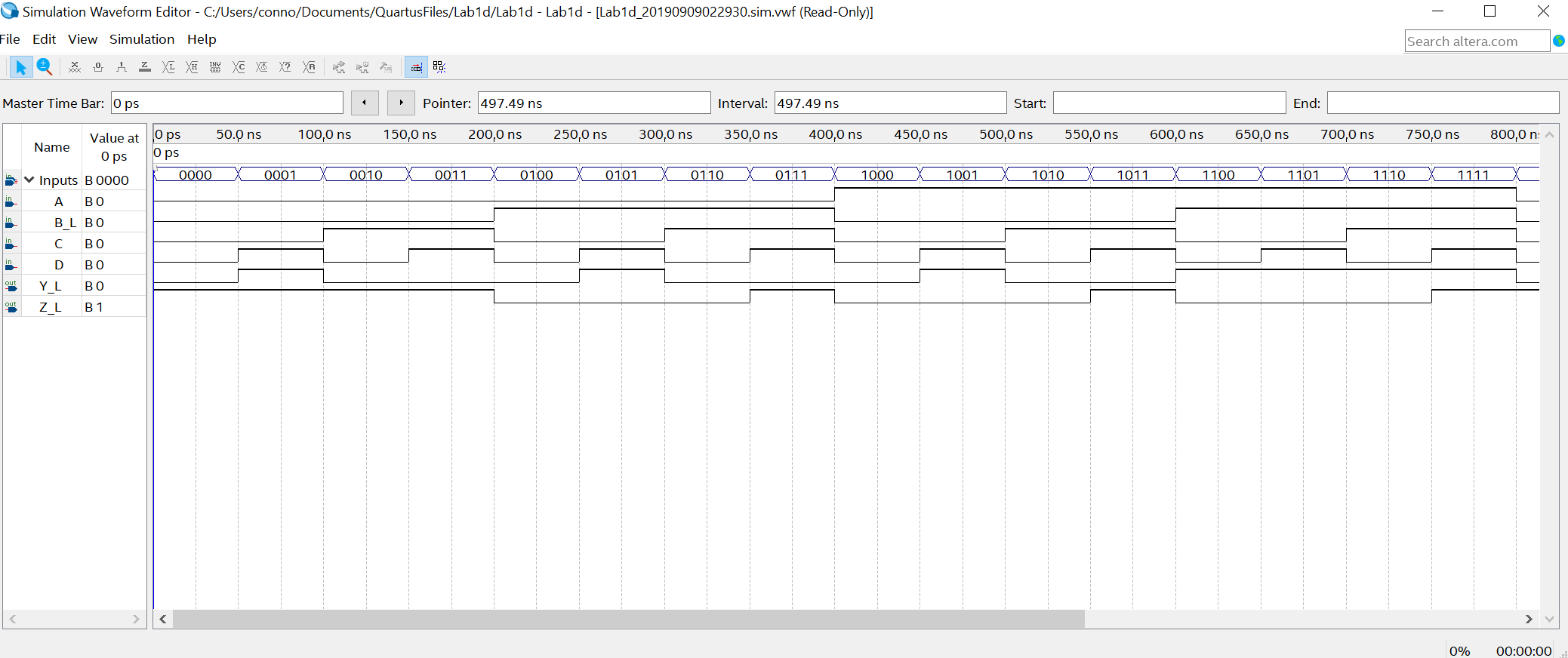
The respective inputs and outputs of the design above. With all input and output signals are active high.

**Part D**

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The respective inputs and outputs of the design above. With input signals A, C, and D being active high and input B being active low. Both output signals are active low.



|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Truth Table (Y) | | | | | | | | |
| A | B\_L | C | D | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)]\_L |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Voltage Table (Y) | | | | | | | | |
| A | B\_L | C | D | /B | /D | (A\*/B) | /(C + /D) | /[(A\*/B)+(C+/D)]\_L |
| L | L | L | L | H | H | L | L | L |
| L | L | L | H | H | L | L | H | H |
| L | L | H | L | H | H | L | L | L |
| L | L | H | H | H | L | L | L | L |
| L | H | L | L | L | H | L | L | L |
| L | H | L | H | L | L | L | H | H |
| L | H | H | L | L | H | L | L | L |
| L | H | H | H | L | L | L | L | L |
| H | L | L | L | H | H | H | L | L |
| H | L | L | H | H | L | H | H | H |
| H | L | H | L | H | H | H | L | L |
| H | L | H | H | H | L | H | L | L |
| H | H | L | L | L | H | L | L | H |
| H | H | L | H | L | L | L | H | H |
| H | H | H | L | L | H | L | L | H |
| H | H | H | H | L | L | L | L | H |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Truth Table (Z) | | | | | | | |
| A | B\_L | C | D | /B | (A + /B) | /(C\*D) | [(A+/B)\*/(C\*D)]\_L |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Voltage Table (Z) | | | | | | | |
| A | B\_L | C | D | /B | (A + /B) | /(C\*D) | [(A+/B)\*/(C\*D)]\_L |
| L | L | L | L | H | H | H | H |
| L | L | L | H | H | H | H | H |
| L | L | H | L | H | H | H | H |
| L | L | H | H | H | H | L | H |
| L | H | L | L | L | L | H | L |
| L | H | L | H | L | L | H | L |
| L | H | H | L | L | L | H | L |
| L | H | H | H | L | L | L | H |
| H | L | L | L | H | H | H | L |
| H | L | L | H | H | H | H | L |
| H | L | H | L | H | H | H | L |
| H | L | H | H | H | H | L | H |
| H | H | L | L | L | H | H | L |
| H | H | L | H | L | H | H | L |
| H | H | H | L | L | H | H | L |
| H | H | H | H | L | H | L | H |

A close up of a map

Description automatically generated