**PRE-LAB QUESTIONS OR EXERCISES**

N/A

**PROBLEMS ENCOUNTERED**

N/A

**REQUIREMENTS NOT MET**

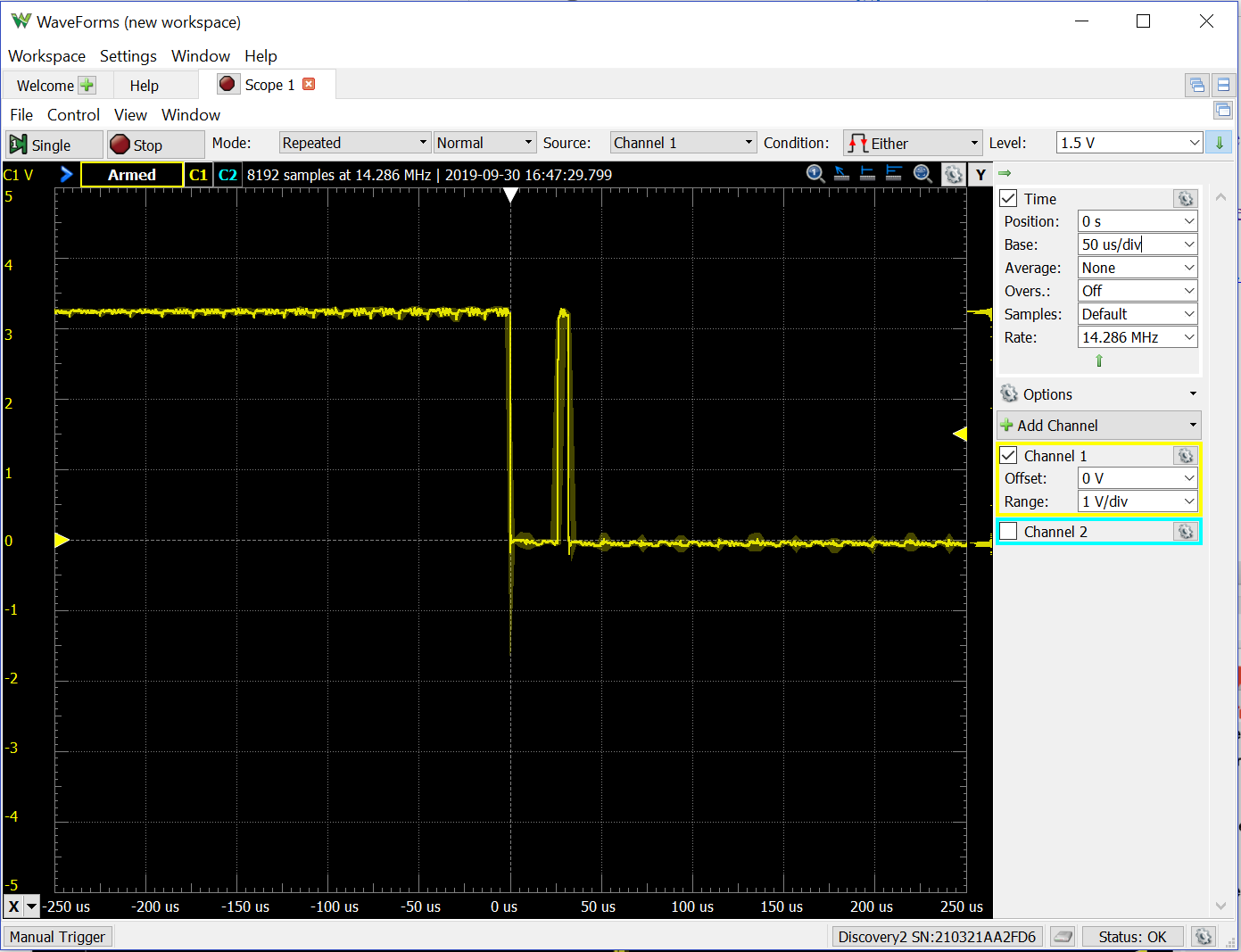
N/A

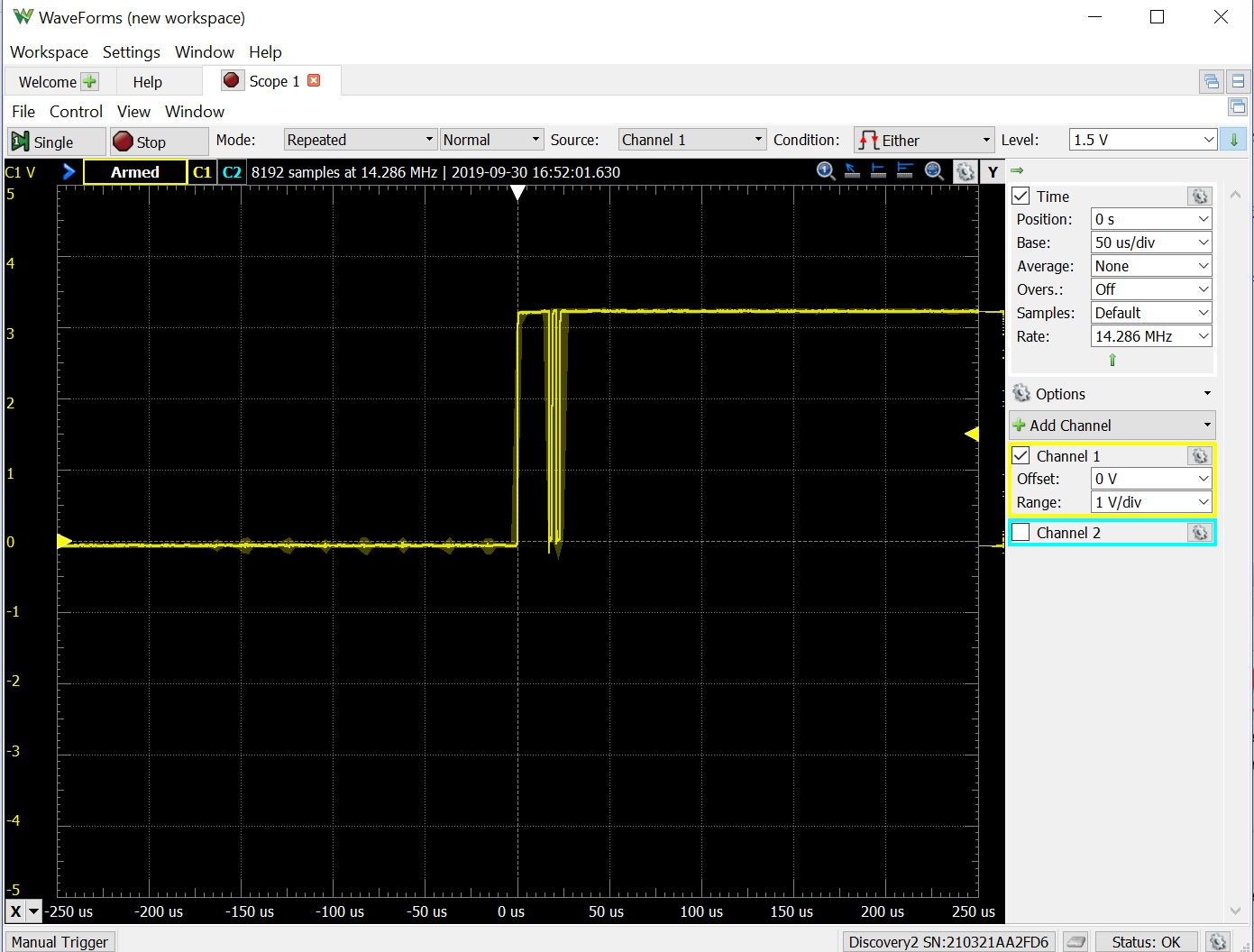
**FUTURE WORK/APPLICATIONS**

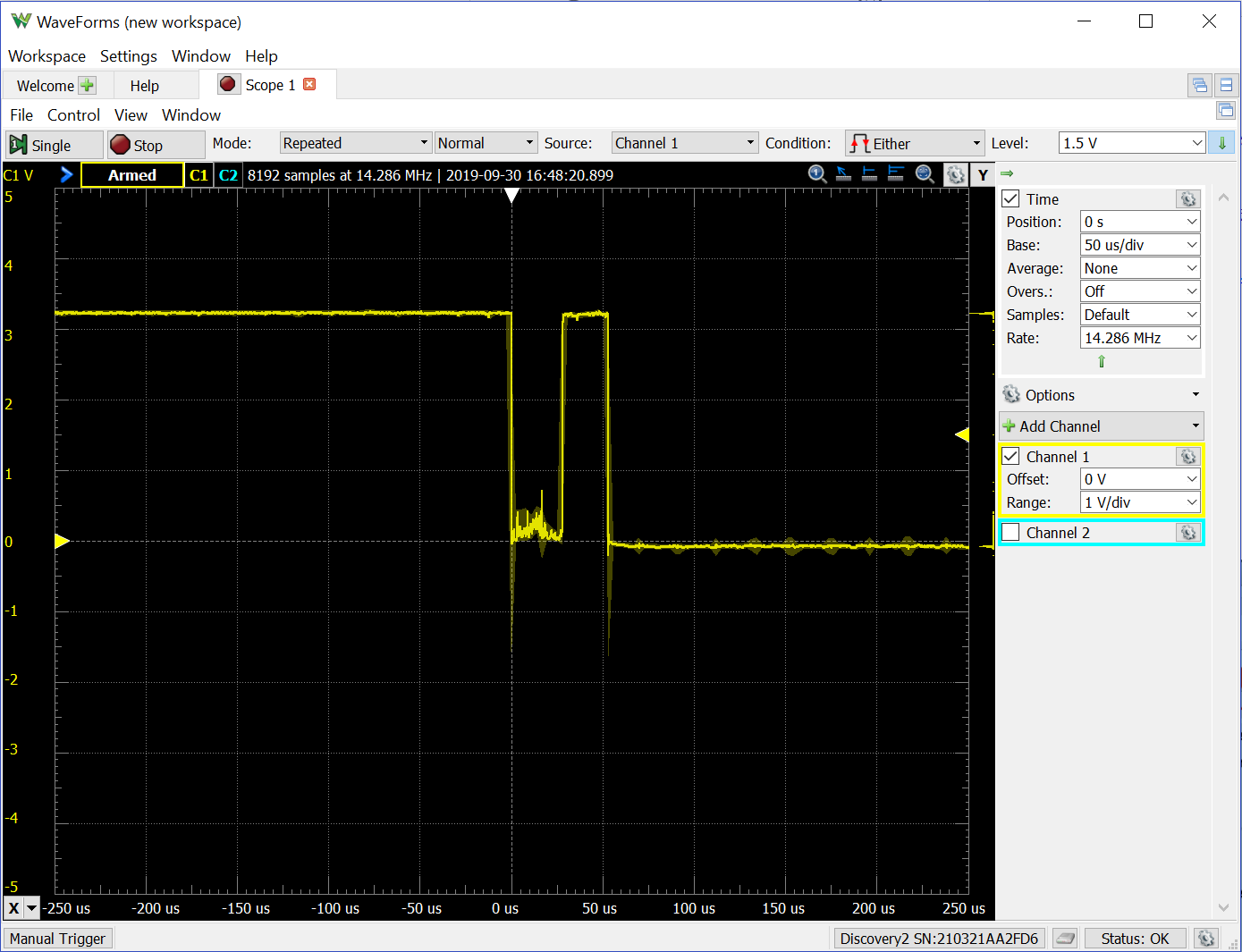
In this lab we use debouncing switch circuit with SPDT switch to act our input for our counters. We also use flip-flops and implement them to create our counter. This understanding of these circuit designs leads to further implementation such as more complex state machines and counters that are even more complex.

**PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)**

**Bouncing SPST Circuit**

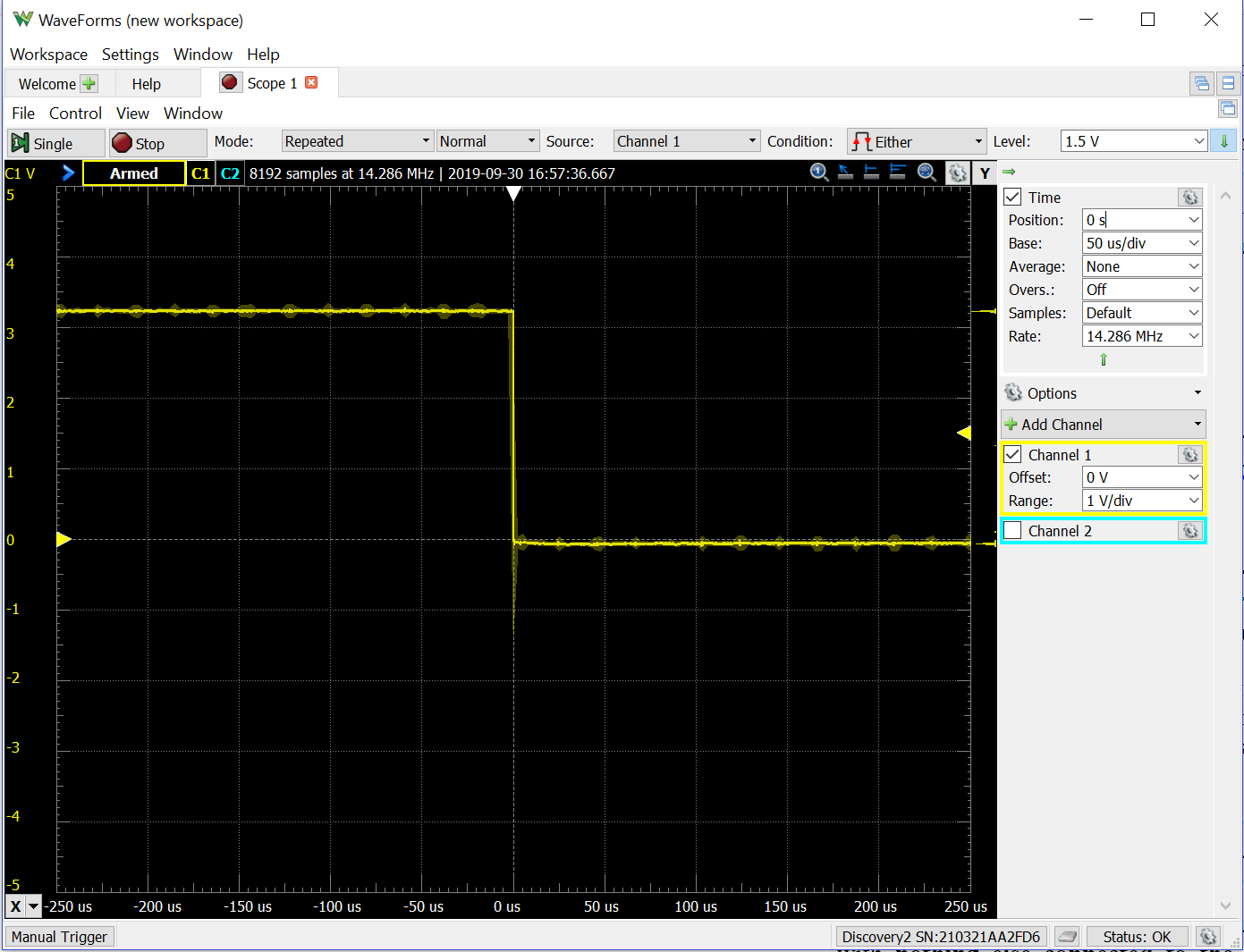
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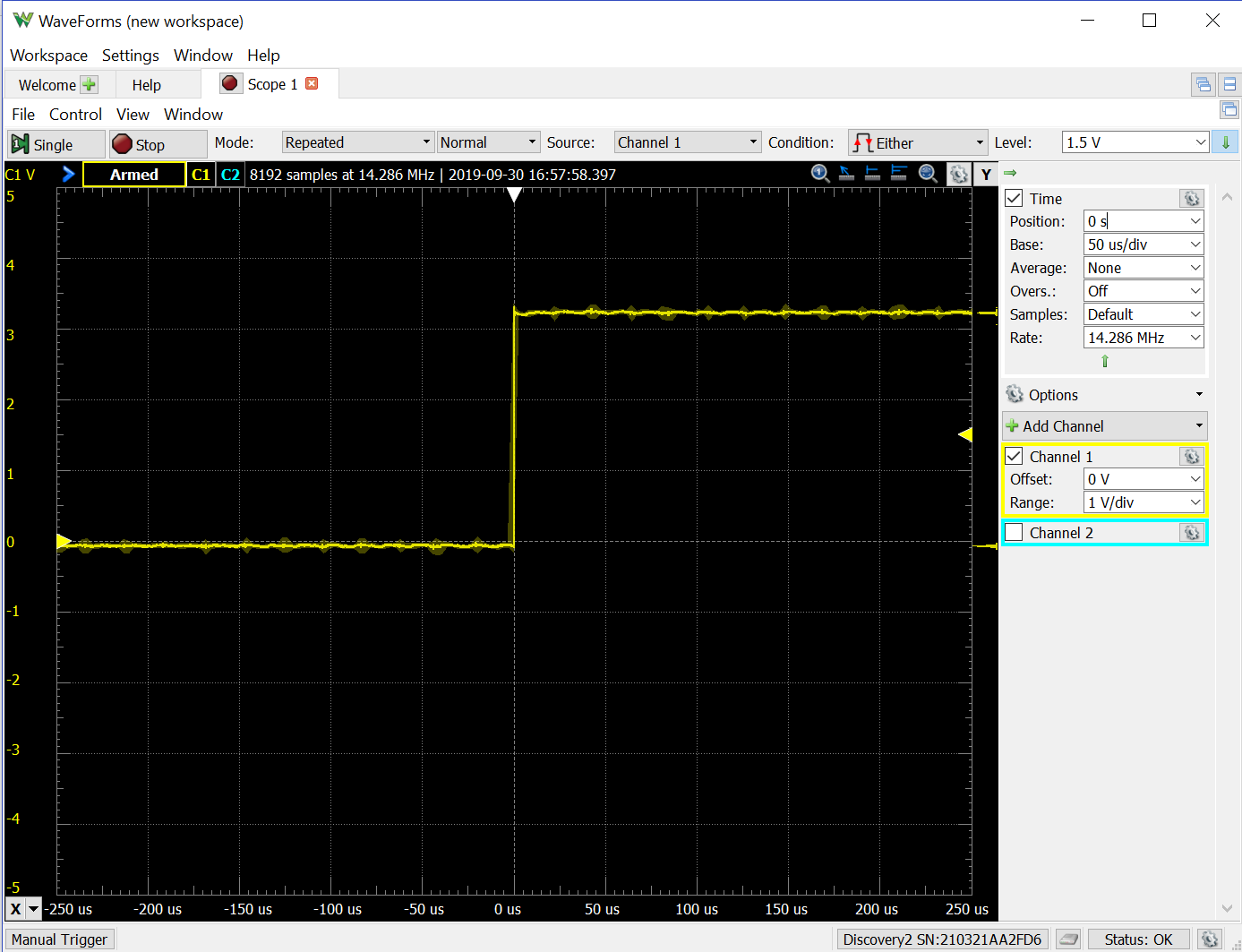
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The clocks that would occur would be the number of times it bounced. In this case it bounced 5 times total so it would be 5 clocks assuming forward.

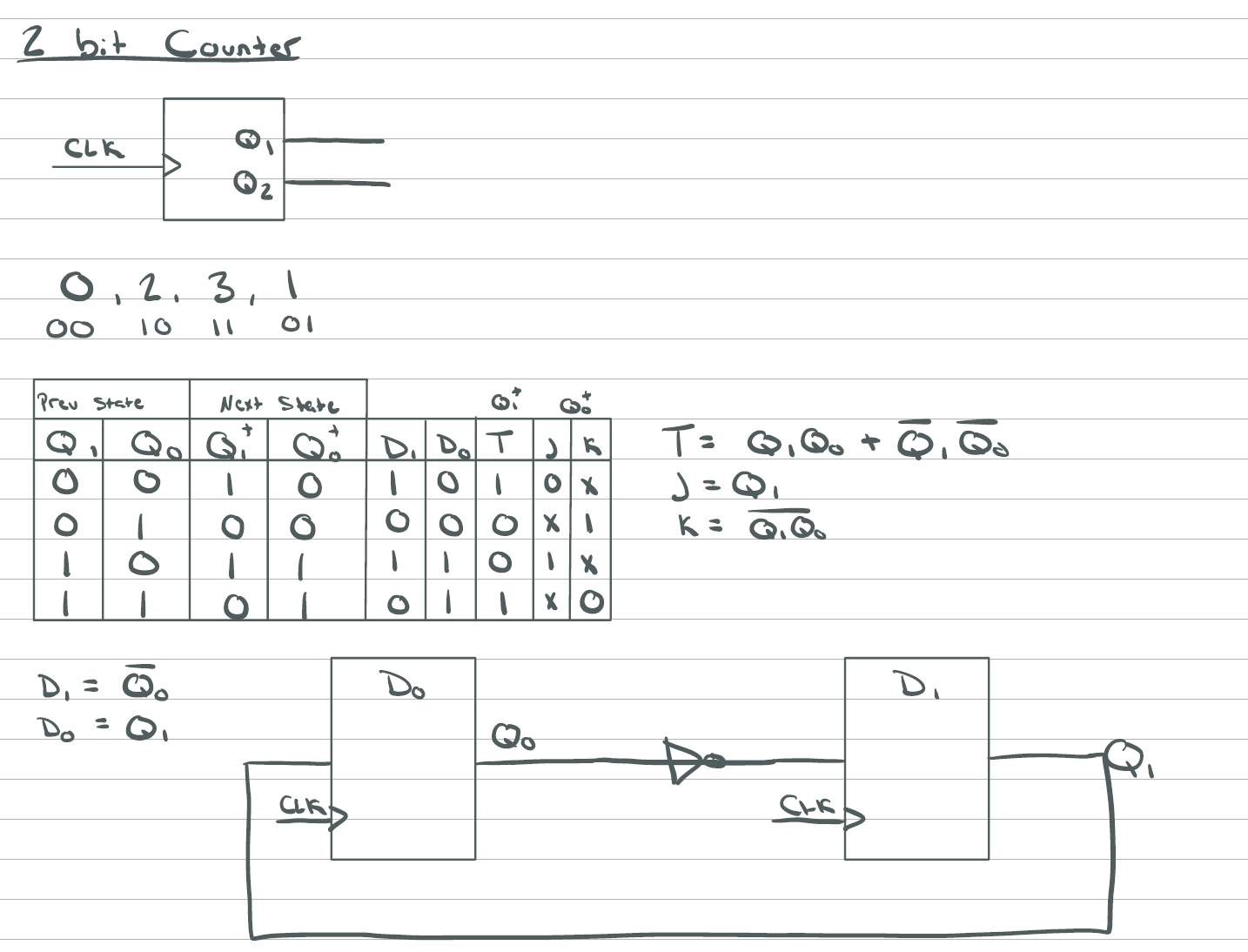
**Debounce SPDT Circuit**

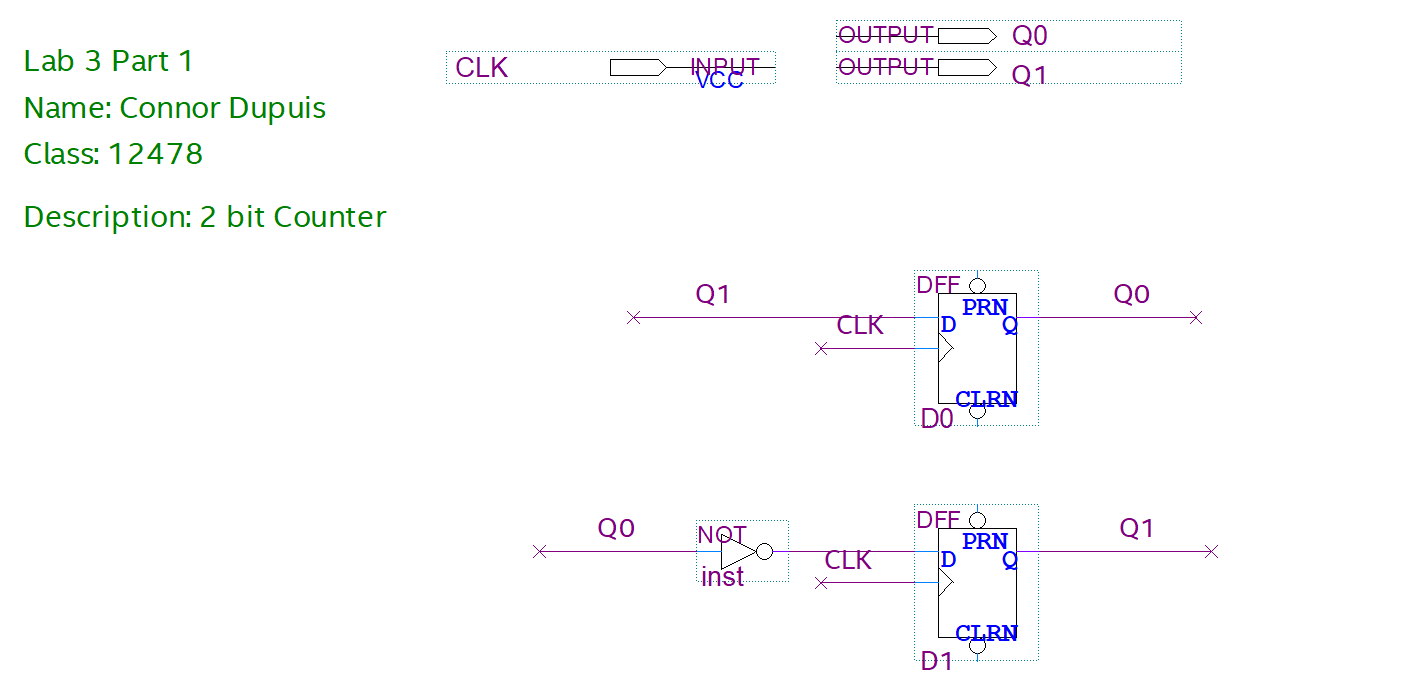
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This switch would only bounces once, so only one clock is recorded.

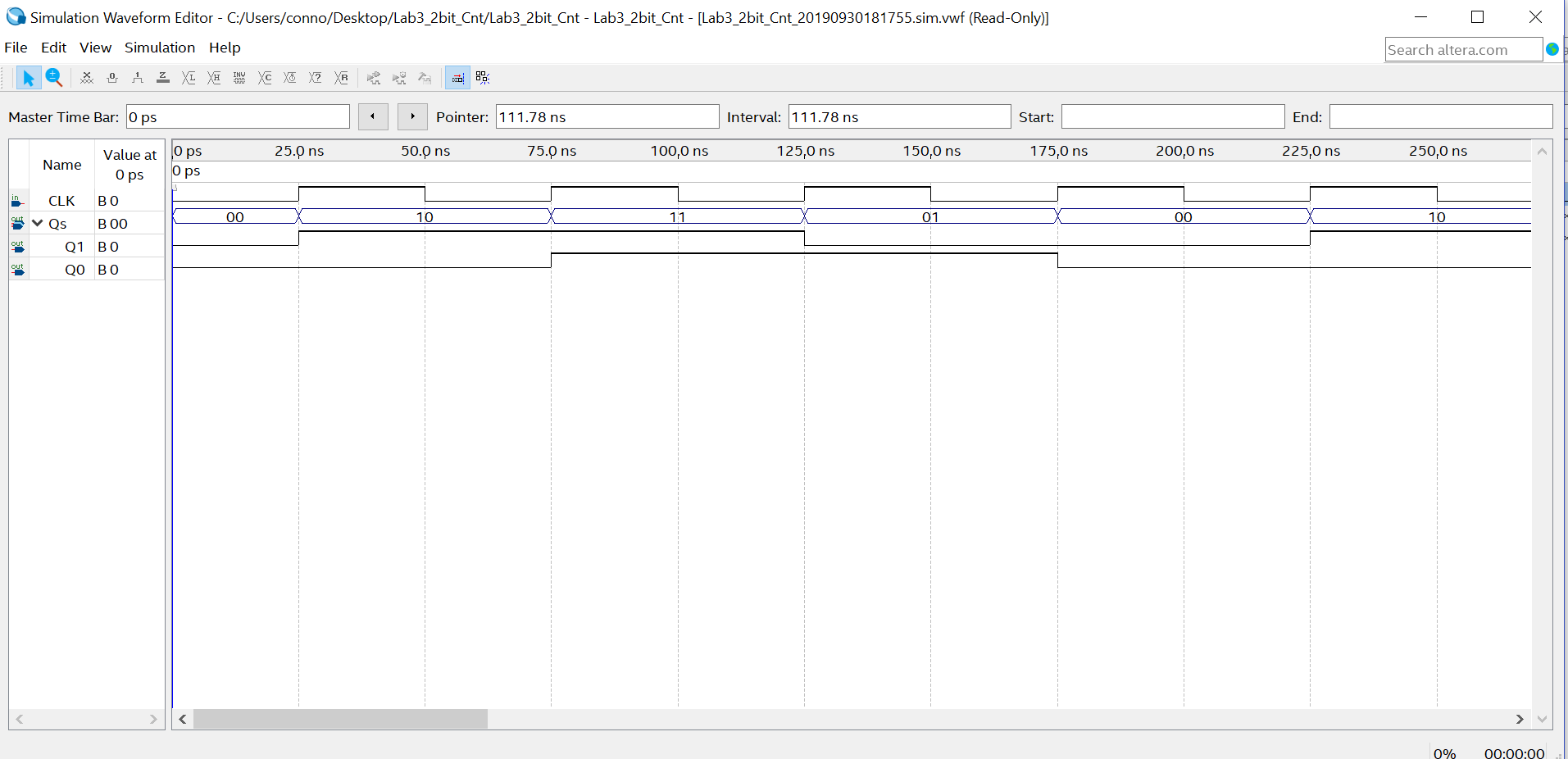
**2-bit Counter**

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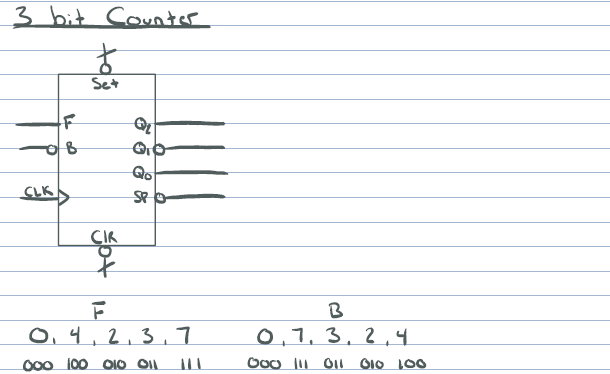
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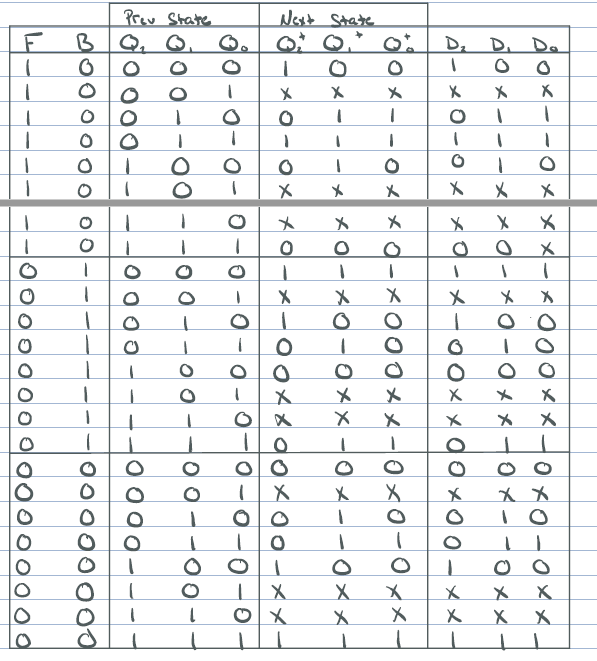
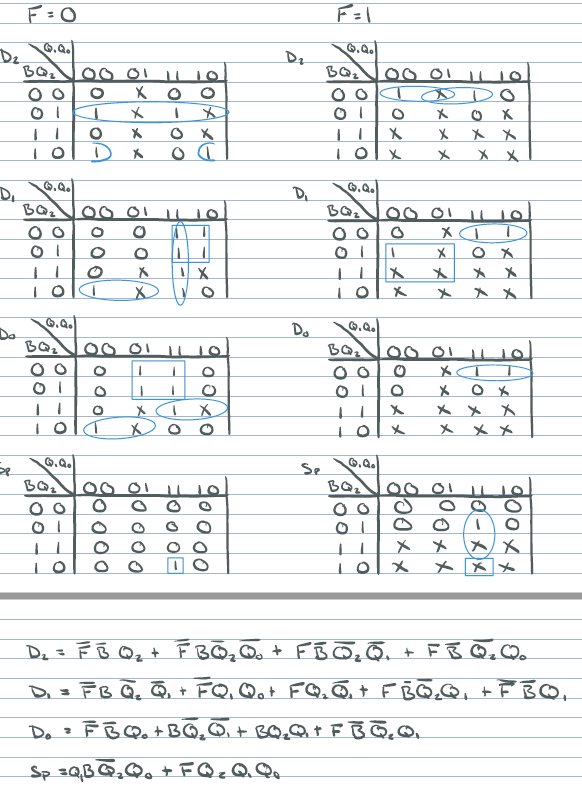
The counting number in binary. 0-2-3-1.

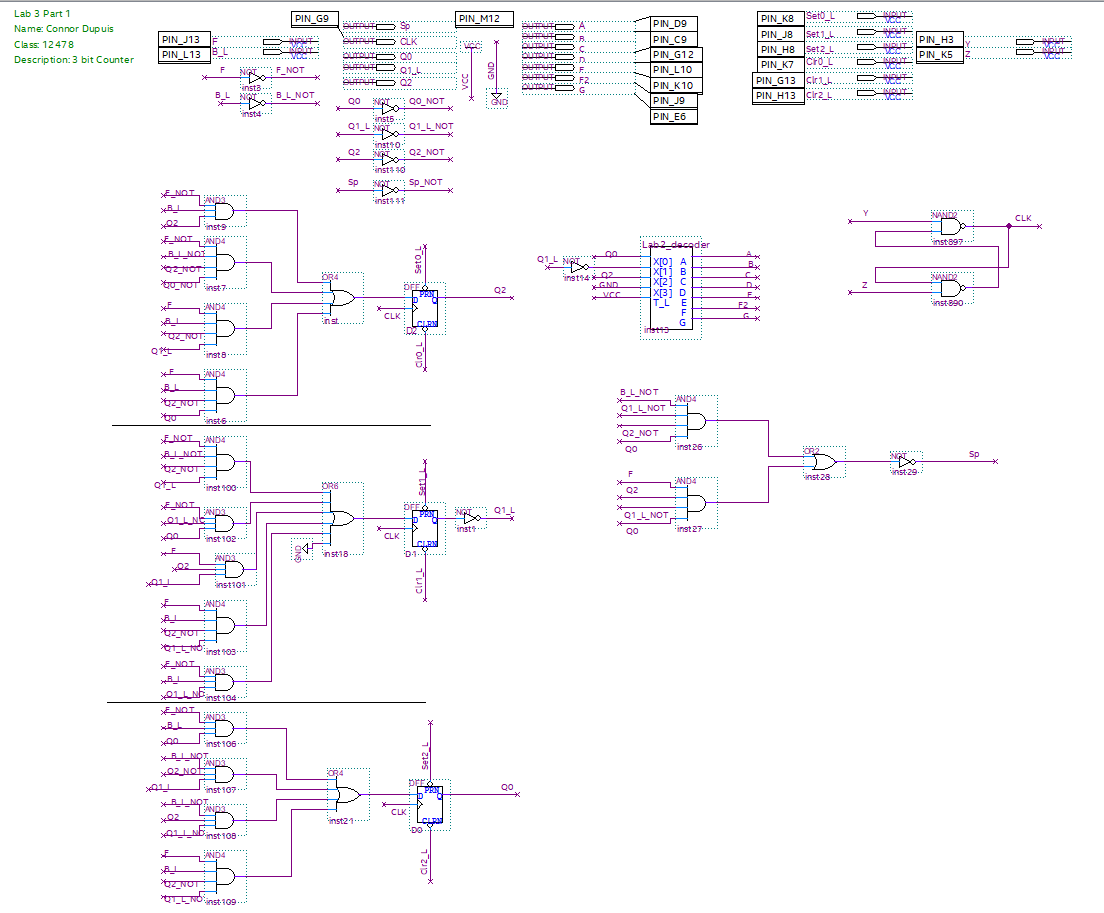
Clock is rising, meaning the count is increasing.

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**3-bit Counter**

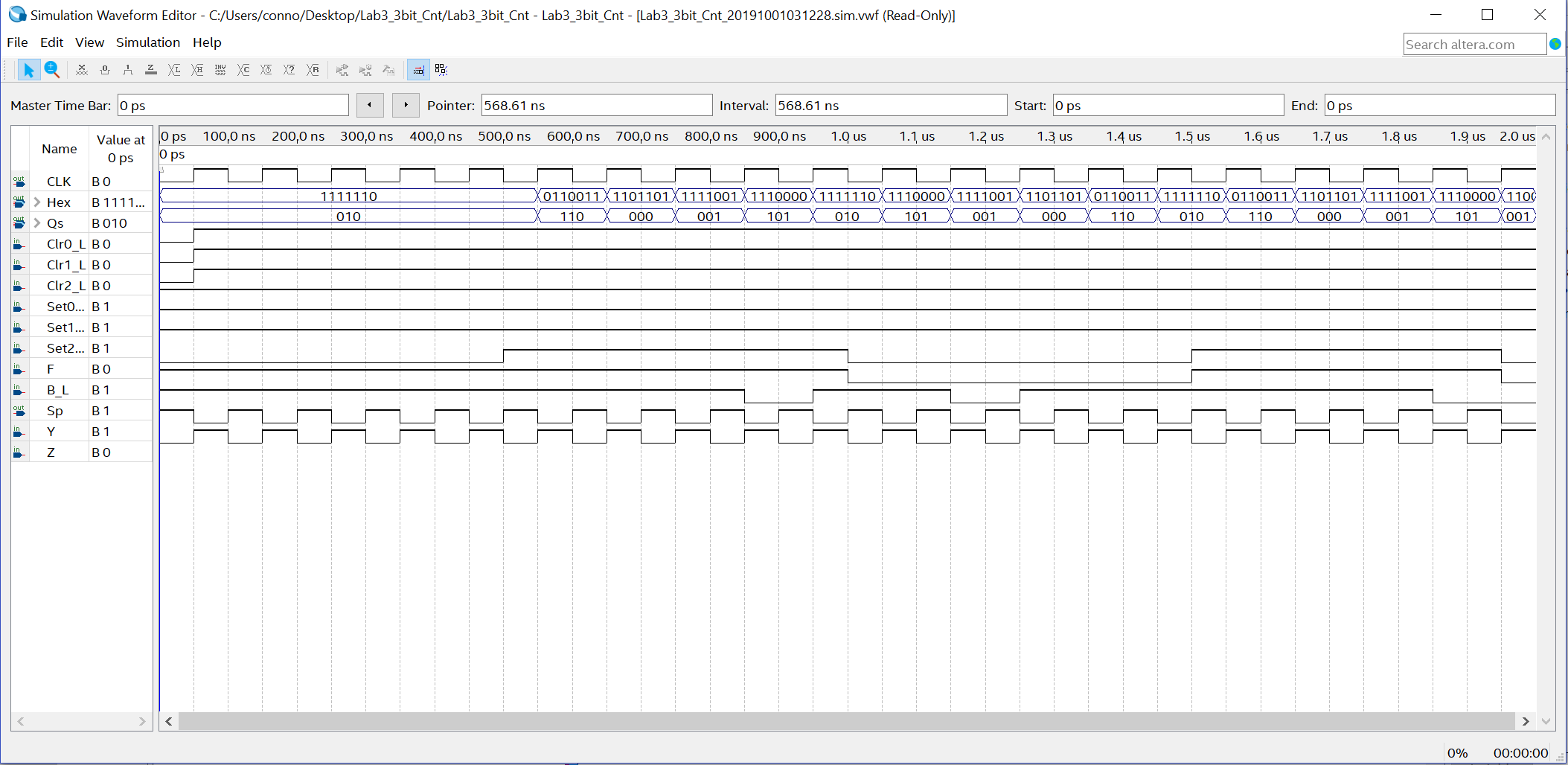
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Special, active low only turns on when F is true at 111, and when B is true at 011.

Clock is rising, meaning the count is increasing.

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F is off and B is on, so the counter is backwards.

F is on and B is off, so the counter is forwards.

F and B are both off, so the number is held.

The activation of the 7-segment display representing Hex.

**2-bit Counter T and JK Redesign**

**A close up of a map

Description automatically generated**

**A picture containing screenshot

Description automatically generated**

The counting number in binary. 0-2-3-1.

Clock is rising, meaning the count is increasing.