MT2523 Series Datasheet

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Features

Platform

- 208MHz ARM® Cortex®-M4 with FPU
- High power efficiency with system DVFS
  - 1.3V, 208MHz
  - 1.2V, 104MHz
  - 1.1V, 104MHz
  - 0.9V, 26MHz
  - 0.7V, 32kHz
- Hardware DVS from deep sleep (0.7V) to active (0.9V or above)
- Fast 7µs wakeup from sleep to active
- Hardware DFS from 1.6MHz to 208MHz
- 17 DMA channels
- One RTC timer and six GPTs
- Crypto engine AES 128/192/256 bits
- True random number generator
- Ambient temperature from -40°C to 85°C

Memory

- 160kB SRAMs
  - Zero-wait state
  - Maximum frequency 208MHz
- 32kB L1 cache
  - High hit rate
  - Zero-wait state
  - Maximum frequency 208MHz
- Embedded flash
  - Sleep current 100nA
  - Maximum frequency 78MHz
- Embedded pseudo SRAM
  - Sleep current 10µA
  - Maximum frequency 104MHz

Connectivity

- One USB2.0
- Two SDIO v2.0
- Three I2C (3.4Mbps) interfaces
- Three UARTs (3Mbps)
- Four SPI master and one SPI slave (13MHz)
- I2S master or slave
- PCM master
- Dual PDM digital MIC
- Six PWM channels
- 38 GPIOs
- 5 channel 12-bit AUXADC
- 10-bit general purpose DAC
- 3 x 3 matrix keypad

Bluetooth

- Bluetooth specification 4.2
- Dual mode (Bluetooth and Bluetooth LE)
- Integrated T/R switch, Balun and PA
- PA provides 7.5dBm output power
- Bluetooth and Bluetooth LE receiver sensitivity of -93dBm and -96.5dBm, respectively
- Up to 7 simultaneous active ACL links
- One SCO or eSCO link with CVSD/mSBC coding

Audio codec

- AAC/SBC for Bluetooth audio
- CVSD/mSBC for Bluetooth speech
- PCM playback with 8-48kHz sample rate

- PCM record with 8kHz and 16kHz sample rate

Display

- Hardware 2D accelerator supporting:
  - 4 overlay layers
  - ARGB8888, RGB888, RGB565, ARGB6666
  - BitBlt supports 7 rotation types
  - Alpha blending and font drawing
  - Hardware display rotation
- Four blending layers with individual color depth, window size, vertical and horizontal offset, source key, dither and alpha value
- Read frame buffer format - RGB565, RGB888, ARGB8888, PARGB8888, ARGB6666, PARGB6666, YUYV422, index-4, index-2 and index-1 color
- DBI serial interface supporting 320 x 320 pixels and 30fps resolution
- 1-lane MIPI DSI interface with 480x320 pixels and 30fps resolution (not supported in MT2523S)

Camera

- MediaTek camera serial interface
- VGA at 30fps with YUV422 or RGB565

Power management

- Wide Li+ battery voltage from 3.0V to 4.8V
- Multiple power supplies for 1.8V, 2.8V and 3.3V
- Power switch of 1.8V, 2.8V, 3.3V for low power mode
- High efficiency buck (from 0.7V to 1.3V) for SOC platform
- Pulse charger supports BC1.2
- 15-bit AUXADC for BATSNS
- Hardware thermal shutdown protection
- Supports LED current sink
- Supports Vibrator driver
- Supports WDT system reset
- Supports power key and long press shutdown

GNSS (MT2523G only)

- GPS, GLONASS, GALILEO and BEIDOU
- Supports multi-GNSS including QZSS, SBAS ranging
- Supports WAAS/EGNOS/MSAS/GAGAN
- 12 multi-tone active interference cancellers (ISSCC2011 award)
- Indoor and outdoor multi-path detection and compensation
- Supports FCC E911 compliance and A-GPS

Package

- Highly integrated chipset technology
- MT2523G: 9.2 x 6.0 x 1.05mm 246-ball TFBGA with 0.4mm pitch (with GNSS)
- MT2523D: 6.2 x 5.8 x 1.05mm 165-ball TFBGA with 0.4mm pitch
- MT2523S: 6.2 x 5.8 x 1.05mm 165-ball TFBGA with 0.4mm pitch

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1. Overview

MediaTek MT2523 series is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT2523 series is a feature-rich and powerful single-chip, ANT hardware ready solution with Bluetooth and Bluetooth Low Energy (LE) connectivity support. Based on ARM Cortex-M4 processor, MT2523 series processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance wearable and leading edge sensor control applications.

MT2523 series is optimized for wearable products with the following strengths:

- Small package size.
- Low power consumption for active and idle modes.
- Dynamic voltage scaling for optimized computing power.
- Built-in sensor hub and optimized sensor data capture engine.

1.1. Platform

MT2523 series runs on Cortex-M4 RISC processor targeting the best trade-off between system performance and power consumption. It also supports internal 32.768kHz real-time clock (RTC) and an internal charger on PMU.

MT2523 series also provides a co-processor to offload the control for Bluetooth or GNSS connectivity.

For large amount of data transfers, high-performance direct memory access (DMA) with hardware flow control is implemented to enhance the data transaction speed while reducing the MCU processing load.

A special sensor DMA provides sensor data capture with low power consumption.

MT2523 series provides hardware security digital rights management for copyright protection. To further safeguard and protect the manufacturer's investment in development, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Table 1.1-1 shows the comparison of MT2523 series chipsets, Figure 1-1 shows the detailed block diagram of MT2523 series chipsets and Figure 1-2 shows the MT2523 system architecture.

Table 1.1-1. MT2523 series chipset comparison

Item	MT2523G	MT2523D	MT2523S
Package size	9.2mm x 6mm x 1.05mm	6.2mm x 5.8mm x 1.05mm	6.2mm x 5.8mm x 1.05mm
Package ball, pitch	246-ball, 0.4mm pitch	165-ball, 0.4mm pitch	165-ball, 0.4mm pitch
GNSS	O	–	–
SiP flash size	32Mbits	32Mbits	16Mbits
SiP PSRAM size	32Mbits	32Mbits	8Mbits
MIPI DSI interface	O	O	–

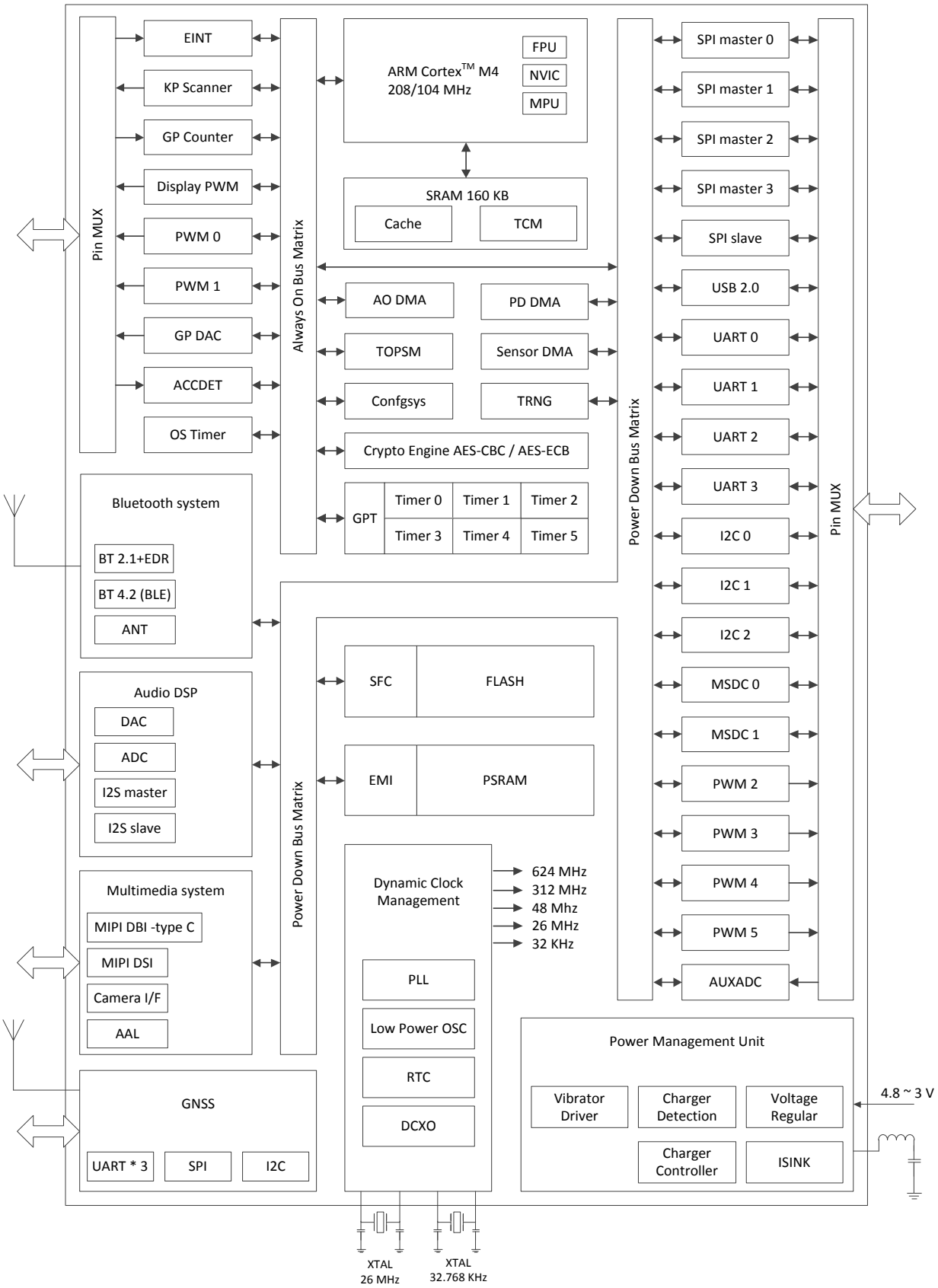


Figure 1-1. MT2523 chipset architecture (only MT2523G with GNSS feature)

UART/I2S	CAM	LCM	PMU
USB-HS	SiP Flash	SiP SRAM	Keypad
I2C	Cortex-M4 with floating point unit 208MHz		ADC 12-bit DAC 10-bit
SDIO	SRAM/cache 160kB	DSP	SiP GNSS
SPI	RTC	Bluetooth® 2.1	Bluetooth® 4.2

Figure 1-2. MT2523 series features

1.1.1. MCU

The supported MCU has the following components and features.

- 208MHz ARM® Cortex®-M4 with floating point unit (FPU).
- High power efficiency with system DVFS.
  - 1.3V, 208MHz
  - 1.2V, 104MHz
  - 1.1V, 104MHz
  - 0.9V, 26MHz
  - 0.7V, 32kHz
- Hardware DVS from deep sleep (0.7V) to active (0.9V or above)
- Fast 7µs wakeup from sleep to active
- Hardware DFS from 1.6MHz to 208MHz

1.1.2. Memory

MT2523 series is embedded with MediaTek-patented low power PSRAM to improve active and idle current consumption.

- MT2523 series support serial flash with various operating frequencies and flash sizes.
  - 160kB SRAMs
  - Zero-wait state
  - Maximum frequency 208MHz
- 32kB L1 cache
  - High hit rate
  - Zero-wait state

- Maximum frequency 208MHz

- SiP Embedded flash
  - Sleep current 100nA
  - Maximum frequency 78MHz
- SiP Embedded pseudo SRAM
  - Sleep current 10µA
  - Maximum frequency 104MHz

1.1.3. Clock source

- 26MHz Digitally Controlled Crystal Oscillator (DCXO), that can supply reference clock for PLLs.
- USB PLL (UPLL) controlled by DCXO with 312MHz fixed frequency.
- Main PLL (MPLL) controlled by UPLL with a maximum frequency at 624MHz.
- Low Frequency RC oscillator (LFOSC) with a maximum frequency at 26MHz. Low power consumption with large frequency variation.
- High Frequency RC oscillator (HFOSC), with a maximum frequency at 312MHz. Low power consumption with large frequency variation.
- 32.768kHz low-speed external crystal (XOSC32K).
- 32.768kHz low-speed internal clock fed from DCXO (DCXO32K).
- 32kHz low-speed internal RC (EOSC32K) with large frequency variation (±5%).

1.1.4. Interfaces and peripherals

MT2523 series supports UART, I2C, SPI, USB 2.0 HS/FS, SDIO and SD storage systems.

MT2523 series brings together all necessary peripheral blocks for multimedia wearable products. The peripheral blocks include real-time clock, PWM and GPIOs, see Table 1.1-2.

Table 1.1-2. MT2523 series peripherals

Peripheral	Counts	Description
Timer	3	–
Keypad	3 x 3 keypad scanner	With double key detection
PWM	6	–
UART	4	Up to 3Mbps
USB	1	2.0 High-Speed
I2C	3	400kbps, Up to 3.4Mbp
I2S	1 master 1 slave	–
SDIO	2	v2.0
SPI	4 masters	–

Peripheral	Counts	Description
	1 slave	
LCM for display	1 serial I/F 1 lane MIPI DSI	MediaTek serial interface
CAM for camera	1 serial I/F	MediaTek serial interface
ADC/DAC	5-channel 12-bit ADC 1-channel 10-bit DAC	–
GPIO	38	Up to 38 ports with 20 interrupts
Crypto engine	1	• Supports AES-CBC/AES-ECB mode. • Key length – 128/192/256 bits.

1.2. Multimedia

The MT2523 series multimedia subsystem provides MediaTek proprietary serial interface for cameras with a camera resolution of up to VGA resolution size and MediaTek proprietary serial interface and MIPI interface for LCM. The resolution of LCM with MIDP DSI interface is up to 480 x 320 pixels and 320 x 320 pixels for DBI serial interface.

The software-based codec can be used to process various video types. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT2523 series are implemented with a high-performance audio synthesis technology and a high-quality audio amplifier. MT2523 also provides voice command feature for wearable applications.

1.2.1. LCD controller

- Supports simultaneous connection to two serial LCD modules.
- Supports DBI serial interface.
- Supports MIPI DSI interface.
- Supported LCM formats — RGB565, RGB666, RGB888.
- Supports LCD module with maximum resolution of 320 x 320 pixels.
- Per pixel alpha channel.
- True color engine.
- Supports hardware display rotation.
- Capable of combining display memories with up to four blending layers.

1.2.2. MIPI DSI interface (MT2523S not support MIPI DSI interface)

- Single clock and single data lane.
- Maximum resolution of 480 x 320 pixels.
- Throughput of up to 100 Mbps.
- Bidirectional data transmission in low-power mode.
- Uni-directional data transmission in high-speed mode.

- 128-entry command queue for command transmission.
- Supports three types of video modes — sync-event, sync-pulse and burst mode.
- Supports non-continuous high-speed transmission in data lanes.
- Supports command mode frame transmission-free run.
- Supports peripheral tearing effect (TE) and external TE signal detection.
- Low power mode control.
- Low frame-rate (LFR) technique.

1.2.3. 2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565 and 24-bpp ARGB6666.
- Four layers of overlay with individual color format, window size, source key, constant alpha and rotation.
- Rectangle fill with constant.
- Bit-boundary block transfer (BitBlt). Supports up to seven rotation types.
- Alpha blending with seven rotation types, per-pixel alpha and pre-multiplied alpha.
- Font drawing. Normal font and anti-aliasing font (Display Adaptive Ambient Light Controller).

1.2.4. Display adaptive ambient light controller

- 33-bin weighted histogram.
- DRE enhancement for sunlight visibility.
- CABC compensation for backlight power saving.

1.3. Audio

Using a highly integrated mixed-signal audio front-end, the MT2523 series architecture enables audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice bands.

1.3.1. Audio CODEC

- Supports AAC and SBC codecs for Bluetooth audio.
- Supports CVSD and mSBC codecs for Bluetooth speech.
- Pure PCM playback for 8-48kHz sample rate.
- Pure PCM record for 8kHz and 16kHz sample rates.

1.3.2. Audio interface and audio front-end

- Pure PCM record for 8kHz and 16kHz sample rates.
- Supports master I2S interface.
- Supports master PCM interface.
- Supports dual PDM microphone.

- High-resolution D/A converters for stereo audio playback.
- Voice band A/D converter support.
- Stereo to mono conversion.

1.4. Bluetooth

MT2523 series offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components is required.

MT2523 series is fully compliant with Bluetooth version 4.2, upgradable to later versions, including BR/EDR and Bluetooth LE and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with IEEE 802.11 protocol.

1.4.1. Radio

- Fully compliant with Bluetooth core specification 4.2.
- Low-IF architecture with high degree of linearity and high order channel filter.
- Integrated T/R switch and balun.
- Fully integrated PA provides 7.5dBm output power.
- -95dBm sensitivity with interference rejection performance.
- Hardware AGC dynamically adjusts receiver performance in changing environments.

1.4.2. Baseband

- Up to seven simultaneous active ACL links.
- Up to eight simultaneous active Bluetooth LE links.
- A single SCO or eSCO link with CVSD/mSBC coding.
- Up to two simultaneous ACL slave links and four simultaneous Bluetooth LE links for audio or voice application, basic rate A2DP.
- AFH and PTA collaborative support for WLAN/Bluetooth coexistence.
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission.
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption.
- Channel quality driven data rate adaptation.
- Channel assessment for AFH.

1.4.3. Core

- Feasibility Bluetooth host subsystem in Cortex-M4 MCU to support customized applications.
- Embedded processor for Bluetooth controller subsystem with built-in memory system.
- Fully verified ROM based system with code patch for feature enhancement.

1.5. Debugging

The JTAG interface enables in-circuit debugging of the software program with the CPU. With this standardized debugging interface, the MT2523 chipset provides a wide selection of ARM development kits from different third-party vendors.

1.6. Power management

The power management is embedded in MT2523 series, including Li-ion battery charger, high performance and low quiescent current LDOs and drivers for LED and backlight.
MT2523 series offers various low-power features to help reduce system power consumption. The chipset is fabricated in an advanced low-power CMOS process to provide an overall ultra-low leakage current consumption.

1.7. Package

- MT2523G is offered in a 9.2mm × 6mm, 246-ball, 0.4mm pitch, TFBGA package.
- MT2523D is offered in a 6.2mm × 5.8mm, 165-ball, 0.4mm pitch, TFBGA package.
- MT2523S is offered in a 6.2mm × 5.8mm, 165-ball, 0.4mm pitch, TFBGA package.

2. Functional Overview

2.1. Host Processor Subsystem

2.1.1. ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has reduced pin count and low power consumption and delivers very high performance efficiency and low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint and trace capabilities.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.

MT2523 series has further enhanced the Cortex-M4 with floating point processor to reduce the power by another 11% (in Dhrystone) compared to the original Cortex-M4. Low power consumption is a significant feature for IoT and Wearables application development.

2.1.2. Cache controller

A configurable 32kB cache is implemented to improve the code fetch performance when the CPU accesses a non-zero wait-state memory such as EMI, external flash or boot ROM through the on-chip bus.

The core cache is a small block of memory containing a copy of small portion of cacheable data in the external memory. If the CPU reads a cacheable datum, the datum will be copied to the core cache. Once the CPU requests the same datum again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory to achieve zero wait-state latency.

The cache can be disabled and this block of memory can be turned into tightly coupled memory (TCM), a high-speed memory for normal data storage. The sizes of TCM and cache can be set to one of the following four configurations:

- 32kB cache, 128kB TCM
- 16kB cache, 144kB TCM
- 8kB cache, 152kB TCM
- 0kB cache, 160kB TCM

2.1.3. Memory management

Three types of memories are implemented for use:

1) On-die memories (SRAMs) up to 160kB at CPU clock speed with zero wait state.

2) Embedded flash to store programs and data.

3) Embedded pseudo SRAM (PSRAM) for application storage.

160kB SRAMs are composed of TCMs and L1 caches. L1 cache (up to 32kB) is implemented to improve processor access performance of the long latency memories (flash and PSRAM).

TCMs are designed for high-speed, low latency and low power demanding applications. Each TCM has its own power state; active, retention or power-down. TCM must be in active state for normal read and write access. Retention state saves the SRAM content and consumes the minimum leakage current with no access. Power-down loses the content and consumes almost zero power.

Other internal AHB masters including DMA or multimedia sub-system for low power applications can also access the TCMs. These applications can run on TCM without powering on PSRAM or Flash to save more power.

Boot ROM is also implemented for processor boot–up and its content is unchangeable.

2.1.4. Memory Protection Unit

The Memory Protection Unit (MPU) is an optional component to manage the CPU access to memory. The MPU provides full support for:

- Protection regions (up to 8 regions and can be further divided up into 8 sub-regions).
- Overlapping protection regions, with region priority.
- Access permissions.
- Exporting memory attributes to the system.

The MPU is useful for applications where a critical code has to be protected against the misbehavior of other tasks. It can be used to define access rules, enforce privilege rules and separate processes.

2.1.5. Nested Vectored Interrupt Controller

The Nested Vectored Interrupt Controller (NVIC) supports up to 64 maskable interrupts and 16 interrupt lines of Cortex-M4 MCU with 64 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

2.1.6. External Interrupt Controller

The external interrupt or event controller (EINT) consists of 32 edge/level detector lines used to generate interrupt or event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both and level) and can be masked independently. A pending register maintains the status of the interrupt requests. Up to 31 GPIOs can be connected to 20 external interrupt lines.

2.1.7. Bus architecture

To better support various IoT applications, MT2523 series adopts 32-bit multi-AHB matrix to provide low-power, fast and flexible data operation. Table 2.1-1 shows the interconnections between bus masters and slaves.

- The bus masters include the Cortex-M4 MCU, four SPI masters, SPI slave, Debug system, Multimedia (MM) system, USB and three DMAs.
- The bus slaves include the Always On (AO) domain APB peripherals, Power Down (PD) domain APB peripherals, TCM, SFC, EMI, MDSYS and BTSYS.

Table 2.1-1. MT2523 series bus connection

Master / Slave	ARM Cortex-M4	AO DMA	PD DMA	Sensor DMA	USB	MM SYS	Debug SYS	SPI Master	SPI Slave
AO APB Peripherals	●	●							
PD APB Peripherals	●		●	●				●	●
TCM	●	●	●	●		●		●	●
EMI	●	●	●	●	●	●	●	●	●
SFC	●	●	●	●				●	●
Audio DSP	●		●	●				●	●
BTSYS	●		●	●				●	●

2.1.8. Direct Memory Access Controller

MT2523 series chipset features three Direct Memory Access Controller (DMA) controllers, containing total of 18 channels in power-down and always-on power domains, respectively. They manage data transfer between the peripheral devices and memory.

There are three types of DMA channels in the DMA controller − full-size DMA channel, half-size DMA channel and virtual FIFO DMA for different peripheral devices. DMA controllers support ring-buffer and double-buffer memory data transactions.

To improve bus efficiency, the DMA controllers provide an unaligned-word access function. When this function is enabled, it can automatically convert the address format from the unaligned type to aligned type, ensuring compliance with the AHB/APB protocol.

Each peripheral device is connected to a dedicated DMA channel that can configure transfer data sizes, source address and destination address by software. The DMA controllers can be used with the following peripherals:

- Two MSDCs
- Two I2C interfaces
- Four UART interfaces
- A single BTIF

2.2. Boot mode

While the chip is starting up, the on-chip boot ROM is executed to determine the next booting sequence, either flash download mode or normal boot mode.

- Flash download mode. The bootloader is located in the embedded flash and can be reprogrammed through UART or USB interface. For USB, there are two methods to trigger the download flow – USB auto-detection by USB plug-in or pulling the pin GPIO_B2 to low.
- Normal boot up mode. In this mode, boot ROM copies the bootloader from embedded flash to the internal memory, without entering flash download mode. When the system finishes boot ROM execution, it will jump to bootloader and execute it.

2.3. Clock source architecture

The clock controller (see Figure 2-1) distributes the clocks from different oscillators to the core circuit and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. The clock controller features:

- **Clock prescaler** — provides the best trade-off between speed and current consumption. The clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching** — clock sources can be adjusted during runtime through a configuration register.
- **Clock management** — reduces the power consumption, the clock controller can stop the clock of the core circuit, individual peripherals or memory. The AHB and APB clocks support dynamic clock slow down or gating when bus fabric is idle.
- **System clock source** — four different clock sources can be used to drive the master clock (F_{CPU} and F_{MEMS}):
  - 26MHz Digitally Controlled Crystal Oscillator (DCXO) that can supply reference clock for PLLs.
  - Main PLL (MPLL) fed by reference clock from UPLL that in turn is fed by DCXO, with a maximum frequency at 624MHz.
  - Low Frequency RC oscillator (LFOSC) — low power consumption with large frequency variation.
  - High Frequency RC oscillator (HFOSC) — low power consumption with large frequency variation.
- **Auxiliary clock source** — Three low power clock sources to drive the real-time clock. In 32k-less mode, DCXO32K and EOSC32K are used, while in 32k mode only XOSC32K is used:
  - 32.768kHz low-speed external crystal (XOSC32K).
  - 32.768kHz low-speed internal clock fed by DCXO (DCXO32K).
  - 32kHz low-speed internal RC (EOSC32K) with larger frequency variation compared to DCXO and XOSC.
- **Peripheral clock sources** — Three types of peripheral clock source options are used. Each peripheral has its own gating register:
  - Peripherals, such as USB, CAM, MSDC, UARTs, DSP, LCD and SFC have their own independent clock sources based on the system clock. HFOSC and MPLL, each having independent outputs enabling high flexibility, can generate independent clocks for MSDC, DSP, LCD and SFC. UPLL can generate independent clocks for USB and CAM.
  - The clock source of peripherals, including I2C_D2D, I2C2, DMA, DMA_AO, SPISLV and BTIF is the same as AHB2/APB2 bus clock (F_{PERI}).
  - The clock source of multi-media related peripherals, including G2D, CAMINF, RESIZER, ROTDMA, PAD2CAM and DSI is the same as AHB1/APB1 bus clock (F_{MEMS}).

- The clock source of low-speed peripherals, including I2C0, I2C1, SPI, SENSOR_DMA, AUXADC and EFUSE is from general 26MHz MUX.

- **Clock-out capability.**
  - FREF. Outputs 26MHz DCXO clock by control GPIO45.
  - CLK0UT. Outputs 32kHz clock based on 32k or 32k-less mode.

26MHz DCXO is selected as a default CPU clock when powering up or resetting the chip. This clock source serves as an input to a set of cascaded PLLs (UPLL and MPLL) to increase the CPU frequency (FCPU) up to 208MHz when VCORE is 1.3V. The application can then select the system clock as either Low Frequency RC oscillator (LFOSC) or High Frequency RC oscillator (HFOSC) to decrease power consumption while frequency variation is acceptable. LFOSC can provide maximum of 26MHz clock while HFSOC can provide maximum of 312MHz clock. The CPU can switch to HFOSC 104MHz as DVFS option while working at VCORE 1.1V. Several prescalers allow the configuration of the memory domain AHB buses. The maximum frequency of the AHB1 and APB1 buses (FMEMS) is 104MHz. The maximum frequency of peripheral AHB2 and high-speed APB2 buses (FPERI) is 62.4MHz, while the maximum frequency of the low-speed APB3 domains is 26MHz. The frequency ratio of FCPU and FMEMS needs to be 2:1. When VCORE is 0.9V, the maximum frequency of the FCPU is 26MHz, FMEMS and FPERI are at 13MHz. The device has dedicated BTPLL and MIPIPLL to operate Bluetooth and MIPI.

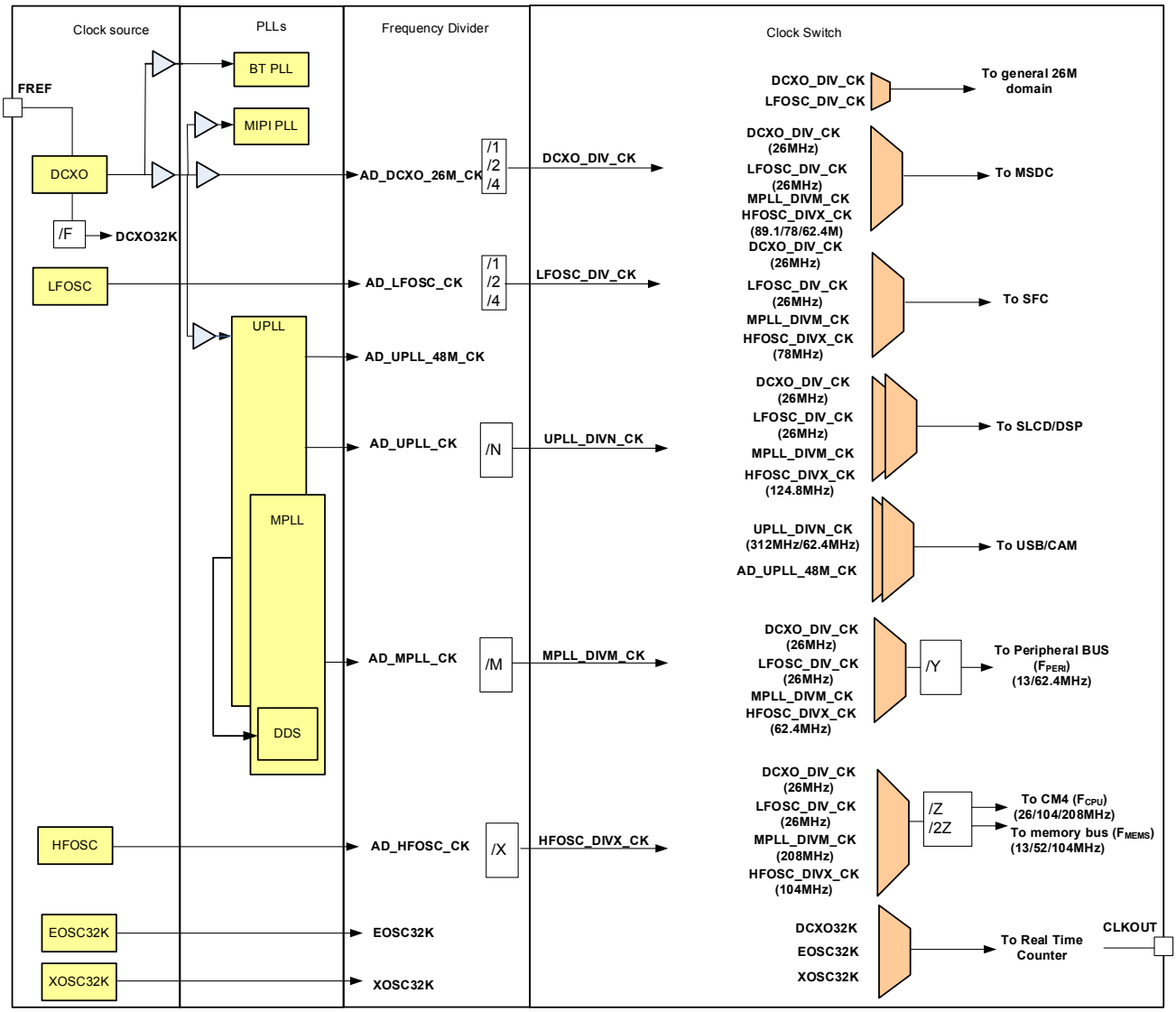


Figure 2-1. MT2523 series clock source architecture

2.4. Communication Interface

2.4.1. Universal Asynchronous Receiver Transmitter

MT2523 series chipset houses four Universal Asynchronous Receiver Transmitters (UARTs). UARTs provide full duplex serial communication channel between the baseband chipset and external devices. UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rates from 110bps up to 921,600bps and baud rate auto-detection function. They provide hardware and software flow control of the RTS/CTS signals.

UARTs can configure data transfer lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits by software. They can be served by the DMA controller.

2.4.2. Serial Peripheral Interface

MT2523 series chipset features four Serial Peripheral Interface (SPI) master controllers and one SPI slave controller to receive/transmit device data using SPI protocol. The SPI controllers can communicate at up to 13 Mbps. SPI master controllers support two chip select outputs to connect the controller to two devices simultaneously.

The chip select signal and SPI clock of SPI master controllers are configurable. The SPI controllers also support DMA mode for large number of data transmission.

2.4.3. Inter-Integrated Circuit Interface

MT2523 series chipset provides three Inter-Integrated Circuit Interface (I2C) master controllers. There are three types of speed modes in the I2C controllers: standard mode (100k bit/s), fast mode (400k bit/s) and high-speed mode (3.4M bit/s), supporting 7-bit/10-bit addressing and can be served by the DMA controller. The I2C package size supports up to 65,535 bytes per transfer and 255 transfers per transaction in DMA mode, and 8 bytes per transfer in non-DMA mode. START/STOP/REPEATED START condition can be increased to support single or multi transfer. These features can be configured by software upon our customers' requirements.

2.4.4. SD memory card controller

The controller fully supports the SD memory card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0.

Furthermore, the controller also partially supports the SDIO card specification version 2.0. However, the controller can only be configured as the host of the SD memory card. Hereafter, the controller is abbreviated as the SD controller.

Main features of the controller:

- 16 or 32-bit access for control registers.
- Built-in CRC circuit.
- CRC generation can be disabled.
- Supports DMA.
- Data rate of up to 48 Mbps in serial mode, 48 x 4Mbps in parallel model. The module is targeted at 48MHz operating clock.
- The serial clock rate on SD bus is programmable.
- Card detection capability in sleep mode.

- Power control for memory card.

2.4.5. USB2.0 high-speed device controller

USB2.0 controller supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) modes. USB2.0 controller provides two endpoints to receive packets and four endpoints to send packets. These endpoints can be individually configured in the software to handle either bulk transfers, interrupt transfers or isochronous transfers. There are four DMA channels, and the embedded RAM size is configurable up to 3,264 bytes. The embedded RAM can be dynamically configured for each endpoint. For more details, see Table 2.4-1.

Table 2.4-1. USB2.0 features

Feature	Description
Speed	HS (480MHz), FS (12MHz), LS (1.5MHz)
Enhanced feature	Generic device
Endpoint	4TX/2RX
DMA channel	4
Embedded RAM	3264 bytes

2.5. Peripherals

2.5.1. Pulse-Width Modulation

There are six Pulse-Width Modulation (PWM) controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers can be configured to use either 13MHz or 32.768kHz clock source to support a wide range of output pulse frequencies.

2.5.2. General Purpose Inputs/Outputs

Each of the General Purpose Inputs/Outputs (GPIO) pins are software configurable as output (push-pull or open-drain) or as input (with or without pull-up or pull-down) that supports input floating with buffer gating to reduce power consumption. Most of the GPIO pins are multiplexed with peripheral functions and have selectable output driving strength. Fast I/O signal transmission allows maximum I/O toggling speed of up to 100MHz. Besides, IO toggling is allowed even when the chip operates in deep sleep mode voltage (0.7V).

2.5.3. Keypad scanner

MT2523 series platform provides a keypad hardware module. The keypad supports two types of keypads: 3 x 3 single keys and 3 x 3 configurable double keys.

The 3 x 3 keypad supports a matrix with 3*3*2 = 18 keys. The 18 keys are divided into 9 subgroups, and each group consists of two keys and a 20Ω resistor. The keypad de-bounce time can be configured for your operation.

2.5.4. General Purpose Timer

The general purpose timer (GPT) includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes — ONE-SHOT, REPEAT, KEEP-GO and FREERUN, and can operate on one of the two clock sources; RTC clock (32.768kHz) and system clock (13MHz).

2.5.5. Real Time Clock

The Real Time Clock (RTC) module provides time and data information, as well as 32.768kHz clock. The clock source is selected between three clock sources: one from the external (XOSC32) and two from the internal (DCXO, EOSC32). If the clock source is internal, the clock source can be configured in software or hardware selection mode. The hardware selection mode automatically switches between the two embedded clock sources at different VBAT levels. The RTC block has an independent power supply. When the MT2523 series platform is powered off, a dedicated regulator will supply power to the RTC block. In addition to providing timing data, an alarm interrupt will be generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum value. The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

2.5.6. True Random Number Generator

The True Random Number Generator (TRNG) is a device in power-down domain that generates random numbers based on the ring oscillator output that is sensitive to the PVT (process, voltage and temperature) variation. The utilized ring oscillator includes Hybrid Fibonacci Ring Oscillator (H-FIRO), Hybrid Ring Oscillator (H-RO) and Hybrid Galois Ring Oscillator (H-GARO). Von Neumann extractor is used to balance the 0/1 probability of the generated random numbers. Error detection detects if the generation time exceeds the timeout limit while enabling the Von Neumann extractor. IRQ is issued when random number is successfully generated or timeout error occurred.

2.5.7. General Purpose Counter

The general purpose counter (GPC) is to count the signal toggle times of chip I/O, and calculate the frequency and duration. It counts once the channel is enabled and provides an interrupt switch trigger when the counter exceeds the threshold. The threshold can be configured by software.

2.5.8. Accessory detector

The accessory detector (ACCDET) detects the plug-in and plug-out of multiple types of external components. This design supports two types of external components, microphone and hook-switch. It uses an internal 2-bit comparator to separate external components. The de-bounce scheme is also supported to resist uncertain input noises.

2.6. Analog baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the data transfer to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete analog baseband signal processing:

1) General purpose DAC. A DAC for general purpose voltage waveform generation. The output may be used as stimulus for external devices.

2) Auxiliary ADC. Provides an ADC for battery and other auxiliary analog function monitoring.

3) Audio mixed-signal block. Provides complete analog voice signal processing, including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.

4) Clock generation. Includes a clock squarer for shaping the system clock and PLL to provide clock signals to MCU and USB.

5) XOSC32. A 32kHz crystal oscillator circuit for RTC applications on analog blocks.

6) LPOSC. Provides 26MHz and 312MHz system clock for low power applications.

2.6.1. General Purpose DAC

2.6.1.1. Block description

General purpose DAC (GPDAC) is a 10-bit DAC with output buffer aiming at automatic power control. Analog pin assignment and functional specifications are shown in Table 2.6-1. It is an event-driven scheme for power saving purposes.

2.6.1.2. Functional specifications

The functional specifications of the general purpose DAC are listed in Table 2.6-1.

Table 2.6-1. GPDAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution	-	10	-	Bit
FS	Sampling rate	-	-	1.0833	MSPS
SINAD	• Signal to noise and distortion ratio (10-kHz sine with 1.0V swing & 100-kHz BW)	47	-	-	dB
	• 99% settling time (full swing on maximal capacitance)	-	-	5	µs
	• Output swing	0	-	2.8	V
	• Output capacitance	-	200	2200	pF
	• Output resistance	0.47	10	-	kΩ
DNL	Differential nonlinearity for code 20 to 970	-	± 1	-	LSB
INL	Integral nonlinearity for code 20 to 970	-	± 1	-	LSB
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	• Current consumption ○ Power-up ○ Power-down	 - -	 400 1	 - -	 µA µA

2.6.2. Auxiliary ADC

2.6.2.1. Block description

The auxiliary ADC includes the following functional blocks:

1) Analog multiplexer. Selects signal from one of the seven auxiliary input pins. Real-world messages are monitored, such as temperature, and transferred to the voltage domain.

2) 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

Table 2.6-2. Auxiliary ADC input channel

Channel	Application	Input range [V]
11~15	GPIO	0 to 2.8V
others	Internal use	N/A

2.6.2.2. Functional specifications

The functional specifications of the auxiliary ADC are listed in Table 2.6-3.

Table 2.6-3. Auxiliary ADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution	-	12	-	Bit
FC	Clock rate	-	1.08	-	MHz
FS	Sampling rate at N-Bit	-	1.08/(N+1)	-	MSPS
	Input swing	0	-	2.8	V
CIN	• Input capacitance ○ Unselected channel ○ Selected channel	 - -	 - -	 50 4	 fF pF
RIN	• Input resistance ○ Unselected channel ○ Selected channel	 400 1	 - -	 - -	 MΩ MΩ
	Clock latency	-	N+1	-	1/FC
DNL	Differential nonlinearity	-	± 1	-	LSB
INL	Integral nonlinearity	-	± 1	-	LSB
OE	Offset error	-	± 10	-	mV
FSE	Full swing error	-	± 10	-	mV
SINAD	Signal to noise and distortion ratio (10-kHz full swing input & 1.0833-MHz clock rate)	-	65	-	dB
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	• Current consumption ○ Power-up ○ Power-down	 - -	 280 1	 - -	 µA µA

2.6.3. Audio mixed-signal blocks

2.6.3.1. Block description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. It includes three parts, as shown in Figure 2-2.

The first block consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (left channel audio DAC) and voice amplifier that produces voice signals to earphones or other auxiliary output devices. The last part is the voice uplink path — an interface between the microphone or other auxiliary input devices and MT2523 series chipset. A set of bias voltage is provided for the external electric microphone.

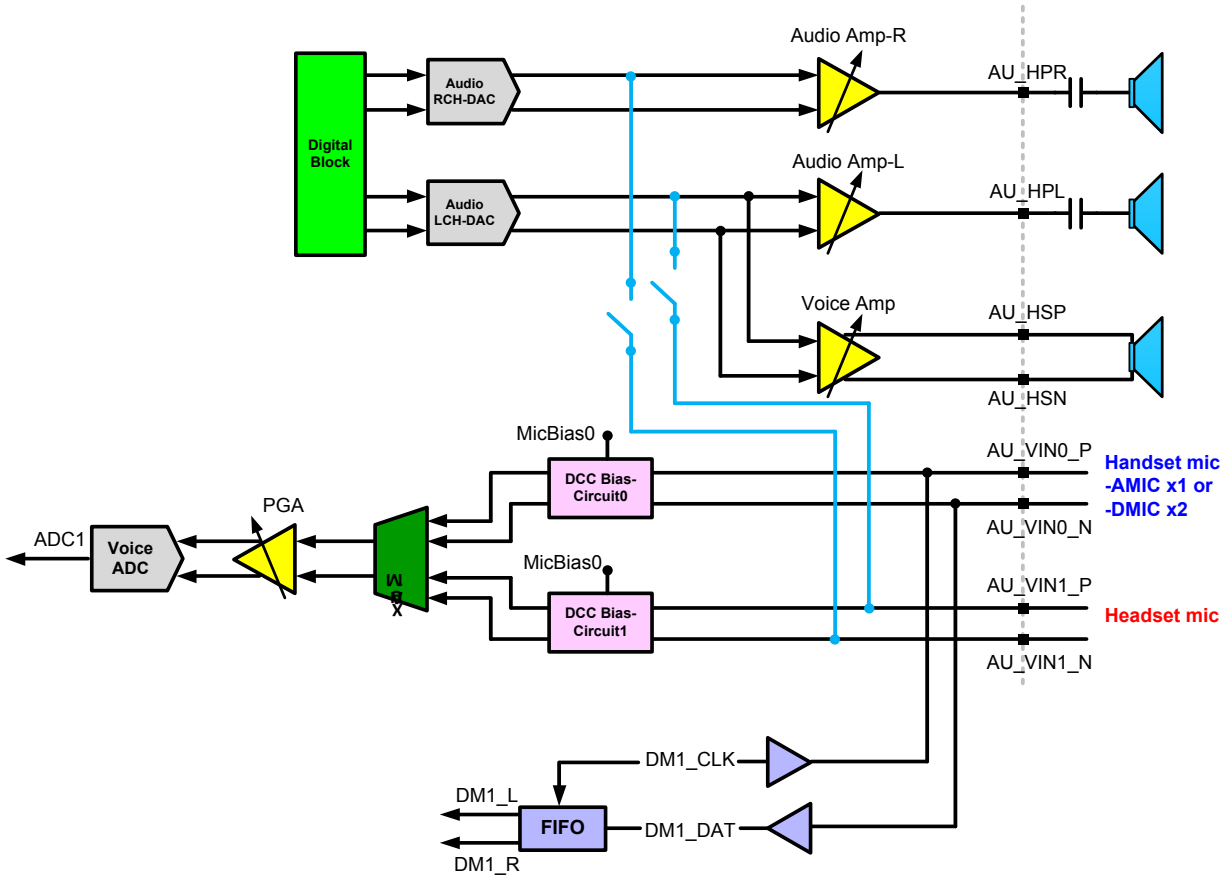


Figure 2-2. Block diagram of audio mixed-signal blocks

2.6.3.2. Functional specifications

See Table 2.6-4 for the functional specifications of voice-band uplink/downlink blocks.

Table 2.6-4. Functional specifications of analog voice blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate	-	6,500	-	kHz
DVDD	Digital power supply	-	1.1	-	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
VMIC	Microphone biasing voltage	-	1.9	2.2	V
IMIC	Current draw from microphone bias pins	-	-	2	mA
Uplink path					
IDC	Current consumption for one channel	-	1.5	-	mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0 Input level: 0 dbm0	 29 -	 - 69	 - -	 dB dB
RIN	Input impedance (differential)	13	20	27	kΩ
ICN	Idle channel noise	-	-	-67	dBm0
Downlink path					
IDC	Current consumption	-	2.2	-	mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	 29 -	 - 69	 - -	 dB dB
RLOAD	Output resistor load (differential)	16	32	-	Ω
CLOAD	Output capacitor load	-	-	250	pF
ICN	Idle channel noise of transmit path	-	-	-64	dBPa
XT	Crosstalk level on transmit path	-	-	-66	dBm0
Digital MIC					
DCLK	DMIC clock frequency	-	3.25/ 1.625	-	MHz
DTY	DMIC clock duty cycle	40	-	60	%
DCRT	DMIC clock rise time (MaxCL = 65p)	-	-	10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)	-	-	10	ns

See Table 2.6-5 for functional specifications of audio blocks.

Table 2.6-5. Functional specifications of analog audio blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency	-	6.5	-	MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
IDC	Current consumption	-	2.2	-	mA

Symbol	Parameter	Min.	Typ.	Max.	Unit
PSNR	Peak signal to noise ratio	-	88	-	dB
DR	Dynamic range	-	88	-	dB
VOUT	Output swing for 0dBFS input level at -1dB headphone gain	-	0.707	-	V_{rms}
$VOUT_{MAX}$	Maximum output swing	-	2.0	-	Vpp
THD	Total harmonic distortion 10mW at 64Ω load	-	-	-70	dB
RLOAD	Output resistor load (single-ended)	64	-	-	Ω
CLOAD	Output capacitor load	-	-	250	pF
XT	L-R channel cross talk	70	-	-	dB

2.6.4. Phase Locked Loop and oscillators

2.6.4.1. Block description

There are two phase-locked loops (PLL) in PLLGP. The UPLL generates 624MHz clock output, and then a frequency divider generates fixed 48MHz clock. The DDS-based MPLL is with target/highest frequency of 624MHz (hopping range is from -8% to 0%, and the frequency is from 574MHz to about 624MHz). These two PLLs do not require off-chip components to operate, and can be turned off to save power. Figure 2-3 shows the block diagram of clock sources.

After powering on, the PLLs are all off by default control register setting, and the source clock signal is selected through multiplexers from 26MHz XTAL. The software maintains the PLL lock time while the clock selection is changing.

There is one high frequency low power oscillator (HFOSC) and one low frequency low power oscillator (LFOSC) in low power oscillator (LPOSC) group. The HFOSC generates 312MHz clock output with from -13% to 0% frequency variation. The LFOSC generates 26MHz clock output with from -8% to 0% variation. The software calibrates two LFOSC by frequency meter before using them.

Note that PLLs and LPOSC need some time to stabilize after powering on. The software maintains the PLL and LPOSC lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL and LPOSC lock time is employed when the PLL lock time is too long.

For power management, the MCU software configuration may stop MCU Clock by setting up the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode and return the MCU to the running mode.

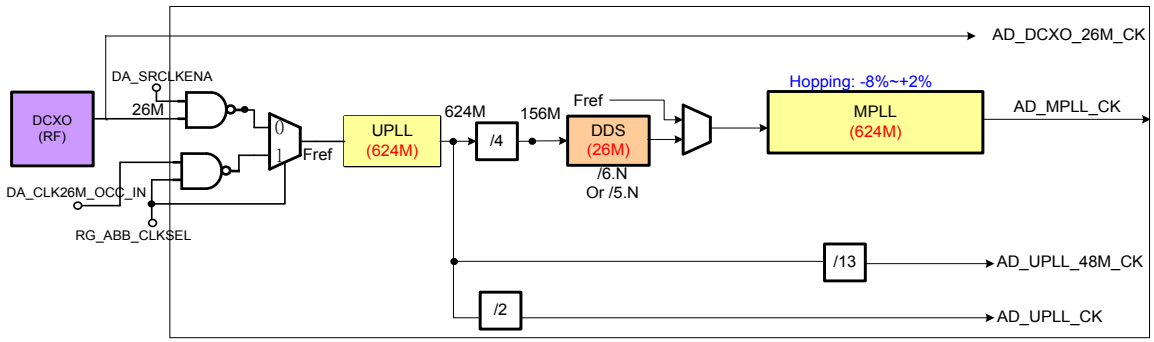


Figure 2-3. Block diagram of PLL clock sources

2.6.4.2. Function specifications

The function specifications of PLLs and oscillators are shown in Table 2.6-6, Table 2.6-7, Table 2.6-8, Table 2.6-9 and Table 2.6-10.

Table 2.6-6. MPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	26	-	MHz
Fout	Output clock frequency	420	624	740	MHz
	Settling time	-	20	-	µs
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)	-	30	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	1.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-7. UPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	26	-	MHz
Fout	Output clock frequency	420	624	740	MHz
	Settling time	-	20	-	µs
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)	-	30	-	ps
DVDD	Digital power supply	-	1.1	-	V

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-42	-	85	°C
	Current consumption	-	1.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-8. DDS specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	156	-	MHz
Fout	Output clock frequency	-	26	-	MHz
	Settling time	-	20	-	µs
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)	-	60	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-42	-	85	°C
	Current consumption	-	0.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-9. HFOSC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	272	287	312	MHz
	Settling time		3.5		µs
	Output clock duty cycle	40	50	60	%
	Output clock jitter (period jitter)		150		ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	0.1	-	mA
	Power-down current consumption	-	-	5	µA

Table 2.6-10. LFOSC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency (after calibration)	24	25	26	MHz
	Settling time	-	3.5	-	µs
	Output clock duty cycle	40	50	60	%
	Output clock jitter (period pk-topk jitter)	-	250	-	ps

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	0.05	-	mA
	Power-down current consumption	-	-	5	µA

2.7. Audio front-end

The audio front-end essentially consists of voice and audio data paths. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset. Figure 2-4 shows the block diagram of the audio front-end digital circuits. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port (DAP) block interfaces with the DSP for control and data communication. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the system simulator for FTA or external Bluetooth or codec modules.

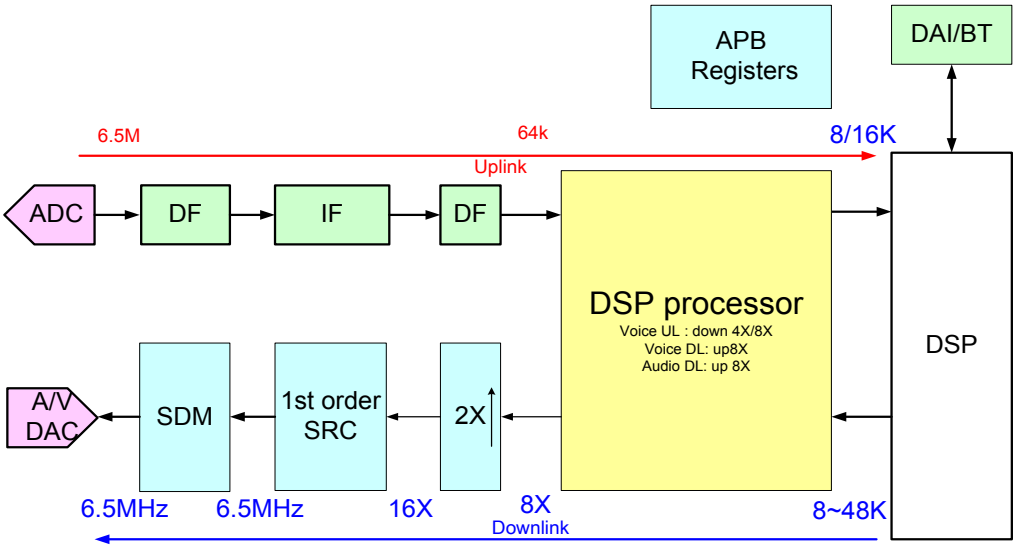


Figure 2-4. Digital circuits of the audio front-end

To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interface are supported. The clock of PCM interface is 256kHz while the frame synchronization is at 8kHz. Both long synchronization and short synchronization interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8kHz sampling rate voice signal. Figure 2-5 shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is on rising edge and data is latched when the clock is on falling edge. Figure 2-6 shows the timing diagram of PCM interface for different clock rates. The clock rate could be configured to 1, 2, 4 or 8 times of the original clock rate.

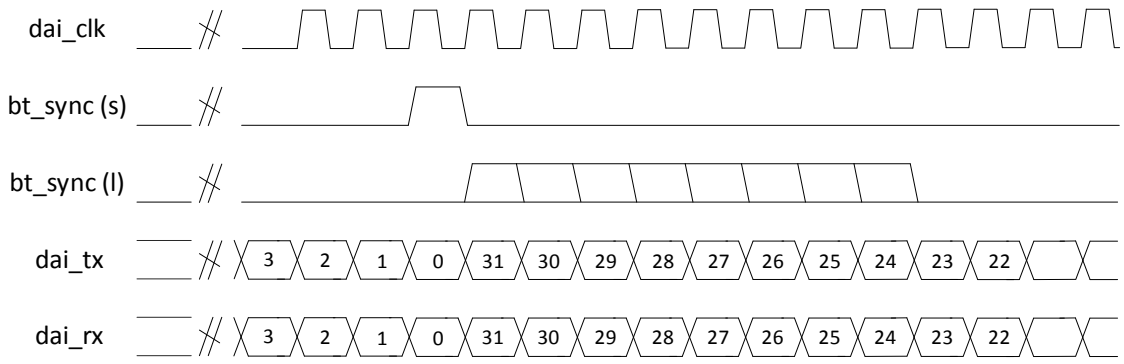


Figure 2-5. Timing diagram of Bluetooth application

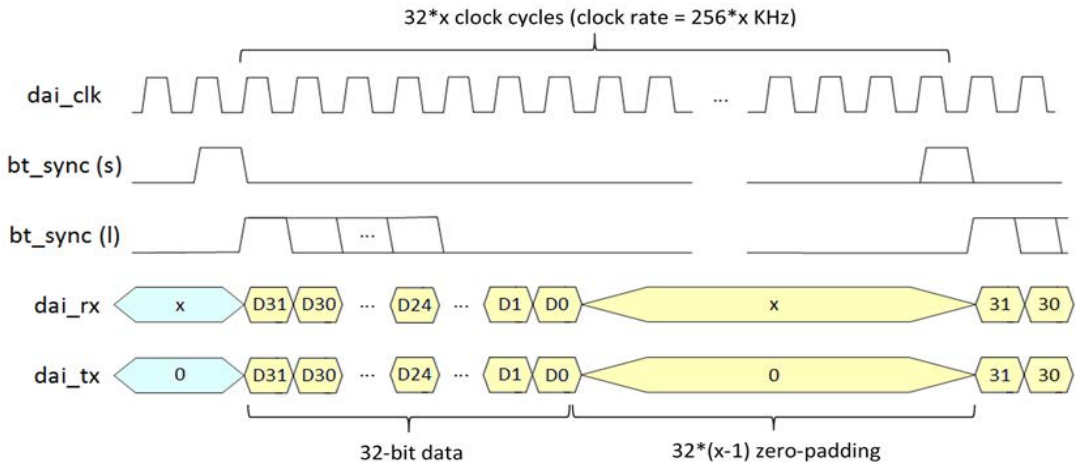


Figure 2-6. Timing diagram of different clock rate Bluetooth applications

I2S/EIAJ interface is designed to transmit high quality audio data. Figure 2-7 and Figure 2-8 illustrate the timing diagram of the two types of interfaces. I2S/EIAJ supports audio signals with 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz sampling rates. The clock frequency of I2S/EIAJ can be 32 × (sampling frequency), or 64 × (sampling frequency). For example, to transmit 44.1kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112MHz or 64 × 44.1 kHz = 2.8224MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. The audio data can be sent to the external DAC through the I2S/EIAJ interface.

In this document, the I2S/EIAJ interface is referred to as External DAC Interface (EDI).

Table 2.7-1 shows the DAI and EDI clock jitter percentage. There has an almost fixed jitter period of DAI/EDI clock, because of hardware saving power implementation. Therefore, the jitter percentage will increase by increasing the audio sampling rate (means decreasing the clock period).

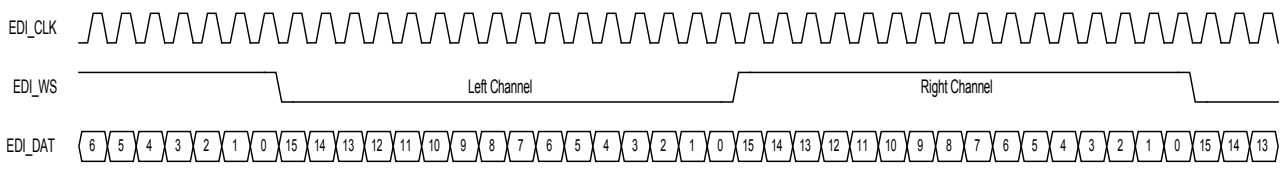


Figure 2-7. EDI Format 1: EIAJ (FMT = 0)

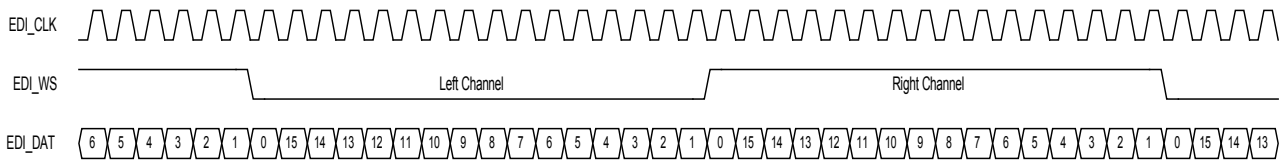


Figure 2-8. EDI Format 1: I2S (FMT = 1)

Table 2.7-1. Clock jitter of DAI and EDI

Clock jitter at 1X clock rate		
Frequency (kHz)	**PCM**	**I2S**
8.000	2.56%	2.56%
11.025	N/A	3.53%
12.000	N/A	3.84%
16.000	N/A	5.12%
22.050	N/A	7.06%
24.000	N/A	7.68%
32.000	N/A	10.24%
44.100	N/A	14.11%
48.000	N/A	15.36%

3. Bluetooth RF Subsystem

3.1. Bluetooth description

The Bluetooth RF subsystem (see Figure 3-1) contains a fully integrated transceiver with on-chip RF bandpass filter (BPF).

For transmitter (TX) path, the baseband data are digitally modulated in the baseband processor and then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 5dBm power for enhanced data rate (EDR) and 8dBm for basic data rate (BDR).

MT2523 Bluetooth module has low intermediate frequency (IF) receiver architecture. RF signal is amplified by LNA and down-converted to IF by mixer. LO is provided by synthesizer, which supports 26MHz reference clock. The mixer output is filtered by complex BPF and then converted to digital signal by ADC. A fast automatic gain control (AGC) enables effective discovery of devices within dynamic range of the receiver.

BBPLL generates sampling clock for ADC and DAC.

MT2523 Bluetooth module features self-calibration schemes to compensate the variation of process and temperature to maintain high performance. Those calibrations are performed automatically right after system boot-up.

Note, the specification value is valid at room temperature (25°C).

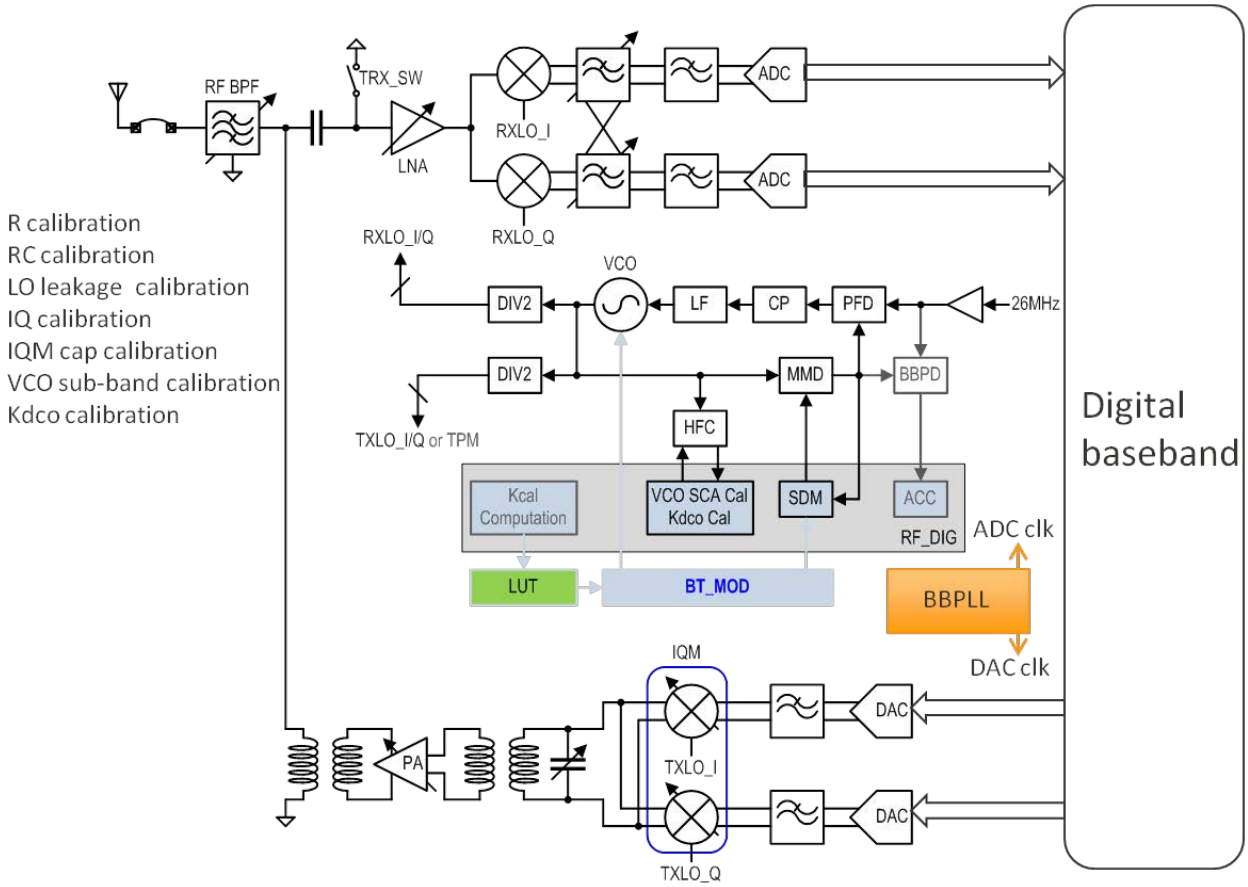


Figure 3-1. Bluetooth RF transceiver system

3.2. Functional specifications

3.2.1. Basic Data Rate – receiver specifications

Table 3.2-1. Basic Data Rate – receiver specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	BER < 0.1% (DH5)	-	-93	-70	dBm
Max. detectable input power	BER < 0.1%	-20	-5	-	dBm
C/I co-channel selectivity	BER < 0.1%	-	6	11	dB
C/I 1 MHz adj. channel selectivity	BER < 0.1%	-	-7	0	dB
C/I 2 MHz adj. channel selectivity	BER < 0.1%	-	-40	-30	dB
C/I ≥ 3 MHz adj. channel selectivity	BER < 0.1%	-	-43	-40	dB
C/I image channel selectivity	BER < 0.1%	-	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	BER < 0.1%	-	-35	-20	dB
Out-of-band blocking	30 to 2,000 MHz	-10	-4	-	dBm
	2,000 to 2,350 MHz	-27	-14	-	dBm
	2,350 to 2,400 MHz	-27	-18	-	dBm
	2,500 to 2,550 MHz	-27	-18	-	dBm
	2,550 to 3,000 MHz	-27	-14	-	dBm
	3,000 MHz to 12.75 GHz	-10	1	-	dBm
Intermodulation		-39	-30	-	dBm

3.2.2. Basic Data Rate – transmitter specifications

Table 3.2-2. Basic Data Rate – transmitter specification

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Maximum transmit power		-	8	-	dBm
Gain step		2	4	8	dB
Δf1avg (00001111)		140	157	175	kHz
Δf2max (10101010)		115	122	-	kHz
Δf1avg/Δf2avg		0.8	0.9	-	kHz
Initial carrier frequency drift		-75	10	75	kHz
Frequency drift	DH1	-25	15	25	kHz
	DH3	-40	18	40	kHz
	DH5	-40	18	40	kHz

Description	Condition	Min.	Typ.	Max.	Unit
Maximum drift rate		-	9		kHz/µs
BW 20dB of TX output spectrum		-	920	1,000	kHz
In-band spurious emission	±2 MHz offset	-	-38	-20	dBm
	±3 MHz offset	-	-43	-40	dBm
	> ±3 MHz offset	-	-43	-40	dBm
Out-of-band spurious emission	30 MHz to 1 GHz	-	-	-36	dBm
	1 to 12.75 GHz	-	-	-30	dBm
	1.8 to 1.9 GHz	-	-	-47	dBm
	5.15 to 5.3 GHz	-	-	-47	dBm

3.2.3. Enhanced Data Rate – receiver specifications

Table 3.2-3. Enhanced Data Rate –Receiver Specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	π/4 DQPSK, BER < 0.01% (2DH5)	-	-93	-70	dBm
	8PSK, BER < 0.01%	-	-87	-70	dBm
Maximum detectable input power	π/4 DQPSK, BER < 0.01% (3DH5)	-20	-5	-	dBm
	8PSK, BER < 0.01%	-20	-5	-	dBm
C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	-	9	13	dB
	8PSK, BER < 0.01%	-	16	21	dB
C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-12	0	dB
	8PSK, BER < 0.01%	-	-6	5	dB
C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-40	-30	dB
	8PSK, BER < 0.01%	-	-36	-25	dB
C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-43	-40	dB
	8PSK, BER < 0.01%	-	-40	-33	dB
C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	-20	-7	dB
	8PSK, BER < 0.01%	-	-15	0	dB
C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-40	-20	dB
	8PSK, BER < 0.01%	-	-30	-13	dB

3.2.4. Enhanced Data Rate – transmitter specifications

Table 3.2-4. Enhanced Data Rate – transmitter specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Max. transmit power	π/4 DQPSK	-	5	-	dBm
	8PSK	-	5	-	dBm
Relative transmit power	π/4 DQPSK	-4	-1.5	1	dB
	8PSK	-4	-1.5	1	dB
Freq. stability ω0	π/4 DQPSK	-10	4	10	kHz
	8PSK	-10	4	10	kHz
Freq. stability ω1	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
| ω0+ω1|	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
RMS DEVM	π/4 DQPSK	-	8	20	%
	8PSK	-	8	13	%
99% DEVM	π/4 DQPSK	-	12	30	%
	8PSK	-	12	20	%
Peak DEVM	π/4 DQPSK	-	17	35	%
	8PSK	-	17	25	%
In-band spurious emission	π/4 DQPSK, ±1 MHz offset	-	-33	-26	dBm
	8PSK, ±1 MHz offset	-	-33	-26	dBm
	π/4 DQPSK, ±2 MHz offset	-	-30	-20	dBm
	8PSK, ±2 MHz offset	-	-30	-20	dBm
	π/4 DQPSK, ±3 MHz offset	-	-43	-40	dBm
	8PSK, ±3 MHz offset	-	-43	-40	dBm

Note: To meet the specifications, use a front-end bandpass filter.

3.2.5. Bluetooth LE – receiver specifications

Table 3.2-5. Bluetooth LE – receiver specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	BER < 30.8%	-	-96.5	-70	dBm
Max. detectable input power	BER < 30.8%	-10	-5	-	dBm
C/I co-channel selectivity	BER < 30.8%	-	6	21	dB
C/I 1 MHz adj. channel selectivity	BER < 30.8%	-	-7	15	dB
C/I 2 MHz adj. channel selectivity	BER < 30.8%	-	-30	-17	dB

Description	Condition	Min.	Typ.	Max.	Unit
C/I ≥ 3 MHz adj. channel selectivity	BER < 30.8%	-	-33	-27	dB
C/I image channel selectivity	BER < 30.8%	-	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	BER < 30.8%	-	-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz	-	-	-30	dBm
	2,001MHz to 2,339MHz	-	-	-35	dBm
	2,501MHz to 3,000MHz	-	-	-35	dBm
	3,001MHz to 12.75GHz	-	-	-30	dBm

3.2.6. Bluetooth LE – transmitter specifications

Table 3.2-6. Bluetooth LE – transmitter specification

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power		-20	0	-	dBm
Modulation characteristic	Δf1avg (00001111)	235	250	265	kHz
	Δf2max (10101010)	185	215	-	kHz
	Δf1avg/Δf2avg	0.8	0.9	-	kHz
Carrier frequency offset and drift	Frequency offset	-150	±5	150	kHz
	Frequency drift	-50	±5	50	kHz
	Maximum drift rate	-20	±3	20	kHz/µs
In-band spurious emission	±2 MHz offset	-	-35	-20	dBm
	±3 MHz offset	-	-40	-30	dBm
	> ±3 MHz offset	-	-40	-30	dBm

4. GNSS

4.1. RF

4.1.1. LNA/Mixer

Upon receiving RF input signal in through either multi-GNSS antenna to internal LNA or external antenna and LNA, the mixer downconverts the amplified signal. The current chip provides two configurations to choose from — high-gain LNA and low-gain LNA. The high-gain LNA is used for low-cost solution without external LNA. The low gain LNA offers high linearity but worse noise figure for external LNA solution. In the application with external LNA, the external LNA gain ranging from 15 to 20 dB is recommended. The down-conversion mixer is single-ended passive mixer with current mode interface between the mixer and multi-mode low pass filter.

4.1.2. VCO/Synthesizer

The frequency synthesizer includes crystal oscillator, VCO, divider, phase frequency detector (PFD), charge pump (CP) and loop filter – all integrated in the MT2523G chip. Once powered on, VCO is auto-calibrated to its required sub-band. The synthesizer adopts fractional-N sigma-delta PLL topology that supports 12.6 to 40MHz reference clock frequencies.

4.1.3. LPF

The current-mode LPF supports multiple modes for different GNSS combinations. The LPF also provides 26dB gain-control range, with approximately 2dB per step.

4.1.4. ADC

The differential IF signal is quantized by a high performance ADC. The sampling clock can be provided from divided clock from LO.

4.2. Digital signal processing

4.2.1. ARM7EJ-S

The ARM7EJ-S processor provides flexibility necessary for building Java-enabled, real-time embedded devices requiring small size, low-power and high performance. It is built on the features and benefits of the established ARM7TDMI core and is delivered in synthesizable form. ARM7EJ-S is supported by a wide variety of development tools and can run at speeds of up to 158MHz.

ARM7EJ-S includes a JTAG interface to provide a standard development and debugging interface. The interface can connect to a variety of off-the-shelf emulators. The emulators provide single-step, trap and access to all the internal registers of MT2523G.

4.2.2. Cache

MT2523G provides cache to speed up program execution and reduce external flash access times. It supports up to 64kbits cache buffer and can be used as internal memory when it is not fully used.

4.2.3. Boot ROM

The embedded boot ROM provides the firmware through the host interface into SRAM. The host interface (UART/SPI/I2C) is decided by strap control.

4.2.4. Real Time Clock

MT2523G provides very low leakage battery backed-up memory, which contains all the necessary multi-GNSS data for quick start-up and a small amount of user configuration parameters. There is a built-in 1.1V LDO for RTC domain and it can be bypassed while an external LDO is applied. The RTC LDO is a voltage regulator having very low quiescent current. The small ceramic capacitor can be used as the output capacitor, and the stable operation region ranges from very light load from about 0 to 3mA. The RTC application circuit is shown in Figure 4-1 and Figure 4-2.

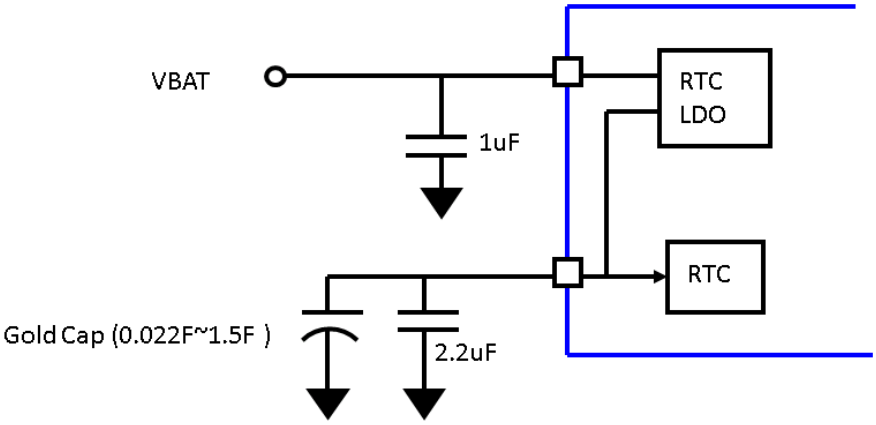


Figure 4-1. RTC with internal RTC LDO application circuit 1

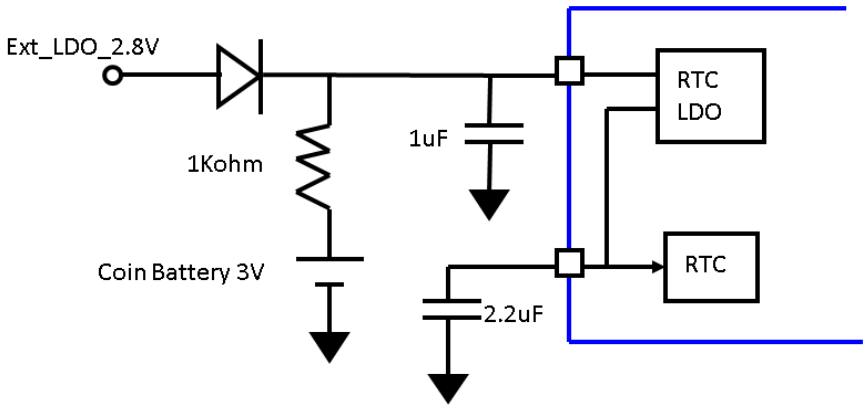


Figure 4-2. RTC with internal RTC LDO application circuit 2

4.2.5. SMPS

A built-in switching mode power supply provides 1.8V power supply for the digital 1.1V CLDO and RF input power. In the active mode, SMPS is operated in the PWM/PFM automatic mode. In the power saving mode, SMPS is operated with reduced switching frequency in the PFM mode. The recommended L/C value is 1µH or 4.7µF.

4.2.6. Timer

The timer function supports a time tick generation of 31.25ms resolution. With the 24-bit counter, the period of timer is from 31.25ms to 524,287s.

4.2.7. GPIO in RTC domain

The "32K_OUT" pin in RTC domain can output 32.768kHz clock to support low clock rate operation mode for applications or peripherals requiring an external clock source. This pin can also be programmed to be an input pin to receive the signal from an external accelerator sensor IC to be the wake-up signal of MT2523G when it is in the low-power mode.

4.2.8. Low power detection

A low power detection circuit is implemented. Whenever the independent power source (AVDD11_RTC) becomes low voltage, the low power detection circuit will detect and reflect this condition and use an indicator signal (output high in normal condition and low in low-power condition).

4.2.9. Clock module

The clock module generates all internal clocks required by processor, correlator, internal memory, bus interface and so on. The referenced input clock is generated from the RF block. For system flexibility and maximum power saving, it supports various power management modes.

4.2.10. Reset controller

The built-in reset controller generates reset signals for all digital blocks. It has power-on reset feature and hardware trapping function. The power-on reset level is 2.7 ± 0.1 V. The software reset function for different circuit blocks are also included for flexible applications.

In Figure 4-3, the voltage drop time T_{drop_vbat} and T_{drop_cldo} depend on the capacitance connection of their power net. But $T_{drop\_vbat} > T_{drop\_cldo}$ should be guaranteed for the correct reset operation during power off. It is strongly recommended to use external LDOs without output discharged function or make sure $T_{drop\_vbat} > 100ms$. The power on/off reset sequence is shown as Figure 4-4.

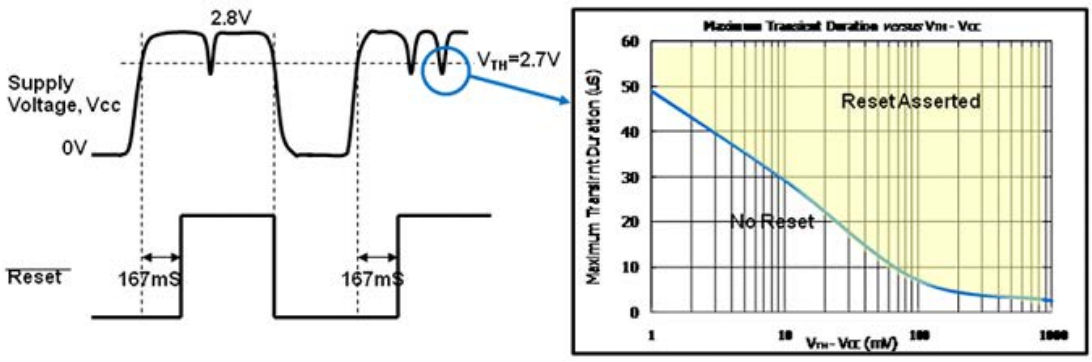


Figure 4-3. Power on reset diagram

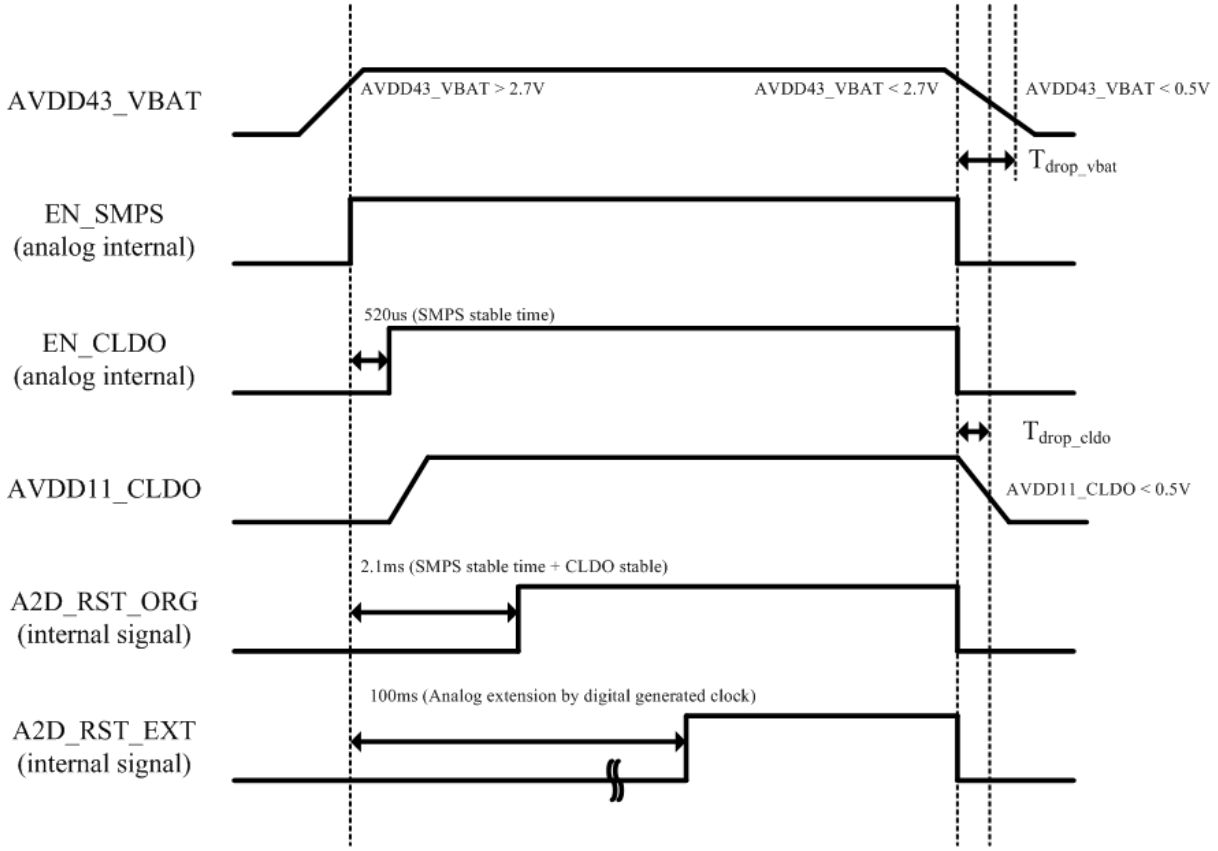


Figure 4-4. Power on/off reset behavior

4.2.11. Host interface

MT2523G supports three different host interfaces − UART, SPI and I2C. The host interface is determined by strap pins. Note, that SPI and I2C interfaces support firmware download only. Only UART could support both firmware download and NMEA output.

4.2.11.1. UART

MT2523G has three full duplex serial ports for serial data communication. UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses.

There are several functions in MT2523G related to UART communication, such as UART data transmit/receive and NMEA sentence input/output. In general, UART0 serves as NMEA output and PMTK command input and UART1 as RTCM input. UART2 port can be adjusted based on the application requirements. The receiver and transmitter side of every port contains a 16-byte FIFO, but only UART0 has 256 bytes of URAM. The bit rates are selectable and range from 4.8 to 921.6 kbps. UART provides signal or message outputs.

4.2.12. Interrupt control unit

The interrupt control unit manages all internal and external sources of interrupts including timer, watchdog, all interfaces such as UART, I2C and SPI and external user interrupt pins. These interrupt sources can be wake-up events in the power saving mode.

4.2.13. Flash

An external SPI serial flash of up to 128Mbits is supported. Specific MediaTek Flash Tool is also supported for downloading firmware into the internal flash.

4.2.14. GPIO

MT2523G supports a variety of peripherals through maximum of 16 GPIO programmable ports. The unit manages all GPIO lines and supports a simple control interface. GPIO provides signal or message outputs.

4.2.15. PPS

The Pulse per Second (PPS) signal is provided through a designated output pin for external applications. The pulse is not only limited to being active every second but also allowed to set up the required duration, frequency and active high/low by programming user-defined settings.

4.2.16. ECLK

ECLK is a clock input pin for introducing an external clock signal to MT2523G and obtaining the relation between the external clock and GNSS local clock. With precise external clock input, the clock drift of the local clock can be correctly estimated. Therefore, the Doppler search range is narrowed down accordingly. The technology is beneficial to speed up the satellite acquisition process. Particularly in the cold start case, due to limited prior information of the satellite's location and local clock uncertainty, a receiver will execute a search in full frequency range. Consequently, a longer acquisition time is expected. However, the ECLK technology is able to reduce the frequency uncertainty so that the search process will be completed in a short time. Efficient acquisition and low power consumption are attained by the ECLK technology.

4.2.17. SYNC

SYNC is a timestamp signal input pin for introducing an external timing to the GNSS receiver and obtaining the relation between the external and local timing of the receiver. With precise external timing input, in particular the GPS time of week (TOW), can be correctly estimated in the receiver. The technology is beneficial for time to first fix (TTFF), particularly in weak signal environments. In hot start, with prior information of the receiver's location and satellite ephemeris data, the receiver uses the correct GPS TOW to predict the signal code chip/phase accurately. Therefore, the code search range can be narrowed down accordingly. Hence, fast TTFF is achieved by the SYNC technology. The SYNC flow is shown in Figure 4-5.

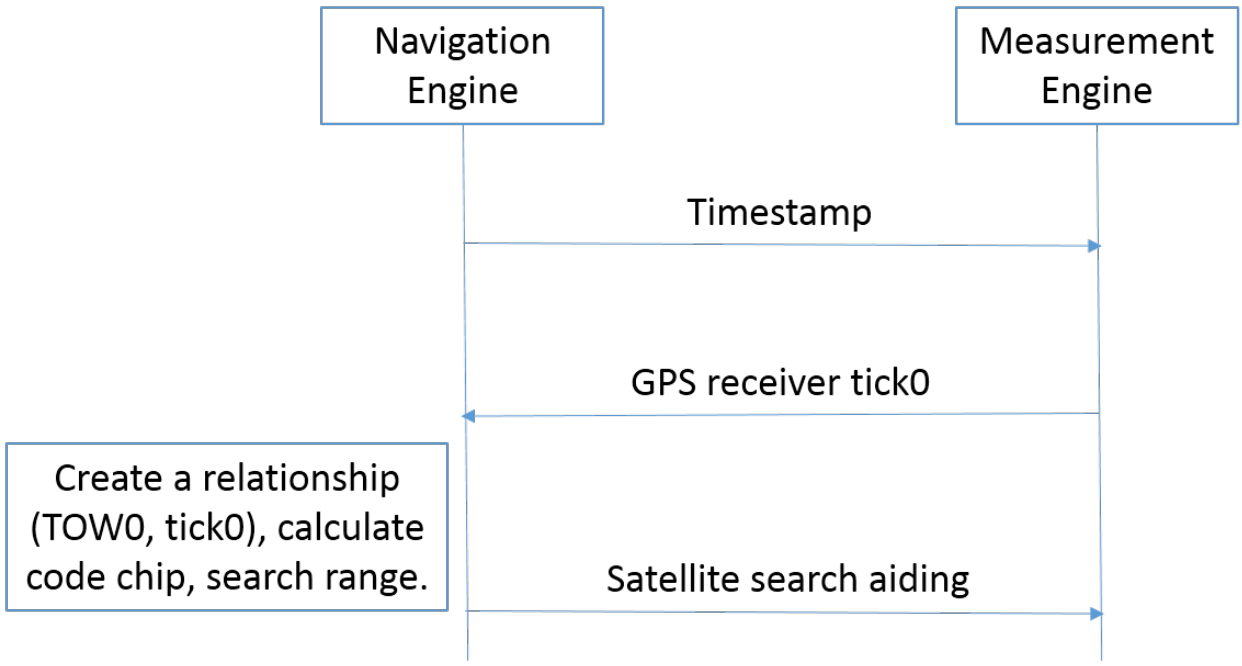


Figure 4-5. Flow diagram of SYNC function

4.2.18. Power scheme

Internal SMPS is used as the power source for the internal RF/BB LDO. It is also used as 1.8V I/O power, external TCXO/LNA voltage source via built-in TCXO switch. The internal SMPS can switch to the LDO mode to supply power to each of the blocks, as described below.

- The minimum/maximum input voltage of AVDD43_VBAT and AVDD43_DCV is 2.8 or 4.3V.
- The power-on reset voltage threshold of AVDD43_VBAT is 2.7 ± 0.1 V. The maximum TLDO dropout voltage at half load (25mA) is 0.2V. If one external LDO provides power to MT2523G, the 3.3V external LDO will be recommended after considering TLDO dropout.
- The power efficiency in SMPS mode will be better than that in the internal LDO mode.
- I/O supports 1.8 and 2.8 volts. The power comes from SMPS output for 1.8V application or TLDO output (AVDD28_TLDO) for 2.8V application.
- The power for internal flash is from AVDD28_TLDO.
- TCXO power is from AVDD_TCXO_SW that can be selected either from AVDD28_TLDO (2.8V) or from AVDD28_CLDO (1.8V) by setting up the power-on strap.
- RTC LDO input power is from backup battery or coin battery.

Here are three power schemes: low power (Figure 4-6), low cost (Figure 4-7) and external PMU (Figure 4-8).

The power on/off for external LDO mode is shown in Figure 4-9.

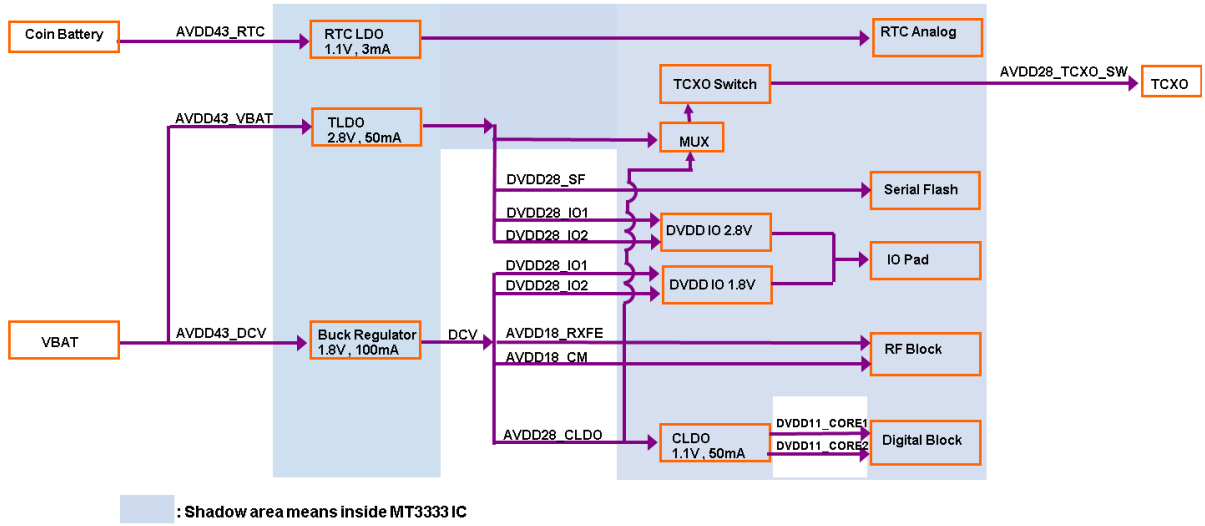


Figure 4-6. Power supply connection (low power)

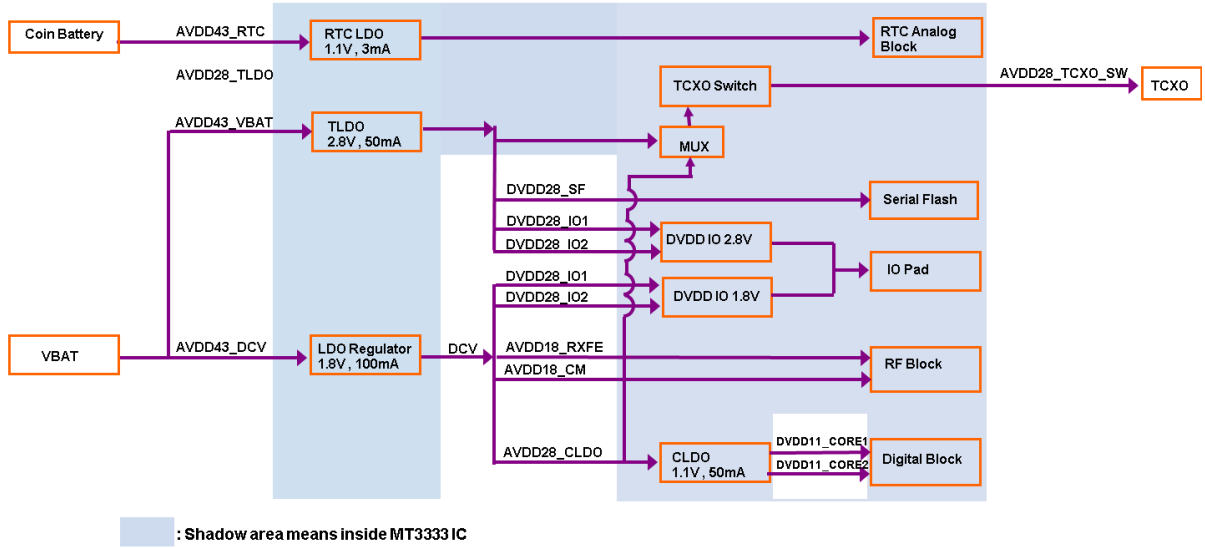


Figure 4-7. Power supply connection (low cost)

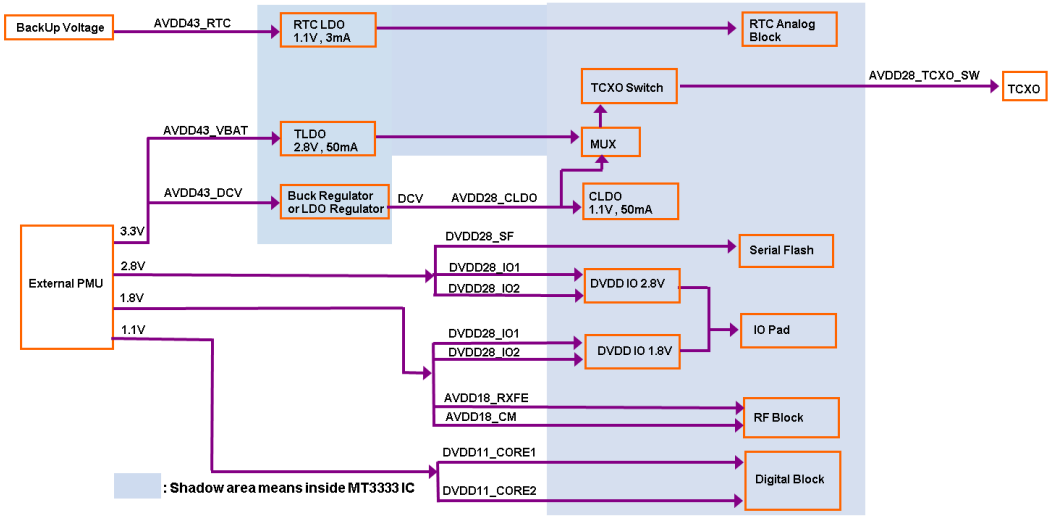


Figure 4-8. Power supply connection (external LDO)

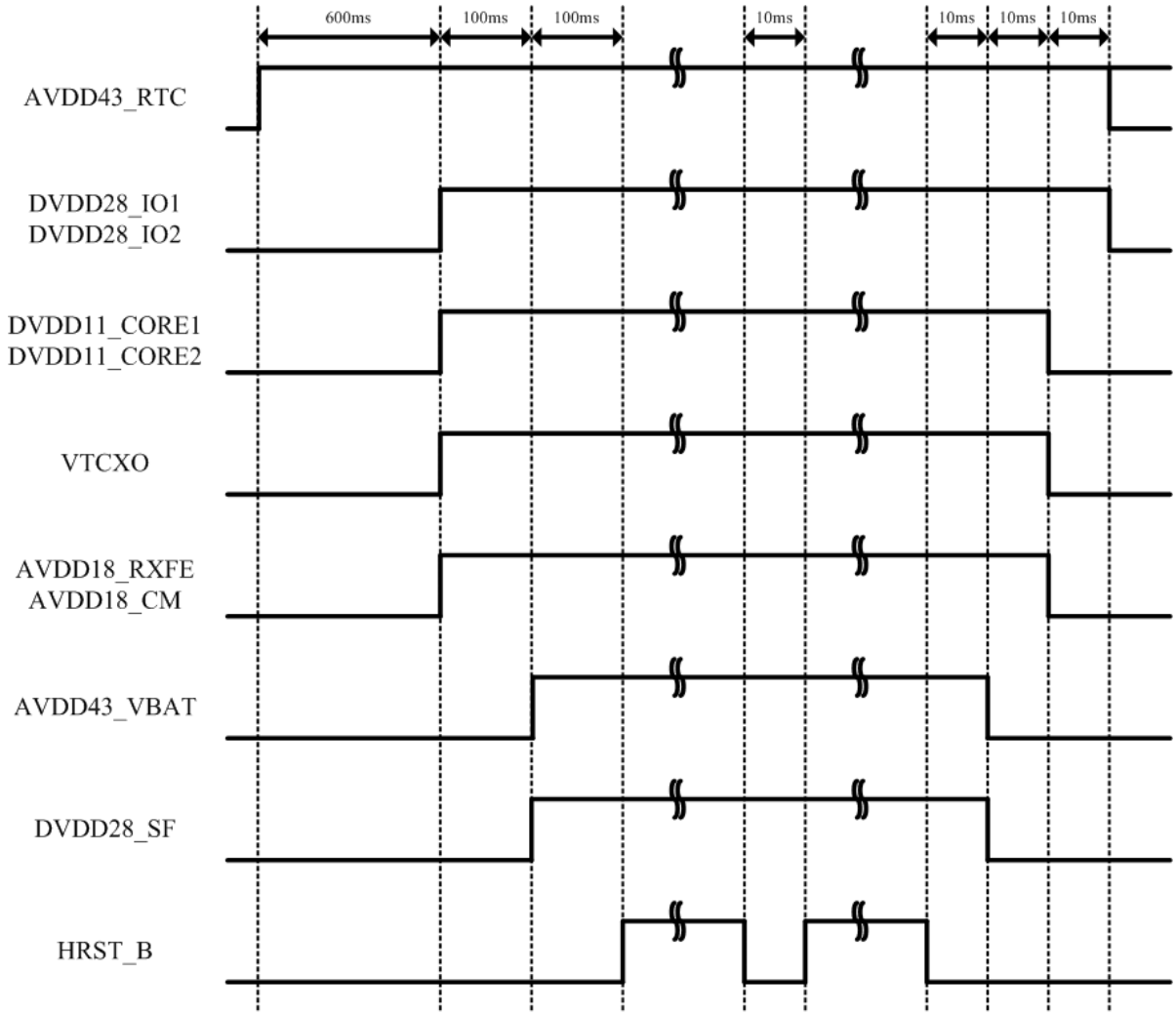


Figure 4-9. Power on/off sequence for external LDO mode

4.3. Interface characteristics

Table 4.3-1. JTAG interface timing

Description	Symbol	Minimum	Maximum	Unit	Note
TDI input setup to rising TCK	T1	0.35T	-	ns	1
TDI input hold from rising TCK	T2	0.15T	-	ns	1
TMS input setup to rising TCK	T1	0.35T	-	ns	1
TMS input hold from rising TCK	T2	0.15T	-	ns	1
Rising TCK to TDO valid	T3	-	0.5T	ns	1
TDO hold from rising TCK	T4	0	-	ns	1

Note, the maximum frequency of JTAG clock cycle (TCK) is 50MHz.

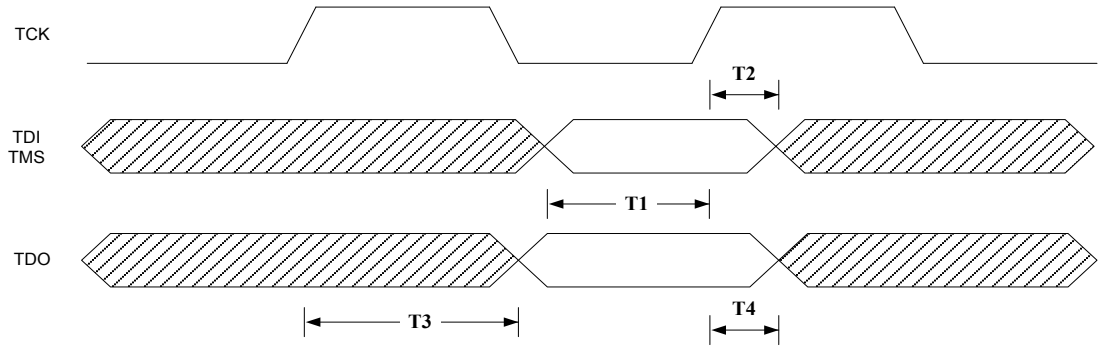


Figure 4-10. Timing diagram of the JTAG interface

Table 4.3-2. RS-232 interface timing

Required baud rate (bps)	Programmed baud rate (bps)	Baud rate error (%)	Baud rate error (%) 3
4,800	4,800.000	0.0000	0.002
9,600	9,600.000	0.0000	0.002
14,400	14,408.451	0.0587	0.0567
19,200	19,164.319	0.0587	0.0567
38,400	38,422.535	0.0587	0.0567
57,600	57,633.803	0.0587	0.0567
115,200	115,267.606	0.0587	0.0567
230,400	230,535.211	0.0587	0.0567
460,800	454,666.667	-1.3310	-1.3330
921,600	909,333.333	-1.3310	-1.3330

Notes:

1) UART baud rate settings with UART_CLK frequency at 16.368MHz (UART_CLK uses the reference clock of the system).

2) The baud rate error is optimized. Each baud rate needs to adjust counter to obtain the optimized error.

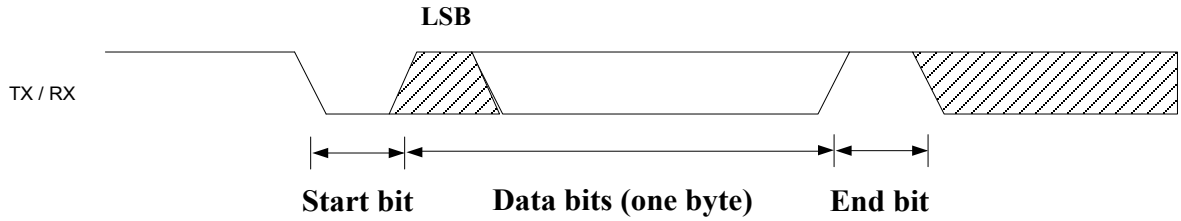


Figure 4-11. Timing diagram of RS-232 interface

4.4. GNSS performance

Table 4.4-1. GNSS time to first fix (TTFF)

TTFF	GPS Only	GPS+GLO	GPS+BDU
Cold start TTFF at -130dBm	31.8s	24.2s	31s
Warm start TTFF at -130dBm	31.3s	23.5s	29.5s
Hot start TTFF at -130dBm	0.9s	1s	1s

Table 4.4-2. GNSS sensitivity

Sensitivity	GPS Only	GPS+GLO	GPS+BDU
Cold start (dBm)	-148	-148	-148
Warm start (dBm)	-151	-151	-151
Hot start (dBm)	-163	-163	-163
Tracking (dBm)	-165	-165	-165

5. Power Management Unit

The power management unit (PMU) manages the power supply of the chipset, including baseband, processor, memory, camera, vibrator, and more. The digital part of PMU is integrated with the analog part (see Figure 5-1).

PMU includes the following analog functions for signal processing:

- Digital Core Buck Converter (V_{core}): The buck converter is optimized for high efficiency and low quiescent current.
- LDO and power switch. Regulate battery voltage to lower voltage level.
- LED current sink (ISINK) switches: Sink current for the LCM module.
- Start-up (STRUP). Generates power on/off control sequence of start-up circuits.
- Pulse charger (PCHR). Controls battery charging.

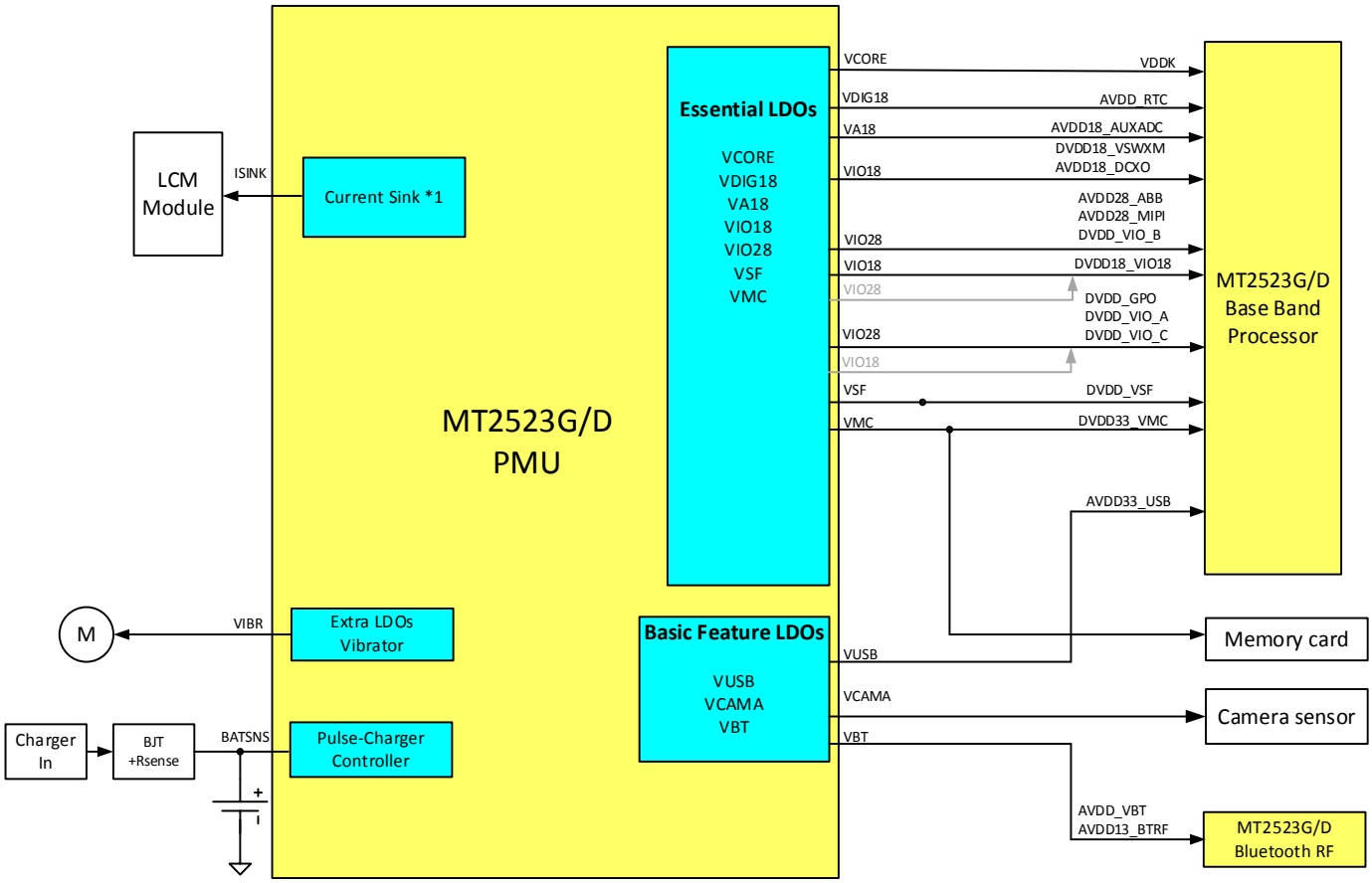


Figure 5-1. MT2523 series PMU architecture

5.1. Power supply schemes

There are four battery input balls for regulator input. The recommended battery operation range is from 3.15V to 4.8V, which is suitable for Li-ion battery applications.

1) VBAT_BUCK_CTRL and VBAT_CORE are power supplies for VCORE in buck mode, VBAT_LDOS1 is the power supply for VCORE in LDO mode, VIO18, VA18, VIO28, VUSB and VDIG18.
2) There is a power switch between VBAT_LDOS1 and PWRSW_OUT to reduce sub-block power leakage current. PWRSW_OUT supplies power for VA28, VCAMA, VBT, VMC and VIBR.
3) VSWXM and VSWDP power switches are supplied with power from VIO18.
4) VSWMP power switch is supplied with power from VIO28.

The LDO input power plan is shown in Table 5.1-1.

Table 5.1-1. LDO input power plan

Input power plan	Type	Name
VBAT_BUCK_CTRL VBAT_VCORE	Buck	VCORE (buck mode)
VBAT_LDOS1	DLDO	VCORE (LDO mode)
VBAT_LDOS2=>PWRSW_OUT	ALDO	VA28
VBAT_LDOS2=>PWRSW_OUT	ALDO	VCAMA
VBAT_LDOS1	DLDO	VIO18
From VIO18	Power switch	VSWXM
From VIO18	Power switch	VSWDP
VBAT_LDOS2=>PWRSW_OUT	ALDO	VBT
VBAT_LDOS1	ALDO	VA18
VBAT_LDOS2	DLDO	VSF
VBAT_LDOS1	DLDO	VIO28
From VIO28	Power switch	VSWMP
VBAT_LDOS1	DLDO	VUSB
VBAT_LDOS2=>PWRSW_OUT	DLDO	VMC
VBAT_LDOS2=>PWRSW_OUT	DLDO	VIBR
VBAT_LDOS1	DVDD18_DIG	VDIG18

5.2. Voltage regulator

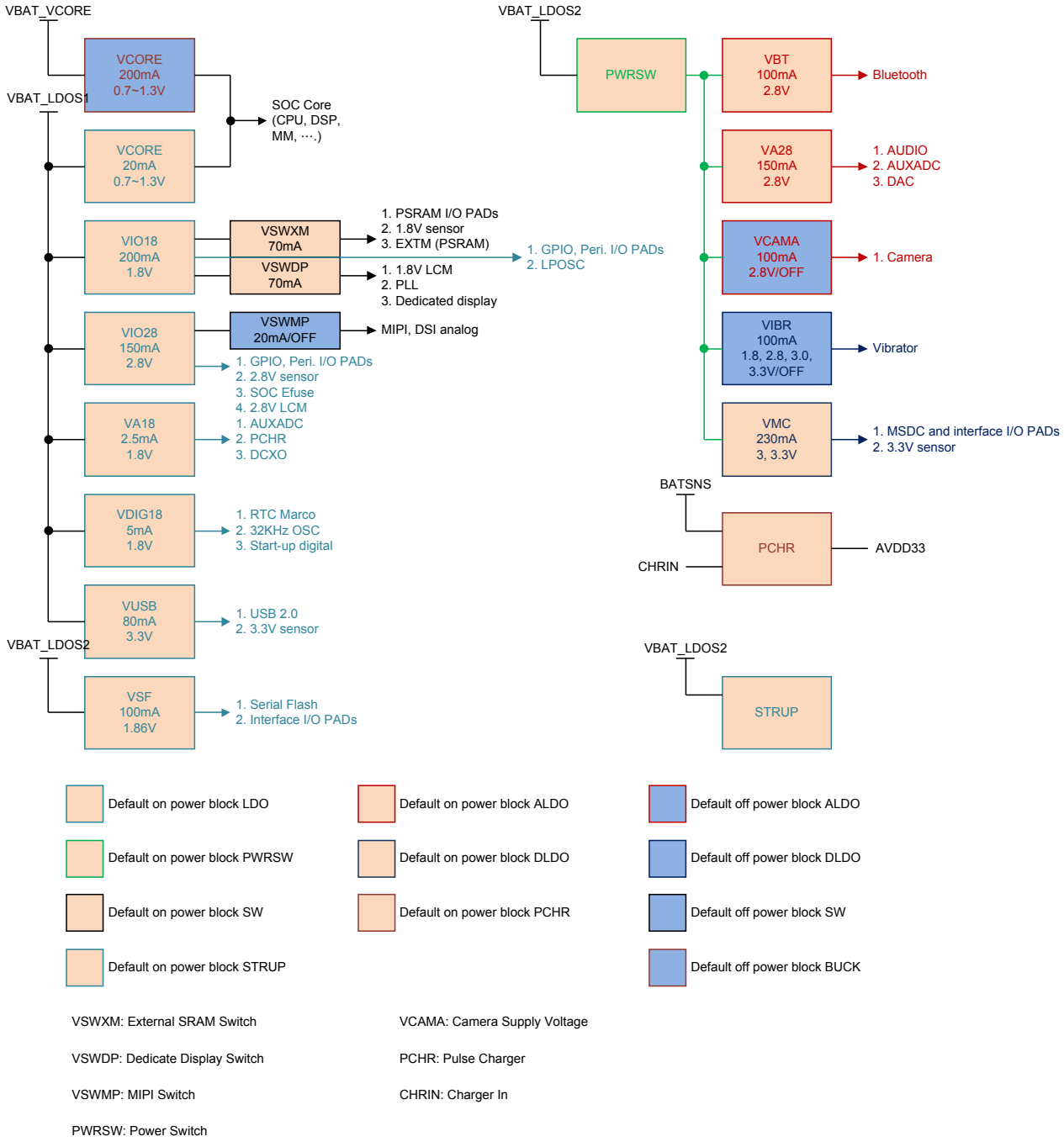


Figure 5-2. MT2523 series power domain

5.2.1. LDO

PMU integrates 12 general low dropout regulators (LDO). Performance optimization is achieved using the APIs for different quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

The LDO is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

The LDO design includes features, such as discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be first discharged to avoid voltage accumulation on the capacitance. The soft-start limits inrush current and controls output-voltage rising time during power-up. The current limit is the current protection to limit LDO's output current and power dissipation.

There are three types of LDOs in PMU for the MT2523 series platform and the general LDO block diagram is shown in Figure 5-3. The analog LDO is optimized for low-frequency ripple rejection to reject VBAT ripples. The digital IO LDO is a linear regulator optimized for very low quiescent current. VDIG18 LDO is a linear regulator that can charge up a capacitor-type backup coin cell that supplies the RTC module.

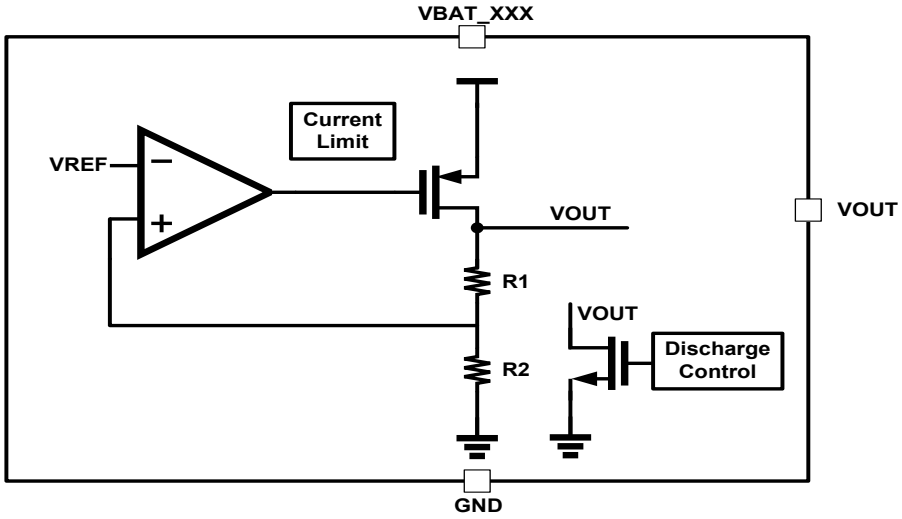


Figure 5-3. General LDO block diagram

5.2.1.1. LDO types

Table 5.2-1. LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax (mA)	Description
ALDO	VBT	2.8	100	Bluetooth
ALDO	VA28	2.8	150	Audio
ALDO	VA18	1.8	2.5	AUXADC
ALDO	VCAMA	2.8	100	Camera sensor
DLDO	VIO28	2.8	150	Digital IO and Bluetooth
DLDO	VUSB	3.3	80	USB
DLDO	VIO18	1.8	200	Digital IO
DLDO	VCORE	0.7~1.30	20	Digital baseband
DLDO	VIBR	1.3/1.5/1.8/2/2.5/2.8/3/3.3	100	Vibrator
DLDO	VMC	1.8/2.8/3.0/3.3	230	Memory card
DLDO	VSF	1.86/3.0/3.3	100	Serial flash
Power Switch	VSWXM	1.8	70	Powered by VIO18 PSRAM I/O.
Power Switch	VSWDP	1.8	70	Powered by VIO18 Dedicated display

Type	LDO name	Vout (Volt)	Imax (mA)	Description
Power Switch	VSWMP	2.8	20	MIPI DSI analog

5.2.1.2. LDO functional specifications

VBAT is from 3.0 to 4.8V, minimum loads are applied to all outputs, unless otherwise noted.

Typical values are at temperature T_A = 25°C. The LDO functional specification is shown in Table 5.2-2.

Table 5.2-2. LDO specifications

Parameter	Type	Conditions		Min	Typ.	Max	Unit
Test conditions for input power range	ALDO and DLDO for VBAT range	Minimum specifications: max {Output Voltage +0.35V; VBAT≧3.0},		-	-	4.8	V
Load/Line regulation	All LDOs Normal mode	Iout= 0~Imax	• Input power range • Typical capacitor • TA = -40°C ~ +85°C	-4	-	+4	%
	All LDOs lite mode	Iout= 0~5%*Imax					
	All LDOs LP mode	Iout= 0~2.5mA					
	All LDOs ULP mode	Iout= 0~10µA					
Power off voltage	ALDO, DLDO and power switch	• Input power range • Typical capacitor • TA = -40°C~+85°C • Iout= 0mA		-	-	0.1	V
Temperature coefficient[1]	ALDO, DLDO and power switch	• VBAT = 3.8V • Typical capacitor • TA = -40°C~+85°C • Iout = 0~Imax		-200	-	200	ppm/C
Load transient response	ALDO, DLDO and power switch	Slew rate= 15mA/µs	• Input power range • Typical capacitor • TA = -40°C ~ +85°C • Iout = 0.01*Imax~0.5*Imax	-5	-	+5	%
Turn-on rise time	VCORE, VIO18, VIO28 and VDIG18	• Input power range • Typical capacitor • TA = +25°C • Iout = 0mA		-	-	6	ms
	ALDO and DLDO			-	-	0.3	
Turn-on	ALDO, DLDO and	• Input power range		-	-	Vout	V

Parameter	Type	Conditions		Min	Typ.	Max	Unit
overshoot	power switch	• Typical capacitor • TA = +25°C • Iout = 0mA				*1.1	
Power off time	ALDO, DLDO and power switch	Bypass capacitor ≦ 2.2µF	• Input power range • TA = +25°C • Iout = 0mA	-	-	4	ms
		Bypass capacitor ≦ 4.7µF		-	-	8	ms
		Bypass capacitor ≦ 10µF		-	-	12	ms
Output noise	ALDO	Frequency = 10Hz to 80kHz	• Input power range • Typical capacitor • TA = +25°C • Iout = 0.2*Imax ~0.5*Imax	-	90	-	uVrms
	DLDO			-	500	-	uVrms
	ALDOs and DLDOs	Frequency = 10Hz to 10MHz		-	1000	-	uVrms
PSRR	ALDO	Frequency = 217Hz to 3kHz	• Input power range • Typical capacitor • TA = +25℃ • Iout = 0.2*Imax / 0.5*Imax	-	50	-	dB
		Frequency= 3kHz to 30kHz		-	38	-	dB
	DLDOs	Frequency = 217Hz		-	40	-	dB
Short current	ALDO and DLDO	OC	• Input power range • Typical capacitor • TA = +25°C	1.2 x Imax	-	7.5 x Imax	
		OCFB		0.2 x Imax	-	5 x Imax	
Quiescent current	ALDOs normal mode	• Input power range • Typical capacitor • TA = +25°C • Iout = 0mA		-	-	55	µA
	DLDOs normal mode (VCORE, VIO18, VIO28, VUSB, VIBR, VSF)			-	28	35	
	DLDOs normal mode (VMC)			-	75	91	
	All LDOs lite mode			-	8	15	
	All LDOs LP mode			-	1.6	2.2	
	All LDOs ULP mode			-	-	0.5	

[1] Temperature slope constraint: < 2.5°C/min.

5.2.1.3. Regulator ON

There are three power modes configured by software when the regulator is on — **Normal** mode, **Lite** mode and **LP** mode. In power-on state, the regulators are powered on by normal mode to achieve fast power-on. The soft start feature limits the inrush current to avoid battery voltage drop. DIG18 LDO is in **ULP** mode at power-off state.

5.2.1.4. Regulator Off

Disabling the regulator and entering the shutdown mode will cause output voltage to discharge through N-MOSFET to ground. In shutdown mode, the quiescent current can be reduced to below 0.1µA.

5.2.2. VCORE (buck mode)

5.2.2.1. Functional specifications

VBAT is from 3.0 to 4.8V, minimum loads are applied to all outputs, unless otherwise noted.

Typical temperature values are at T_A = 25°C. The VCORE functional specification is shown in Table 5.2-3.

Table 5.2-3. VCORE specifications

Parameter	Conditions	Min.	Typ.	Max.	Unit
Buck – VCORE					
Turn-on overshoot	• Vout = 1.2V • No load • Cout = 10µF	-	-	10	%
Current limit	• VBAT = 3.8V	0.24	0.4	0.8	A
Temperature coefficient[1]	• VBAT = 3.8V • I_Load = from 0 to Full load	-200	-	+200	ppm/C
Efficiency	• VBAT = 3.8V, Vout = 1.2V, • I_Load = 1mA • Inductor DCR, typ = 58mΩ	-	75	-	%
	• VBAT = 3.8V, Vout = 1.2V, • I_Load = 10mA • Inductor DCR, typ = 58mΩ	-	80	-	%
	• VBAT = 3.8V, Vout = 1.2V, • I_Load = 50mA • Inductor DCR, typ = 58mΩ	-	81	-	%
	• VBAT = 3.8V, Vout = 1.2V, • I_Load = 130mA • Inductor DCR, typ = 58mΩ	-	82	-	%
Turn-on rise time	• Vout = 1.2V • No load or 10mA • Cout = 10µF, Register EN	-	-	0.2	ms

Parameter	Conditions	Min.	Typ.	Max.	Unit
Output ripple voltage	• VBAT = 3.8V, Vout = 1.2V • I_Load = from 0 to Full load • 20MHz measurement BW • Cout = 10µF	-	-	50	mVpp
Load transient	• a. LOAD = 50mA~200mA (TR/TF=1µs) • b. LOAD = 1mA~50mA • (TR/TF = 1µs)	-3.5	-	+3.5	%
DC accuracy (including Line/Load regulation at PWM)	• VBAT = 2.5V to 4.8V • I_Load = from 0 to Full load • TA= +25℃	-2	-	+2	%

[1] Temperature slope constraint: < 2.5℃/min.

5.3. Low power mode

The device supports four low-power modes to achieve the best compromise in low power consumption.

The **ULP** mode LDO is only implemented in DIG18, VCOR_LOD, VIO18, VIO28 and VSF.

LDO mode selection can be configured through the PSI register. The selection of LDO mode depends on the system requirements, details are shown in Table 5.3-1. Note the output current capability of each LDO mode.

Table 5.3-1. LDO mode quiescent current

LDO mode	Conditions	Min.	Typ.	Max.	Unit
ALDOs normal mode	• Input power range • Typical capacitor • TA = +25℃ • Iout = 0mA	-	-	55	µA
DLDOs normal mode (VCORE, VIO, VIO28, VUSB, VIBR)		-	28	35	
DLDOs normal mode (VMC,VSF)		-	75	91	
All LDOs lite mode		-	8	15	
All LDOs LP mode		-	1.6	2.2	
All LDOs ULP mode		-	-	0.5	

5.4. Pulse Charger (PCHR)

The charger controller senses the charger input voltage from either a standard AC-DC adapter or a USB charger. When the charger input voltage is within a pre-determined range, the charging process is activated. This detector can resist higher input voltage than other parts of the PMU.

5.4.1. Charger detection

Whenever an invalid charging source is detected (> 5.5V), the charger detector will stop the charging process immediately to prevent the chip even the device from burning out. In addition, if the charger-in level is not high enough (< 4.15V), the charger will also be disabled to avoid improper charging behavior.

5.4.2. Charging control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports **pre-charge mode** (VBAT < 3.45V, PMU power-off state), **CC mode** (constant current mode or fast charging mode at the range 3.45V < VBAT < 4.2V) and **CV mode** (constant voltage mode) to optimize the charging process for Li-ion battery. Figure 5-4 and Figure 5-5 are the charging block/state diagrams.

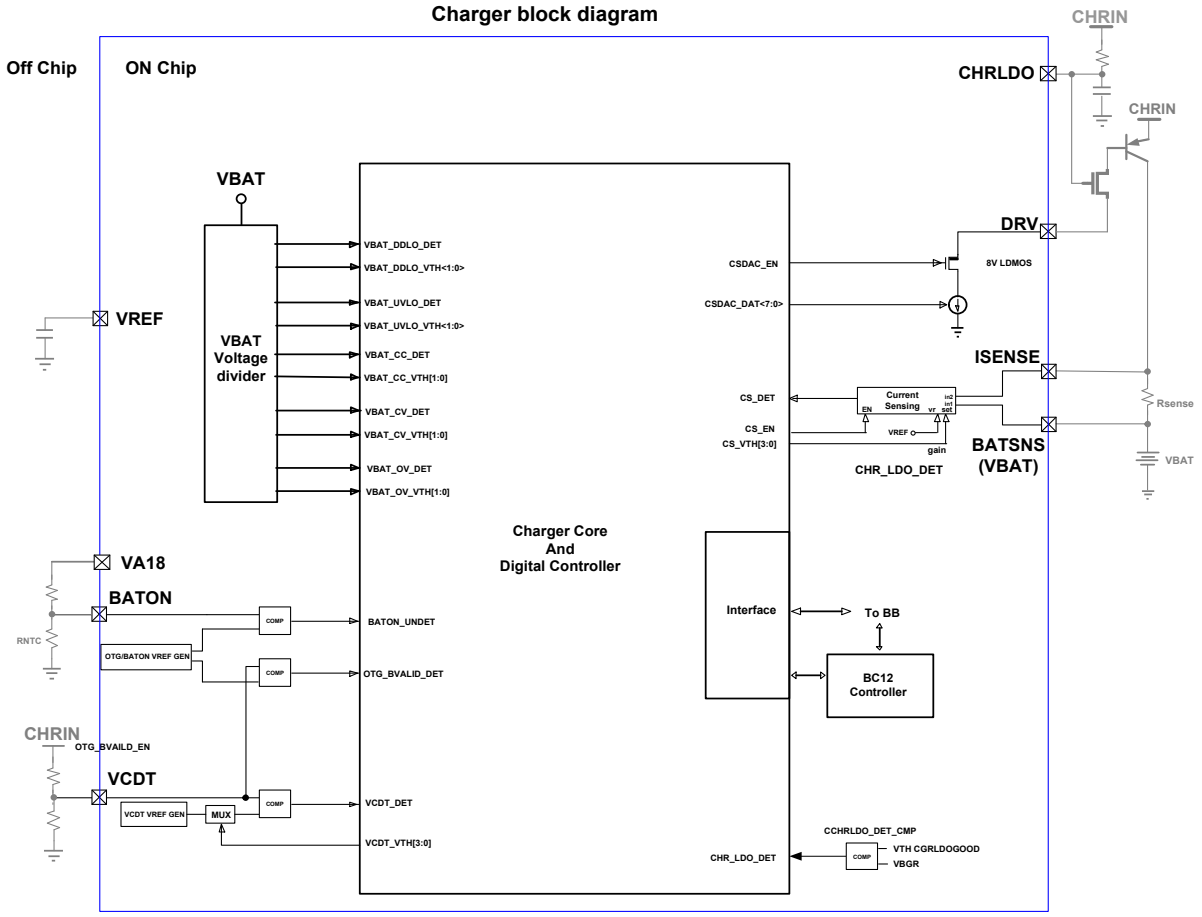


Figure 5-4. PCHR schematics

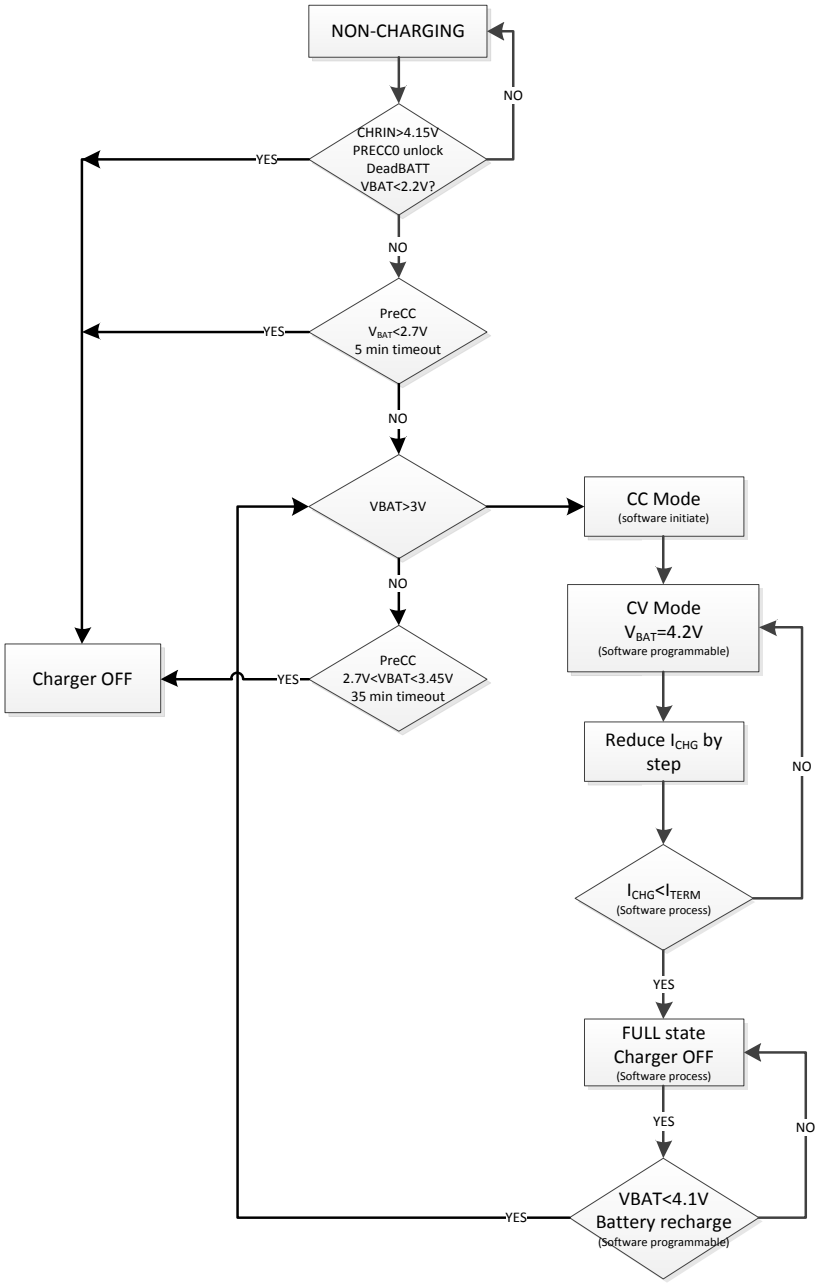


Figure 5-5. Charging control modes

Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. When the battery voltage is deeply discharged below 2.2V, PRECC0 trickle charging current will be applied to the battery.

The PRECC0 trickle charging current is about 550ms pulse 11mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, called the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 3.92mV (despite AC charger or USB host plug-in. The closed-loop pre-charge current can be calculated:

$$I_{PRECC1} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.45V, it can be switched to the CC mode. (CHR_EN should be high.) In CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.56Ω, the CC mode charging current can be set from 7 to 150mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage will be used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current will gradually decrease, and the end-of-charging process will start. This may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process completes once the current automatically reaches zero using different batteries for optimization.

BC1.2 dead-battery support of Chinese standard

MT2523 series supports dead-battery condition (called BC1.2). The specification protects dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after trickle current is applied, the charger will be disabled. On the other hand, if the battery voltage is raised to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be PRECC1 current.

Under the condition of battery voltage being from 2.2V to 3.45V, the charger will charge the battery with the PRECC1 current.

A dedicated 5-min (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35-min (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.45V under charging.

The trickle current (IUNIT) and two dedicated timers will protect the charging action if the battery is dead.

5.4.3. Pulse charger functional specifications

Table 5.4-1. Charger detection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charger detect-on range		4.0	-	5.5	V

Table 5.4-2. Pre-charge specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IUNIT with 500ms pulse	VBAT < 2.2V	-	11	-	mA
	Pre-charging current	VBAT < 2.2V (500ms pulse)	-	11	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		VBAT ≥ 2.2V (USB host & AC adapter)	-	3.92	-	mV
	Pre-charging off threshold	CHR_EN = L	-	3.45	-	V

Table 5.4-3. Constant current specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current (CS_VTH)	CS_VTH [3:0] = 0000	-5%	84mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0001	-5%	75.6mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0010	-5%	67.2mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0011	-5%	61.6mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0100	-5%	56mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0101	-5%	50.4mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0110	-5%	44.8mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 0111	-5%	39.2mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1000	-5%	36.4mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1001	-5%	30.8mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1010	-5%	25.2mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1011	-5%	16.8mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1100	-5%	11.2mV/R_{sense}	+5%	mA
		CS_VTH [3:0] = 1101	-10%	7.884mV/R_{sense}	+10%	mA
		CS_VTH [3:0] = 1110	-10%	6.234mV/R_{sense}	+10%	mA
		CS_VTH [3:0] = 1111	-10%	3.92mV/R_{sense}	+10%	mA

Table 5.4-4. Constant voltage and over-voltage protection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charging complete threshold	Programmable: 3.6~4.48 V	-30	-	+30	mV
	Battery over-voltage protection threshold (OV)	Programmable: 3.8~4.7 V	-30	-	+30	mV

Table 5.4-5. BC1.2 specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
IUNIT	BC1.2 trickle current	VBAT < 2.2V	-	11	-	mA
IPRECC1 (USB host and AC adapter)	PRECC1 current	2.2 < VBAT < 3.3V	-	3.92mV/Rsense	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T1	5 minute dedicated timer	2.2 < VBAT < 2.7V	3.5	5	6.5	min.
T2	35 minute dedicated timer	2.7 < VBAT < 3.3V	25.6	32	38.4	min.
TUNIT	BC1.1 trickle current period		-	-	1	seconds

5.5. Power On/Off sequence

PMU handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state ($V_{BAT} \geq UVLO_{VTHH}$) nor in thermal condition, there will be three methods to power on the handset.

1) Pulling the PWRKEY low (press PWRKEY).
2) Setting the PWRHOLD to high.
3) Plugging in a valid charger.

The power on/off sequence is shown in Figure 5-6 and Figure 5-7.

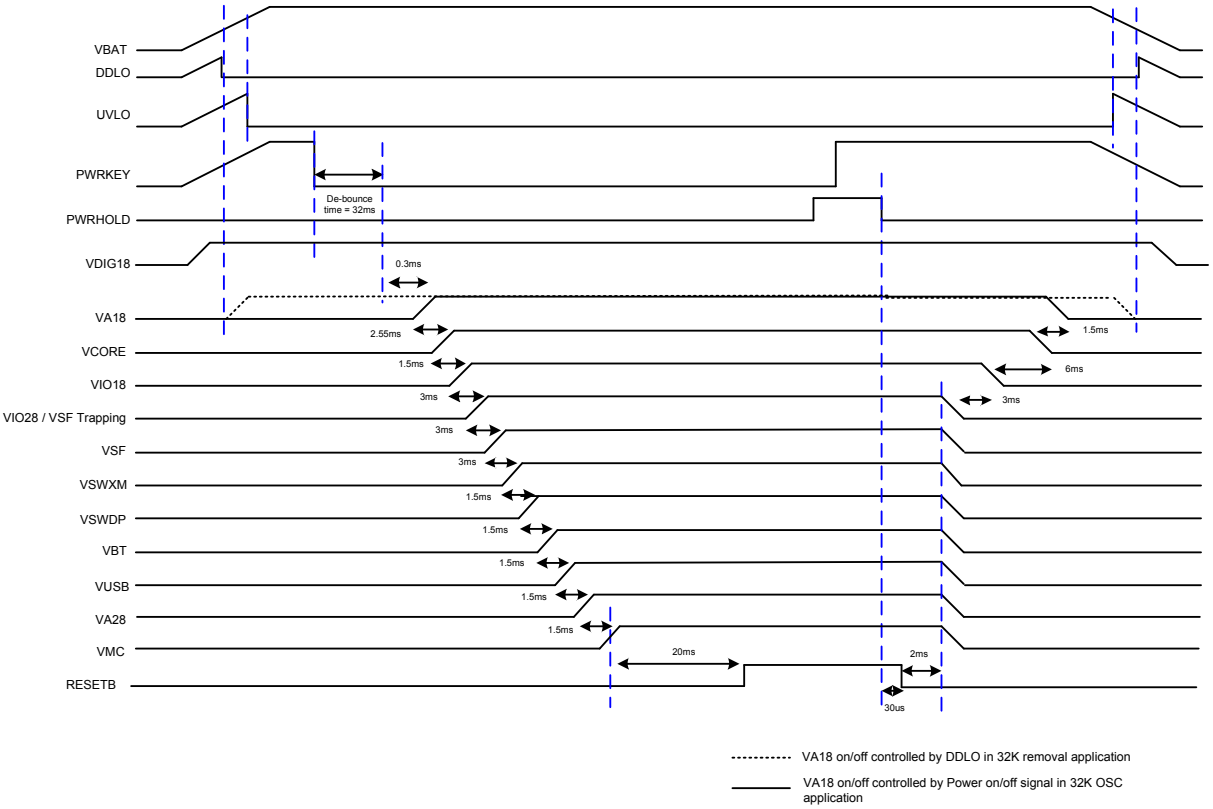


Figure 5-6. Power-on/off control sequence by pressing PWRKEY

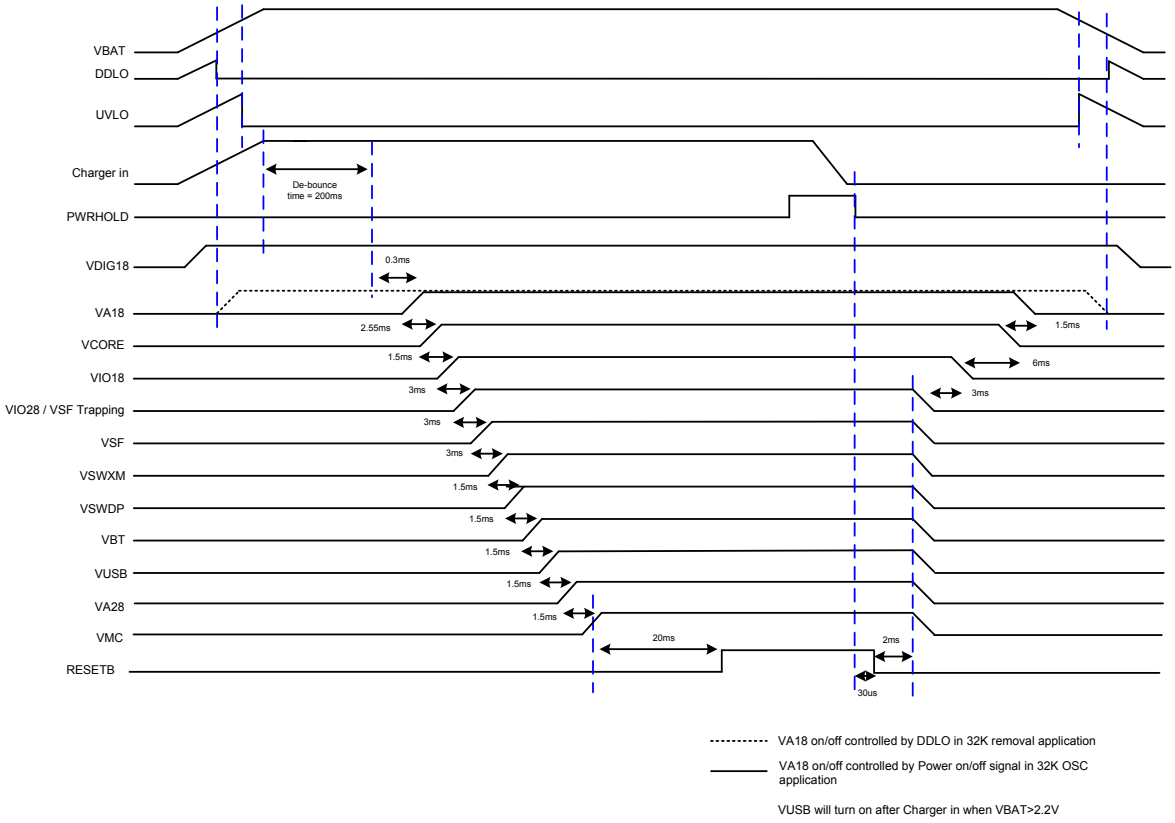


Figure 5-7. Power-on/off control sequence by charger plug in

1) Pushing PWRKEY (pulling the PWRKEY pin to low level).

Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends once all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2) RTC module generates PWRHOLD to wake up the system.

If the RTC module is scheduled to wake up the handset at some time, the PWRHOLD signal will be directly sent to PMIC. In this case, PWRHOLD becomes high at specific moment and allows PMIC power-on. This is called RTC alarm.

3) Valid charger plug-in (CHRIN voltage within valid range).

The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage is greater than CHGIN_VTHH and VSYS>UVLO, the handset will also be powered on.

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VBATSNS. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator, to ensure smooth power-on. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit that takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 125°C (typical condition), PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

5.6. LED current sink (ISINK)

Maximum of two indicator LED drivers are supported. Figure 5-8 provides the usage of indicator LED drivers. The LED driver of MT2523 series supports PWM mode and breath mode. The LED current changing from small to large then descending is the breath mode. The breathing cycle time, including `Trising_1`, `Trising_2`, `Ton`, `Toff`, `Tfalling_1`, and `Tfalling_2` period can be modified through software configuration of the registers.

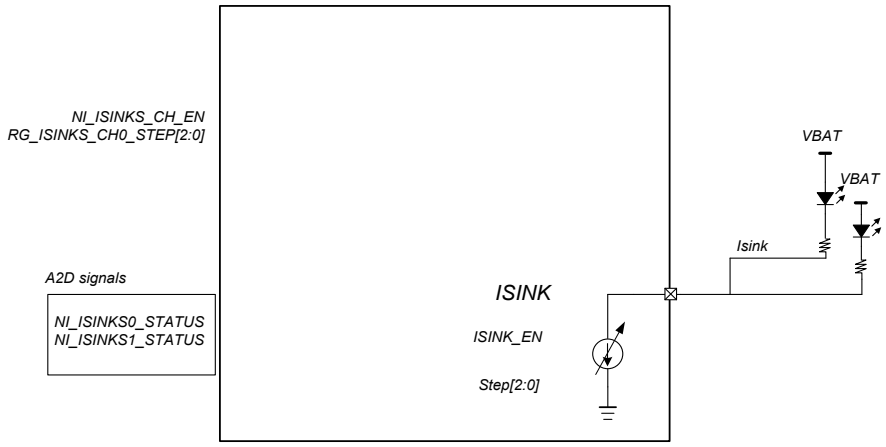


Figure 5-8. ISINK block diagram

5.6.1. ISINK functional specifications

Table 5.6-1. ISINK specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 000	-	4	-	mA
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 001	-	8	-	mA
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 010	-	12	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 011	-	16	-	mA
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 100	-	20	-	mA
	Sink current of ISINK	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 101	-	24	-	mA
	Current accuracy	Von > 0.3V, 100% dimming duty	-15	-	15	%

5.7. Vibrator driver

The VIBR driver power allows up to 100mA current for eccentric rotating mass (ERM) or coin type vibrator with programmable output voltage.

5.8. PMU AUXADC

The PMU auxiliary ADC includes the following functional blocks:

- Analog multiplexer: Selects signals from one of the input channels. The signal, such as temperature, are monitored and transferred to the voltage domain.
- 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

The PMU auxiliary ADC input range and specification is shown in Table 5.8-1 and Table 5.8-2.

Table 5.8-1. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	3.0 ~ 4.8
1	ISENSE	3.0 ~ 4.8
2	VCDT	0 ~ 1.5
3	BATON	0.1 ~ 1.7
Others	Internal use	N/A

Table 5.8-2. AUXADC specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Supply voltage		1.7	1.8	1.9	V
Resolution	BATSNS / ISENSE	-	-	15	Bits
	Others	-	-	12	Bits
Analog-input bandwidth		-	50	-	kHz
Sample rate		-	100	-	kHz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output	-2	-	+2	LSB
DNL	15-bit output	-2	-	+2	LSB

Parameter	Conditions	Min.	Typical	Max.	Unit
Current consumption	Active mode	-	350	-	µA
Fuel Gauge application					
Time-Base Accuracy	Active mode	-0.5	-	0.5	%
Current consumption with 10S tracking period (Hardware)	Average current	-	0.091	-	µA
BATSNS Voltage Error	VBAT=4.2V , TA = 25 ℃	-5	-	5	mV
	TA =-20 ~ 70 ℃	-	±10	-	mV

6. Low Power Control System

6.1. Power sources

The power structure embedded with various LDOs is shown in Figure 6-1. Detailed descriptions of the control interface and register definition of each LDO and BUCK is provided in section 5, “Power Management Unit”.

The VCBUCK or VCLDO is reserved for the digital core power, and the IO power is generally connected with VIO18, VIO28 and VMC. The VA is dedicated to the analog components, such as audio AD/DA and PLL in the chip. Power source options for the external device such as PSRAM, sensors, SD card, and camera are also available. The VMC is reserved for an external SD card extension. The VCAMA is reserved for camera applications.

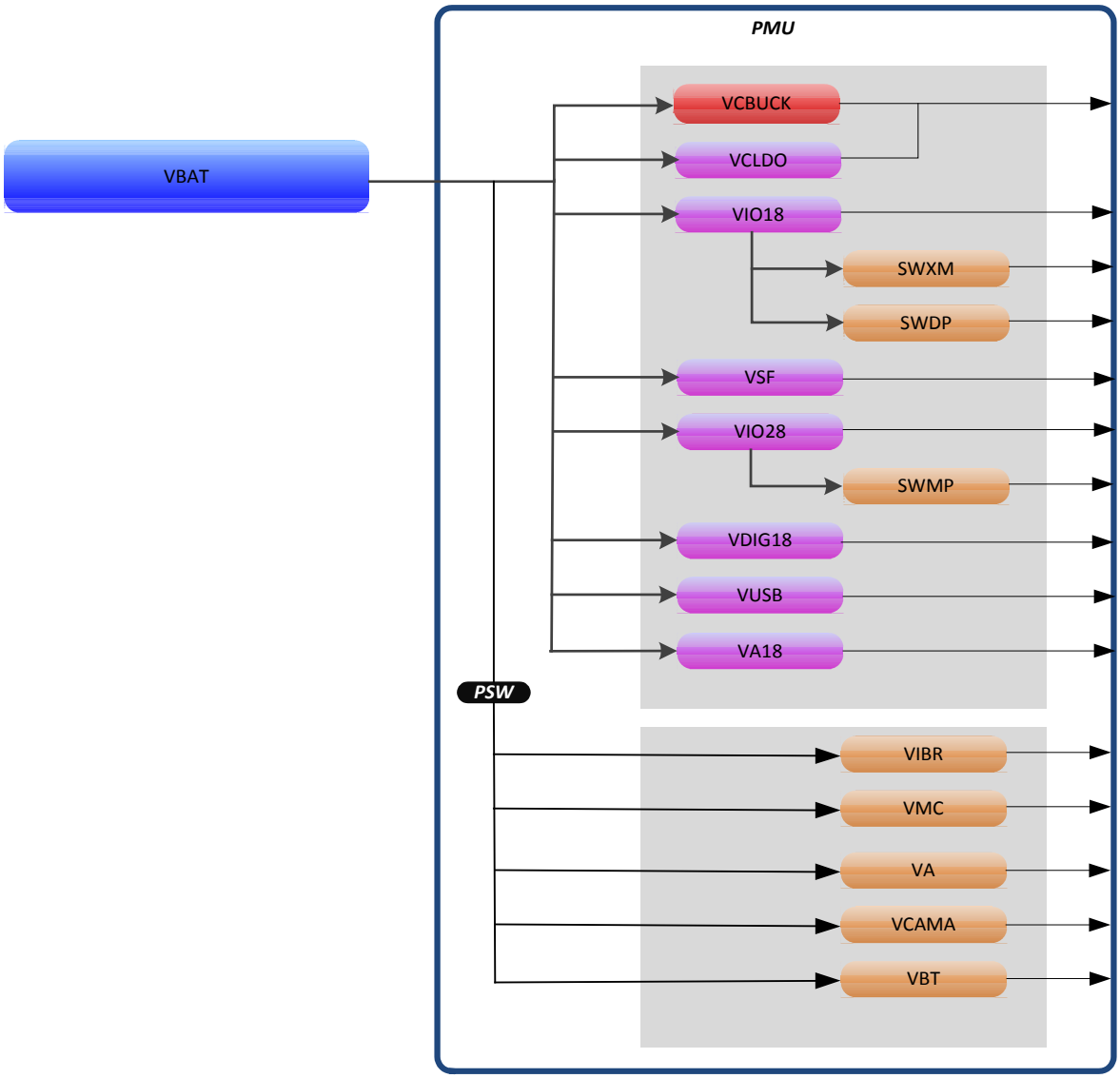


Figure 6-1. Power sources provided by PMU for system power planning

6.2. MTCMOS power domain

The MTCMOS technology is adopted to reduce the power consumption according to different scenarios. Table 6.2-1 provides the list of MTCMOS partitions. Each domain can be optionally turned on and off by software control.

Table 6.2-1. The MTCMOS power domain

MTCMOS domain	Description
AO_PD	Always on power domain. To save the power, only limited resources such as wakeup logics and modules that should keep register retention are designed in this domain.
INFRA_PD	The Infrasys MTCMOS domain. The major bus fabric and peripheral designs, such as I2C, UART, PWM, SPI, DMA and USB, are in this domain.
CPU_PD	CPU MTCMOS domain. The CPU core, cache controllers with ROM and RAM. This MTCMOS domain contains Cortex-M4 core and the cache controller with ROM and SRAM. It will power-off only in sleep or deep sleep mode.
MMSYS_PD	Multimedia system MTCMOS domain. The display engine, 2D graphic engine, image processing unit and camera interface are in this domain.
BT_AO_PD	BT_AO MTCMOS domain. Circuits that belong to BT/BLE/ANT are designed in this domain.
BT_OFF_PD	BT_OFF MTCMOS domain. Circuits that belong to BT/BLE/ANT are designed in this domain.
DSP_PD	DSP MTCMOS domain. The FD216 DSP with ROM and RAM and the audio interface (I2S, PCM and MIC) are supported in this domain.

6.3. Power modes

Different power modes are designed to optimize the current consumption further. Table 6.3-1 summarizes the power modes and peripheral usage.

Table 6.3-1. Power modes

Feature	Configurable power mode					
	High-Speed	**Full-Speed**	**Low-Speed**	**Sleep**	**DeepSleep**	**PowerOff**
CPU	Active	Active	Active	Off	Off	Off
CPU Frequency	208Mhz	104Mhz	26Mhz	Off	Off	Off
BUS Frequency	62.4Mhz	62.4Mhz	13M	Off	Off	Off
VCORE Voltage[1]	1.3	1.1	0.9	0.9	0.9	Off
Flash	On	On	On	PowerDown	PowerDown	Off
PSRAM	On	On	On	HalfSleep[2]	HalfSleep	Off

[1] It means the minimum VCORE voltage requirement for CPU frequency reaches 208MHz, 104MHz and 26MHz for each power mode, respectively.

[2] The data is retained in this mode.

Feature	Configurable power mode					
SRAM	On	On	On	Retention/Off	Retention/Off	Off
MCU Clock Source	PLL	HFOSC	DCXO/LFOSC	Off	Off	Off
RTC	On	On	On	On	On	On
System Current	85µA/MHz	55µA/MHz	50µA/MHz	48µA	35µA	17µA
MCU Current	70µA/MHz	50µA/MHz	40µA/MHz	–	–	–
Wakeup time[3]	–	–	–	LowSpeed: 7µs Others: 320µs	320µs	50ms

1) **Active mode** for **High-Speed**, **Full-Speed** and **Low-Speed**

In these modes, the maximum frequency of MCU is 208Mhz, 104Mhz and 26Mhz, respectively, and the minimum VCORE voltage requirement is 1.3V, 1.1V and 0.9V, respectively, for different performance requirements and low power optimization. The code can be executed from SRAM, PSRAM and Serial Flash device. There is also an independent clock gating control to lower the power consumption, if the peripherals are idle.

2) **Idle mode** for **Sleep** and **DeepSleep**

In this mode, there is only 32kHz clock available, the other clock sources are turned off. In **Sleep** mode, the voltage is fixed to 0.9V and the wakeup time for **LowSpeed** is only 7µs when fast wakeup is required. In **DeepSleep** mode, the wakeup time is 320µs but current consumption is lower than in **Sleep** mode.

3) **PowerOff mode**

In this mode, all power supply sources are off except VRTC. It supports RTC timer to wake up the system and can detect the charger and if it's plugged-in, and more.

6.4. Power performance summary

Table 6.4-1 lists example current consumptions in VBAT domain. Note that the current measurement conditions are typical conditions for process, voltage and temperature. Besides, the RTC is configured in SCXO mode.

Table 6.4-1. Current consumption in different power modes

Power mode	Test Conditions	Typical	Unit
PowerOff	• System Off • No SRAM retained • Only RTC and PMU AO are alive	17	µA
DeepSleep	• 160kB SRAM is retained • Serial Flash in deep power down mode • DC-DC off • All MTCMOS off • PSRAM power off • VCORE = 0.7V	35	µA

[3] The wakeup time defines the instant the CPU can execute the first instruction.

Power mode	Test Conditions	Typical	Unit
	• 160kB SRAM is retained • Flash in deep power down mode • DC-DC off • All MTCMOS off • PSRAM power on	48	µA
Sleep	• 160kB SRAM is retained • Flash in deep power down mode • DC-DC off • All MTCMOS off • PSRAM power off	42	µA
	• 160kB SRAM retained • Flash in deep power down mode • DC-DC off • All MTCMOS off • PSRAM power on	54	µA
CPU Power Efficiency			
CoreMark_TCM at Low-Speed(1)	• Running from TCM • DC-DC on • PSRAM power off • CPU clock frequency 25MHz by using LFOSC	0.26mA and 40µA/MHz	–
CoreMark_TCM at Full-Speed	• Running from TCM • DC-DC on • PSRAM power off • CPU clock frequency 95MHz by using HFOSC	0.44mA and 50µA/MHz	–
CoreMark_TCM at High-Speed	• Running from TCM • DC-DC on • PSRAM power off • CPU clock frequency 208MHz by using DCXO and PLL	3.2mA and 70µA/MHz	–
CoreMark_Cache at Low-Speed	• Running from serial flash, cache enabled • DC-DC on • CPU clock frequency 25MHz by using LFOSC	0.32mA and 53µA/MHz	–
CoreMark_Cache at Full-Speed	• Running from serial flash, cache enabled	0.48mA and 70.5	–

(1) The power consumption is represented as MCU power efficiency with the power, including the PMU, PLL, DCXO, RTC etc.

Power mode	Test Conditions	Typical	Unit
	• DC-DC on • CPU clock frequency 95MHz by using HFOSC	µA/MHz	
CoreMark_Cache High-Speed	• Running from serial flash, cache enabled • DC-DC on • CPU clock frequency 208MHz by using DCXO and PLL	3.3mA and 98 µA/MHz	–
Bluetooth RF only Power Consumption			
Bluetooth TX Current	Bluetooth RF TX Current, 0dBm	16	mA
Bluetooth RX Current	Bluetooth RF RX Current, 1 Mbps	9	mA
Chip Power Consumption in Bluetooth use cases			
Bluetooth LE connection	1T1R; Period: 1280ms; TX Power: 0dBm; PSRAM off;	69	µA
Bluetooth LE advertising	3T3R; Period: 1280ms; TX Power: 0dBm; PSRAM off;	72	µA
Bluetooth paging scan	Period: 1280ms; TX Power: 0dBm; PSRAM off;	182	µA
Bluetooth sniff	Period: 1280ms; TX Power: 0dBm; PSRAM off;	127	µA
Bluetooth voice	• Bluetooth Voice - Connection: eSCO; • Packet Type: 2-EV3 • Codec: mSBC • Air Coding: Transparent Data • PSRAM power off	15	mA
BLUETOOTH A2DP	• A2DP Stereo streaming MPEG-2,4 AAC LC: • 44.1 kHz sampling • No sniff • Channel Mode Support : 2 • PSRAM power off	12	mA
GNSS Power Consumption[2]			
GNSS Track Mode	The receiver is tracking and not searching for satellites in order to save power after 3D fix. This mode has optimized power for navigation.	18	mA
GNSS Low Power Mode	• GNSS On-Sleep duty cycle operation within 1 second to save power.	7	mA

[2] Only for MT2523G

Power mode	Test Conditions	Typical	Unit

	• Supports dynamic duty operation to balance performance and power consumption.
	• Automatically return to normal mode
	  ○ when in difficult environment to maintain accuracy. Minimum SNR to enter duty cycle operation is about 21dB.
	  ○ when decoding the navigation message is requested.		

6.5. Peripheral constraints and voltage for power mode

Table 6.5-1 and Table 6.5-2 list the operation state of peripherals in the always-on and power-down domains.

Table 6.5-1. Always-on power domain peripherals

Peripheral	High/Full/Low-speed Mode	Wakeup Source for Sleep and DeepSleep modes
eFUSE	Mandatory, VCORE = 1.2V	-
Always-on DMA controller	O	-
MIPI	Mandatory, VCORE ≥ 1.1V	-
Keypad Scanner	O	O
GPC	O	O
GPT	O	O
PWM (0, 1)	O	-
Display PWM	O	-
GPDAC	O	-
ACCDET	O	O

Table 6.5-2. INFRA_PD power-down domain peripherals

Module Description	High/Full/Low-speed Mode	Wakeup Source for Sleep and DeepSleep mode
Power-down DMA controller	O	-
TRNG	O	-
SDIO (0, 1)	O	O
Serial flash	O	-

Module Description	High/Full/Low-speed Mode	Wakeup Source for Sleep and DeepSleep mode
PSRAM controller	O	-
UART (0, 1, 2, 3)	O	O
SPI_MASTER (0, 1, 2, 3)	O	-
SPI_SLAVE	O	O
PWM (2, 3, 4, 5)	O	-
I2C (0, 1, 2)	O	-
AUXADC	O	O
USB controller	Mandatory, VCORE ≥ 1.2V	O

- The wakeup source for peripherals, such as UART, is from IO. When an interrupt is detected, the sleep controller turns on the CPU_PD and INFRA_PD MTCMOS domains by default.
- There are voltage constraints for VCORE for eFUSE, MIPI and USB. The voltage control is software configurable.

7. Pin Description

7.1. MT2523G ball diagram

For MT2523G, a TFBGA 9.2mm*6mm, 246-ball, 0.4mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 7-1.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	<DUMMY_NET>	BATSNS	ISENSE	VCDT		GPO_1		DVDD_GPO	XTAL1	XTAL2	EXT_CLK_SEL	BT_LNA	AVDD13_BTRF	AVDD_VBT	GPIO_C4	DVDD_VIO_C		CMCSK	CMCSD1		GPS_AVSS43_DCV	<DUMMY_NET>	A
B	VDRV	TESTMODE	AVDD18_AUXADC	AVSS_VREF	VREF	GPO_3	UTXD0	URXD0		GPIO_C3		AVSS_BT	GPIO_B2		GPIO_A1	CMCSD0	CMRST	CMPDN	CMMCLK	GPO_2	GPS_AVDD43_DCV	GPS_AVDD11_CLDO	B
C		BATON	VBT	AVDD33_USB	PWRKEY	SRCLKENAI	AVDD18_DCXO	FREF		GPIO_B5	AVSS_BT	AVSS_BT	GPIO_C1		GPIO_A4			GPIO_A0	GPS_DVSS11_CORE	GPS_DCV_FB	GPS_DCV	GPS_AVSS11_CLDO	C
D	ISINK	CHRLDO	USB_DP	AVSS33_USB				DVDD_VIO_B	GPIO_B4	GPIO_B1		AVSS_BT	GPIO_C2	GPIO_C0	GPIO_A2	GPIO_A3	GPIO_A5		GPS_AVDD43_RTC	GPS_FORCE_ON	DVDD_VIO_A	GPS_AVDD28_CLDO	D
E	VSF	VMC	USB_DM	AVSS28_MIPI		USB_VRT	AVSS_PMU	AVSS_PMU	AVSS_DCXO	GPIO_B3	GPIO_B0	AVSS_BT	SDA0	SCL0	DVDD_VSF	GPS_TX1	GPS_32K_OUT					GPS_AVDD28_TLDO	E
F	VBAT_LDOS2	VBATSW	AVDD28_MIPI	TDN			AVSS_PMU	GND	GND	GND	GND	GND	GND	GND	GND	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS11_CORE		GPS_OSC	GPS_AVDD11_RTC	GPS_AVDD_TCXO_SW	F
G	VCAMA			TDP				GND	GND	GND	GND	GND	GND	GND	GND	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVDD11_CORE1	GPS_JCK	GPS_RX1	GPS_AVSS43_MISC	GPS_AVDD43_VBAT	G
H	VIBR	VA28	VDDK		TCN			AVSS_PMU	GND	GND	GND	GND	GND	GND	GND	GPS_DVSS11_CORE	GPS_DVSS11_CORE			GPS_DVDD28_IO1		GPS_VREF	H
J	VUSB33			TVRT	TCP			AVSS_PMU	AVSS_PMU	GND		GND	GND	GND	GND	GPS_DVSS11_CORE	GPS_DVSS28_IO	GPS_TX2		GPS_DVDD28_SF	GPS_DVSS28_SF		J
K	VSWMP	VIO28	VA18		AVSS28_ABB	AU_HSP	AU_HSN		DVDD18_VIO18	GND	VDDK	DVDD18_VSWXM	LSCE_B	LSRSTB	GND	GPS_JDI	GPS_SCK1				GPS_XIN	GPS_XOUT	K
L	VBAT_LDOS1	VSWDP	VIO18	AVSS_VREF	AVSS28_ABB	AVSS28_HP	SYSRSTB_IN	AUXADCIN_4	FSOURCE_A	GPO_0	RESETB_OUT	LSDA	LSCK	LSA0			GPS_JRCK	GPS_RX2	GPS_DVDD11_CORE2	GPS_T1P	GPS_T1N	GPS_AVDD18_CM	L
M	VSWXM	AU_HPR	AVDD28_ABB	AUD_VREF	ACCDET	GPDAC		AUXADCIN_2	FSOURCE_D		AUXADCIN_3	AUXADCIN_1		DVDD_VIO_B	LPTE	GPS_TX0		GPS_RX0	GPS_XTEST		GPS_HRST_B	GPS_AVDD18_RXFE	M
N	VCORE_LDO	AU_HPL	AU_VIN1_N	AU_VIN1_P	AU_MICBIAS0	VCORE_FB	VBAT_BUCK_CTRL	AUXADCIN_0	VDIG18	MCDA3	MCDA2	MCDA1	MCCM0	AVDD_RTC	XIN	RTC_XOSC32_ENB	GPS_JRST_	GPS_JMS	GPS_EINT0	GPS_EINT1		GPS_RFIN	N
P	<DUMMY_NET>	AU_VIN0_N	AU_VIN0_P		<DUMMY_NET>	VBAT_VCORE	VCORE_BUCK		GND_VCORE	MCCK		MCDA0	DVDD33_VMC		XOUT		GPS_SCS1_	GPS_JDO		GPS_DVDD28_IO2	GPS_AVSS_RF	<DUMMY_NET>	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 7-1. MT2523G ball diagram and top view

7.1.1. MT2523G pin coordination

Table 7.1-1. MT2523G pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	<DUMMY_NET>	E3	USB_DM	K2	VIO28
A10	XTAL2	E4	AVSS28_MIPI	K21	GPS_XIN
A11	EXT_CLK_SEL	E6	USB_VRT	K22	GPS_XOUT
A12	BT_LNA	E7	AVSS_PMU	K3	VA18
A13	AVDD13_BTRF	E8	AVSS_PMU	K5	AVSS28_ABB
A14	AVDD_VBT	E9	AVSS_DCXO	K6	AU_HSP
A15	GPIO_C4	F1	VBAT_LDOS2	K7	AU_HSN
A16	DVDD_VIO_C	F10	GND	K9	DVDD18_VIO18
A18	CMCSK	F11	GND	L1	VBAT_LDOS1
A19	CMCSD1	F12	GND	L10	GPO_0

Pin#	Net name	Pin#	Net name	Pin#	Net name
A2	BATSNS	F13	GND	L11	RESETB_OUT
A21	GPS_AVSS43_DCV	F14	GND	L12	LSDA
A22	<DUMMY_NET>	F15	GND	L13	LSCK
A3	ISENSE	F16	GPS_DVSS11_CORE	L14	LSA0
A4	VCDT	F17	GPS_DVSS11_CORE	L17	GPS_JRCK
A6	GPO_1	F18	GPS_DVSS11_CORE	L18	GPS_RX2
A8	DVDD_GPO	F2	VBATSW	L19	GPS_DVDD11_CORE2
A9	XTAL1	F20	GPS_OSC	L2	VSWDP
B1	VDRV	F21	GPS_AVDD11_RTC	L20	GPS_T1P
B10	GPIO_C3	F22	GPS_AVDD_TCXO_SW	L21	GPS_T1N
B12	AVSS_BT	F3	AVDD28_MIPI	L22	GPS_AVDD18_CM
B13	GPIO_B2	F4	TDN	L3	VIO18
B15	GPIO_A1	F7	AVSS_PMU	L4	AVSS_VREF
B16	CMCSD0	F8	GND	L5	AVSS28_ABB
B17	CMRST	F9	GND	L6	AVSS28_HP
B18	CMPDN	G1	VCAMA	L7	SYSRSTB_IN
B19	CMMCLK	G10	GND	L8	AUXADCIN_4
B2	TESTMODE	G11	GND	L9	FSOURCE_A
B20	GPO_2	G12	GND	M1	VSWXM
B21	GPS_AVDD43_DCV	G13	GND	M11	AUXADCIN_3
B22	GPS_AVDD11_CLDO	G14	GND	M12	AUXADCIN_1
B3	AVDD18_AUXADC	G15	GND	M14	DVDD_VIO_B
B4	AVSS_VREF	G16	GPS_DVSS11_CORE	M15	LPTE
B5	VREF	G17	GPS_DVSS11_CORE	M16	GPS_TX0
B6	GPO_3	G18	GPS_DVDD11_CORE1	M18	GPS_RX0
B7	UTXD0	G19	GPS_JCK	M19	GPS_XTEST
B8	URXD0	G20	GPS_RX1	M2	AU_HPR
C10	GPIO_B5	G21	GPS_AVSS43_MISC	M21	GPS_HRST_B
C11	AVSS_BT	G22	GPS_AVDD43_VBAT	M22	GPS_AVDD18_RXFE
C12	AVSS_BT	G4	TDP	M3	AVDD28_ABB
C13	GPIO_C1	G8	GND	M4	AUD_VREF
C15	GPIO_A4	G9	GND	M5	ACCDET
C18	GPIO_A0	H1	VIBR	M6	GPDAC
C19	GPS_DVSS11_CORE	H10	GND	M8	AUXADCIN_2
C2	BATON	H11	GND	M9	FSOURCE_D
C20	GPS_DCV_FB	H12	GND	N1	VCORE_LDO
C21	GPS_DCV	H13	GND	N10	MCDA3
C22	GPS_AVSS11_CLDO	H14	GND	N11	MCDA2
C3	VBT	H15	GND	N12	MCDA1

Pin#	Net name	Pin#	Net name	Pin#	Net name
C4	AVDD33_USB	H16	GPS_DVSS11_CORE	N13	MCCM0
C5	PWRKEY	H17	GPS_DVSS11_CORE	N14	AVDD_RTC
C6	SRCLKENAI	H2	VA28	N15	XIN
C7	AVDD18_DCXO	H20	GPS_DVDD28_IO1	N16	RTC_XOSC32_ENB
C8	FREF	H22	GPS_VREF	N17	GPS_JRST_
D1	ISINK	H3	VDDK	N18	GPS_JMS
D10	GPIO_B1	H5	TCN	N19	GPS_EINT0
D12	AVSS_BT	H8	AVSS_PMU	N2	AU_HPL
D13	GPIO_C2	H9	GND	N20	GPS_EINT1
D14	GPIO_C0	J1	VUSB33	N22	GPS_RFIN
D15	GPIO_A2	J10	GND	N3	AU_VIN1_N
D16	GPIO_A3	J12	GND	N4	AU_VIN1_P
D17	GPIO_A5	J13	GND	N5	AU_MICBIAS0
D19	GPS_AVDD43_RTC	J14	GND	N6	VCORE_FB
D2	CHRLDO	J15	GND	N7	VBAT_BUCK_CTRL
D20	GPS_FORCE_ON	J16	GPS_DVSS11_CORE	N8	AUXADCIN_0
D21	DVDD_VIO_A	J17	GPS_DVSS28_IO	N9	VDIG18
D22	GPS_AVDD28_CLDO	J18	GPS_TX2	P1	<DUMMY_NET>
D3	USB_DP	J20	GPS_DVDD28_SF	P10	MCCK
D4	AVSS33_USB	J21	GPS_DVSS28_SF	P12	MCDA0
D8	DVDD_VIO_B	J4	TVRT	P13	DVDD33_VMC
D9	GPIO_B4	J5	TCP	P15	XOUT
E1	VSF	J8	AVSS_PMU	P17	GPS_SCS1_
E10	GPIO_B3	J9	AVSS_PMU	P18	GPS_JDO
E11	GPIO_B0	K1	VSWMP	P2	AU_VIN0_N
E12	AVSS_BT	K10	GND	P20	GPS_DVDD28_IO2
E13	SDA0	K11	VDDK	P21	GPS_AVSS_RF
E14	SCL0	K12	DVDD18_VSWXM	P22	<DUMMY_NET>
E15	DVDD_VSF	K13	LSCE_B	P3	AU_VIN0_P
E16	GPS_TX1	K14	LSRSTB	P5	<DUMMY_NET>
E17	GPS_32K_OUT	K15	GND	P6	VBAT_VCORE
E2	VMC	K16	GPS_JDI	P7	VCORE_BUCK
E22	GPS_AVDD28_TLDO	K17	GPS_SCK1	P9	GND_VCORE

7.2. MT2523D and MT2523S ball diagram

For MT2523D and MT2523S, a TFBGA 6.2mm x 5.8mm, 165-ball, 0.4mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 7-2.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	BATSNS	ISENSE	VCDT		DVDD_GPO	GPO_1		XTAL1	XTAL2	EXT_CLK_SEL	BT_LNA	AVDD13_BTRF		AVDD_VBT	GPIO_C1	A
B	VDRV	TESTMODE	AVSS_VREF	VREF	AVDD18_AUXADC	GPO_3	UTXD0	URXD0	FREF	AVSS_BT	AVSS_BT	GPIO_C4	GPIO_C2	GPIO_C0	DVDD_VIO_C	B
C		BATON	VBT	AVDD33_USB	PWRKEY	SRCLKENAI		AVDD18_DCXO		AVSS_BT	AVSS_BT	CMCSD0		SDA0		C
D	ISINK	CHRLDO	USB_DP	AVSS33_USB					AVSS_DCXO	AVSS_BT	GPIO_C3	CMMCLK	CMCSK	SCL0	CMCSD1	D
E	VSF	VMC	USB_DM	AVSS28_MIPI		USB_VRT	AVSS_PMU		AVSS_BT		GPO_2	CMPDN	CMRST	DVDD_VSF	DVDD_VIO_A	E
F	VBAT_LDOS2	VBATSW	VIBR	TDN			AVSS_PMU	GND	GND	GND		GND		GPIO_A2		F
G	VCAMA		VDDK	TDP			AVSS_PMU	GND	GND	GND	GPIO_B2	GPIO_A4	GPIO_A3	GPIO_A0	GPIO_A1	G
H	VA28		AVDD28_MIPI	TVRT	TCN		AVSS_PMU	AVSS_PMU	GND	GND	GPIO_B5	GPIO_A5		GPIO_B0	DVDD_VIO_B	H
J	VUSB33	VA18			TCP		AU_HSP	AVSS_PMU	AVSS_PMU	GND	GPIO_B4			GPIO_B3		J
K	VSWMP	VIO28				AVSS28_HP	AU_HSN	AVSS_PMU	LPTE		RESETB_OUT	GPO_0	GPIO_B1	DVDD18_VSWXM	VDDK	K
L	VBAT_LDOS1	VSWDP	VIO18	AVSS_VREF		AVSS28_ABB	ACCDET	AUXADCIN_4	LSCE_B	LSA0	GND	LSCK		LSDA	FSOURCE_D	L
M	VSWXM	AU_HPR	AVDD28_ABB	AUD_VREF	<DUMMY_NET>	GPDAC		AUXADCIN_2	LSRSTB		DVDD18_VIO18	FSOURCE_A	AVDD_RTC	AUXADCIN_3		M
N	VCORE_LDO	AU_HPL	AU_VIN1_P	AU_MICBIAS0	VCORE_FB	VBAT_BUCK_CTRL		AUXADCIN_0	SYSRSTB_IN	MCCK	MCDA1	MCDA0	MCCM0	AUXADCIN_1	RTC_XOSC32_ENB	N
P	AU_VIN0_N	AU_VIN0_P	AU_VIN1_N		VBAT_VCORE	VCORE_BUCK	GND_VCORE	VDIG18		MCDA3	MCDA2		DVDD33_VMC	XOUT	XIN	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 7-2. MT2523D and MT2523S ball diagram and top view

7.2.1. MT2523D and MT2523S pin coordination

Table 7.2-1. MT2523D and MT2523S pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
BATSNS	A1	USB_DM	E3	AVSS28_HP	K6
EXT_CLK_SEL	A10	AVSS28_MIPI	E4	AU_HSN	K7
BT_LNA	A11	USB_VRT	E6	AVSS_PMU	K8
AVDD13_BTRF	A12	AVSS_PMU	E7	LPTE	K9
AVDD_VBT	A14	AVSS_BT	E9	VBAT_LDOS1	L1
GPIO_C1	A15	VBAT_LDOS2	F1	LSA0	L10
ISENSE	A2	GND	F10	GND	L11
VCDT	A3	GND	F12	LSCK	L12
DVDD_GPO	A5	GPIO_A2	F14	LSDA	L14
GPO_1	A6	VBATSW	F2	FSOURCE_D	L15
XTAL1	A8	VIBR	F3	VSWDP	L2
XTAL2	A9	TDN	F4	VIO18	L3

Pin#	Net name	Pin#	Net name	Pin#	Net name
VDRV	B1	AVSS_PMU	F7	AVSS_VREF	L4
AVSS_BT	B10	GND	F8	AVSS28_ABB	L6
AVSS_BT	B11	GND	F9	ACCDET	L7
GPIO_C4	B12	VCAMA	G1	AUXADCIN_4	L8
GPIO_C2	B13	GND	G10	LSCE_B	L9
GPIO_C0	B14	GPIO_B2	G11	VSWXM	M1
DVDD_VIO_C	B15	GPIO_A4	G12	DVDD18_VIO18	M11
TESTMODE	B2	GPIO_A3	G13	FSOURCE_A	M12
AVSS_VREF	B3	GPIO_A0	G14	AVDD_RTC	M13
VREF	B4	GPIO_A1	G15	AUXADCIN_3	M14
AVDD18_AUXADC	B5	VDDK	G3	AU_HPR	M2
GPO_3	B6	TDP	G4	AVDD28_ABB	M3
UTXD0	B7	AVSS_PMU	G7	AUD_VREF	M4
URXD0	B8	GND	G8	<DUMMY_NET>	M5
FREF	B9	GND	G9	GPDAC	M6
AVSS_BT	C10	VA28	H1	AUXADCIN_2	M8
AVSS_BT	C11	GND	H10	LSRSTB	M9
CMCSD0	C12	GPIO_B5	H11	VCORE_LDO	N1
SDA0	C14	GPIO_A5	H12	MCCK	N10
BATON	C2	GPIO_B0	H14	MCDA1	N11
VBT	C3	DVDD_VIO_B	H15	MCDA0	N12
AVDD33_USB	C4	AVDD28_MIPI	H3	MCCM0	N13
PWRKEY	C5	TVRT	H4	AUXADCIN_1	N14
SRCLKENAI	C6	TCN	H5	RTC_XOSC32_ENB	N15
AVDD18_DCXO	C8	AVSS_PMU	H7	AU_HPL	N2
ISINK	D1	AVSS_PMU	H8	AU_VIN1_P	N3
AVSS_BT	D10	GND	H9	AU_MICBIAS0	N4
GPIO_C3	D11	VUSB33	J1	VCORE_FB	N5
CMMCLK	D12	GND	J10	VBAT_BUCK_CTRL	N6
CMCSK	D13	GPIO_B4	J11	AUXADCIN_0	N8
SCL0	D14	GPIO_B3	J14	SYSRSTB_IN	N9
CMCSD1	D15	VA18	J2	AU_VIN0_N	P1
CHRLDO	D2	TCP	J5	MCDA3	P10
USB_DP	D3	AU_HSP	J7	MCDA2	P11
AVSS33_USB	D4	AVSS_PMU	J8	DVDD33_VMC	P13
AVSS_DCXO	D9	AVSS_PMU	J9	XOUT	P14
VSF	E1	VSWMP	K1	XIN	P15
GPO_2	E11	RESETB_OUT	K11	AU_VIN0_P	P2
CMPDN	E12	GPO_0	K12	AU_VIN1_N	P3

Pin#	Net name	Pin#	Net name	Pin#	Net name
CMRST	E13	GPIO_B1	K13	VBAT_VCORE	P5
DVDD_VSF	E14	DVDD18_VSWXM	K14	VCORE_BUCK	P6
DVDD_VIO_A	E15	VDDK	K15	GND_VCORE	P7
VMC	E2	VIO28	K2	VDIG18	P8

7.3. MT2523 series pins

Table 7.3-1. Acronym for pin types and I/O structure

Name	Abbreviation	Description
Pin Type	AI	Analog input
	AO	Analog output
	AIO	Analog bi-direction
	DI	Digital input
	DO	Digital output
	DIO	Digital bi-direction
	P	Power
	G	Ground
IO Structure	TYPE0	pull-up/down
	TYPE1	pull-up/down, 3.63V tolerance
	TYPE2	pull-up/down, Keypad scan (column) 3.63V tolerance
	TYPE3	pull-up/down, Keypad scan (row) 3.63V tolerance
	TYPE4	pull-up/down, AUXADC input, 3.63V tolerance
	TYPE5	Dedicated input I/O with weak pull-up resistor
	TYPE6	Dedicated input I/O with weak pull-down resistor

Table 7.3-2. MT2523 series pin function description and power domain (group1)

Pin Number		Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
MT2523G	MT2523D MT2523S						
System							
L11	K11	RESETB_OUT	DO	TYPE1	System reset output	-	DVDD18_VIO18
C6	C6	SRCLKENAI	DI	TYPE1	26MHz clock request by external devices	-	DVDD_GPO
L7	N9	SYSRSTB_IN	DI	TYPE5	System reset input	-	VIO18
General purpose I/O – Group A							
C18	G14	GPIO_A0	DIO	TYPE1	GPIO, Group A, Pin 0	SDIO (1), I2S Slave, UART (1), SPI_MASTER (0)	DVDD_VIO_A
B15	G15	GPIO_A1	DIO	TYPE1	GPIO, Group A, Pin 1	SDIO (1), I2S Slave, UART (1), SPI_MASTER (0)	DVDD_VIO_A
D15	F14	GPIO_A2	DIO	TYPE1	GPIO, Group A, Pin 2	SDIO (1), I2S Slave, UART (2), SPI_MASTER (0)	DVDD_VIO_A
D16	G13	GPIO_A3	DIO	TYPE1	GPIO, Group A, Pin 3	SDIO (1), I2S Slave, UART (2), SPI_MASTER (0)	DVDD_VIO_A
C15	G12	GPIO_A4	DIO	TYPE1	GPIO, Group A, Pin 4	SDIO (1), I2C (2)	DVDD_VIO_A
D17	H12	GPIO_A5	DIO	TYPE1	GPIO, Group A, Pin 5	SDIO (1), I2C (2)	DVDD_VIO_A
General purpose I/O – Group B							
E11	H14	GPIO_B0	DIO	TYPE3	GPIO, Group B, Pin 0, with KEYPAD function	Keypad Scanner, UART (1,3), CM4 JTAG	DVDD_VIO_B
D10	K13	GPIO_B1	DIO	TYPE3	GPIO, Group B, Pin 1, with KEYPAD function	Keypad Scanner, I2C (2), CM4 JTAG	DVDD_VIO_B
B13	G11	GPIO_B2	DIO	TYPE3	GPIO, Group B, Pin 2, with KEYPAD function	Keypad Scanner, I2C (2)	DVDD_VIO_B
E10	J14	GPIO_B3	DIO	TYPE2	GPIO, Group B, Pin 3, with KEYPAD function	Keypad Scanner, GPCOUNTER (0),	DVDD_VIO_B

Pin Number		Pin Name	Pin	IO	Pin Description	Alternate	Power domain
						CM4 JTAG	
D9	J11	GPIO_B4	DIO	TYPE2	GPIO, Group B, Pin 4, with KEYPAD function	Keypad Scanner, UART (1,3), CM4 JTAG	DVDD_VIO_B
C10	H11	GPIO_B5	DIO	TYPE2	GPIO, Group B, Pin 5, with KEYPAD function	Keypad Scanner, CM4 JTAG	DVDD_VIO_B
General purpose I/O – Group C							
D14	B14	GPIO_C0	DIO	TYPE1	GPIO, Group C, Pin 0	I2S Master, I2S Slave, PWM (0), SPI_MASTER (1)	DVDD_VIO_C
C13	A15	GPIO_C1	DIO	TYPE1	GPIO, Group C, Pin 1	I2S Master, I2S Slave, PWM (1), SPI_MASTER (1)	DVDD_VIO_C
D13	B13	GPIO_C2	DIO	TYPE1	GPIO, Group C, Pin 2	I2S Master, I2S Slave, PWM (2), SPI_MASTER (1)	DVDD_VIO_C
B10	D11	GPIO_C3	DIO	TYPE1	GPIO, Group C, Pin 3	I2S Master, I2S Slave, PWM (3), SPI_MASTER (1)	DVDD_VIO_C
A15	B12	GPIO_C4	DIO	TYPE1	GPIO, Group C, Pin 4	PWM (4)	DVDD_VIO_C
General purpose I/O with AUXADC input channel							
N8	N8	AUXADCIN_0	DIO	TYPE4	GPIO with AUXADX input channel 0	AUXADCIN (0), UART (2), PWM (0), SPI_MASTER (0,1), I2S Master	DVDD_VIO_B
M12	N14	AUXADCIN_1	DIO	TYPE4	GPIO with AUXADX input channel 1	AUXADCIN (1), UART (2), PWM (1), SPI_MASTER (0,1), I2S Master	DVDD_VIO_B
M8	M8	AUXADCIN_2	DIO	TYPE4	GPIO with AUXADX input channel 2	AUXADCIN (2), UART (3), SPI_MASTER (0,1), I2S Master	DVDD_VIO_B
M11	M14	AUXADCIN_3	DIO	TYPE4	GPIO with AUXADX input channel 3	AUXADCIN (3),	DVDD_VIO_B

Pin Number		Pin Name	Pin	IO	Pin Description	Alternate	Power domain
						UART (3), SPI_MASTER (0,1), I2S Master	
L8	L8	AUXADCIN_4	DIO	TYPE4	GPIO with AUXADX input channel 4	AUXADCIN (4)	DVDD_VIO_B
General purpose output							
L10	K12	GPO_0	DO	TYPE1	General purpose output, Pin 0	Display PWM	DVDD18_VIO18
A6	A6	GPO_1	DO	TYPE1	General purpose output, Pin 1	-	DVDD_GPO
B20	E11	GPO_2	DO	TYPE1	General purpose output, Pin 2	-	DVDD_VIO_A
B6	B6	GPO_3	DO	TYPE1	General purpose output, Pin 3	-	DVDD_GPO
UART interface							
B8	B8	URXD0	DIO	TYPE1	UART0 receive data	-	DVDD_GPO
B7	B7	UTXD0	DIO	TYPE1	UART0 transmit data	-	DVDD_GPO
Camera interface							
B17	E13	CMRST	DIO	TYPE1	CMOS sensor reset signal output	GPCOUNTER (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
B18	E12	CMPDN	DIO	TYPE1	CMOS sensor power down control	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
B16	C12	CMCSD0	DIO	TYPE1	CMOS sensor data input 0	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
A19	D15	CMCSD1	DIO	TYPE1	CMOS sensor data input 1	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
B19	D12	CMMCLK	DIO	TYPE1	CMOS sensor pixel clock input	PCM, SPI_MASTER (2,3), SPI_SLAVE (0),	DVDD_VIO_A

Pin Number		Pin Name	Pin	IO	Pin Description	Alternate	Power domain
						Cortex-M4 JTAG, SDIO (1)	
A18	D13	CMCSK	DIO	TYPE1	CMOS sensor pixel clock output	SDIO (1)	DVDD_VIO_A
SDIO interface							
P10	N10	MCCK	DIO	TYPE1	SD serial clock/memory stick serial clock	I2C (0,2), PWM (0), UART (1), SDIO (0)	DVDD33_VMC
N13	N13	MCCM0	DIO	TYPE1	SD command output/memory stick bus state output	I2C (0,2), PWM (1), UART (1), SDIO (0)	DVDD33_VMC
P12	N12	MCDA0	DIO	TYPE1	SD serial data IO 0/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
N12	N11	MCDA1	DIO	TYPE1	SD serial data IO 1/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
N11	P11	MCDA2	DIO	TYPE1	SD serial data IO 2/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
N10	P10	MCDA3	DIO	TYPE1	SD serial data IO 3/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
I2C interface							
E14	D14	SCL0	DIO	TYPE1	I2C clock pin of controller 0	-	DVDD_VIO_A
E13	C14	SDA0	DIO	TYPE1	I2C data pin of controller 0	-	DVDD_VIO_A
LCM interface							
K14	M9	LSRSTB	DIO	TYPE1	Serial display interface reset signal	I2C (1)	DVDD18_VIO18
K13	L9	LSCE_B	DIO	TYPE1	Serial display interface chip select output	I2C (1), SPI_MASTER (2)	DVDD18_VIO18
L13	L12	LSCK	DIO	TYPE1	Serial display interface clock	SPI_MASTER (2)	DVDD18_VIO18
L12	L14	LSDA	DIO	TYPE1	Serial display interface data	I2C (1),	DVDD18_VIO18

Pin Number		Pin Name	Pin	IO	Pin Description	Alternate	Power domain
						SPI_MASTER (2)	
L14	L10	LSA0	DIO	TYPE1	Serial display interface address	SPI_MASTER (2)	DVDD18_VIO18
M15	K9	LPTE	DIO	TYPE1	Serial display tearing signal	I2C (1)	DVDD18_VIO18

Table 7.3-3. MT2523 series pin function description and power domain (group2)

Pin#		Pin Name	Pin Type	Description	Power domain
MT2523G	MT2523D MT2523S				
Bluetooth					
A12	A11	BT_LNA	AIO	Bluetooth RF single-ended input	AVDD_VBT
Clock 26MHz DCXO					
C8	B9	FREF	AO	DCXO reference clock output	AVDD18_DCXO
A9	A8	XTAL1	AIO	Input 1 for DCXO crystal	AVDD18_DCXO
A10	A9	XTAL2	AIO	Input 2 for DCXO crystal	AVDD18_DCXO
A11	A10	EXT_CLK_SEL	AIO	DCXO mode selection	AVDD18_DCXO
USB					
E3	E3	USB_DM	AIO	D- data input/output	-
D3	D3	USB_DP	AIO	D+ data input/output	-
E6	E6	USB_VRT	AIO	USB reference voltage	-
Real-time clock					
N15	P15	XIN	AIO	Input pin for 32K crystal	AVDD_RTC
P15	P14	XOUT	AIO	Input pin for 32K crystal	AVDD_RTC
N16	N15	RTC_XOSC32_ENB	AIO	Pin option for external 32K crystal	AVDD_RTC
Analog baseband					
M2	M2	AU_HPR	AO	Audio head phone output (R channel)	AVDD28_ABB
N2	N2	AU_HPL	AO	Audio head phone output (L channel)	AVDD28_ABB
K6	J7	AU_HSP	AO	Voice handset output (positive)	AVDD28_ABB
K7	K7	AU_HSN	AO	Voice handset output (negative)	AVDD28_ABB
P3	P2	AU_VIN0_P	AI	Microphone 0 input (positive)	AVDD28_ABB
P2	P1	AU_VIN0_N	AI	Microphone 0 input (negative)	AVDD28_ABB
N4	N3	AU_VIN1_P	AI	Microphone 1 input (positive)	AVDD28_ABB
N3	P3	AU_VIN1_N	AI	Microphone 1 input (negative)	AVDD28_ABB
M4	M4	AUD_VREF	AI	Audio reference voltage	-
L4	B3 L4	AVSS_VREF	AI	Audio reference ground	-

Pin#		Pin Name	Pin Type	Description	Power domain
N5	N4	AU_MICBIAS0	AI	Microphone bias source 0	-
M6	M6	GPDAC	AO	General purpose DAC output	AVDD28_ABB
M5	L7	ACCDET	AI	Accessory detection	AVDD28_ABB
Power management unit					
K3	J2	VA18	AO	LDO output	VBAT_LDOS1
H2	H1	VA28	AO	LDO output for ABB	VBAT_LDOS2
G1	G1	VCAMA	AO	LDO output for camera	VBAT_LDOS2
H1	F3	VIBR	AO	LDO output for vibrator	VBAT_LDOS2
L3	L3	VIO18	AO	LDO output	VBAT_LDOS1
K2	K2	VIO28	AO	LDO output	VBAT_LDOS1
E2	E2	VMC	AO	LDO output for memory card	VBAT_LDOS2
E1	E1	VSF	AO	LDO output	VBAT_LDOS2
C3	C3	VBT	AO	LDO output	VBAT_LDOS2
N9	P8	VDIG18	AO	LDO output for RTC, PMU digital part	VBAT_LDOS1
K1	K1	VSWMP	AO	LDO output	VBATSW
M1	M1	VSWXM	AO	LDO output	VBATSW
J1	J1	VUSB33	AO	LDO output for USB	VBAT_LDOS1
N1	N1	VCORE_LDO	AO	LDO output for digital core circuit	VBAT_LDOS1
D1	D1	ISINK	AI	Backlight driver channel 0	VBAT_LDOS2
P7	P6	VCORE_BUCK	AO	VCORE BUCK output	VBAT_VCORE
N6	N5	VCORE_FB	AI	VCORE BUCK feedback	VBAT_VCORE
N7	N6	VBAT_BUCK_CTRL	AI	VCORE BUCK control	VBAT_VCORE
B5	B4	VREF	AO	Band gap reference	BATSNS
B4 L4	B3 L4	AVSS_VREF	AO	Band gap reference ground	BATSNS
A4	A3	VCDT	AI	Charger-In level sense pin	BATSNS
B1	B1	VDRV	AO	IDAC current output open-drain pin	BATSNS
C2	C2	BATON	AI	Battery Pack, NTC connected pin	BATSNS
A3	A2	ISENSE	AO	Top node of current sensing 0.2Ω Rsense resistor	BATSNS
D2	D2	CHRLDO	AO	2.8V shunt-regulator output	BATSNS
B2	B2	TESTMODE	AI	Test mode	BATSNS
C5	C5	PWRKEY	AI	PWR key	BATSNS
A2	A1	BATSNS	P	Battery node of battery pack	-
F2	F2	VBATSW	P	Battery switch output	-
L1	L1	VBAT_LDOS1	P	Battery input for LDOS1 group	-
F1	F1	VBAT_LDOS2	P	Battery input for LDOS2 group	-
P6	P5	VBAT_VCORE	P	Battery input for VCORE BUCK	-

Pin#		Pin Name	Pin Type	Description	Power domain
P9	P7	GND_VCORE	G	Ground for VCORE BUCK	-
Analog power					
C4	C4	AVDD33_USB	P	USB 3.3V power input	-
F3	H3	AVDD28_MIPI	P	MIPI 2.8V power input	-
M3	M3	AVDD28_ABB	P	ABB 2.8V power input	-
A14	A14	AVDD_BT	P	BTRF power input	-
A13	A12	AVDD13_BTRF	P	BTRF 1.3V power input	-
C7	C8	AVDD18_DCXO	P	DCXO 1.8V power input	-
B3	B5	AVDD18_AUXADC	P	PMU AUXADC power input	-
N14	M13	AVDD_RTC	P	RTC power input	-
Analog ground					
D4	D4	AVSS33_USB	G	USB ground	-
E4	E4	AVSS28_MIPI	G	MIPI ground	-
K5 L5	L6	AVSS28_ABB	G	ABB ground	-
L6	K6	AVSS28_HP	G	ABB headphone ground	-
B12 C11 C12 D12 E12	B10 B11 C10 C11 D10 E9	AVSS_BT	G	BT ground	-
E9	D9	AVSS_DCXO	G	DCXO ground	-
E7 E8 F7 H8 J8 J9	E7 F7 G7 H7 H8 J8 J9 K8	AVSS_PMU	G	PMU ground	-
Digital IO power					
D21	E15	DVDD_VIO_A	P	Power input of GPIO group A	-
D8 M12	H15	DVDD_VIO_B	P	Power input of GPIO group B	-
A	B15	DVDD_VIO_C	P	Power input of GPIO group C	-
A8	A5	DVDD_GPO	P	Power input of GPO group	-
K9	M11	DVDD18_VIO18	P	Power input of LCM and VIO18 IO	-
P13	P13	DVDD33_VMC	P	Power input of MSDC IO	-
E15	E14	DVDD_VSF	P	Power input of serial flash IO	-

Pin#		Pin Name	Pin Type	Description	Power domain
K12	K14	DVDD18_VSWXM	P	Power input of SIP PSRAM	-
Digital core power					
H3 K11	G3 K15	VDDK	P	Core power	-
eFUSE power					
M9	L15	FSOURCE_D	P	EFUSE power input of digital	-
L9	M12	FSOURCE_A	P	EFUSE power input of PMU	-
Digital ground					
-	-	GND	G	Ground	-

Table 7.3-4. Pins for GNSS module functionality (MT2523G only)

Pin# MT2523G	Pin Name	Pin Type	IO Structure	Description	Power Domain
System interface					
M21	GPS_HRST_B	DI	TYPE5	System reset. Active low Default: pull-up	GPS_DVDD28_IO2
M19	GPS_XTEST	DI	TYPE6	Test mode. Must be kept low in normal mode. Default: pull-down	GPS_DVDD28_IO2
Peripheral interface					
M18	GPS_RX0	DIO	TYPE0	Serial input for UART 0 Default: pull-up Default: 8mA driving	GPS_DVDD28_IO1
M16	GPS_TX0	DIO	TYPE0	Serial output for UART 0 Default: pull-up Default: 8mA driving	GPS_DVDD28_IO1
G20	GPS_RX1	DIO	TYPE0	Serial input for UART 1 Default: pull-up Default: 8mA driving	GPS_DVDD28_IO1
E16	GPS_TX1	DIO	TYPE0	Serial output for UART 1 Default: pull-up Default: 8mA driving	GPS_DVDD28_IO1
L18	GPS_RX2	DIO	TYPE0	Serial input for UART 2 Default: pull-up Default: 8mA driving	GPS_DVDD28_IO1
J18	GPS_TX2	DIO	TYPE0	Serial output for UART 2 Default: pull-up Default: 8mA driving Strap pin `tcxo_sw_sel` 1'b0: AVDD_TCXO_SW output	GPS_DVDD28_IO1

Pin# MT2523G	Pin Name	Pin Type	IO Structure	Description	Power Domain
				1.8V 1'b1: AVDD_TCXO_SW output 2.8V	
K17	GPS_SCK1	DIO	TYPE0	SPI clock output Default: pull-up Default: 8mA driving Strap pin `clk_sel[0]` `Clk_sel[1:0]` Mode 2'b00: XTAL mode 2'b01: External clock mode 2'b10: TCXO mode 2'b11: 16.368MHz TCXO mode	GPS_DVDD28_IO1
P17	GPS_SCS1_	DIO	TYPE0	SPI slave selection 1 Default: pull-up Default: 8mA driving Strap pin `clk_sel[1]`	GPS_DVDD28_IO2
G19	GPS_JCK	DIO	TYPE0	JTAG interface clock Default: pull-down Default: 8mA driving	GPS_DVDD28_IO1
N18	GPS_JMS	DIO	TYPE0	JTAG interface mode selection Default: pull-down Default: 8mA driving	GPS_DVDD28_IO2
K16	GPS_JDI	DIO	TYPE0	JTAG interface data input. Default: pull-down Default: 8mA driving	GPS_DVDD28_IO1

7.4. MT2523 series pin multiplexing

MT2523 series platform offers 48 GPIO pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on the pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count. To facilitate application use, the software can configure the clock to send outside the chip. There are six clock-out ports embedded in 48 GPIO pins and each clock-out can be programmed to output an appropriate clock source. Besides, when two GPIOs function for the same peripheral IP, the smaller GPIO serial number has higher priority than the one with larger number.

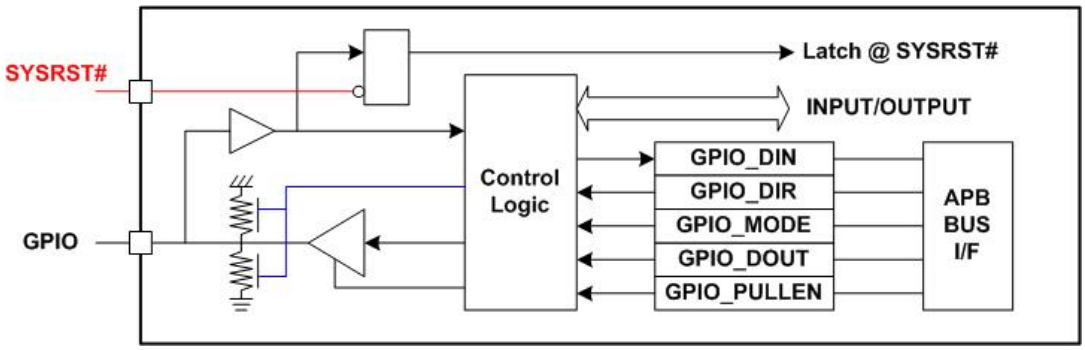


Figure 7-3. GPIO block diagram

MT2523 series has rich peripheral functions and the peripheral signals are shown as the table. The SDIO, SPI Master and SPI Slave can support signal group allocate on different pins.

Alternate Function	Signal List
SDIO (0)	MC0_CK MC0_CM0 MC0_DA0 MC0_DA1 MC0_DA2 MC0_DA3
SDIO (1)	MC1_A_CK MC1_A_CM0 MC1_A_DA0 MC1_A_DA1 MC1_A_DA2 MC1_A_DA3
	MC1_B_DA3 MC1_B_DA2 MC1_B_CM0 MC1_B_CK MC1_B_DA0 MC1_B_DA1

Alternate Function	Signal List
UART (0)	URXD0 UTXD0
UART (1)	URXD1 UTXD1
UART (2)	URXD2 UTXD2
UART (3)	URXD3 UTXD3
I2C (0)	SCL0 SDA0
I2C (1)	SCL1 SDA1
I2C (2)	SCL2 SDA2
I2S Master	MA_EDIDO MA_EDIDI MA_EDIWS MA_EDICK

Alternate Function	Signal List
SPI_MASTER (0)	MA_SPI0_A_CS MA_SPI0_A_SCK MA_SPI0_A_MOSI MA_SPI0_A_MISO
	MA_SPI0_B_CS MA_SPI0_B_SCK MA_SPI0_B_MOSI MA_SPI0_B_MISO
SPI_MASTER (1)	MA_SPI1_A_CS MA_SPI1_A_SCK MA_SPI1_A_MOSI MA_SPI1_A_MISO
	MA_SPI1_B_CS MA_SPI1_B_SCK MA_SPI1_B_MOSI MA_SPI1_B_MISO
SPI_MASTER (2)	MA_SPI2_A_CS MA_SPI2_A_SCK MA_SPI2_A_MOSI MA_SPI2_A_MISO
SPI_MASTER (3)	MA_SPI3_A_CS MA_SPI3_A_SCK MA_SPI3_A_MOSI MA_SPI3_A_MISO
	MA_SPI3_B_CS MA_SPI3_B_SCK MA_SPI3_B_MOSI MA_SPI3_B_MISO
SPI_SLAVE (0)	SLV_SPI0_CS SLV_SPI0_SCK SLV_SPI0_MOSI SLV_SPI0_MISO
PCM	DAISYNC DAIPCMIN DAICLK DAIPCMOUT

Alternate Function	Signal List
I2S Slave	SLA_EDIDO SLA_EDIDI SLA_EDIWS SLA_EDICK
PWM (0)	PWM0
PWM (1)	PWM1
PWM (2)	PWM2
PWM (3)	PWM3
PWM (4)	PWM4
PWM (5)	PWM5
Camera Interface	CMRST CMPDN CMCSD0 CMCSD1 CMMCLK CMCSK
LCM Interface	LSRSTB LSCE_B LSCK LSDA LSA0 LPTE
AUXADC	AUXADCIN_0 AUXADCIN_1 AUXADCIN_2 AUXADCIN_3 AUXADCIN_4
CM4 JTAG	JTDI JTMS JTCK JTRSTB JTDO

Table 7.4-1. PinMux description

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode 8	Mode 9
General purpose I/O – Group A										
GPIO_A0	GPIO4	EINT3	MC1_A_CK	SLA_EDIDO			URXD1	MA_SPI0_B_CS		
GPIO_A1	GPIO5	EINT4	MC1_A_CM0	SLA_EDIDI			UTXD1	MA_SPI0_B_SCK		
GPIO_A2	GPIO6	EINT5	MC1_A_DA0	SLA_EDIWS	URXD2			MA_SPI0_B_MOSI		
GPIO_A3	GPIO7	EINT6	MC1_A_DA1	SLA_EDICK	UTXD2		BT_BUCK_EN_HW	MA_SPI0_B_MISO		
GPIO_A4	GPIO8	EINT7	MC1_A_DA2				SCL2			
GPIO_A5	GPIO9	EINT8	MC1_A_DA3				SDA2			
General purpose I/O – Group B										
GPIO_B0	GPIO18	KCOL2	URXD1	URXD3			LSCE1_B1		JTDI	BTJTDI
GPIO_B1	GPIO19	KCOL1	EINT18	UART0_RTS	SCL2				JTMS	BTJTMS
GPIO_B2	GPIO20	KCOL0	GPSFSYNC	UART0_CTS	SDA2		MA_SPI2_CS1			
GPIO_B3	GPIO21	KROW2		GPCOUNTER_0	UART1_RTS (Out)				JTCK	BTJTCK
GPIO_B4	GPIO22	KROW1	UTXD1	UTXD3					JTDO	BTDBGIN
GPIO_B5	GPIO23	KROW0	EINT19	CLKO0	UART1_CTS (In)		MC_RST		JTRSTB	BTJTRSTB
General purpose I/O – Group C										
GPIO_C0	GPIO11	EINT9	BT_BUCK_EN_HW	MA_EDIDO	MA_SPI1_B_CS	PWM0	SLA_EDIDO			
GPIO_C1	GPIO12	EINT10		MA_EDIDI	MA_SPI1_B_SCK	PWM1	SLA_EDIDI			
GPIO_C2	GPIO13	EINT11	CLKO3	MA_EDIWS	MA_SPI1_B_MOSI	PWM2	SLA_EDIWS			
GPIO_C3	GPIO14	EINT12	CLKO4	MA_EDICK	MA_SPI1_B_MISO	PWM3	SLA_EDICK			
GPIO_C4	GPIO15	EINT13				PWM4				

General purpose I/O with AUXADC input channel										
AUXADCIN_0	GPIO0	EINT0	AUXADCIN_0	URXD2	PWM0	MA_SPI1_A_CS	MA_EDIDO	MA_SPI0_A_CS		BTJTDO
AUXADCIN_1	GPIO1	EINT1	AUXADCIN_1	UTXD2	PWM1	MA_SPI1_A_SCK	MA_EDIDI	MA_SPI0_A_SCK		BTDBGACKN
AUXADCIN_2	GPIO2	EINT2	AUXADCIN_2	URXD3	UART0_CTS (In)	MA_SPI1_A_MOSI	MA_EDIWS	MA_SPI0_A_MOSI		BT_BUCK_EN_HW
AUXADCIN_3	GPIO3	EINT14	AUXADCIN_3	UTXD3	UART0_RTS (Out)	MA_SPI1_A_MISO	MA_EDICK	MA_SPI0_A_MISO		BT_PRI
AUXADCIN_4	GPIO10	EINT15	AUXADCIN_4							BT_PRI
General purpose output										
GPO_0	GPO44	LSCE1_B1	DISP_PWM							
GPO_1	GPO46	MA_SPI0_CS1								
GPO_2	GPO47	MA_SPI1_CS1								
GPO_3	GPO48	MA_SPI3_CS1								
UART Interface										
URXD0	GPIO16	URXD0		EINT16						
UTXD0	GPIO17	UTXD0		EINT17						
Camera Interface										
CMRST	GPIO24	CMRST	LSRSTB	CLKO1	EINT9	GPCOUNTER_0	JTDI		MC1_B_DA3	
CMPDN	GPIO25	CMPDN	LSCK1	DAICLK	MA_SPI2_A_CS	MA_SPI3_A_CS	JTMS		MC1_B_DA2	SLV_SPI0_CS
CMCSD0	GPIO26	CMCSD0	LSCE_B1	DAIPCMIN	MA_SPI2_A_SCK	MA_SPI3_A_SCK	JTCK		MC1_B_CM0	SLV_SPI0_SCK
CMCSD1	GPIO27	CMCSD1	LSDA1	DAIPCMOUT	MA_SPI2_A_MOSI	MA_SPI3_A_MOSI	JTRSTB		MC1_B_CK	SLV_SPI0_MOSI
CMMCLK	GPIO28	CMMCLK	LSA0DA1	DAISYNC	MA_SPI2_A_MISO	MA_SPI3_A_MISO	JTDO		MC1_B_DA0	SLV_SPI0_MISO
CMCSK	GPIO29	CMCSK	LPTE		CMCSD2	EINT10			MC1_B_DA1	
SDIO Interface										
MCCK	GPIO30	SCL0	EINT11	PWM0	URXD1	MC0_CK				SCL2
MCCM0	GPIO31	SDA0	EINT12	PWM1	UTXD1	MC0_CM0				SDA2

MCDA0	GPIO32	SLV_SPI0_CS	EINT13	PWM2	DAISYNC	MC0_DA0				MA_SPI3_B_CS
MCDA1	GPIO33	SLV_SPI0_SCK	EINT14	PWM3	DAIPCMIN	MC0_DA1				MA_SPI3_B_SCK
MCDA2	GPIO34	SLV_SPI0_MOSI	EINT15	PWM4	DAICLK	MC0_DA2				MA_SPI3_B_MOSI
MCDA3	GPIO35	SLV_SPI0_MISO	EINT3	PWM5	DAIPCMOUT	MC0_DA3	CLKO2			MA_SPI3_B_MISO
I2C Interface										
SCL0	GPIO36	SCL0	SCL1							
SDA0	GPIO37	SDA0	SDA1							
LCM Interface										
LSRSTB	GPIO38	LSRSTB		CMRST	CLKO3					SCL1
LSCE_B	GPIO39	LSCE_B0	EINT4	CMCSD0	CLKO4				SCL1	MA_SPI2_C_CS
LSCK	GPIO40	LSCK0		CMPDN						MA_SPI2_C_SCK
LSDA	GPIO41	LSDA0	EINT5	CMCSD1	WIFITOBT				SDA1	MA_SPI2_C_MOSI
LSA0	GPIO42	LSA0DA0	LSCE1_B0	CMMCLK					CLKO5	MA_SPI2_C_MISO
LPTE	GPIO43	LPTE	EINT6	CMCSK	CMCSD2					SDA1

8. System Configuration

8.1. System mode selection and trapping

Apply the following pin trappings to configure the chip in different modes (see Table 8.1-1)

Table 8.1-1. Mode selection

Mode Selection	Pin name	Description	Trapping Resistor	Trapping condition
26MHz clock source	EXT_CLK_SEL	GND: Uses DCXO as 26MHz clock source AVDD18_DCXO: Uses external clock as 26M clock source	Pull-down/up with 10kΩ resistor	DCXO Power-on reset
Serial flash power supply voltage	GPO_3	GND: Uses 1.8V serial flash device DVDD_GPO: Uses 3.3V serial flash device	Pull-down with 10kΩ resistor (Default internal pull-down with 47kΩ resister)	Power-on reset
USB download	GPIO_B2	GND: Boots ROM to enter USB download mode DVDD_VIO_B: Normal boot-up mode	Pull-down with 10K resistor (Default internal pull-down with 47kΩ resister)	Power-on reset
Cortex-M4 JTAG pin out	{GPO_1,GPO_0}	{GND, GND}: No JTAG {GND, DVDD18_VIO18}: JTAG at keypad pins {DVDD_GPO, GND}: JTAG at GPIO pins {DVDD_GPO, DVDD18_VIO18}: JTAG at camera pins	Pull-up with 10K resistor (Default internal pull-down with 47kΩ resistor)	Power-on reset

9. Electrical Characteristics

9.1. Absolute maximum ratings

Table 9.1-1. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_LDOS1	Battery voltage used as analog LDOS1 input	-0.3	+4.8	V
VBAT_LDOS2	Battery voltage used as analog LDOS2 input	-0.3	+4.8	V
VBAT_VCORE	Battery voltage used as analog VCORE Buck input	-0.3	+4.8	V
VBAT_SW	VBAT input for switchable LDOs	-0.3	+4.8	V
VDDK	1.3V core power	-0.3	+1.43	V

Table 9.1-2. Absolute maximum ratings for I/O power supply

Symbol or pin name	Description	Min.	Typ.1	Typ.2	Max.	Unit
DVDD_VIO_A	Power supply for GPIO group A	1.62	1.8	2.8	3.08	V
DVDD_VIO_B	Power supply for GPIO group B	2.52	-	2.8	3.08	V
DVDD_VIO_C	Power supply for GPIO group C	1.62	1.8	2.8	3.08	V
DVDD_GPO	Power supply for GPO group	1.62	1.8	2.8	3.08	V
DVDD18_VIO18	Power supply for IO 1.8V group	1.62	1.8	-	1.98	V
DVDD33_VMC	Power supply for SDIO group	1.62	1.8	3.3	3.63	V

Table 9.1-3. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.63	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.63	V

Table 9.1-4. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

Table 9.1-5. Absolute maximum ratings for GNSS (MT2523G only)

Symbol	Parameter	Rating	Unit
GPS_AVDD43_DCV	SMPS power supply	-0.3 ~ 4.3	V
GPS_AVDD43_VBAT	2.8VTLDO power supply	-0.3 ~ 4.3	V
GPS_AVDD28_CLDO	1.1V CLDO power supply	-0.3 ~ 3.6	V
GPS_DVDD28_SF	Embedded flash power supply	-0.3 ~ 3.6	V
GPS_DVDD28_IO1	IO 2.8V or 1.8V power supply	-0.3 ~ 3.6	V

Symbol	Parameter	Rating	Unit
GPS_DVDD28_IO2			
GPS_DVDD11_CORE1 GPS_DVDD11_CORE2	Baseband 1.1V power supply	-0.3 ~ 1.21	V
GPS_AVDD43_RTC	RTC 1.1V LDO power supply	-0.3 ~ 4.3	V
GPS_AVDD18_RXFE	1.8V supply for RF core circuits	-0.3 ~ 3.6	V
GPS_AVDD18_CM		-0.3 ~ 3.6	V

9.2. Operating conditions

9.2.1. General operating conditions

Table 9.2-1. General operating conditions

Item	Description	Condition	Min.	Typ.	Max.	Unit
F_{CPU}	Internal Cortex-M4 & TCM & Cache clock	VCORE = 0.9V	0	-	26	MHz
		VCORE = 1.1V	0	-	104	MHz
		VCORE = 1.3V	0	-	208	MHz
F_{MEMS}	Internal memory (SFC and EMI) related AHB and APB clock. Synchronous with F_{CPU}.	VCORE = 0.9V	0	-	13	MHz
		VCORE = 1.1V	0	-	52	MHz
		VCORE = 1.3V	0	-	104	MHz
F_{PERI}	Internal peripheral AHB and APB clock. Asynchronous with FCPU.	VCORE = 0.9V	0	-	13	MHz
		VCORE = 1.1V to 1.3V	0	-	62.4	MHz

Table 9.2-2. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_LDOS1	LDO group 1 battery voltage input	3.4	3.8	4.8	V
VBAT_LDOS2	LDO group 2 battery voltage input	3.4	3.8	4.8	V
VBAT_VCORE	VCORE Buck group battery voltage input	3.4	3.8	4.8	V
VBAT_SW	VBAT input for LDO switch	3.4	3.8	4.8	V
VDDK	Digital core power	0.7	1.2	1.3	V

Table 9.2-3. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V

Table 9.2-4. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
Tc	Operating temperature	-20	-	85	°C

Table 9.2-5. Recommended operating conditions for GNSS (MT2523G only)

Symbol	Parameter	Min.	Typ.	Max.	Unit
GPS_AVDD43_DCV	SMPS power supply	2.8	3.3	4.3	V
GPS_AVDD43_VBAT	2.8V TLDO power supply	2.8	3.3	4.3	V
GPS_DVDD11_CORE1 GPS_DVDD11_CORE2	1.1V baseband core power	0.99	1.1	1.21	V
GPS_DVDD28_IO1 GPS_DVDD28_IO2	2.8V digital IO power	2.52	2.8	3.08	V
	1.8V digital IO power	1.62	1.8	1.98	V
GPS_DVDD28_SF	Embedded flash power supply	2.7	2.8	3.6	V
GPS_AVDD18_RXFE	1.35V supply for RF core circuits in bypass mode	1.3	1.35	1.98	V
	1.8V supply for RF core circuits in LDO mode	1.62	1.8	3.08	V
GPS_AVDD18_CM	1.35V supply for common RF block in bypass mode	1.3	1.35	1.98	V
	1.8V supply for common RF block in LDO mode	1.62	1.8	3.08	V

9.2.2. Input or output port characteristics

Table 9.2-6. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	• PU/PD disabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		• PD enabled, • DVDIO = 2.8V, • 2.1<VIN1<3.1	6.1	-	82.5	
DIIL1	Digital low input current for IO Type 1	• PU/PD disabled, • DVDIO = 2.8V, • -0.3 < VIN1 < 0.7	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		• PD enabled, • DVDIO = 2.8V, • -0.3 < VIN1 < 0.7	-12.5	-	22.5	
DIOH1	Digital high output current	• DVOH > 2.38V,	-16	-	-	mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	for IO Type 1	• DVDIO = 2.8V				
DIOL1	Digital low output current for IO Type 1	• DVOL < 0.42V, • DVDIO = 2.8V	-	-	16	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	• DVDIO = 2.8V	40	85	190	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	• DVDIO = 2.8V	40	85	190	kΩ
DVOH1	Digital output high voltage for IO Type 1	• DVDIO = 2.8V	2.38			V
DVOL1	Digital output low voltage for IO Type 1	• DVDIO = 2.8V			0.42	V
DIIH2	Digital high input current for IO Type 2	• PU/PD disabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		• PD enabled, • DVDIO = 2.8V, • 2.1<VIN1<3.1	6.1	-	82.5	
		• PU/PD disabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-5	-	5	µA
		• PU enabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		• PD enabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	• PU/PD disabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		• PD enabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		• PU/PD disabled, • DVDIO = 1.8V,	-5	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• -0.3 < VIN1 < 0.45				
		• PU enabled, • DVDIO = 1.8V, • -0.3 < VIN1 < 0.45	-35	-	0.8	
		• PD enabled, • DVDIO = 1.8V, • -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	• DVOH > 2.38V, • DVDIO = 2.8V	-16	-	-	mA
		• DVOH > 1.53V, • DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	• DVOL < 0.42V, • DVDIO = 2.8V	-	-	16	mA
		• DVOL < 0.27V, • DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	• DVDIO = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	• DVDIO = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	• DVDIO = 2.8V	2.38			V
		• DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	• DVDIO = 2.8V			0.42	V
		• DVDIO = 1.8V			0.27	V

9.2.3. GNSS IO port characteristics (MT2523G only)

Table 9.2-7. General DC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
IIL	Input low current	No pull-up or down	-1	1	µA
IIH	Input high current	No pull-up or down	-1	1	µA
IOZ	Tri-state leakage current		-10	10	µA

Table 9.2-8. DC electrical characteristics for 2.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		2.52	2.8	3.08	V
VIL	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIH	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
VOL	Output low voltage	VDDIO = min IOL = -2 mA	-	-	0.15*VDDIO	V
VOH	Output high voltage	VDDIO = min IOH = -2 mA	0.85*VDDIO	-	-	V
RPU	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
RPD	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

Table 9.2-9. DC electrical characteristics for 1.8V voltage operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
VIL	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
VIH	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
VOL	Output low voltage	VDDIO = min IOL = -2 mA	-	-	0.15*VDDIO	V
VOH	Output high voltage	VDDIO = min IOH = -2 mA	0.85*VDDIO	-	-	V
RPU	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	kΩ
RPD	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	kΩ

Table 9.2-10. DC electrical characteristics for 1.1V voltage operation (for FORCE_ON and 32K_OUT)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Supply voltage of core power		0.99	1.1	1.21	V
VDDIO	Supply voltage of IO power		0.99	1.1	1.21	V
VIL	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
VIH	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
VOL	Output low voltage	VDDIO = min IOL = -2 mA	-	-	0.15*VDDIO	V
VOH	Output high voltage	VDDIO = min IOH = -2 mA	0.85*VDDIO	-	-	V
RPU	Input pull-up resistance	VDDIO = typ Vinput = 0 V	130		560	kΩ
RPD	Input pull-down resistance	VDDIO = typ Vinput = 1.1 V	130		560	kΩ

9.2.4. GNSS analog related characteristics (MT2523G only)

Table 9.2-11. SMPS DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_DCV	SMPS input supply voltage	2.8	3.3	4.3	V	
DCV	SMPS output	1.74	1.84	1.94	V	
Icc	SMPS output current	-	-	100	mA	
ΔV_PWM	Ripple of PWM mode	-	-	40	mV	With L=1µH, C=4.7µF
ΔV_PFM	Ripple of PFM mode	-	-	90	mV	With L=1µH, C=4.7µF

Table 9.2-12. TCXO LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_VBAT	TCXO LDO input supply voltage	2.8	3.3	4.3	V	Will change to bypass mode under 3.1 volts
AVDD28_TLDO	TCXO LDO output	2.71	2.8	2.89	V	
Icc	LDO output current	-	-	50	mA	Not include external devices
	PSRR-30 kHz	35	-	-	dB	Co = 1µF, ESR = 0.05, I_{load} = 25mA
	Load regulation	-84	10	84	mV	

Table 9.2-13. TCXO SWITCH DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD_TCXO_SW	TCXO switch output voltage at TCXO switch input = AVDD28_TLDO	2.66	-	-	V
AVDD_TCXO_SW	TCXO switch output voltage at TCXO switch input = AVDD28_CLDO	1.71	-	-	V
Imax	TCXO SWITCH current limit	-	-	30	mA

Table 9.2-14. 1.1 volts core LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
AVDD28_CLDO	1.2V LDO input supply voltage	1.62	1.8	3.08	V
AVDD11_CLDO	1.1V LDO output	1.05	1.12	1.2	V
Icc	LDO output current	-	-	50	mA
	Load regulation	-	-	-	mV

Table 9.2-15. 1.1V RTC LDO DC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD43_RTC	RTC LDO input supply voltage	2	4	4.3	V	
AVDD11_RTC	RTC LDO output	0.99	1.1	1.21	V	
Icc	LDO output current	-	-	3	mA	
Ileak	Leakage current	2.2	10	-	µA	Including LDO and RTC domain circuit

Table 9.2-16. 32kHz crystal oscillator (XOSC32)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
AVDD11_RTC	Analog power supply	0.99	-	1.21	V	
Dcyc	Duty cycle	-	50	-	%	

9.2.5. GNSS RF related characteristics (MT2523G only)

Table 9.2-17. DC electrical characteristics for RF part

Symbol	Parameter	Min.	Typ.	Max.	Unit
Icc (GPS and GLONASS)	Total supply current:	-	8.9	-	mA

Table 9.2-18. RX chain (GPS+GLONASS mode)

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	1575.4	-	MHz
LO frequency		-	1588.6	--	MHz
LO leakage	Measured at balun matching network input at LNA high gain	-	-70	-	dBm
Input return loss	Differential input and external matched to 50Ω source using balun matching network for all gain	-10	-	-	dB
Gain (Av) (integrated average over Fc+-4M)	High current mode with max PGA gain	80	76	70	dB
	Low current mode with max PGA gain	-	64		dB
PGA Gain range		-	24	-	dB
PGA Gain step		-	2	-	dB
NF (integrated average over Fc+-4M)	High current mode with max PGA gain	-	2.2	-	dB

Table 9.2-19. Crystal oscillator (XO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Ftcxo	TCXO oscillation frequency	12.6	16.368	40	MHz
Vtcxo	TCXO output swing	0.8	1.2	-	Vpp

9.2.6. External clock source

9.2.6.1. Digitally Controlled Crystal Oscillator (DCXO)

The Digitally Controlled Crystal Oscillator (DCXO) uses a two-pin 26MHz crystal resonator. Both crystals with 1612 and 3225 footprint are supported. See Table 9.2-20 for the crystal resonator capacitance load and tuning sensitivity range supported. On-chip programmable capacitor array is used for frequency-tuning, whereby the tuning range is ±50ppm. This DCXO supports 32kHz crystal-less operation.

Table 9.2-20. DCXO Characteristics (TA = 250C, VDD = 1.8V unless otherwise stated) (1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency	Fref			26		MHz
Crystal C load	CL		7	7.5		pF
Crystal tuning sensitivity	TS		10	33		ppm/pF
Static range	SR	CDAC from 0 to 511	± 40	± 50		ppm
Start-up time	TDCXO	Frequency error < 10ppm Amplitude > 90 %		0.6	2.5	ms
Pushing figure				0.2		ppm/V
Fref buffer output level	VFref	Max. loading = 10pF		1.1		V_{p-p}
Fref buffer output phase noise		10kHz offset Jitter noise		-140		dBc/Hz

(1) Guaranteed by design, not tested in production.

9.2.6.2. 32kHz crystal oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. It is designed to be a clock source of RTC for lower power platform. See Table 9.2-21 for the key performance.

The minimum VRTC value means if the crystal oscillator starts up successfully, the minimum VRTC for the clock to still be alive will be 1V.

The crystal parameters determine the oscillation allowance. Table 9.2-22 lists recommendations for the crystal parameters to be used well with XOSC32.

Table 9.2-21. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power		1.8		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
	Current consumption			1.5	µA
T	Operating temperature	-40		85	°C

Table 9.2-22. Recommended parameters for 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			1.5	µW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	kΩ
C0	Static capacitance		1.3	1.5	pF
CL1	Load capacitance		7		pF

Under such CL range and crystal, the –R is more than 3 times bigger. If larger CL is selected , the frequency accuracy will be decreased, and the –R will degrade, too.

9.2.7. ESD electrical sensitivity

Table 9.2-23. ESD electrical characteristic of MT2523 series

ESD mode	Description	Pin name	Min.	Max.	Unit
HBM		JESD22-A114-F	-2000	2000	V
CDM	All pins exclude corner pins	JESD22-C101-D	-500	500	V
	Corner pins	JESD22-C101-D	-750	750	V

9.3. Communications interfaces

9.3.1. SPI master interface characteristics

The operating characteristics of the SPI master controller at typical temperature (25°C) are shown in Figure 9-1, Figure 9-2 and Table 9.3-1. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data.

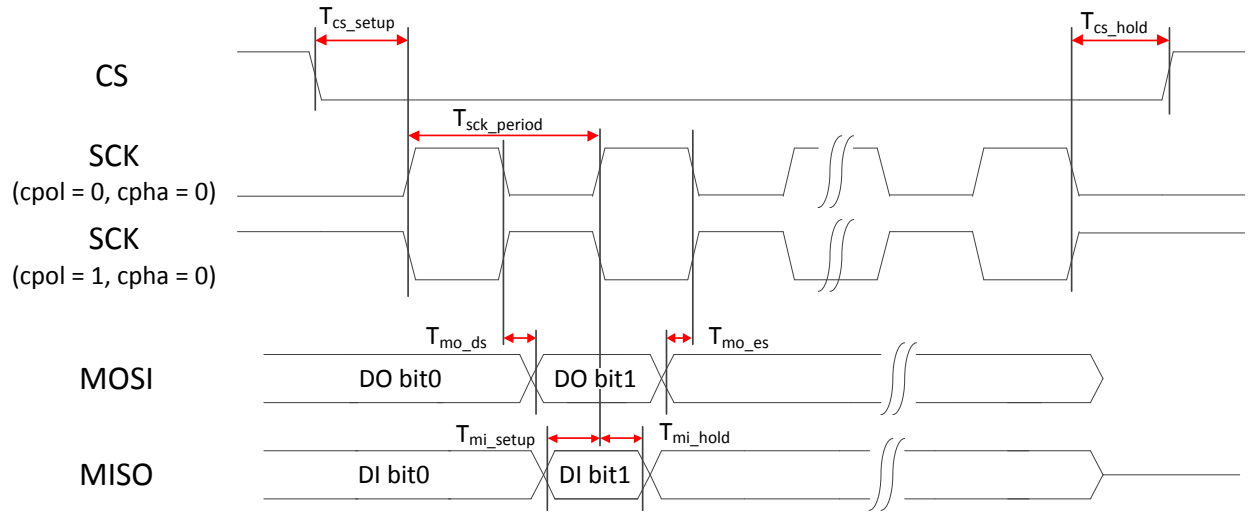


Figure 9-1. SPI master interface timing diagram (CPHA=0)

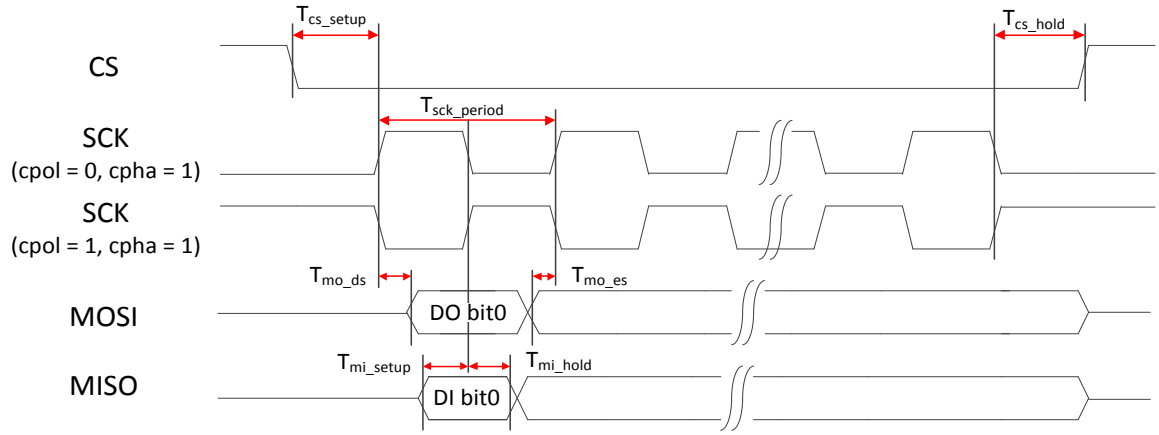


Figure 9-2. SPI master interface timing diagram (CPHA=1)

Table 9.3-1. SPI master interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CS	T_{cs_setup}	Chip select setup time	21	-	ns	
	T_{cs_hold}	Chip select hold time	21	-	ns	
SCK	T_{sck_period}	Serial clock period	77	-	ns	
MOSI	T_{mo_ds}	SPI master data output delay skew	-	3	ns	
	T_{mo_es}	SPI master data output early skew	-	3	ns	
MISO	T_{mi_setup}	SPI master data input valid time	20	-	ns	
	T_{mi_hold}	SPI master data input hold time	20	-	ns	

9.3.2. SPI slave interface characteristics

The operating characteristics of the SPI slave controller at typical temperature (25°C) are shown in Figure 9-3, Figure 9-4 and Table 9.3-2. CPOL defines the clock polarity in the transmission. CPHA defines the legal timing to sample data.

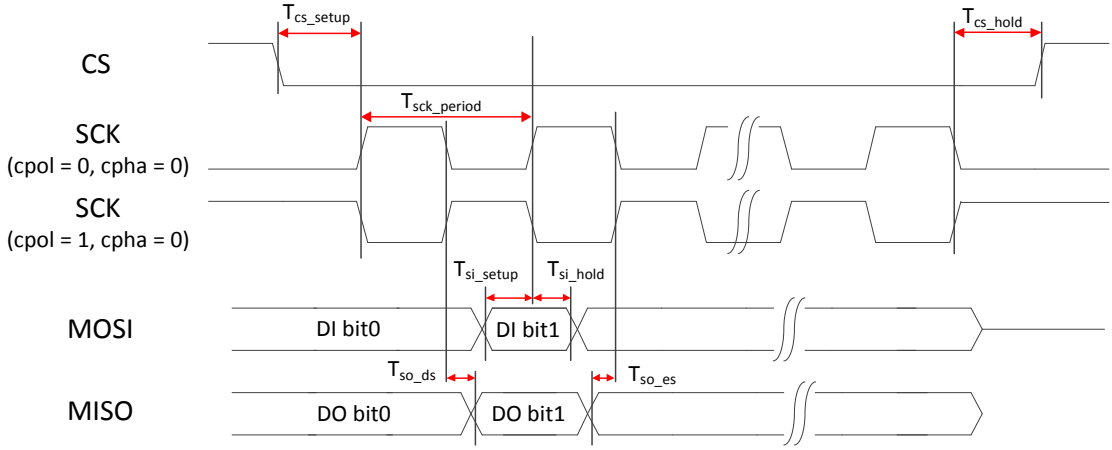


Figure 9-3. SPI slave interface timing diagram (CPHA=0)

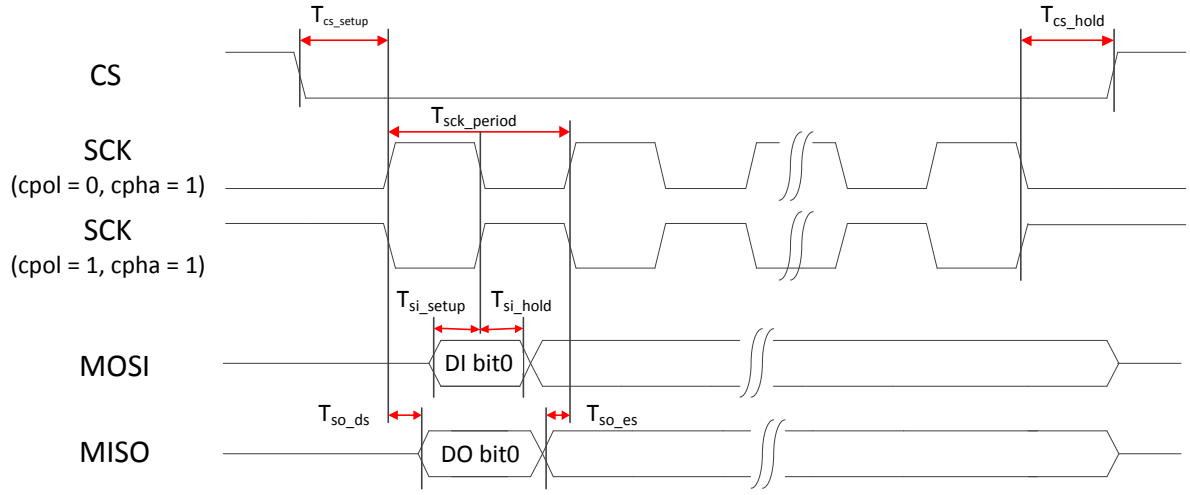


Figure 9-4. SPI slave interface timing diagram (CPHA=1)

Table 9.3-2. SPI slave interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CS	T_{cs_setup}	Chip select setup time	21	–	ns	
	T_{cs_hold}	Chip select hold time	21	–	ns	
SCK	T_{sck_period}	Serial clock period	77	–	ns	
MOSI	T_{si_setup}	SPI slave data input valid time	20	–	ns	
	T_{si_hold}	SPI slave data input hold time	20	–	ns	
MISO	T_{so_ds}	SPI slave data output delay skew	–	3	ns	
	T_{so_es}	SPI slave data output early skew	–	3	ns	

9.3.3. I2S master interface characteristics

The operating characteristics of the I2S master controller at typical temperature (25°C) are shown in Figure 9-5 and Table 9.3-3. Example: I2S master transmitter with data rate of 0.512MHz (±10%) (0.512MHz = 16KHz x 32 , Audio Sampling Rate x Sample Bits).

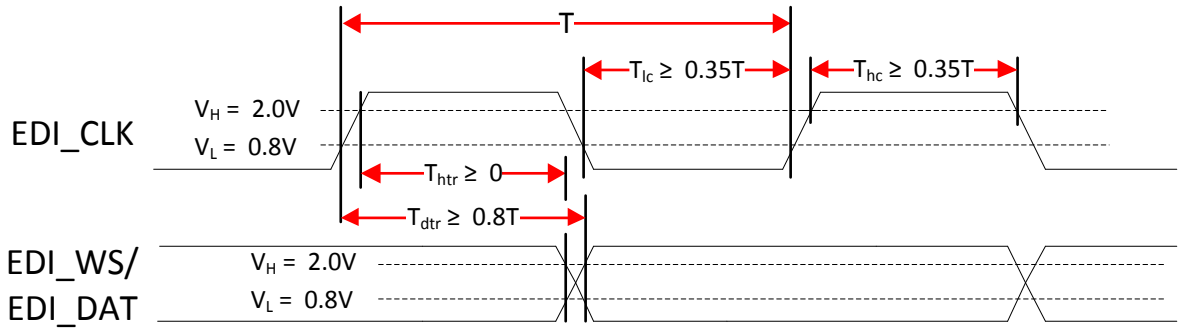


Figure 9-5. I2S master interface timing diagram

Table 9.3-3. I2S master interface characteristics

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
EDI_CLK	T	Clock period	1758	2148	ns	
	T_{hc}	Clock high	700	–	ns	Min > 0.35T = 684 (at typical data rate)
	T_{lc}	Clock low	700	–	ns	Min > 0.35T = 684 (at typical data rate)
EDI_WS/ EDI_DAT	T_{dtr}	Delay time	–	1540	ns	Max < 0.8T = 1562 (at typical data rate)
	T_{htr}	Hold time	400	–	ns	Min > 0

9.3.4. I2C interface characteristics

The operating characteristics of the I2C controller at typical temperature (25°C) are shown in Figure 9-6, Figure 9-6 and Table 9.3-4.

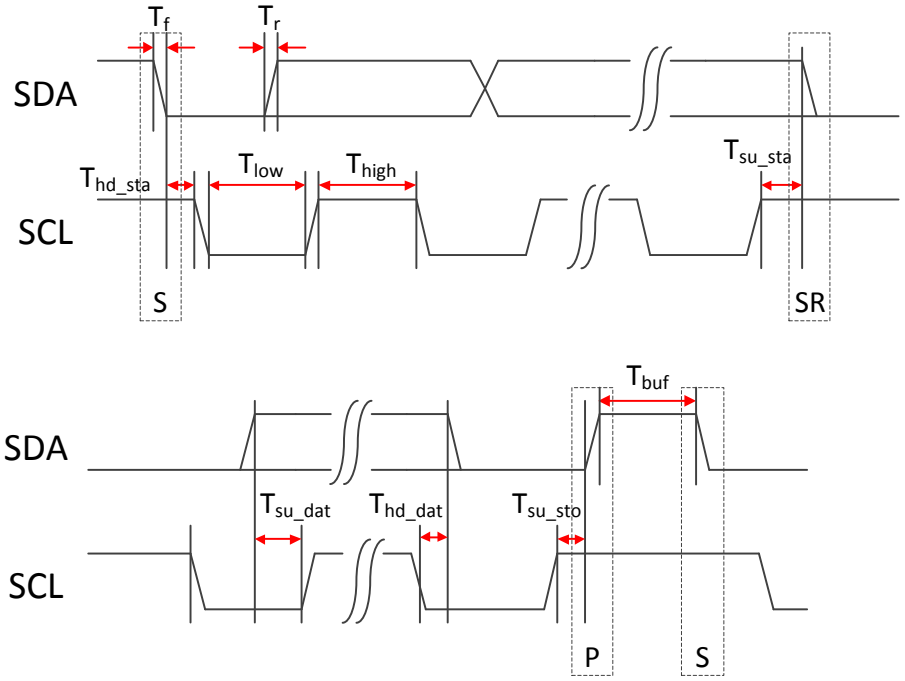


Figure 9-6. I2C interface timing diagram

Table 9.3-4. I2C interface characteristics

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL clock frequency	F_{scl}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	T_{hd_sta}	4.0	–	0.6	–	µs
LOW period of the SCL clock	T_{low}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	T_{high}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	T_{su_sta}	4.7	–	0.6	–	µs

Parameter	Symbol	Standard Mode		Fast Mode		Unit
Data set-up time	T_{su_dat}	250	–	100	–	ns
Rise time of both SDA and SCL signals	T_r	–	1000	20 + $0.1C_b$[(1)]	300	ns
Fall time of both SDA and SCL signals	T_f	–	300	20 + $0.1C_b$[(1)]	300	ns
Set-up time for STOP condition	T_{su_sto}	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	T_{buf}	4.7	–	1.3	–	µs

(1) C_b = total capacitance of one bus line in pF. If mixed with high-speed mode devices, faster fall-times according to Figure 9-5 are allowed.

9.3.5. SD interface characteristics

The operating characteristics of the SD controller's default speed mode at typical temperature (25°C) are shown in Figure 9-7, Figure 9-8 and Table 9.3-6. The operating characteristics of the SD controller high-speed mode at typical temperature (25°C) are shown in Figure 9-9, Figure 9-10 and Table 9.3-7.

Table 9.3-5. SD controller Threshold Level for High Voltage (BUS operating conditions for 3.3V signaling)

Parameter	Symbol	Min.	Max.	Unit	Description
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}	–	V	I_{OH}= -2mA at $V_{DD\ min}$
Output Low Voltage	V_{OL}	–	0.125*V_{DD}	V	I_{OL}= 2mA at $V_{DD\ min}$
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{DD}	V	
Power Up Time		–	250	ms	From 0V to $V_{DD\ min}$

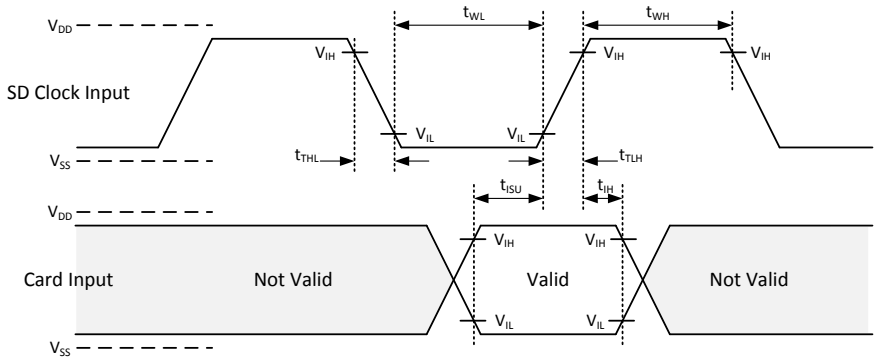


Figure 9-7. SD controller input timing (default speed mode)

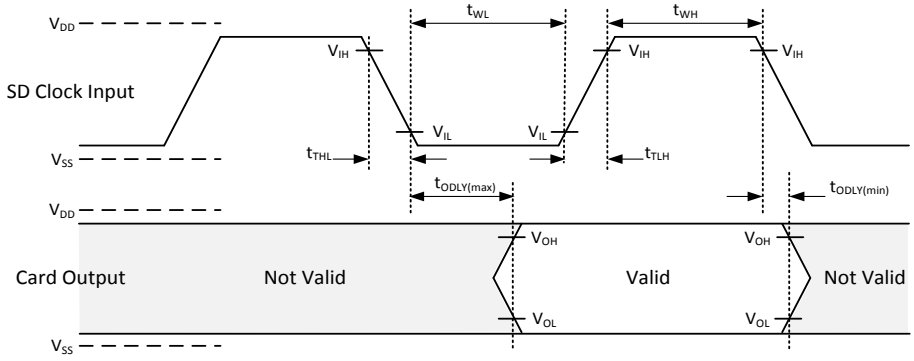


Figure 9-8. SD controller output timing (default speed mode)

Table 9.3-6. SD controller interface characteristics (Default Speed Mode)

Parameter	Symbol	Min.	Max.	Unit	Description
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{pp}	0	25	MHz	$C_{CARD} \leqq 10pF$(1 card)
Clock frequency Identification Mode	f_{OD}	0[(1)]/100	400	kHz	$C_{CARD} \leqq 10pF$(1 card)
Clock low time	t_{WL}	10	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock high time	t_{WH}	10	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock rise time	t_{TLH}	–	10	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock fall time	t_{THL}	–	10	ns	$C_{CARD} \leqq 10pF$(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Input hold time	t_{IH}	5	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_{CARD} \leqq 40pF$(1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_{CARD} \leqq 40pF$(1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required

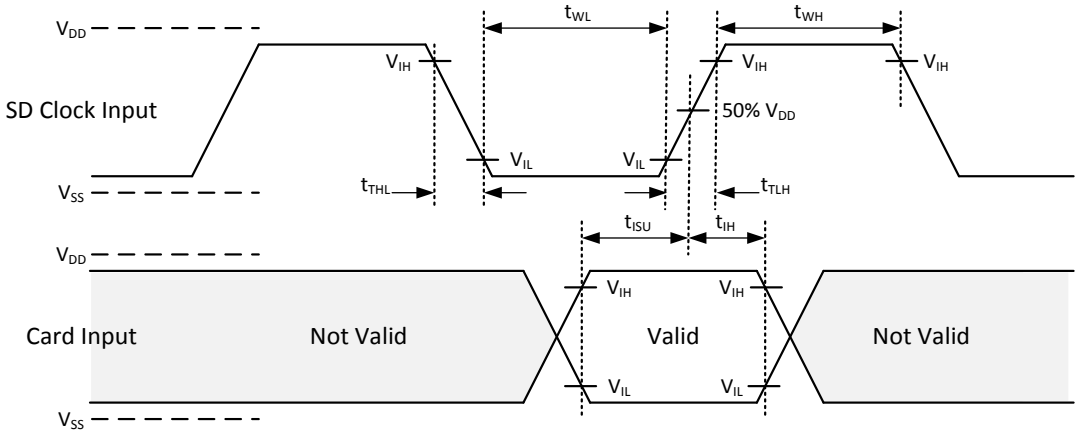


Figure 9-9. SD controller input timing (high-speed mode)

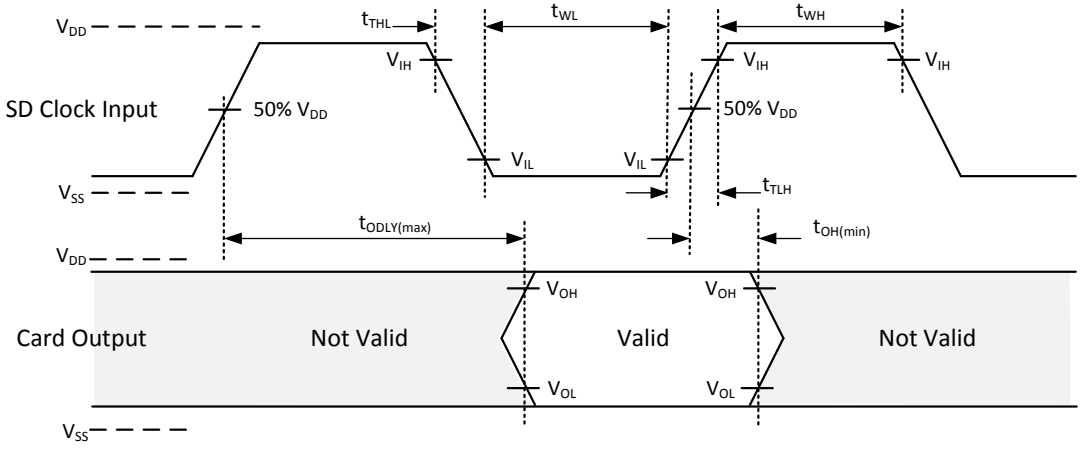


Figure 9-10. SD controller output timing (high-speed mode)

Table 9.3-7. SD controller interface characteristics (high-speed mode)

Parameter	Symbol	Min.	Max.	Unit	Description
Clock CLK (All values are referred to min (V_{IH}) and max (V_{IL})					
Clock frequency Data Transfer Mode	f_{pp}	0	50	MHz	$C_{CARD} \leqq 10pF$(1 card)
Clock low time	t_{WL}	7	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock high time	t_{WH}	7	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock rise time	t_{TLH}	–	3	ns	$C_{CARD} \leqq 10pF$(1 card)
Clock fall time	t_{THL}	–	3	ns	$C_{CARD} \leqq 10pF$(1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6	–	ns	$C_{CARD} \leqq 10pF$(1 card)
Input hold time	t_{IH}	2	–	ns	$C_{CARD} \leqq 10pF$(1 card)

Parameter	Symbol	Min.	Max.	Unit	Description
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	–	14	ns	$C_{CARD} \leqq 40pF$(1 card)
Output Hold time	t_{OH}	2.5	–	ns	$C_{CARD} \leqq 15pF$(1 card)
Total System capacitance for each line[1]	C_L	–	40	pF	1 card

[1]In order to satisfy severe timing, host shall drive only one card.

9.3.6. eMMC interface characteristics

The operating characteristics of the eMMC controller at typical temperature (25°C) are shown in Figure 9-11 and Table 9.3-10.

Table 9.3-8. eMMC interface push-pull signal level----2.7V – 3.6V V_{CCQ} range (high voltage eMMC)

Parameter	Symbol	Min.	Max.	Unit	Description
Output High Voltage	V_{OH}	0.75*V_{CCQ}		V	I_{OH}= -100uA @V_{CCQ} min
Output Low Voltage	V_{OL}		0.125*V_{CCQ}	V	I_{OL}= 100uA @V_{CCQ} min
Input High Voltage	V_{IH}	0.625*V_{CCQ}	V_{CCQ}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.25*V_{CCQ}	V	

Table 9.3-9. eMMC interface push-pull signal level----1.70V – 1.95V V_{CCQ} voltage range

Parameter	Symbol	Min.	Max.	Unit	Description
Output High Voltage	V_{OH}	V_{CCQ} -0.45V	–	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	–	0.45V	V	I_{OL}= 2mA
Input High Voltage	V_{IH}	0.65*V_{CCQ} [1]	V_{CCQ}+0.3	V	
Input Low Voltage	V_{IL}	V_{SS}-0.3	0.35*V_{CCQ}[2]	V	

[1]0.7*V_{DD} for MMC4.3 and older revisions

[2]0.3*V_{DD} for MMC4.3 and older revisions

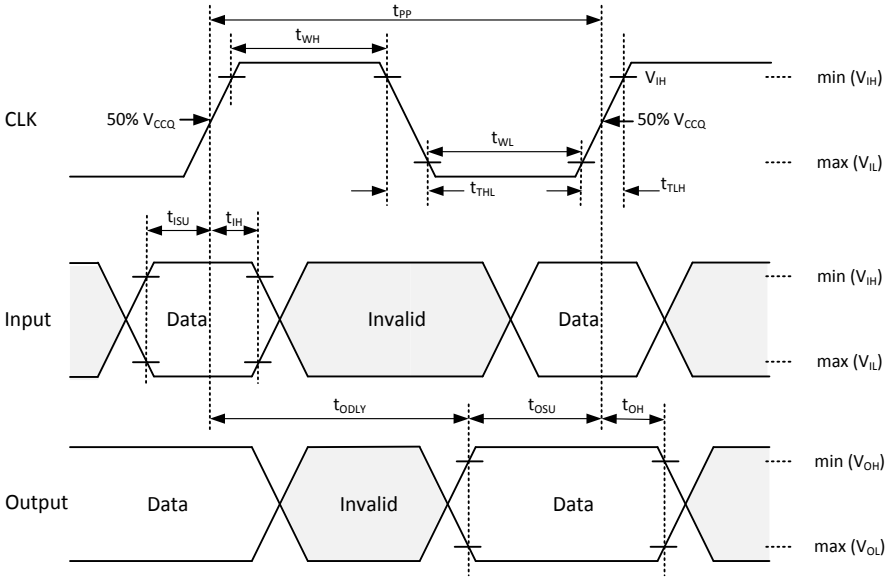


Figure 9-11. eMMC interface timing diagram

Table 9.3-10. eMMC interface characteristics (backward-compatible device)

Parameter	Symbol	Min.	Max.	Unit	Description [1]
Clock CLK[2]					
Clock frequency data transfer Mode (PP)[3]	f_{pp}	0	26	MHz	CL≦30pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10	–	ns	CL≦30pF
Clock high time	t_{WH}	10	–	ns	CL≦30pF
Clock rise time[4]	t_{TLH}	–	10	ns	CL≦30pF
Clock fall time	t_{THL}	–	10	ns	CL≦30pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	–	ns	CL≦30pF
Input hold time	t_{IH}	3	–	ns	CL≦30pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	t_{OSU}	11.7	–	ns	CL≦30pF
Output hold time[5]	t_{OH}	8.3	–	ns	CL≦30pF

[1]The device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

[2]CLK timing is measured at 50% of V_{CCQ}

(3)For compatibility with devices that support the v4.2 standard or earlier, host should not use frequency greater than 26MHz before switching to high-speed interface timing.

(4)CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL})

(5)t_{OSU} and t_{OH} are defined as values from clock rising edge. However, there may be devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set t_{WL} values as long as possible within the range which will not go over t_{CK}-$t_{OH(min)}$ in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between t_{WL} and t_{OSU} or between t_{CK} and t_{OSU} for the device in its own datasheet as a note or an application notes.

Table 9.3-11. eMMC interface characteristics (High-speed Device)

Parameter	Symbol	Min.	Max.	Unit	Description
Clock CLK(1)					
Clock frequency Data Transfer Mode (PP)(2)	f_{pp}	0	52(3)	MHz	$C_L \leqq 30pF$ Tolerance:+100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance:+20KHz
Clock low time	t_{WL}	6.5	–	ns	$C_L \leqq 30pF$
Clock high time	t_{WH}	6.5	–	ns	$C_L \leqq 30pF$
Clock rise time(4)	t_{TLH}	–	3	ns	$C_L \leqq 30pF$
Clock fall time	t_{THL}	–	3	ns	$C_L \leqq 30pF$
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	–	ns	$C_L \leqq 30pF$
Input hold time	t_{IH}	3	–	ns	$C_L \leqq 30pF$
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	t_{ODLY}	–	13.7	ns	$C_L \leqq 30pF$
Output hold time	t_{OH}	2.5	–	ns	$C_L \leqq 30pF$
Signal rise time(5)	T_{RISE}	–	3	ns	$C_L \leqq 30pF$
Signal fall time	T_{FALL}	–	3	ns	$C_L \leqq 30pF$

(1)CLK timing is measured at 50% of V_{CCQ}

(2)An eMMC shall support the full frequency range from 0MHz – 26MHz, or 0MHz – 52MHz

(3)Devices can operate as high-speed device interface timing at 26MHz clock frequency.

(4)CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

(5)Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

9.3.7. USB2.0 interface characteristics

The operating characteristics of the USB2.0 controller at typical temperature (25°C) are shown in Figure 9-12, Figure 9-13 and Table 9.3-12.

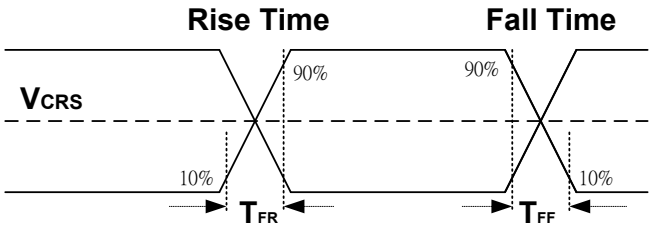


Figure 9-12. USB2.0 interface timing diagram (Full-Speed)

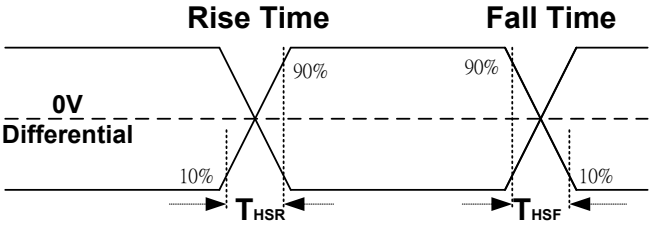


Figure 9-13. USB2.0 interface timing diagram (high-speed)

Table 9.3-12. USB2.0 interface characteristics

Parameter	Symbol	Min.	Max.	Unit	Description
Input Levels for Full-Speed					
Differential Input Sensitivity	V_{DI}	0.2	–	V	
Differential Common Mode Range	V_{CM}	0.8	2.5	V	
Output Levels for Full-Speed					
Low	V_{OL}	0.0	0.3	V	
High	V_{OH}	2.8	3.6	V	
SE1	V_{OSE1}	0.8	–	V	
Full-Speed Driver Characteristics					
Rise Time	T_{FR}	4	20	ns	
Fall Time	T_{FF}	4	20	ns	
Output Signal Crossover Voltage	V_{CRS}	1.3	2.0	V	
Input Levels for High-Speed					
Squelch detection threshold	V_{HSSQ}	100	200	mV	
Data signaling common mode range	V_{HSCM}	-50	500	mV	
Output Levels for High-Speed					
High-speed idle level	V_{HSOI}	-10.0	10.0	mV	

Parameter	Symbol	Min.	Max.	Unit	Description
High-speed data signaling high	V_{HSOH}	360	440	mV	
High-speed data signaling low	V_{HSOL}	-10.0	10.0	mV	
Chirp J level (differential voltage)	V_{CHIRPJ}	700	1100	mV	
Chirp K level (differential voltage)	V_{CHIRPK}	-900	-500	mV	
High-Speed Driver Characteristics					
Rise Time (10% - 90%)	T_{HSR}	500	–	ps	
Fall Time (10% - 90%)	T_{HSF}	500	–	ps	
High-Speed Clock Timings					
Data Rate	T_{HSDRAT}	479.76	480.24	Mb/s	
Terminations					
Pull-up Resistor	R_{PU}	0.9	1.575	kΩ	
Pull-down Resistor	R_{PD}	14.25	24.8	kΩ	

9.4. Display controller

The display controller provides MIPI DBI TYPE-C (Display Bus Interface — serial data transfer type interface mode and MIPI DSI (Display Serial Interface) interface mode with the following features:

- Supports four layers of overlay with individual color depth, window size, vertical and horizontal offset, source key, dither and alpha value
- Supports ARGB8888, PARGB8888, ARGB6666, PARGB6666, RGB888, RGB 565, YUYV422, 1/2/4 index input color formats
- Supports index color look-up table of up to 16 colors
- Supports per pixel alpha channel
- Supports hardware display rotation
- Supports true color engine
- Supports 65K color levels (RGB565), 262K color levels (RGB666) and 16M color levels (RGB888) LCM formats
- Supports adaptive ambient light control for DRE enhancement and CABC compensation for sunlight visibility and backlight power saving

9.4.1. MIPI DBI TYPE-C Interface

MIPI DBI TYPE-C interface has the following features:

- Supports LCD module with maximum resolution of up to 320 x 320 (when operating in 2-data-pin mode)
- Supports 3-wire and 4-wire serial data interface (9/10/16/18-bit data per transaction)
- Supports 2-data-pin serial interface (16/18/24-bit data per transaction)

- Supports `cs_stay_low` and single A0 mode
- Supports start byte mode
- Capable of simultaneous connection to two serial LCD modules (LSCE0, LSCE1)

9.4.2. MIPI DSI Interface

The display serial interface (DSI) is based on MIPI Alliance Specification, supporting high-speed serial data transfer between the host processor and peripheral devices such as display modules. DSI supports command mode data transfer defined in MIPI specification, and it also provides bidirectional transmission with low-power mode to receive messages from the peripheral.

The DSI engine has the following features for display serial interface:

- One clock lane and one data lane
- Throughput up to 100 Mbps for one data lane
- Bidirectional data transmission in low-power mode in data lane 0
- Uni-directional data transmission in high-speed mode in data lane 0
- DCS command transmission
- Pixel format of RGB565/loosely RGB666/RGB888
- Supports non-continuous high-speed transmission in data lanes
- Supports peripheral TE and external TE signal detection
- Supports ultra-low power mode control

9.5. MIPI DBI TYPE-C interface characteristics

For 3-wire serial data interface:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.
- LSCK: Serial transfer clock
- LSDA: Serial input/output data

For 4-wire serial data interface:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.
- LSCK: Serial transfer clock
- LSDA: Serial input/output data
- LSA0: Data/command select. Will be HIGH if there is data transaction; otherwise LOW

For 2-data-pin mode:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.

- LSCK: Serial transfer clock
- LSDA: Serial input/output data
- LSA0: Serial output data

9.5.1. Serial Data Write Mode

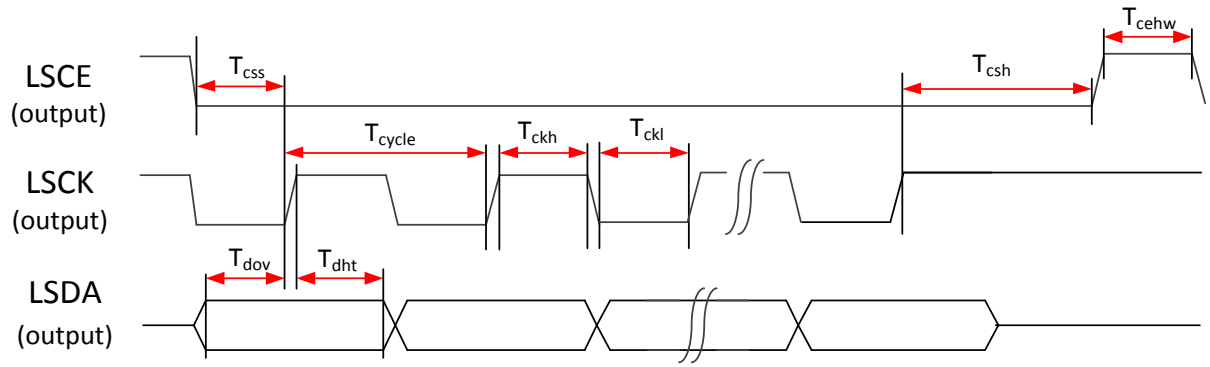


Figure 9-14. 3-wire serial data interface

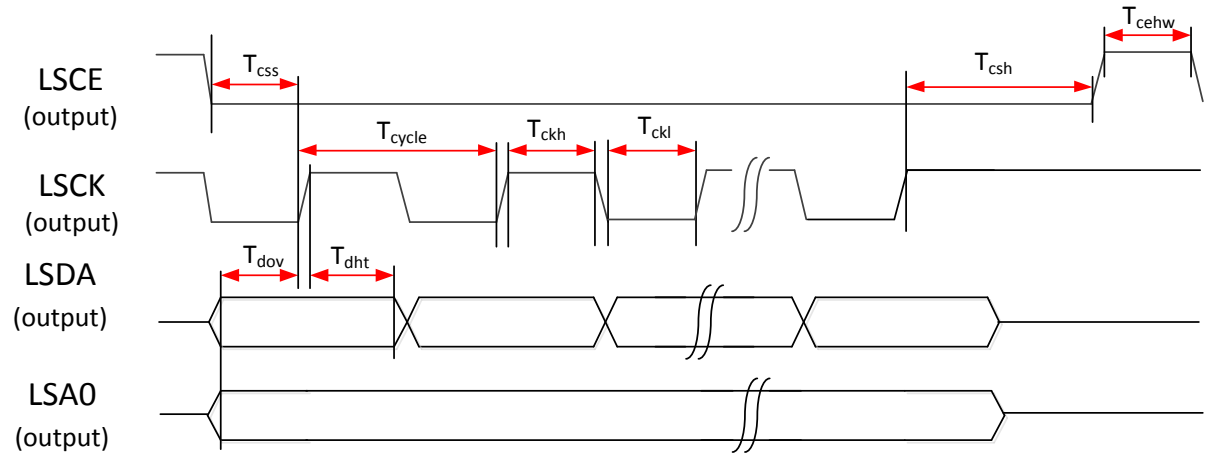


Figure 9-15. 4-wire serial data interface

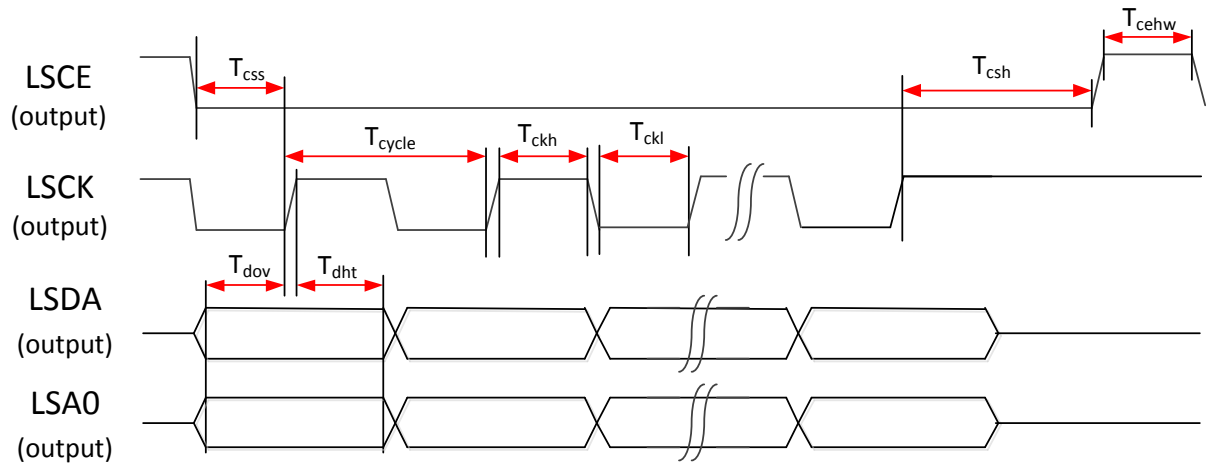


Figure 9-16. 2-data pin mode

Table 9.5-1. Serial interface characteristics during write operation

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
LSCK	Tcycle	Serial clock cycle	16	–	ns	
	Tckh	Clock High pulse width	7.2	–	ns	
	Tckl	Clock Low pulse width	7.2	–	ns	
LSCE	Tcehw	Chip select High pulse width	16	–	ns	
	Tcss	Chip select valid time	15	–	ns	
	Tcsh	Chip select hold time	15	–	ns	
LSDA/LSA0	Tdov	Data output valid time	7	–	ns	
	Tdht	Data output hold time	7	–	ns	

9.5.2. Serial Data Read Mode

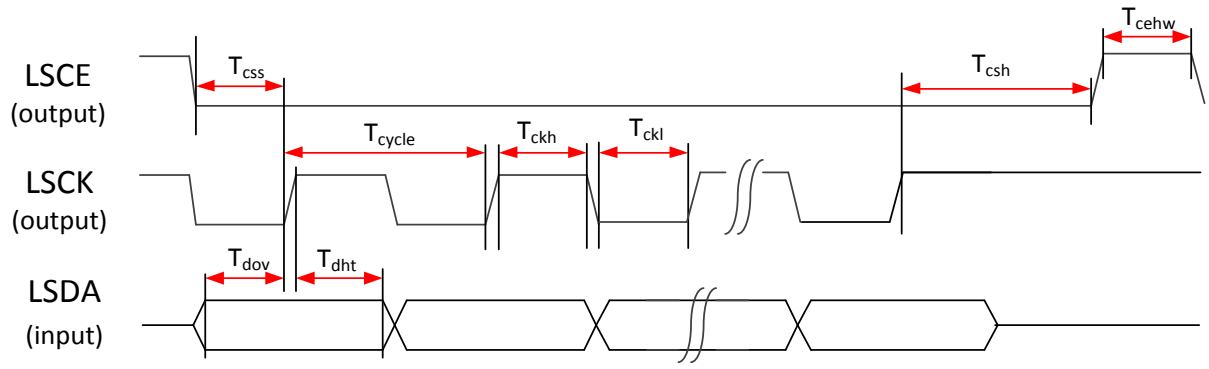


Figure 9-17. 3-wire serial interface

Table 9.5-2. Serial interface characteristics during read operation

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
LSCK	Trcycle	Serial clock cycle (read)	67	-	ns	
	Trckh	Read clock High pulse width (read)	33	-	ns	
	Trckl	Clock Low pulse width (read)	33	-	ns	
LSCE	Trcehw	Chip select High pulse width (read)	67	-	ns	
	Trcss	Chip select valid time (read)	44	-	ns	
	Trcsh	Chip select hold time (read)	44	-	ns	
LSDA/LSA0	Tridrs	Input data required setup time (read)	33	-	ns	
	Tridrh	Input data required hold time (read)	33	-	ns	

9.6. MIPI DBI TYPE-C Interface Color Coding

9.6.1. 3-wire Serial Data Interface Write (A0+8-bit)

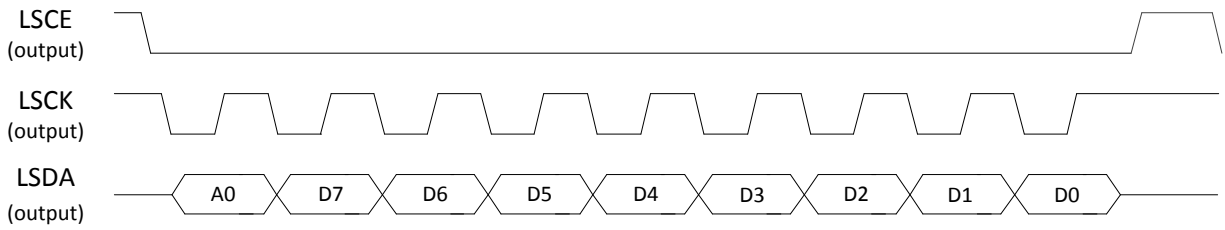


Figure 9-18. 3-wire serial interface (A0+8-bit)

- For RGB565 output format:

  D[15:0] ={ R[4:0] ,G[5:0] , B[4:0] }, 1 pixel/2 transactions

- For RGB666 output format:

  {D[23:18],D[15:10],D[7:2]}= {R[5:0],G[5:0],B[5:0]}, 1 pixel/3 transactions

- For RGB888 output format:

  D[23:0] ={ R[7:0] ,G[7:0] , B[7:0] }, 1 pixel/3 transactions

9.6.2. 3-wire Serial Data Interface Write (A0+9-bit)

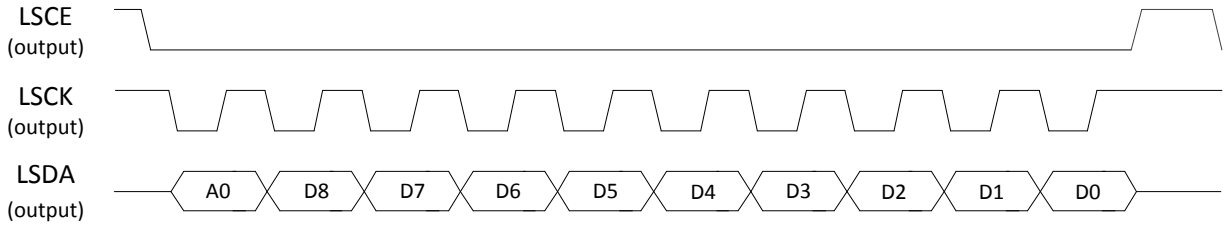


Figure 9-19. 3-wire serial interface (A0+9-bit)

- For RGB666: {D[17:0]}= {R[5:0],G[5:0],B[5:0]}, 1 pixel/2 transactions

Three other modes:

1. A0+ 16-bit mode for RGB565: 1 pixel/1 transaction
2. A0+ 18-bit mode for RGB666: 1 pixel/1 transaction
3. A0+ 24-bit mode for RGB888: 1 pixel/1 transaction

9.6.3. 4-wire Serial Data Interface Write (8-bit)

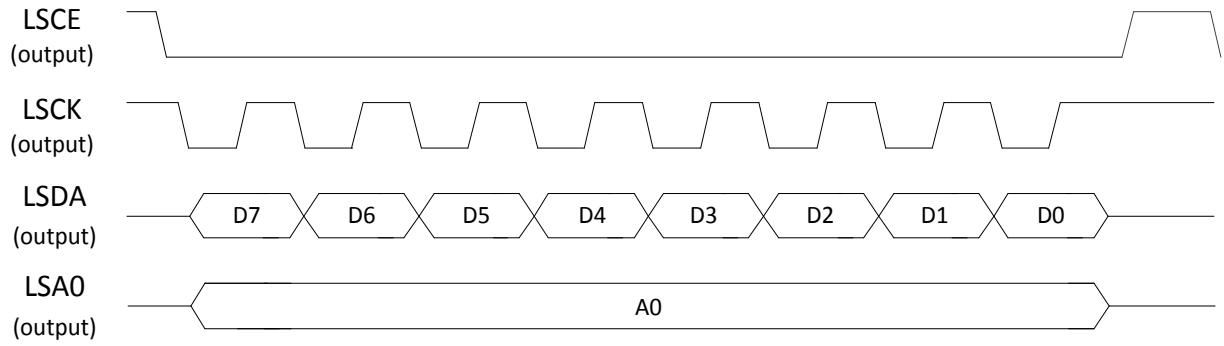


Figure 9-20. 4-wire serial interface write (8-bit)

- For RGB565:

  D[15:0] ={ R[4:0] ,G[5:0] , B[4:0] }, 1 pixel/2 transactions

- For RGB666:

  {D[23:18],D[15:10],D[7:2]}= {R[5:0],G[5:0],B[5:0]}, 1 pixel/3 transactions

- For RGB888:

  D[23:0] ={ R[7:0] ,G[7:0] , B[7:0] }, 1 pixel/3 transactions

Four other modes:

- 9-bit mode for RGB666: 1 pixel/2 transactions
- 16-bit mode for RGB565: 1 pixel/1 transaction
- 18-bit mode for RGB666: 1 pixel/1 transaction
- 24-bit mode for RGB888: 1 pixel/1 transaction

9.6.4. 2-data-pin Mode Write (A0+8-bit)

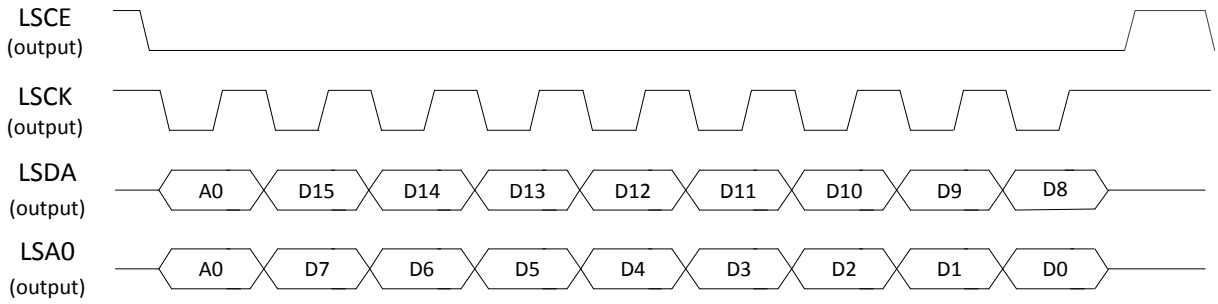


Figure 9-21. 2-data-pin mode write (A0+8-bit)

- For RGB565:

  {D[15:0]}= {R[4:0],G[5:0],B[5:0]}, 1 pixel/1 transaction

- For RGB888:

  D[47:23] = R1{7:0], G1 [7:0],B1 [7:0]}

  D [23: 0] = R0{7:0], G0 [7:0],B0 [7:0]}, 2 pixels/3 transactions

9.6.5. 2-data-pin Mode Write (A0+9-bit)

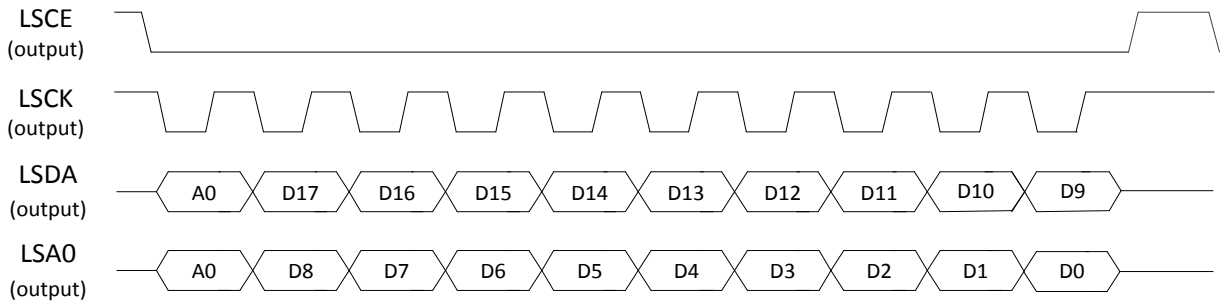


Figure 9-22. 2-data-pin mode write (A0+9-bit)

- For RGB666:

  D[17:0]= {R[5:0],G[5:0],B[5:0]}, 1 pixel/1 transaction

9.6.6. 2-data pin Mode Write (A0+12-bit)

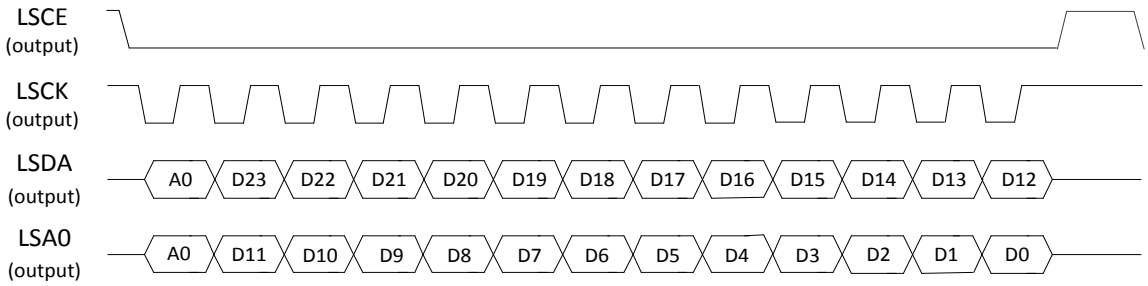


Figure 9-23. 2-data-pin mode write (A0+12-bit)

- For RGB888:

  D[23:0] ={ R{7:0], G[7:0],B [7:0]}, 1 pixel/1 transaction

9.7. MIPI DSI interface characteristics

9.7.1. MIPI D-PHY HS/LP Transmitter characteristic

The parameters given in Table 9.7-1 are MIPI HS/LP Transmitter DC/AC characteristics.

Table 9.7-1 HS transmitter DC specifications

Parameter	Description	Min.	Nom.	Max.	Units
ΔVCMTX(LF)	Common-level variation	–	–	25	mVPEAK
tR and tF	20%-80% rise time and fall time	–	–	0.3	UI
		100	–	–	ps

Parameter	Description	Min.	Nom.	Max.	Units
			–	–	

Table 9.7-2 HS Transmitter AC Specifications

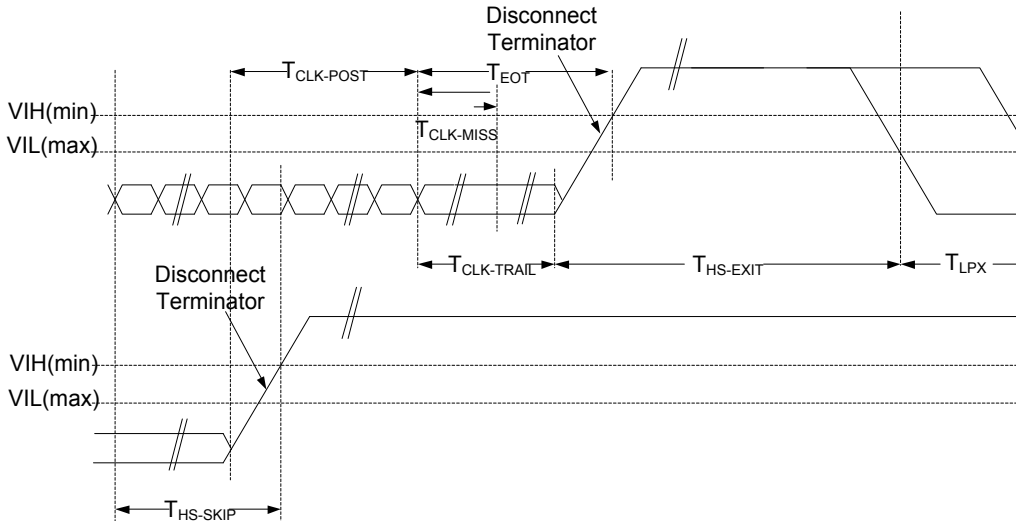
Parameter	Description	Min.	Nom.	Max.	Units
VCMTX	HS transmit static common-mode voltage	150	200	250	mV
|ΔVCMTX(1,0)|	VCMTX mismatch when output is Differential-1 or Differential-0	–	–	5	mV
|VOD|	HS transmit differential voltage	140	200	270	mV
|ΔVOD|	VOD mismatch when output is Differential-1 or Differential-0	–	–	14	mV
VOHHS	HS output high voltage	–	–	360	mV
ZOS	Single ended output impedance	40	50	62.5	Ω
ΔZOS	Single ended output impedance mismatch	–	–	10	%

Table 9.7-3 LP Transmitter AC Specifications

Parameter	Description	Min.	Nom.	Max.	Units
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V
		0.95	–	1.3	V
V_{OL}	Thevenin output low level	-50	–	50	mV
Z_{OLP}	Output impedance of LP transmitter	110	–	–	Ω

9.7.2. HS clock transmission

Figure 9-24 shows high-speeds clock transmission waveform the parameters are listed in Table 9.7-4.



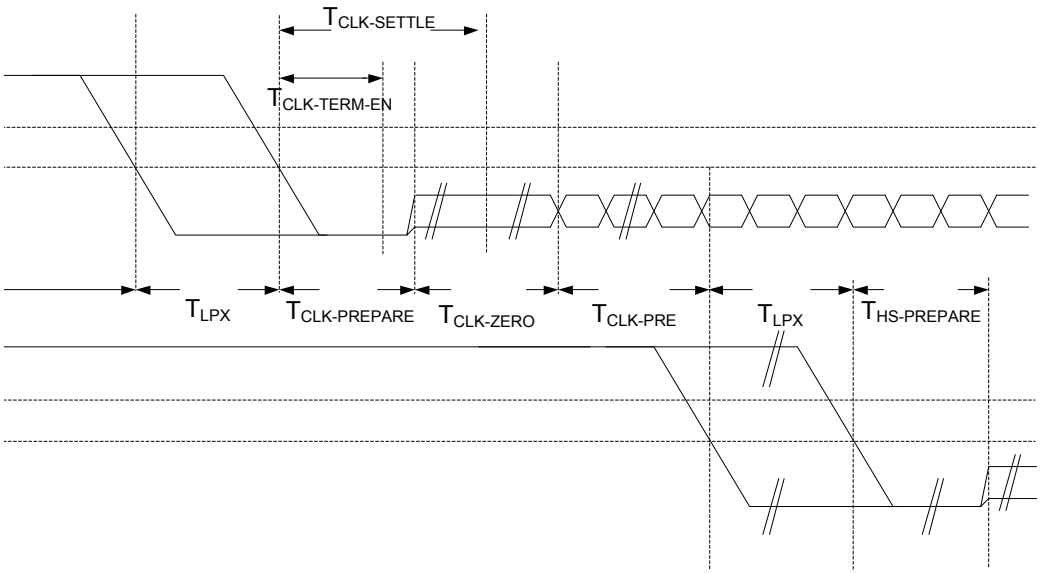


Figure 9-24. HS clock transmission

Table 9.7-4. HS clock transmission timing parameters

Parameter	Description	Min.	Typ.	Max.	Unit
TCLK-MISS	Timeout for receiver to detect absence of clock transitions and disable the Clock Lane HS-RX	–	–	60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP mode. The interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI	–	–	ns
TCLK-PRE	Time that the HS clock should be driven by the transmitter prior to any associated Data Lane starting the transition from LP to HS mode	8	–	–	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starts the HS transmission	38	–	95	ns
TCLK-SETTLE	Time interval during which the HS receiver should ignore any Clock Lane HS transition, starting from the beginning of TCLK-PREPARE	95	–	300.0	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	Time for Dn to reach VTERM-EN	–	38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60	–	–	ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the clock	300	–	–	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst	–	–	105 ns + n*12*UI	ns

9.7.3. HS data transmission

Figure 9-25 shows high-speeds data transmission waveform and the parameters are listed in Table 9.7-5.

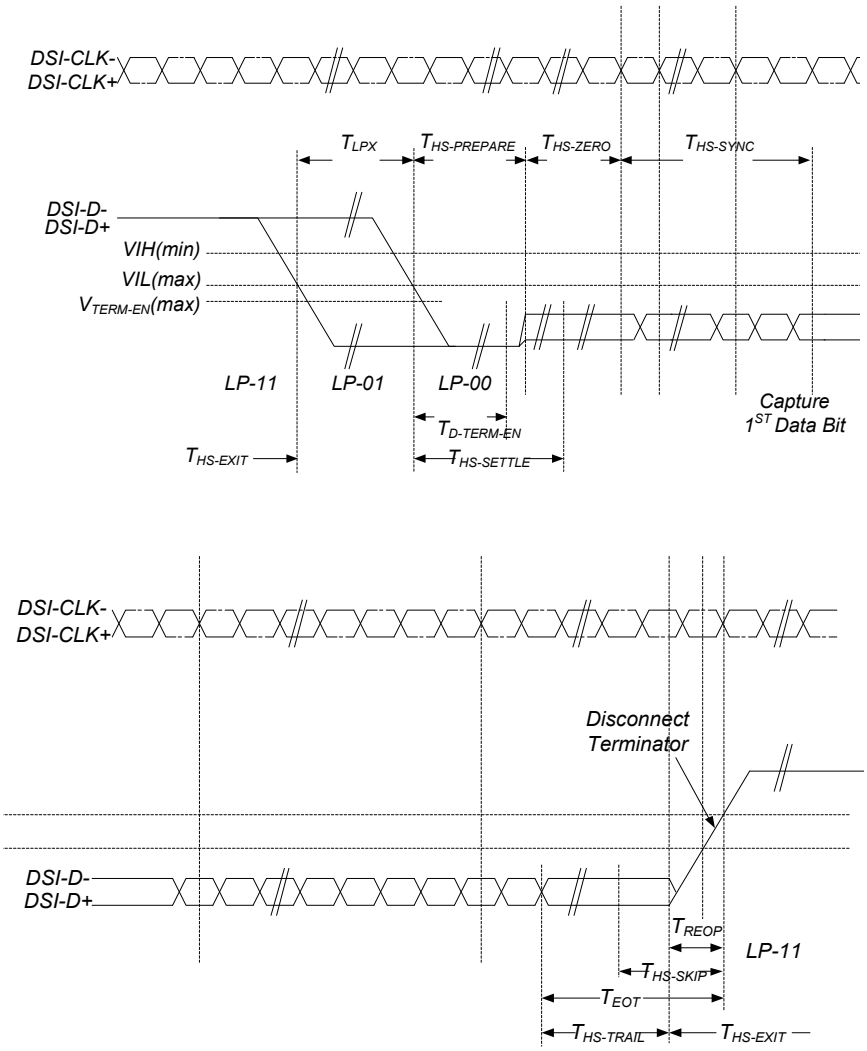


Figure 9-25. HS data transmission in bursts

Table 9.7-5. HS data transmission timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	Time for Dn to reach VTERM-EN	–	35 ns + 4*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst	100	–		ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starts the HS transmission	40 ns + 4*UI	–	85 ns + 6*UI	ns
	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence	145 ns + 10*UI	–		ns

Parameter	Description	Min.	Typ.	Max.	Unit
THS-SETTLE	Time interval during which the HS receiver should ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver should ignore any Data Lane transition before the minimum value, and the HS receiver should respond to any Data Lane transition after the maximum value.	85 ns + 6*UI	–	145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40	–	55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)	–	–	ns

9.7.4. Turnaround Procedure

Figure 9-26 and Figure 9-27 shows turnaround procedure and the parameters are listed in Table 9.7-6.

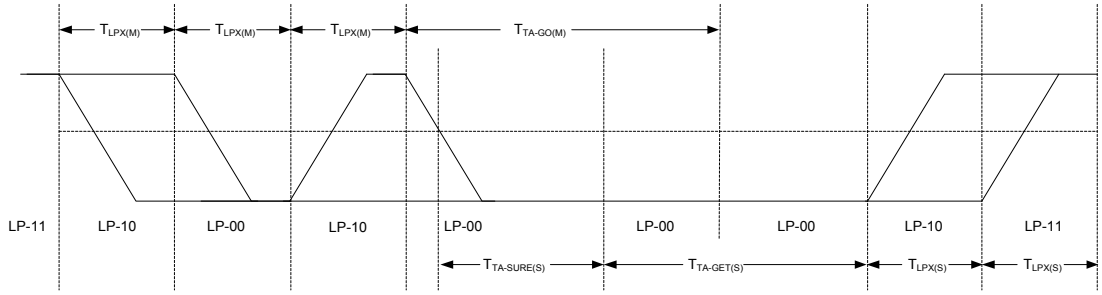


Figure 9-26. Turnaround procedure from MCU to display module

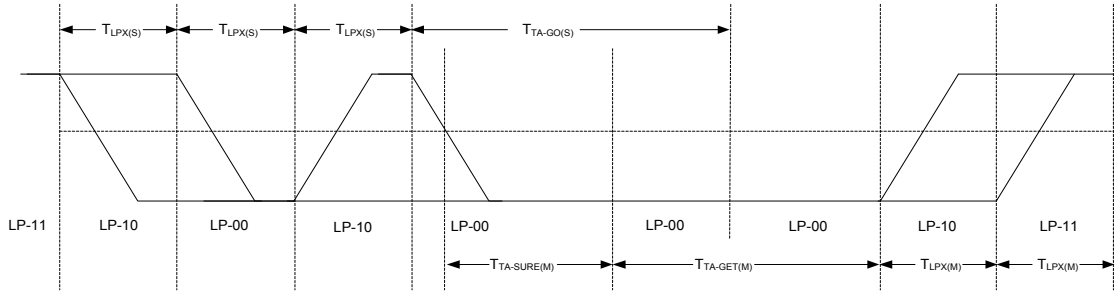


Figure 9-27. Turnaround procedure from display module to MCU

Table 9.7-6. Low power mode timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
TLPX(M)	Transmitted length of any Low-Power state period from MCU to display module	100	–	–	ns
TTA-GET(M)	Time that the MCU drives the Bridge state (LP-00) after accepting control during a Link Turnaround	–	$5*T_{LPX}$	–	ns

Parameter	Description	Min.	Typ.	Max.	Unit
TTA-GO(M)	Time that the MCU drives the Bridge state (LP-00) before releasing control during a Link Turnaround	–	4*T_{LPX}	–	ns
TTA-SURE(M)	Time that the MCU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	T_{LPX}	–	2*T_{LPX}	ns
TLPX(D)	Transmitted length of any Low-Power state period from display module to MCU	100	–	–	ns
TTA-GET(D)	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	–	5*T_{LPX}	–	ns
TTA-GO(D)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround	–	4*T_{LPX}	–	ns
TTA-SURE(D)	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	T_{LPX}	–	2*T_{LPX}	ns

9.8. MIPI DSI Interface Color Coding

The MIPI DSI interface supports RGB565/loosely RGB666/RGB888 pixel formats as defined in MIPI DCS specification.

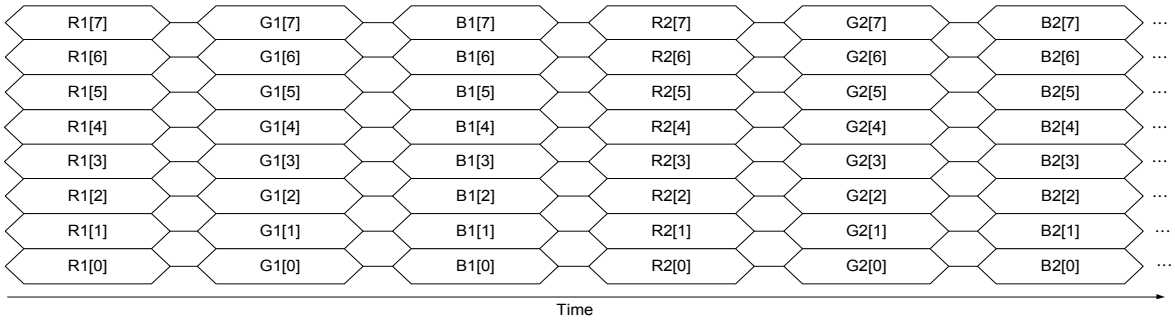


Figure 9-28. Pixel format of RGB565

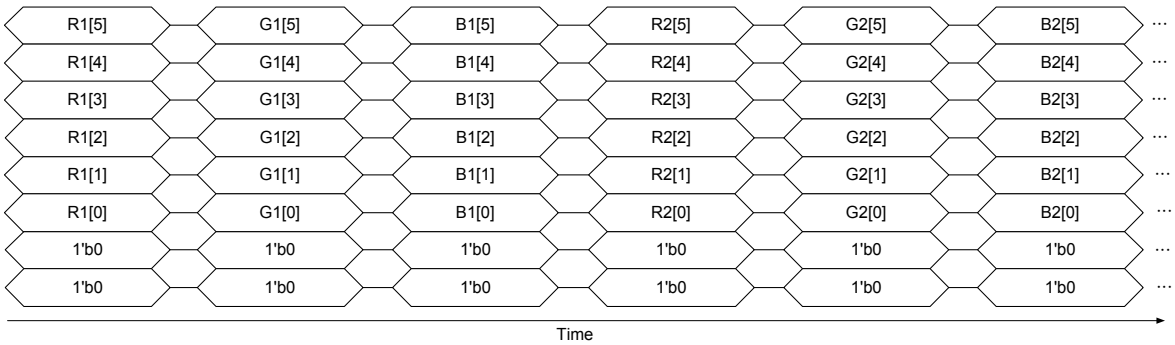


Figure 9-29. Pixel format of loose RGB666

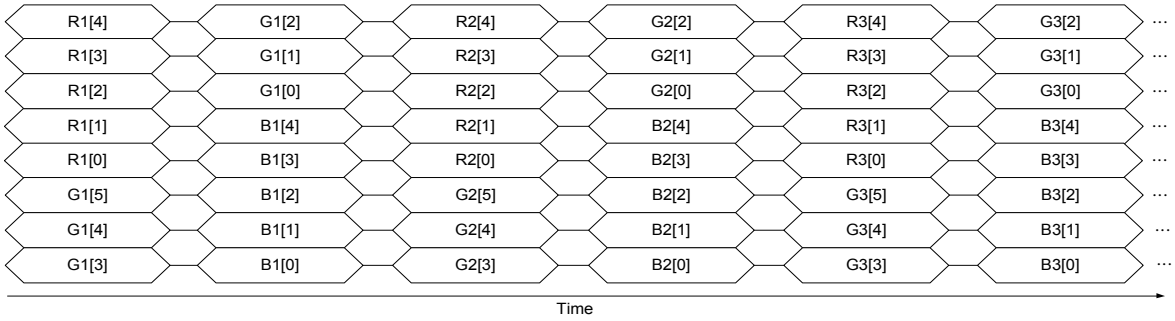


Figure 9-30. Pixel format of RGB565

9.9. Camera interface

The camera interface supports receiving image data streams following the protocol of MTK camera serial interface. There are six main pins for the camera interface, CMPDN, CMRST, CMMCLK, CMCSK, CMCSD0 and CMCSD1. The followings are the pin descriptions.

Table 9.9-1. I/O Port of MTK camera serial interface

Pin name	Direction	Description
CMPDN	Output	Power down sensor
CMRST	Output	Reset sensor
CMMCLK	Output	Camera master clock to sensor
CMCSK	Input	Camera serial clock from sensor
CMCSD0	Input	Camera serial data 0 from sensor
CMCSD1	Input	Camera serial data 1 from sensor

The maximum supported size is up to VGA at 30fps. Our camera interface also supports YUV422 and RGB565 color format with SDR mode and DDR mode.

9.9.1. Multidata channels

MediaTek camera serial interface can be configured to have one or two data channels. One data channel is the fundamental type. Both the transmitter and receiver should be configured to the same number of data channels. The data transmission order is illustrated in the figures below.

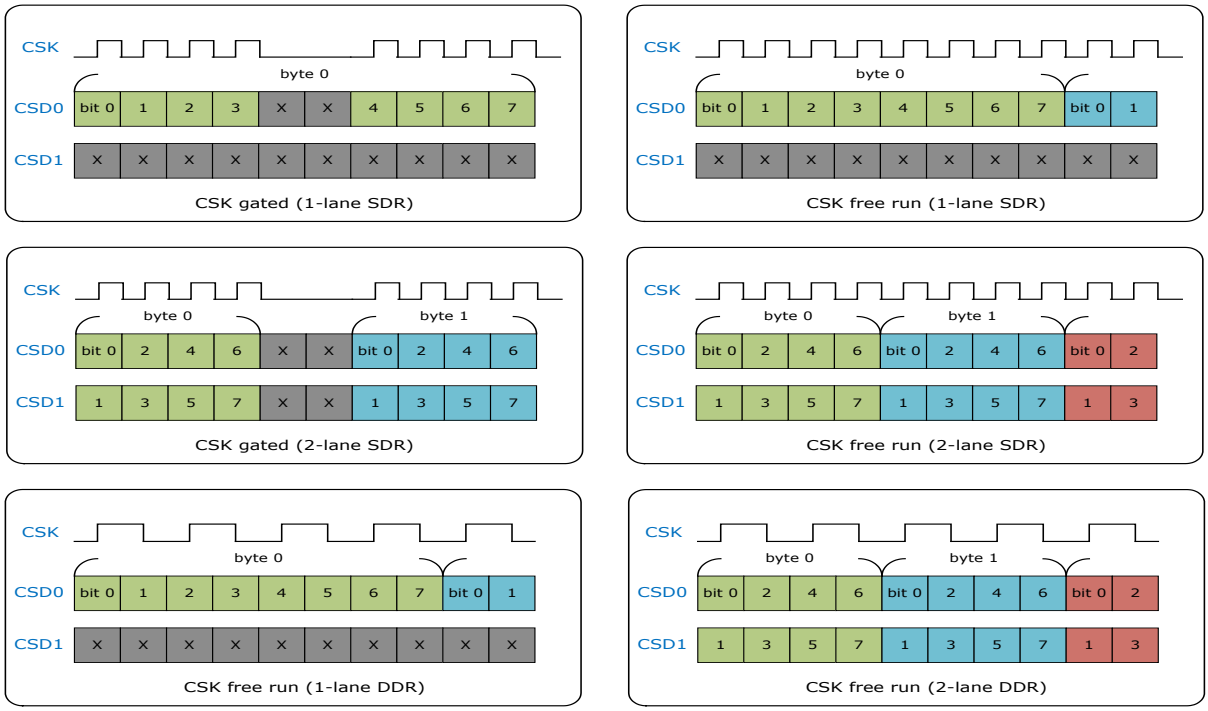


Figure 9-31. Transmission order of multi data channels

9.9.2. Camera interface characteristics

For camera serial interface with SDR mode,

- Camera serial data are sampled at the positive edge or the negative edge of camera serial clock
- CMMCLK: camera master clock to sensor
- CMCSK: camera serial clock from sensor
- CMCSD: camera serial data from sensor

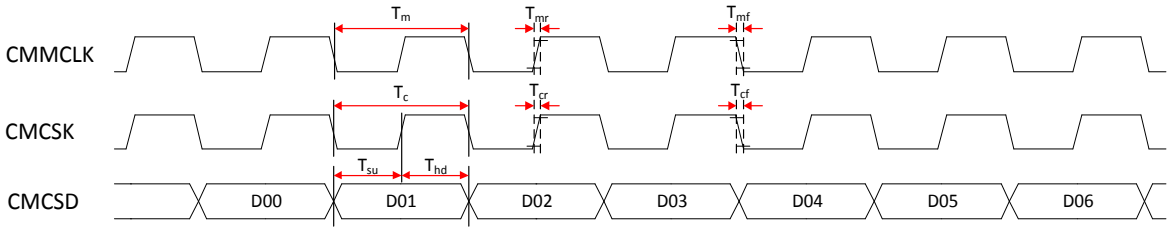


Figure 9-32. I/O port timing of SDR mode

For camera serial interface with DDR mode,

- Camera serial data are sampled at the positive edge and the negative edge of camera serial clock
- CMMCLK: camera master clock to sensor
- CMCSK: camera serial clock from sensor
- CMCSD: camera serial data from sensor

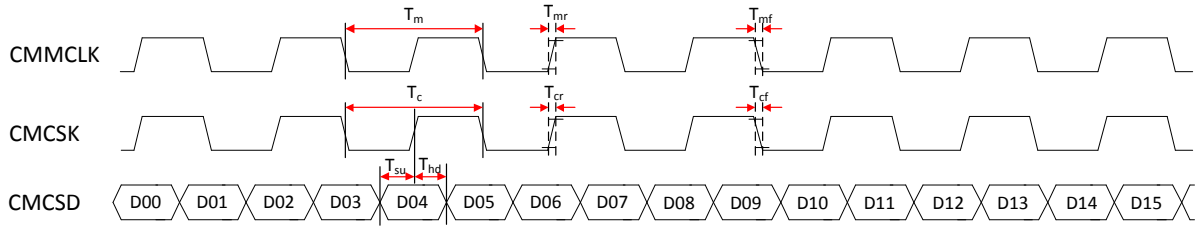


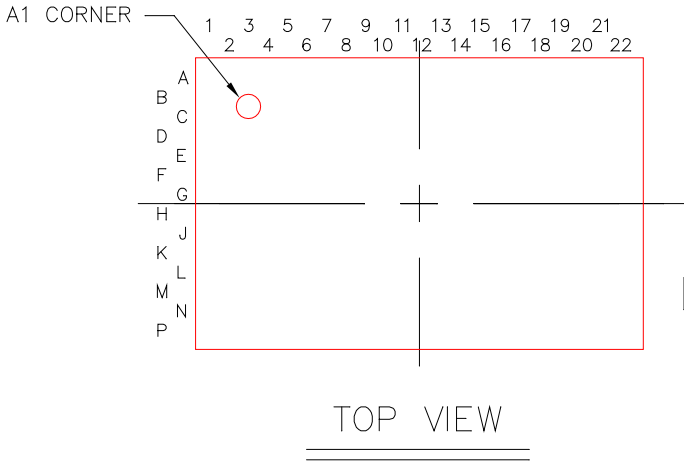
Figure 9-33. I/O port timing of DDR mode

Table 9.9-2. I/O port of MTK camera serial interface timing parameter

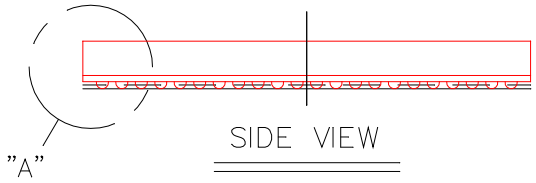
Signal	Direction	Symbol	Parameter	Min.	Max.	Unit	Description
CMMCLK	Output	tm	CMMCLK period	19.23	-	ns	
		tmr	CMMCLK rising time	-	5	ns	
		tmf	CMMCLK falling time	-	5	ns	
CMCSK	Input	tc	CMCSK period	19.23	-	ns	
		tcr	CMCSK rising time	-	1	ns	
		tcf	CMCSK falling time	-	1	ns	
CMCSD	Input	tsu	CMCSD setup time	2	-	ns	
		thd	CMCSD hold time	2	-	ns	

10. Package Information

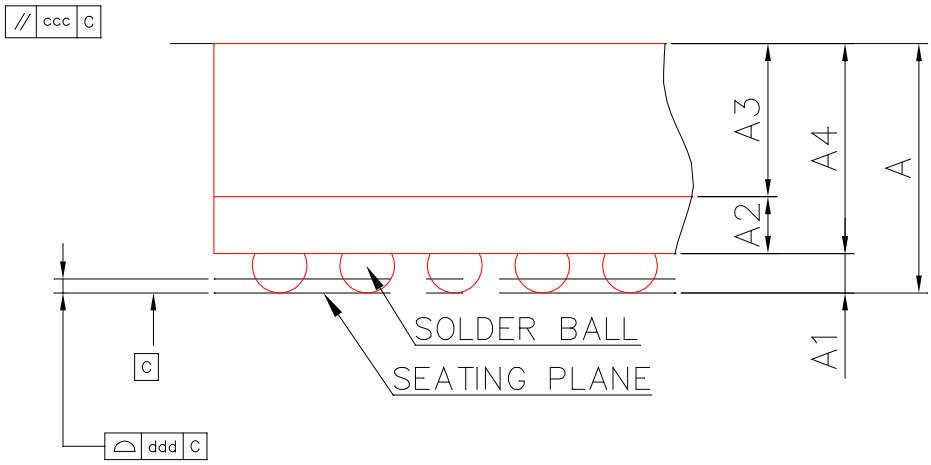
10.1. MT2523G mechanical data of the package



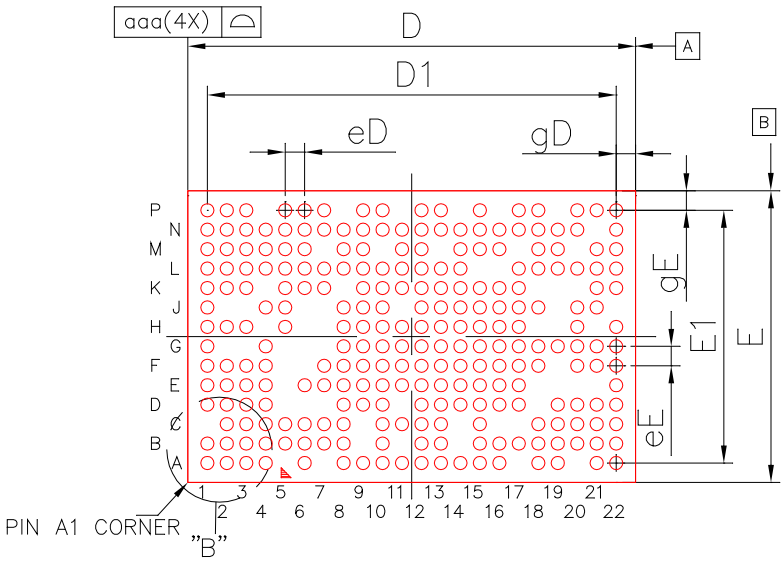
TOP VIEW



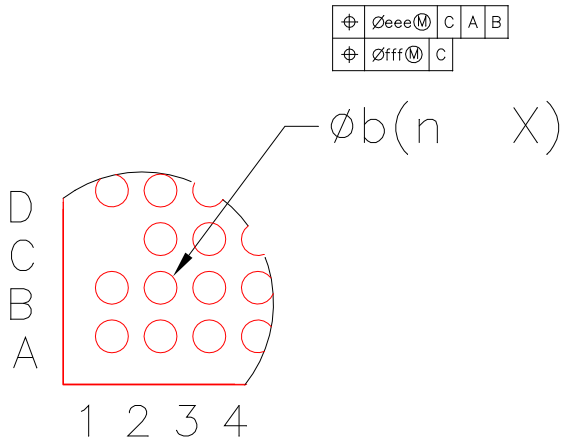
SIDE VIEW



DETAIL : "A"



BOTTOM VIEW



DETAIL : "B"

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	9.10	9.20	9.30
	Y	E	5.90	6.00	6.10
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.70 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.78	0.83	0.88
Total Thickness		A	-	-	1.05
Ball Diameter				0.25	
Ball Stand Off		A1	0.10	0.15	0.20
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		246	
Edge Ball Center to Center	X	D1		8.40	
	Y	E1		5.20	
Edge Ball Center to Package Edge	X	gD		0.40	
	Y	gE		0.40	

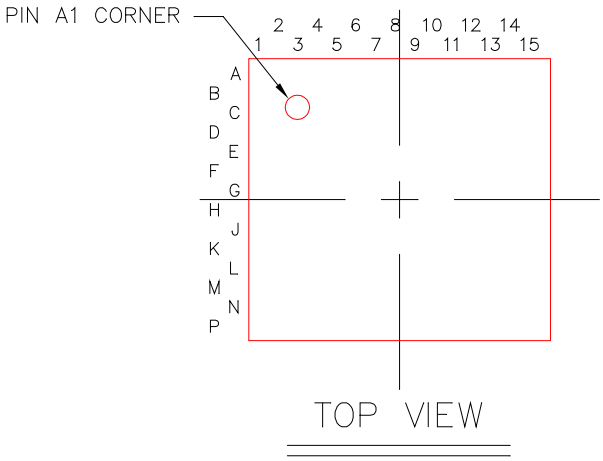
Figure 10-1. Outlines and dimensions of MT2523G TFBGA 9.2 mm*6 mm, 246-ball, 0.4mm pitch package

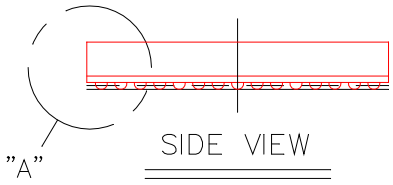
10.2. MT2523G thermal operating specifications

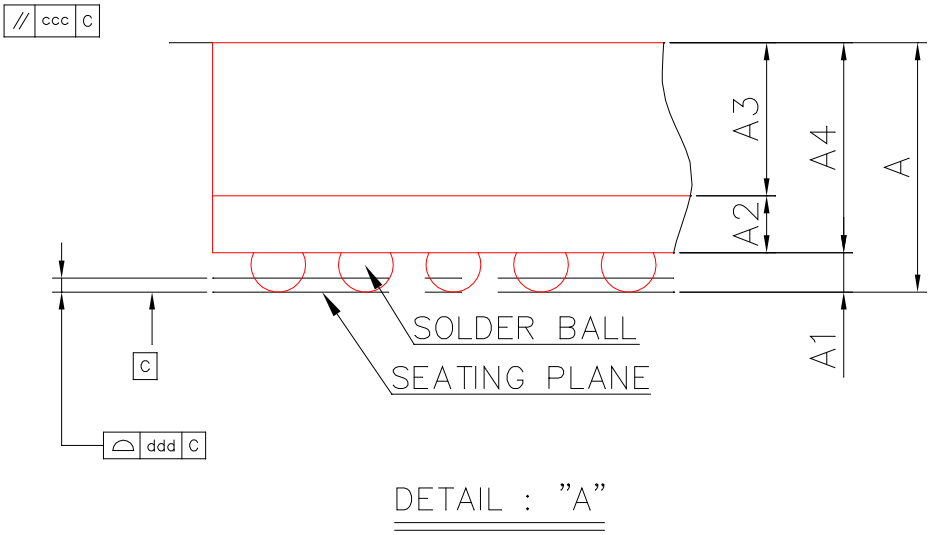
Table 10.2-1. MT2523G thermal operating specifications

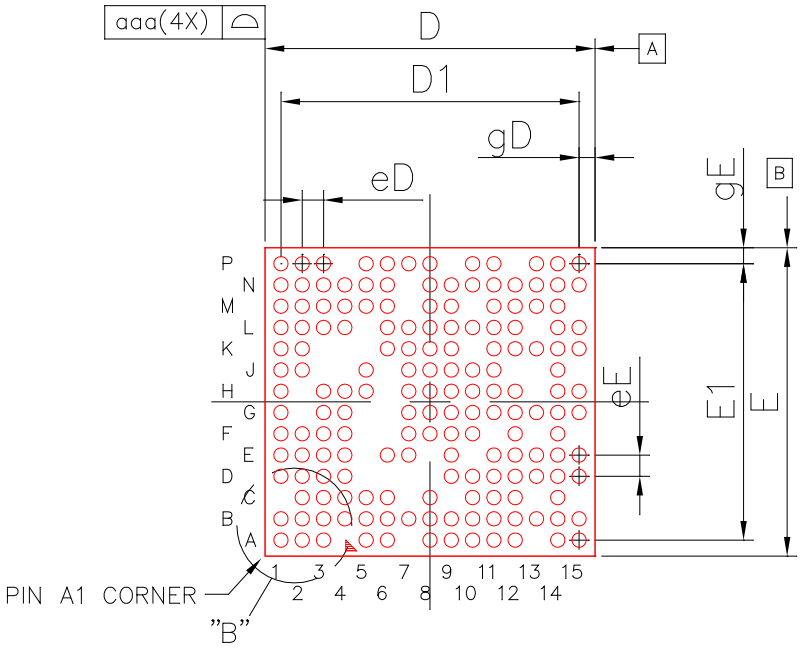
Description	Value	Unit
Thermal resistance from device junction to package case	14	C/W
Maximum package temperature	65	Deg C
Maximum power dissipation	0.7	W

10.3. MT2523D and MT2523S package mechanical data

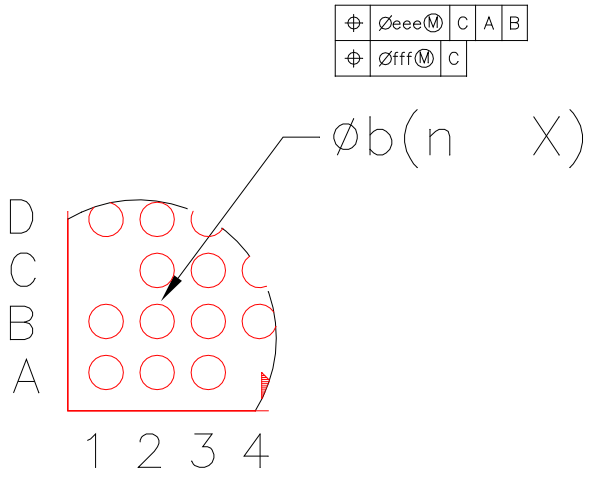








BOTTOM VIEW



DETAIL : "B"

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			TFBGA		
Body Size	X	D	6.10	6.20	6.30
	Y	E	5.70	5.80	5.90
Ball Pitch	X	eD	0.40		
	Y	eE	0.40		
Mold Thickness		A3	0.70 Ref.		
Substrate Thickness		A2	0.13 Ref.		
Substrate+Mold Thickness		A4	0.78	0.83	0.88
Total Thickness		A	-	-	1.05
Ball Diameter			0.25		
Ball Stand Off		A1	0.10	0.15	0.20
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa	0.05		
Mold Flatness		ccc	0.10		
Coplanarity		ddd	0.08		
Ball Offset (Package)		eee	0.15		
Ball Offset (Ball)		fff	0.05		
Ball Count		n	165		
Edge Ball Center to Center	X	D1	5.60		
	Y	E1	5.20		
Edge Ball Center to Package Edge	X	gD	0.30		
	Y	gE	0.30		

Figure 10-2. Outlines and dimensions of MT2523D and MT2523S TFBGA 6.2 mm*5.8 mm, 165-ball, 0.4mm pitch package

10.4. MT2523D and MT2523S thermal operating specifications

Table 10.4-1. MT2523D thermal operating specifications

Description	Value	Unit
Thermal resistance from device junction to package case	14.23	C/W
Maximum package temperature	85	°C
Maximum power dissipation	0.55	W

10.5. MT2523 series lead-free packaging

The MT2523 series platform is provided in a lead-free package and meets RoHS requirements.

11. Ordering Information

11.1. MT2523 series top marking definition

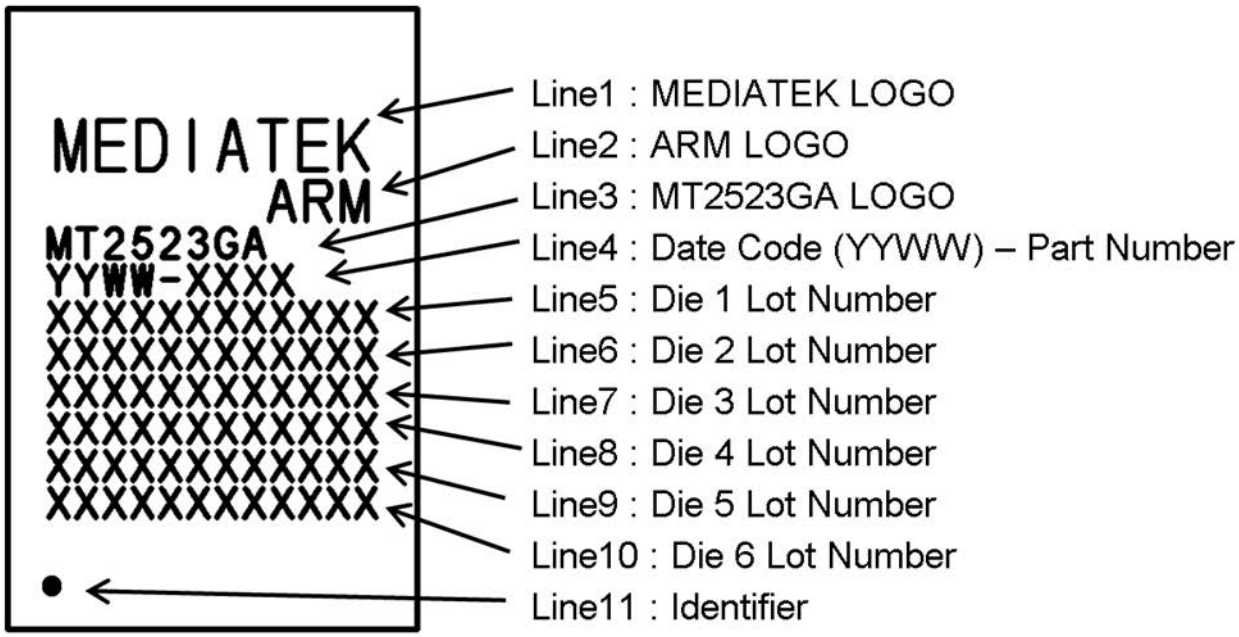


Figure 11-1. Mass production top marking of MT2523G

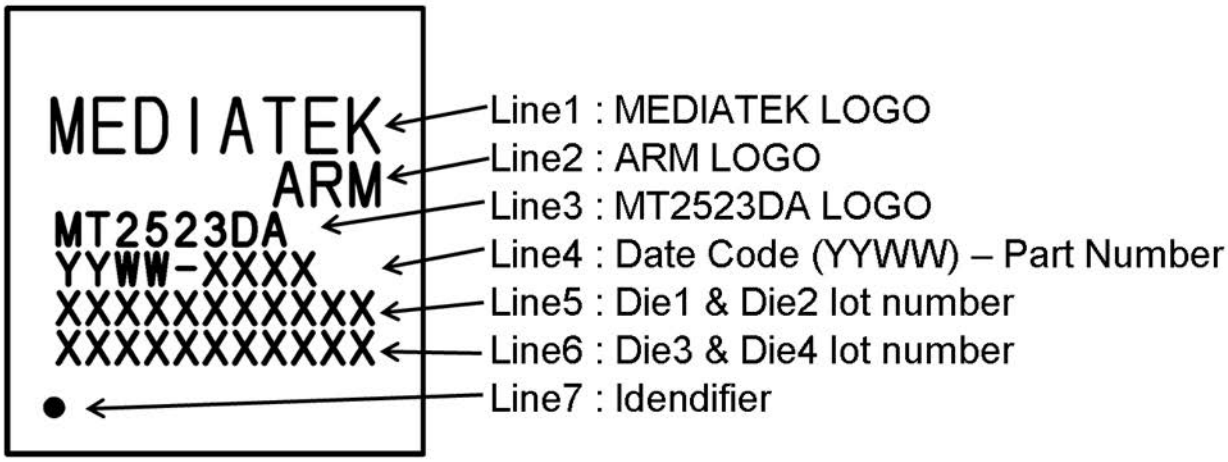


Figure 11-2. Mass production top marking of MT2523D

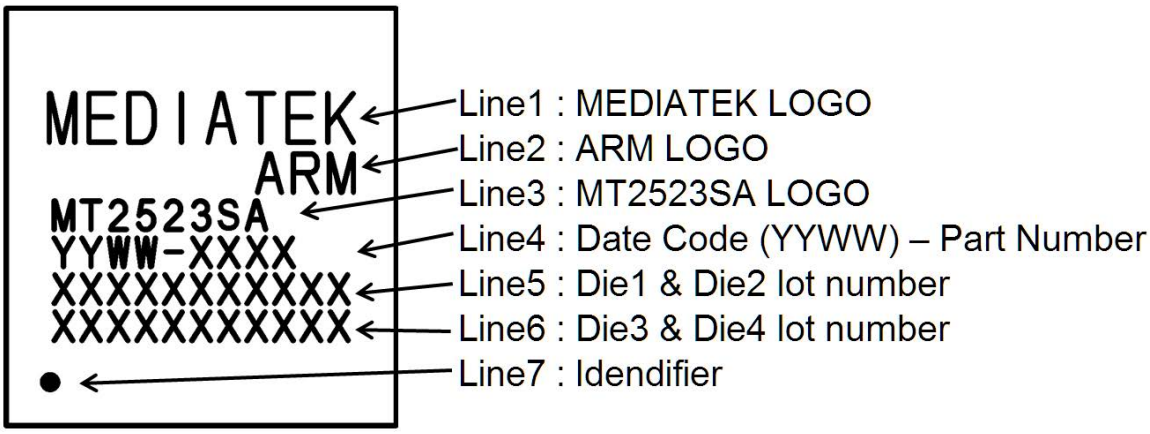


Figure 11-3. Mass production top marking of MT2523S

Table 11.1-1. Ordering information

Product number	Package	Description
MT2523GA	TFBGA	9.2mm*6mm, 246-ball, 0.4mm pitch Package, non-security version
MT2523DA	TFBGA	6.2mm*5.8mm, 165-ball, 0.4mm pitch Package, non-security version
MT2523SA	TFBGA	6.2mm*5.8mm, 165-ball, 0.4mm pitch Package, non-security version