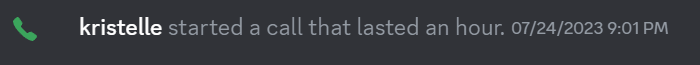
ELECTENG/COMPSYS 209 Minutes

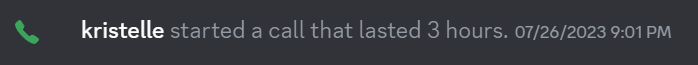
# Meeting 1 - Labs

* Time - 9pm-10pm
* Date - 24/07/23
* Attendance - All present
* Where - Online
* Summary:
  + Discussed Lab 1 tasks to be completed
  + Set targets to be achieved at the time.
* Proof of Meeting -



# Meeting 2 - Labs

* Time - 9pm-12am
* Date - 26/07/23
* Attendance - All present
* Where - Online
* Summary:
  + Met to finish off lab 1 quiz
  + Cross-verified answers before submitting
  + Basic preparation for the first interview
* Proof of Meeting -



# Meeting 3 - Labs

* Time - 8:30pm-10pm
* Date - 07/08/23
* Attendance - All present
* Where - Online
* Summary:
  + Clarified confusions regarding task 4
  + Had doubts regarding the RC filter. Mainly the bode plot and how to calculate the bode magnitude and phase
  + Also had a doubt in Q4.4 with regards to why we shouldn’t choose a breakpoint frequency too close to the fundamental frequency
  + Cleared all doubts and head on to finish quiz for lab 2
* Proof of Meeting -   
  

# Meeting 4 - Labs

* Time - 12pm-4pm
* Date - 08/08/23
* Attendance - All present
* Where - Engineering Building level 3
* Summary:
* Proof of Meeting -

# Meeting 5 - Labs

* Time - 8pm-9pm
* Date - 14/08/23
* Attendance - All present
* Where - Online
* Summary:
  + Completed Lab 3 quiz together
  + Helped each other with the code for Task 4
* Proof of Meeting -



# Meeting 6 - Labs

* Time - 9pm-12am
* Date - 20/08/23
* Attendance - All present
* Where - Online
* Summary:
  + Attempted to create a comparator together
  + Calculated our Vth and Vtl threshold ranges
  + Finished UART for progress review
* Proof of Meeting -

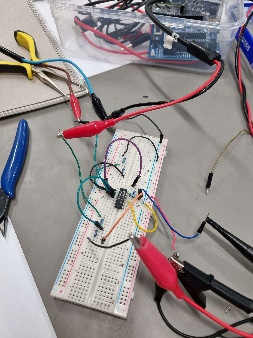


# Meeting 7 - Labs

* Time - 9pm -11.30pm
* Date - 21/08/23
* Attendance - All present
* Where - Online
* Summary:
  + Finished the comparator and checked resistor values
  + Added comparator to a final implementation
  + Chose all the resistor values
  + Verified the circuit
* Proof of Meeting -



# Meeting 8 - Prototyping

* Time – 11am-4pm
* Date - 31/08/23
* Attendance – All present
* Where – In person
* Summary:
  + For the voltage and current sensing circuits, we realized during the breadboarding that instead of using two resistors in parallel for the feedback loop we can just use one resistor
  + Instead of using different resistors for the voltage sensing circuit we replaced all 4 resistors as 100k ohms for simplicity.
  + Came across an issue where for the non-inverting terminal, only one resistor was connected. Same with the inverting terminal that had the feedback loop connected to it. We had to modify the breadboard circuit to resolve that issue.
  + The issue was with the ground connection. We had established a separate ground connection that was not fully connected with the circuit. We modified the circuit so that everything was with respect to the opamp ground.
* Proof of Meeting -   
    
  

# Meeting 9 - Prototyping

* Time - 11am-6pm
* Date – 01/09/23
* Attendance – All present
* Where – In person
* Summary:
  + To achieve a lower VoL, we are going to make a modification in our design by implementing a 2nd order filter.
  + We designed the 2nd order filter using a breakpoint of 10khz
  + Analog testing - changed resistor values to be within E12 resistors. Our breadboard circuit matched with our simulations on LTSpice.
  + Could not test first order filters for voltage and current sensing because 16nF capacitors were not available
  + Regulator: Rin1 changed to 22 ohms, RL1 changed to 56 ohms, 5V is maintained
  + Voltage Divider + Buffer: R13 changed to 47k and R14 changed to 33k, we will get 2.06V instead of 2.1V. We have checked all E12 resistors and it is the closest we divider we can get
* Proof of Meeting –

A white electronic device with a screen and buttons

Description automatically generated

# Meeting 10 - Prototyping

* Time - All day
* Date – 04/09/23
* Attendance – All present
* Where - In person
* Summary:
  + Did breadboard prototyping for regulator cct. Achieved the expected output
  + Started tracing for the through hole PCB design
  + Started working on SMT design on the side
* Proof of Meeting – A person standing in front of a machine

  Description automatically generated

# Meeting 11 – Prototyping and PCB design

* Time – All day
* Date – 07/09/23
* Attendance - All present
* Where – In person
* Summary:
  + Finished prototyping the circuit and finalised values
  + Planned the design on the SMT PCB
  + Received feedback from lecturers
* Proof of Meeting – source: trust me bro

# Meeting 12 - Soldering

* Time – 4pm-6pm
* Date – 22/09/23
* Attendance – All present
* Where – In person
* Summary:
  + Everyone attempted to try SMT soldering
  + Figured out how to read SMT resistor values and capacitors
* Proof of Meeting - A hand holding a plastic bag with small objects

  Description automatically generated

# Meeting 13 - Software

* Time – 12pm-10pm
* Date – 15/10/23
* Attendance – All present
* Where – In person
* Summary:
  + Tried to sample voltage and current values at the same time.
  + Plotted our raw ADC values into excel to check periods.
  + Got told that we were reading our ADC values wrong (we were polling when we weren’t supposed to)
  + Realised that we can use our comparator to check for zero crossings. Tried to implement this, but our code was slightly wrong.
  + Created backup code for single conversion
* Proof of Meeting – check github

# Meeting 14 – Completed Code and PCB

* Time – 12pm – 9pm
* Date – 16/10/23
* Attendance – All present
* Where – In person
* Summary:
  + Integrated rising edge detection for ADC conversion correctly.
  + Compiled all parts of the code.
  + Completed soldering.
* Proof of Meeting - A hand holding a green circuit board

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