Files
*.GTO - Top Overlay
*.GTP - Top Paste
*.GTS - Top Solder
*.GTL - L1
*.G1 - L2 (GND)
*.G2 - L3
*.GBL - L4
*.GBS - Bottom Solder
*.GBP - Bottom Paste
*.GBO - Bottom Overlay
*.GM1 - Board Outline
*.GM12 - Fab Notes
*.GD1 - Drill Drawing
*.GG1 - Drill Guide

Layer Stack Table: JLC3313

BOARD INFORMATION

Minimum Track: 146um
Minimum Gap: 100um
Minimum Through Hole VIA: 0.20mm (drill). Drilling: L1-L4

1. REMOVE ALL NON-FUNCTIONAL INNER LAYER PADS.

2. THIS BOARD CONTAINS IMPEDANCE CONTROLLED TRACKS, TRACK AND GAP SIZES ARE AS FOLLOWS:

TYPE;	Impedance;	Layer (Reference);	Width (um);	Gap (um);
SE;	50 ohm;	L1(L2), L4(L3);	146	
DIFF;	90 ohm;	L1(L2), L4(L3);	180;	170;

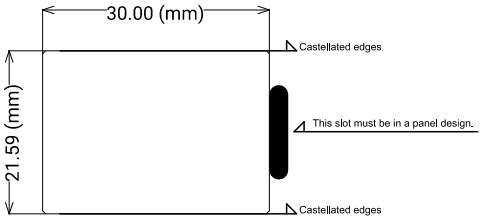
3. FINISHED PANEL THICKNESS IS NOT CRITICAL: TO BE APPROXIMATELY 1.6mm

4. SURFACE FINISH: Immersion Gold (ENIG)

5. SOLDER RESIST: APPLY TO BOTH SIDES COLOR - MATT GREEN

6. COMPONENT IDENT: COLOR TO BE WHITE

7. PANEL BY PCB MANUFACTURER



ALL ARTWORK VIEWED FROM TOP SIDE	PRJ TITLE = Core_ESP32-S3_JLC_PCB	REV = A
LAYER NAME = Fab Notes	PRJ # = None	DRAWN BY JW
CONTACT = john.kim@libmcu.org	GENERATED = 2023-02-12 18:52:15	