

[illegible]

A battery voltage of 2.8 V to 4.2 V is scaled down to 377mV to 565mV.

The image shows a detailed PCB layout for the NRF52840-QIAA-R. It features two ICs, U4A and U4B, with their pin connections and component values. The layout includes a power supply section with a 3V3 regulator, a crystal oscillator (OSC1), and various passive components like capacitors and inductors. The ICs are connected to a USB interface (ANT, VSS_PA, AD4, AD6, D+, D-) and a SWO pin. The layout also shows connections to a CS# pin, a SCL pin, and a WP# pin. The components are labeled with their values and the ICs are labeled with their part numbers.

U4A: NRF52840-QIAA-R

Pin Connections:

- OSC1: 4, 1 (GND), 3 (+3V3), 2 (VDD, CLK)
- SIT1532AC-J5-DCC-32.768E
- P0.00/XL1: D2
- P0.01/XL2: A1
- P0.02/AIN0: P0.03/SPI_MOSI
- P0.03/AIN1: P0.04/AIN2
- P0.04/AIN3: P0.05/AIN3
- QSPI_DATA3: L1
- QSPI_nCS: M2
- QSPI_SCK: N1
- QSPI_DATA2: P0.06, P0.07, P0.08, P0.09/NFC1, P0.10/NFC2, P0.11, P0.12, P0.13, P0.14, P0.15, P0.16, P0.17, P0.18/RESET, P0.19, P0.20, P0.21, P0.22, P0.23/UART_TX, P0.24, P0.25/UART_RX, P0.26/miRQ_BQ
- nRESET: AC15
- YLVGREEN: D4
- R9: 510R
- R14: 100K
- C10: 1uF
- R15: 10K
- ANT: H23
- VSS_PA: F23
- AD4: USB_D_N
- AD6: USB_D_P
- D+: W23
- D-: W24
- SWO: V23
- P1.07/BUTTON: P2
- QSPI_DATA1: R1
- QSPI_DATA0: A20
- P1.12/I2C_SCL: B19
- P1.13/I2C_SDA: B17
- P1.15/SPI_nCS: A16
- P0.27/EN_VBAT_MON: A14
- P0.28/SPI_CLK: B11
- P0.29/SPI_MISO: A10
- P0.30/AIN6: B9
- P0.31/VBAT_MON: A8

U4B: NRF52840-QIAA-R

Pin Connections:

- VDD: W1
- VDD: B1
- VDD: AD23
- VDD: AD14
- VDD: A22
- VDD: Y2
- VDDH: B3
- DCC: AB2
- DCCH: AB2
- VBUS: AD2
- XC1: B24
- XC2: A23
- SWDCLK: AA24
- SWDIO: AC24
- DECUSB: AC5
- EXP: B7
- VSS: B7
- C1: 4.7uF
- C12: 4.7uF
- C13: 100nF
- C14: 100nF
- C15: 100nF
- C17: 8pF
- X1: 32 MHz
- C23: 80pF
- C19: 1nF
- C20: 1uF
- C21: 100pF
- C22: 100nF

U5: MX25V1635E

Pin Connections:

- CS#: 1
- SCLK: 6
- SI(100): 5
- SO(101): 2
- WP#(102): 3
- HOLD#(103): 4

The diagram shows two pin headers, J2 and J3, for the Double_Header_1x11_2_54 connector. Header J2 has 11 pins with the following connections: Pin 1 to +3V3, Pin 2 to P0_20, Pin 3 to P0_22, Pin 4 to P0_04/AIN2, Pin 5 to P0_05/AIN3, Pin 6 to P0_19, Pin 7 to P0_21, Pin 8 to P0_23/UART_TX, and Pin 9 to P0_25/UART_RX. Header J3 has 11 pins with the following connections: Pin 1 to +VIN_SV0, Pin 2 to +VSYS, Pin 3 to +VBAT, Pin 4 to P0_29/SPL_MISO, Pin 5 to P0_28/SPL_CLK, Pin 6 to P0_03/SPL_MOSI, Pin 7 to P1_15/SPI_nCS, Pin 8 to P1_13/I2C_SDA, and Pin 9 to P1_12/I2C_SCL. Pins 10 and 11 of both headers are unconnected.

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