

1

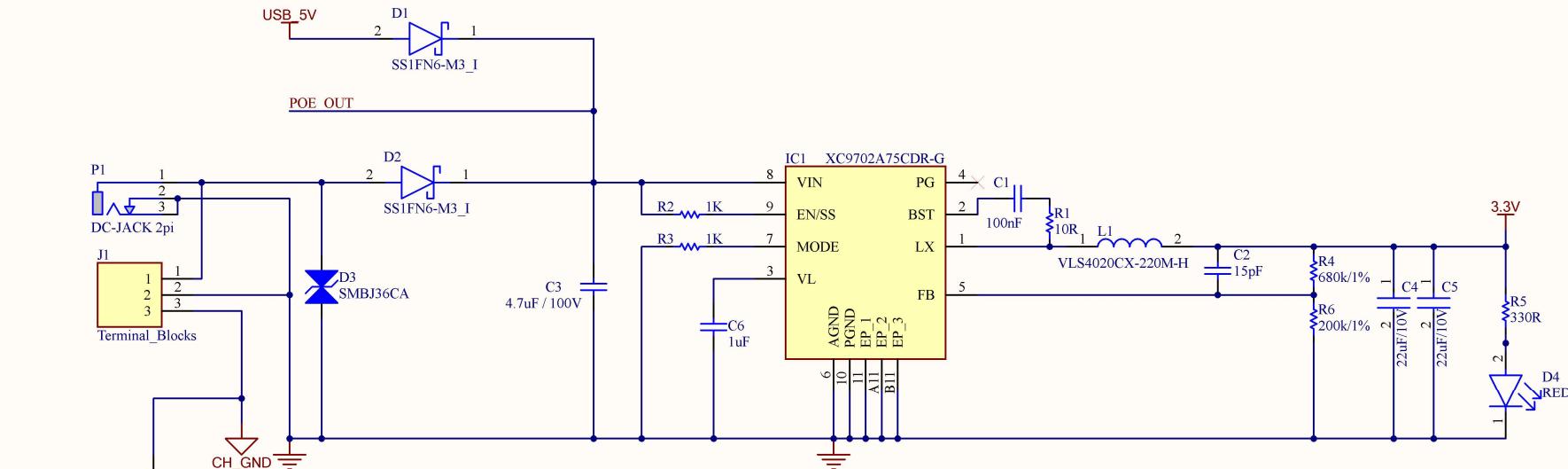
2

3

4

A

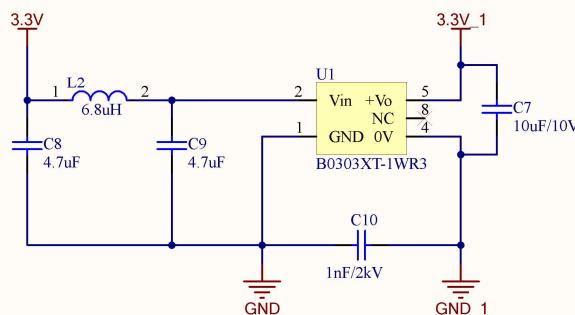
A



B

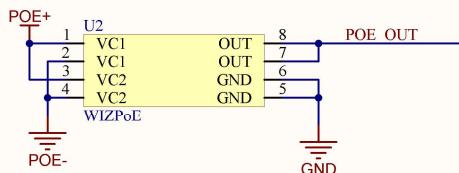
B

232CH_GND



C

C



D

D

Title: W232N_R100.PrjPcb

Page Contents: 01. POWER.SchDoc

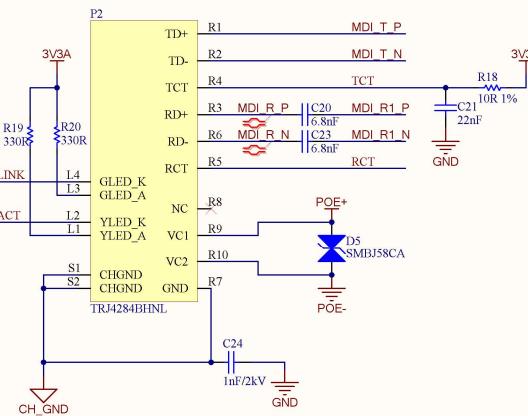
Drawn By: Jaden

Size: A4 Revision: 100

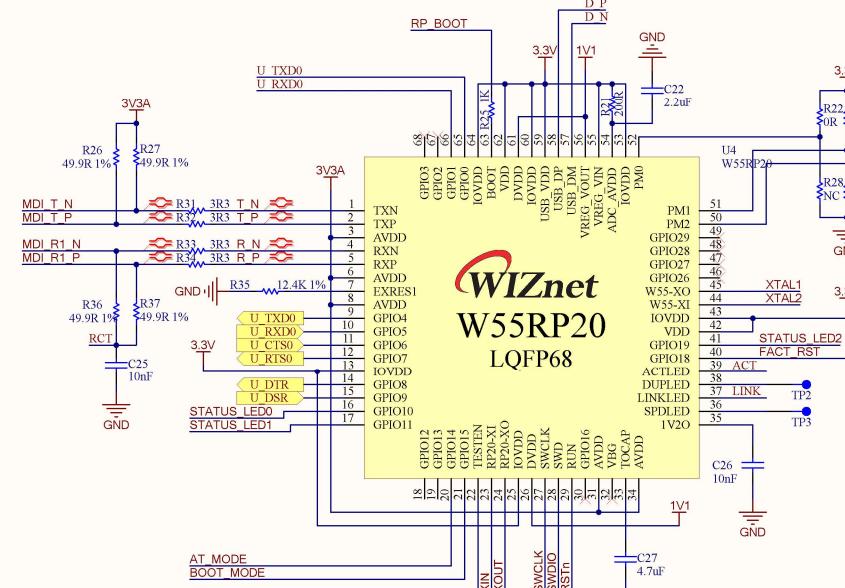
Date: 2024-09-05 Time: 오후 2:24:19 Sheet 1 of 4



A

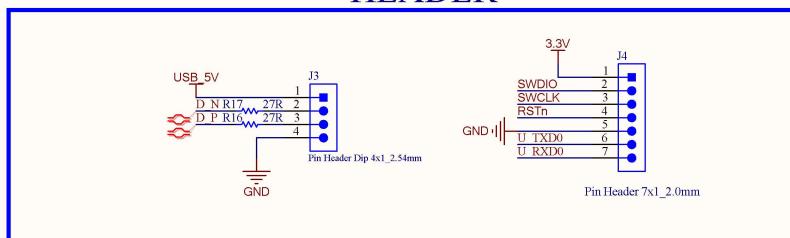


B

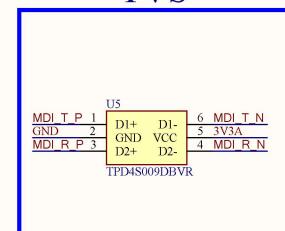


WIZnet
W55RP20
LQFP68

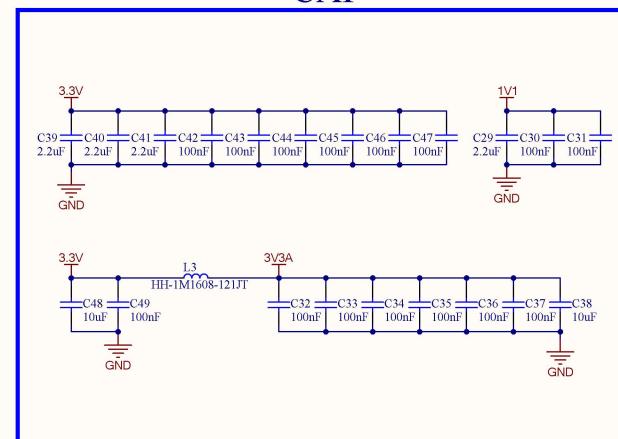
HEADER



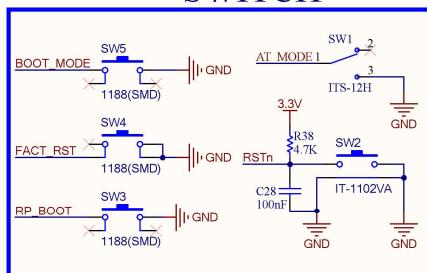
TVS



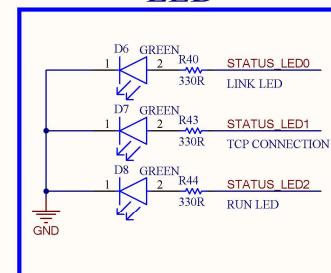
CAP



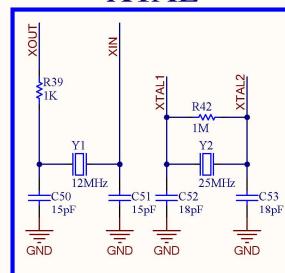
SWITCH



LED



XTAL



Title: W232N_R100.PrcPcb

Page Contents: 02_W55RP20.SchDoc

Drawn By: Jaden

Size A3 Revision: 100

Date: 2024-09-05 Time: 22:24:19 Sheet 2 of 4

WIZnet

1

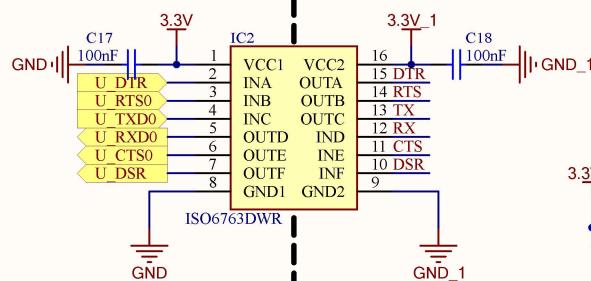
2

3

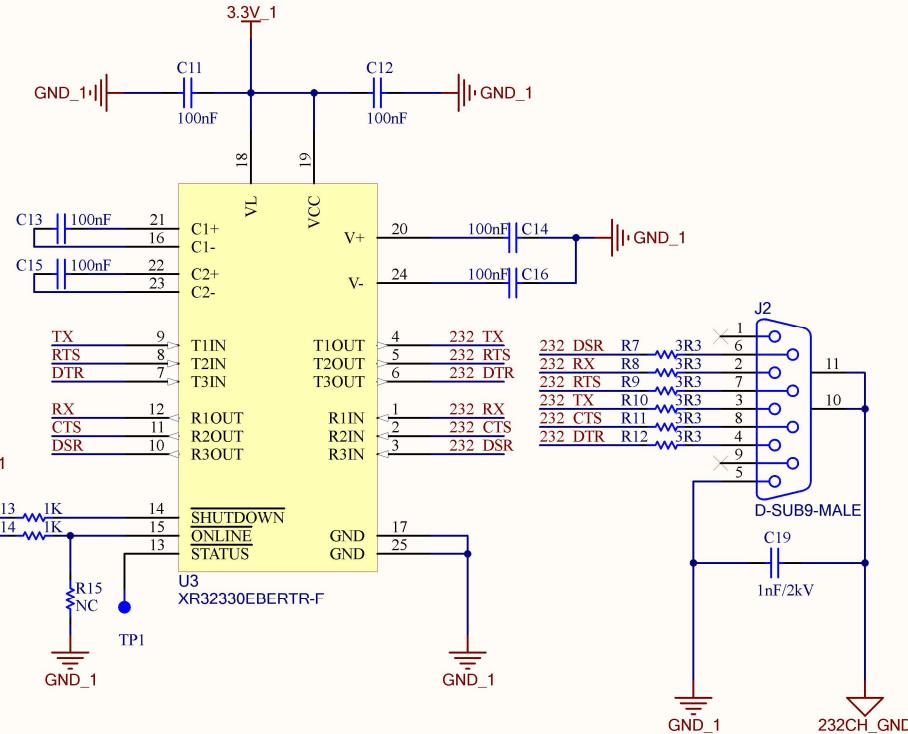
4

A

ISOLATION



B



C

D

Title: W232N_R100.PnjPcb

Page Contents: 03.RS232.SchDoc

Drawn By: Jaden

Size: A4 Revision: 100

Date: 2024-09-05 Time: 오후 2:24:19 Sheet 3 of 4

WIZnct

A

A

B

B

C

C

D

D

Funtion	Type	Pin Num	GPIO Num	Description
Debug UART Tx	O	65	0	Output Debug Messages
Debug UART Rx	I	66	1	
DATA UART TX PIN	O	9	4	TX pin for Data UART transmission
DATA UART RX PIN	I	10	5	RX pin for Data UART reception
DATA UART CTS PIN	I	11	6	CTS pin for Data UART flow control
DATA UART DTR PIN	O	12	7	RTS pin for Data UART flow control
DATA DTR PIN	O	14	8	DTR pin for Data UART control
DATA DSR PIN	I	15	9	DSR pin for Data UART control
STATUS PHYLINK PIN	O	16	10	Output High when the PHY link is established
STATUS TCPCONNECT PIN	O	17	11	Output High when TCP connection is active
HW TRIG PIN	I	20	14	When this pin is Low during a device reset, it enters AT Command Mode
BOOT MODE PIN	I	21	15	When this pin is Low during a device reset, it enters Boot Mode
FAC RSTn PIN	I	40	18	Holding Low for more than 5 seconds triggers a factory reset

Title: W232N_R100.PjPcb

Page Contents: 04.Pin_Description.SchDoc

Drawn By: *

Size: A4 Revision: 100

Date: 2024-09-05 Time: 오후 2:24:19 Sheet 4 of 4

