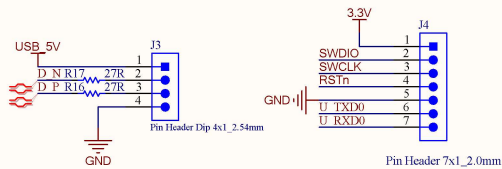


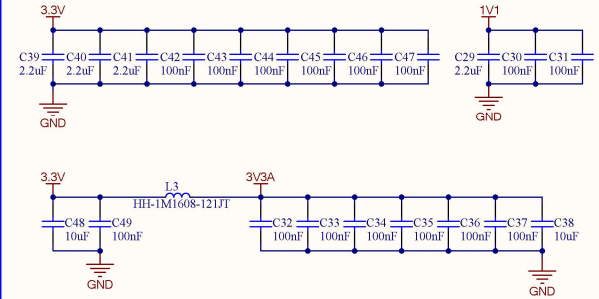
## HEADER



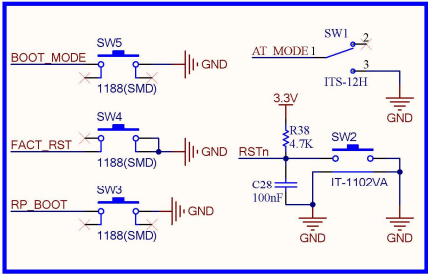
## Pin Description

Function	Type	Pin Num	GPIO Num	Description
Debug_UART_Tx	O	65	0	Output Debug Messages
Debug_UART_Rx	I	66	1	
DATA_UART_TX_PIN	O	9	4	TX pin for Data UART transmission
DATA_UART_RX_PIN	I	10	5	RX pin for Data UART reception
DATA_UART_CTS_PIN	I	11	6	CTS pin for Data UART flow control
DATA_UART_RTS_PIN	O	12	7	RTS pin for Data UART flow control
DATA_DTR_PIN	O	14	8	DTR pin for Data UART control
DATA_DSR_PIN	I	15	9	DSR pin for Data UART control
STATUS_PHYLINK_PIN	O	16	10	Output High when the PHY link is established
STATUS_TCPCONNECT_PIN	O	17	11	Output High when TCP connection is active
HW_TRIG_PIN	I	20	14	When this pin is Low during a device reset, it enters AT Command Mode
BOOT_MODE_PIN	I	21	15	When this pin is Low during a device reset, it enters Boot Mode
FACT_RSTn_PIN	I	40	18	Holding Low for more than 5 seconds triggers a factory reset

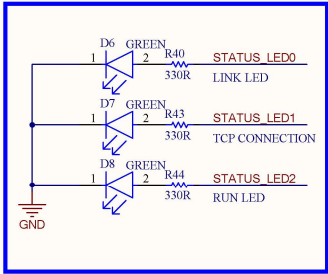
## CAP



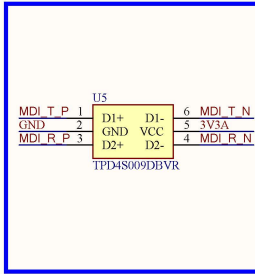
## SWITCH



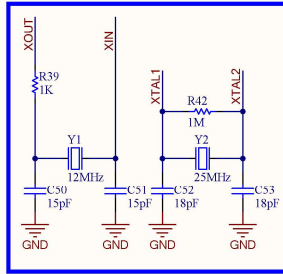
## LED

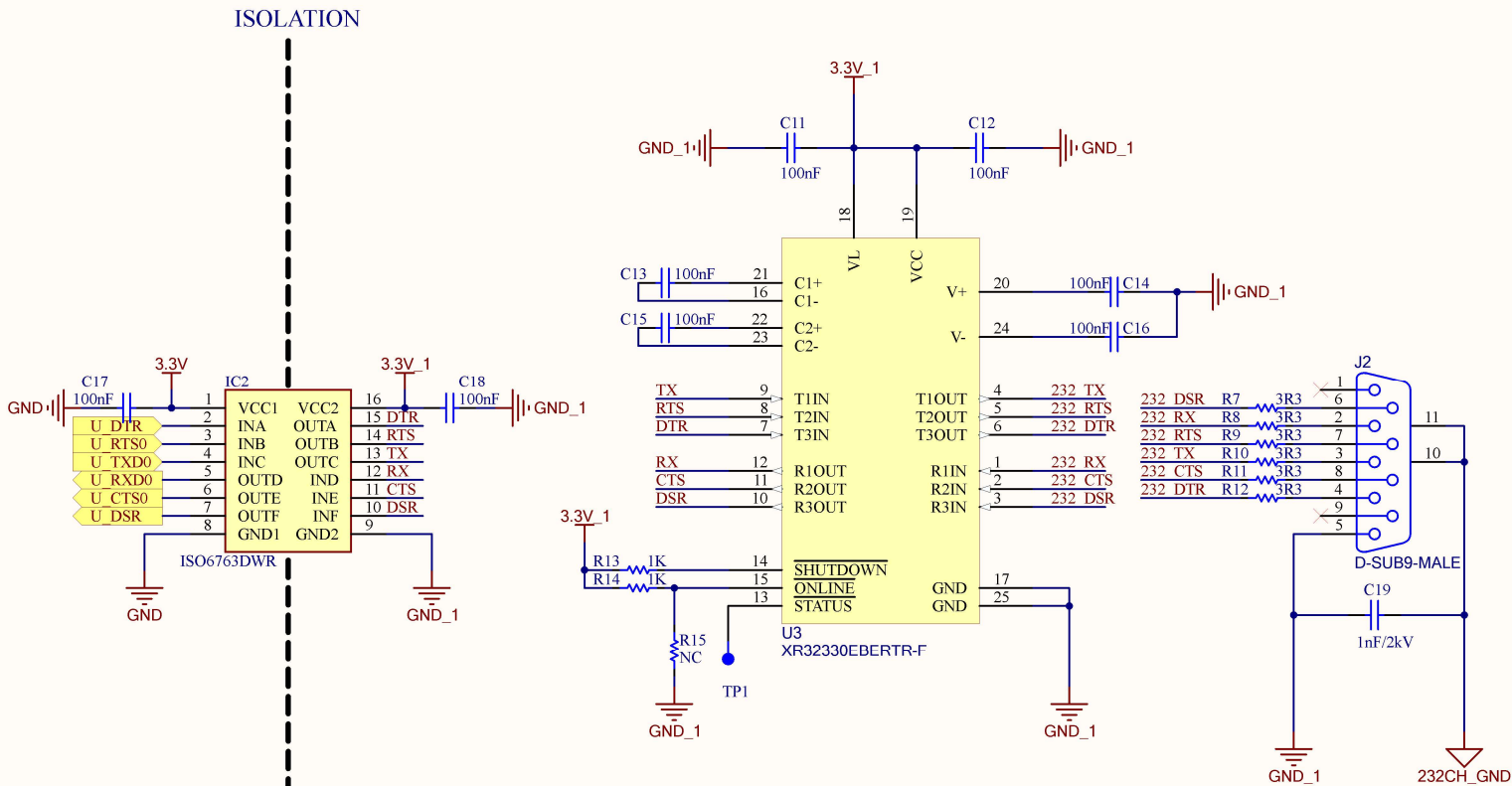


## TVS



## XTAL





Title: **W232N\_R100.PrjPcb**

Page Contents: 03.RS232.SchDoc

Drawn By: Jaden

Size: A4

Date: 2024-09-05 Time: 오전 11:25:35

Revision: 001

Sheet 4 of 6

**WIZnet**