WIZ-IP55 User Manual

V1.0

☞ For more information, visit our website at http://www.wiznet.io

Document Revision History

Version	Date	Note
V1.0	2025/08/07	First release

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1 Introduction

1.1 Overview

WIZ-IP55 is a network offloading module that integrates the W5500 chip (with built-in PHY physical layer and TCP/IP hardware protocol stack) and an RJ45 connector with integrated network transformer. As a plug-and-play component, it enables seamless interface connection between the W5500 and the transformer without the need for additional circuit design.

For users who wish to quickly develop networked systems, WIZ-IP55 is an ideal choice.

Note: For detailed information on the hardware TCP/IP protocol stack, please refer to W5500 datasheet.

The WIZ-IP55 module is composed as follows:

- Network port connector section: Integrated network transformer network port (including W5500 chip, network transformer and RJ45).
- TCP/IP protocol stack and Ethernet MAC: Implemented by W5500 chip.
- Ethernet PHY: Integrated by W5500 chip.

1.1.1 Functional Features

- Supports full hardware TCP/IP protocol: TCP, UDP, WOL, ICMP, IGMPv1/v2, IPv4, ARP, PPPoE
- Supports 8 independent SOCKET concurrent communication
- Supports half-duplex/full-duplex operation mode
- Supports Ethernet power-off mode
- Supports UDP-based network wake-up (WOL) function
- High-speed SPI interface (MODE 0/3)
- Built-in total 32Kbytes of send/receive cache
- Integrated 10BaseT/100BaseTX Ethernet PHY
- Supports Ethernet auto negotiation (full/half-duplex,10Base-T/100Base-TX)
- Operating voltage:3.3V (I/O compatible with 5V signal voltage)
- 19-pin pin header interface
- Package size (length×width×height):32.5×16.5×17.3(mm)
- Compatible with WIZnet's IO module carrier board development board

1.1.2 Product features

- All-hardware TCP/IP protocol stack network chip W5500
- Ethernet
  - 10/100Mbps Adaptive Ethernet
- Connect to the host interface
  - Standard SPI: MISO, MOSI, CLK, CSn
- Power supply
  - Input power supply: 3.3V DC
- Mechanical parameters
  - Dimensions(length×width×height):32.5×16.5×17.3(mm)
- Working temperature
  - Industrial grade:-40 ~ +85℃
- Save Environment
  - -40 ~ +85 ℃,5 ~ 95% RH

1.2 Product Specifications

1.2.1 Electrical Parameters

1.2.1.1 Power Supply Parameters

Unless otherwise specified,the parameters listed in Table 1-1 and Table 1-2 refer to the values at a temperature of 25℃.

Table 1-1 Power Parameters

Numbering	Category	Specification			
		Min	Typical	Max	Organization
VDD	Module voltage	2.97	3.3	3.63	V
I	Module current	152	162	173	mA

1.2.1.2 Power Consumption Parameters

Table 1-2 Power consumption parameters

Working condition	Test value (mA)	Working condition	Test value (mA)
Standby	65	100 Mbps without connection	128
10 Mbps without connection	75	100Mbps for data communication	162
10 Mbps for data communication	79		

1.2.2 Mechanical Dimensions

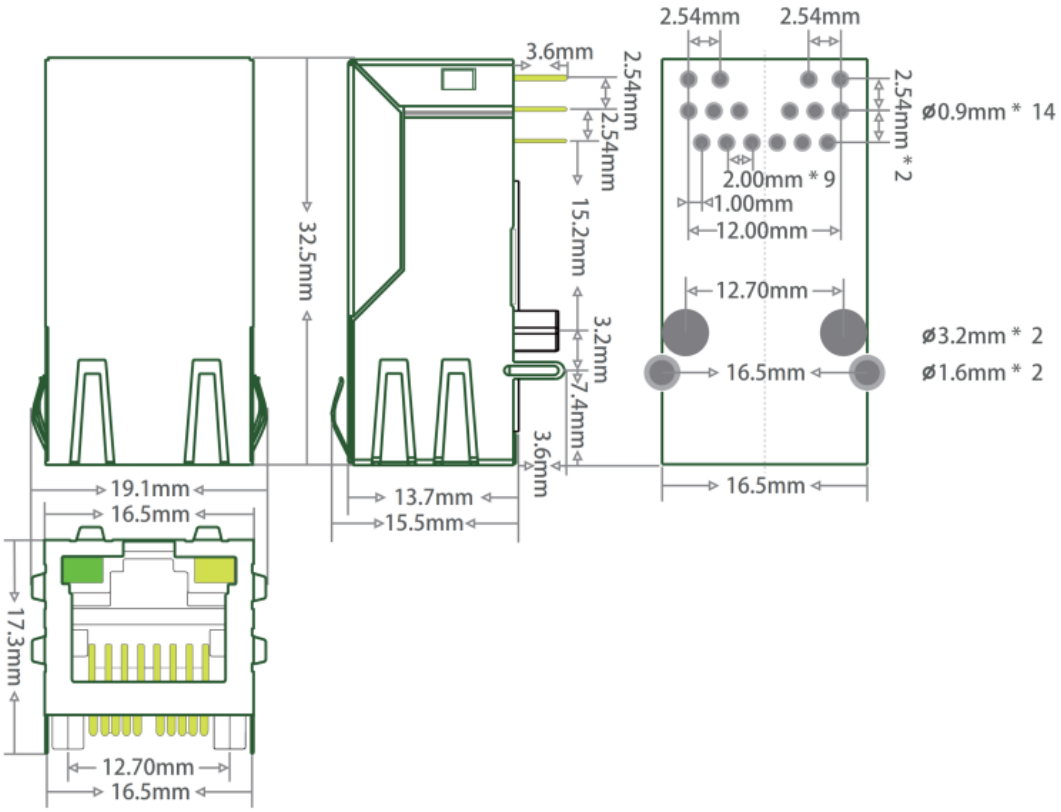

Figure 1-1 All product displays

1.2.3 Temperature Characteristics

Table 1-3 Temperature characteristics

Name	Level	Working temperature	Storage temperature
WIZ-IP55	Industrial grade	-40 ~ +85 ℃	-40 ~ +85 ℃

2 Hardware Section Description

2.1 Pin Layout Description

Now, let's introduce the pins of WIZ-IP55 and the usage of the accompanying IO module carrier board for the evaluation board.

The appearance of WIZ-IP55 is shown in Figure 2-1.

Figure 2-2 shows the pin layout of WIZ-IP55, and Table 2-1 provides the pin description for WIZ-IP55.

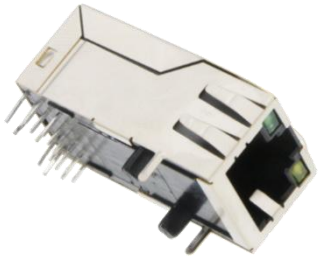

Figure 2-1 The external view of the WIZ-IP55 module

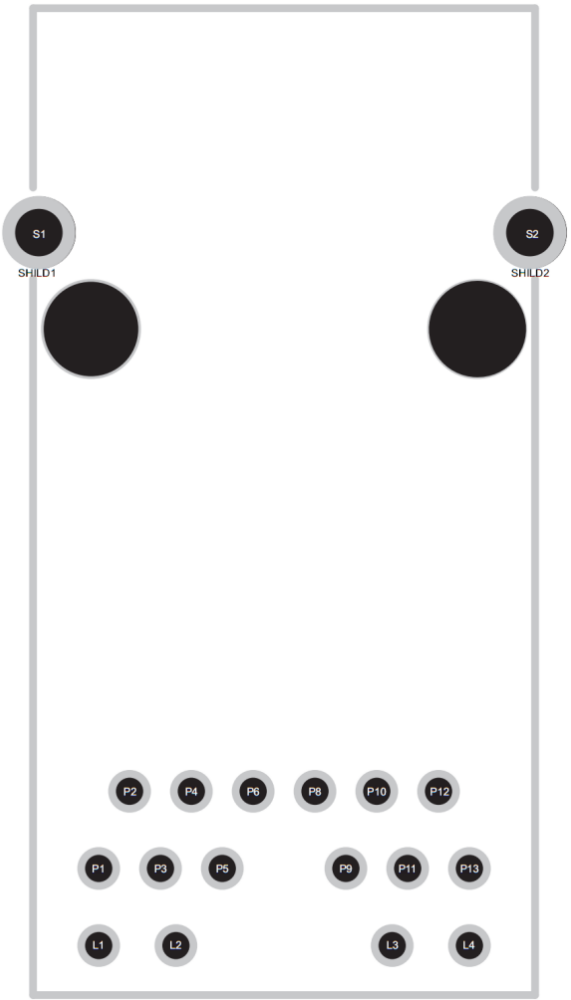

Figure 2-2 Pin Assignment of WIZ-IP55

Table 2-1 Pin Description

Pin number	Pin name	Function
P1	ACT_LED	Data reception/transmission activity indicator light
P2	VCC	3.3V power supply pin
P3	GND	Power ground
P4	CSn	SPI interface chip selects signal pin, with low level as the effective state
P5	CLK	SPI clock input pin
P6	MISO	SPI master input, slave output
P8	MOSI	SPI master output from slave input
P9	INTn	Interrupt output pin, low level is effective
P10	RESETn	Reset pin, low level effective (must be maintained for at least 500us)
P11	NC	Retention function
P12	NC	Retention function
P13	LINK_LED	Network connection indicator light
L1	LED1-	Connect to P1
L2	LED1+	Connected in series with the resistor to VCC
L3	LED2+	Connected in series with the resistor to VCC
L4	LED2-	Connect to P13
S1	SHILD1	Shell
S2	SHILD2	Shell

2.2 Introduction to the Evaluation Board

The IO module carrier board is an evaluation board that facilitates users to test and apply the modules. This evaluation board integrates the mainstream single-chip microcontroller STM32F103RCT6 and the USB to TTL converter chip CP2102.The schematic diagram of the IO module carrier board is shown in Figure 2 and Figure 3.

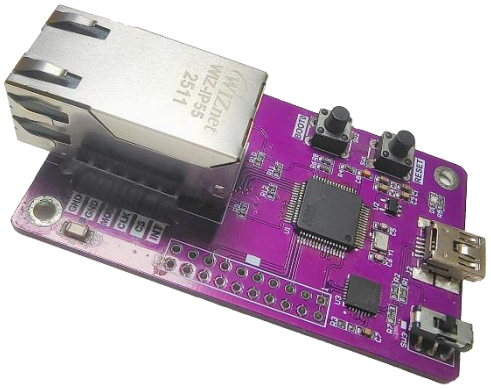

Figure 2-3: Outline drawing of the IO module carrier board

- The USB Mini interface provides 5V DC power supply for the evaluation board and one serial port for the MCU, which can be used for ISP-style program download and data communication testing.
- Key instructions for the IO module carrier board

Table 2-2 IO module carrier board Key Instructions

Numbering	Explanation
RESET（SW1）	Hardware reset button
BOOT（SW2）	Enter the BOOT button of the microcontroller

- Download method for the IO module carrier board program

The IO module carrier board supports the ISP download method. The operation steps are as follows: first, press and hold the BOOT button, then press the RESET button once, and finally release the BOOT button. This will enable you to enter the program download mode. Open the ISP tool of STM32 and select the corresponding firmware to complete the download.

- The reference design schematic diagram of the peripheral circuit for WIZ-IP55 is shown in Figure2-4.

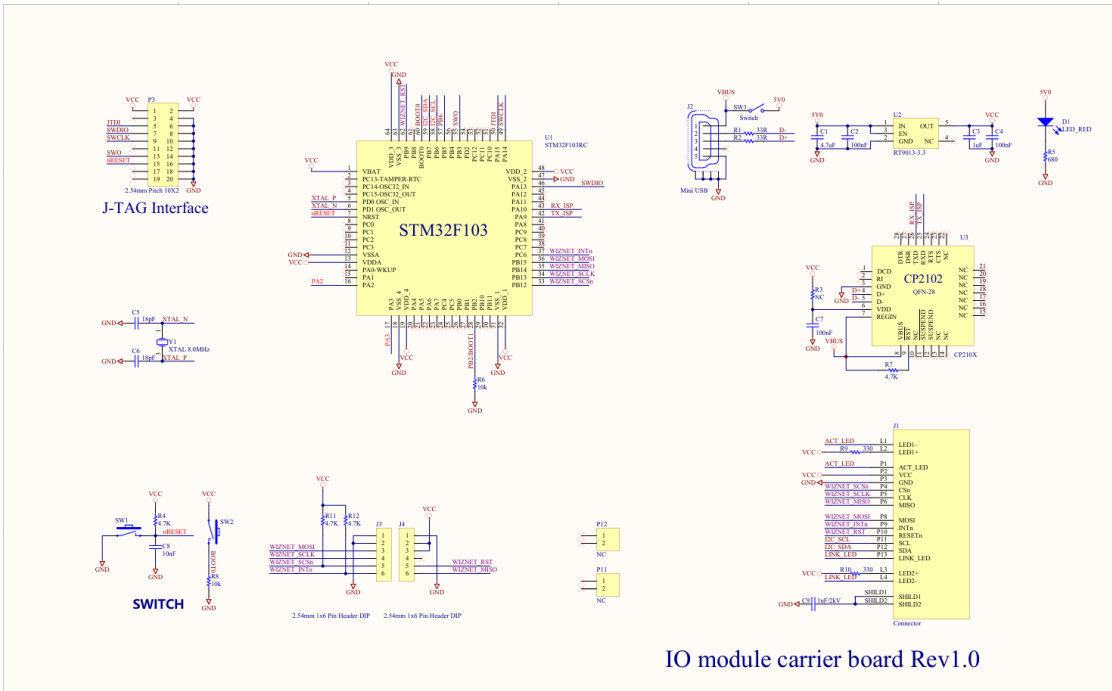

Figure 2-4: Reference design schematic diagram of the peripheral circuit of WIZ-IP55

2.3 Quick Evaluation Board Wiring Instructions

Users can download the corresponding reference code for W5500 from www.w5500.com and burn it onto the IO module carrier board for performance testing and evaluation, as shown in Figure 2-5.

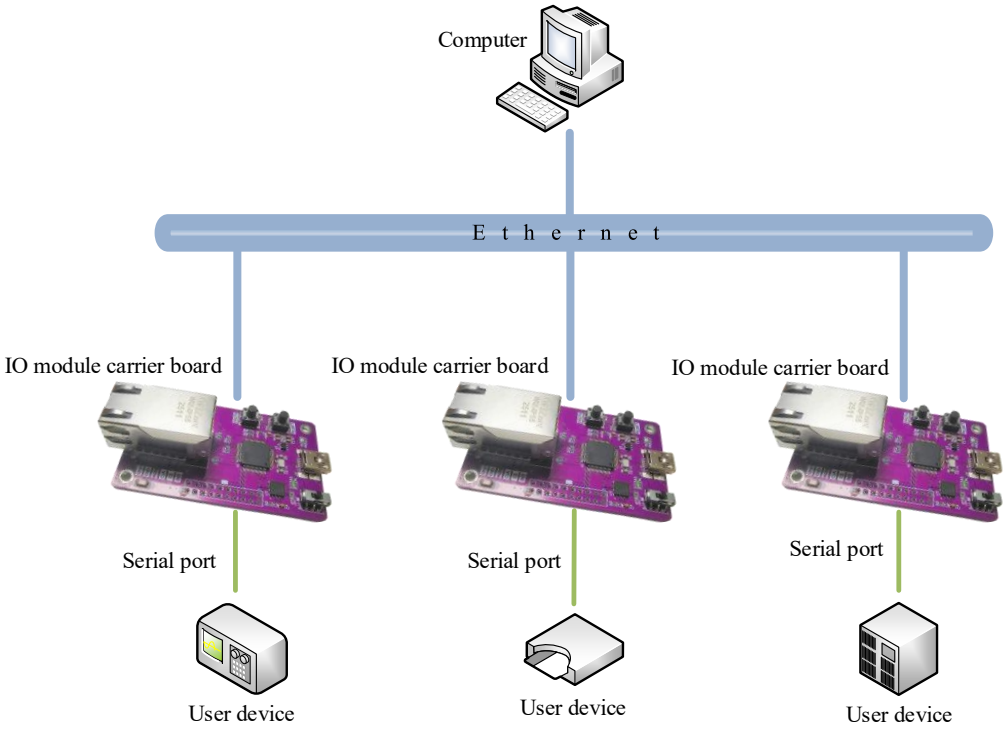

Figure 2-5:Schematic Diagram for Test and Evaluation of IO Module Carrier Board

3 SPI operations

The SPI configuration method of WIZ-IP55 can be found in the W5500 datasheet.

4 Sequence Diagram

4.1 Reset Timing Sequence

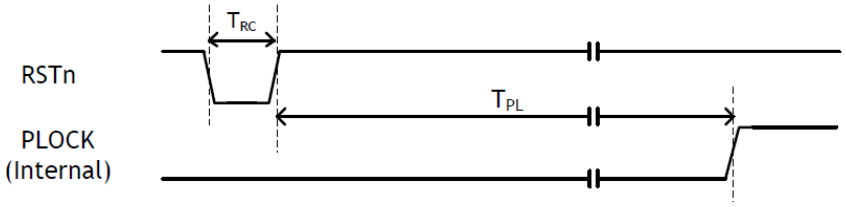

Figure 4-1 Reset Timing

Table 4-1 Reset Timing

Symbol	Description	Min	Max
T_{RC}	Reset Cycle Time	500us	-
T_{PL}	RSTn to internal PLOCK (PLL Lock)	-	50ms

4.2 SPI Timing Sequence

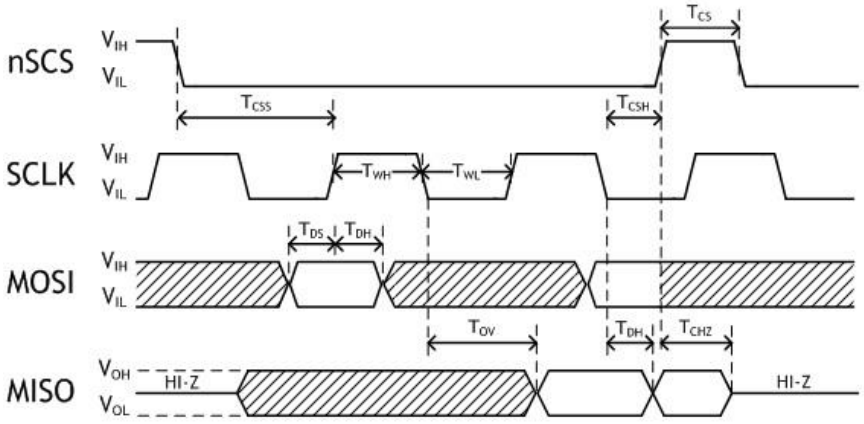

Figure 4-2 SPI Timing

Table 4-2 SPI Timing

Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency	-	80	MHz
T_{WH}	SCK High Time	6	-	ns
T_{WL}	SCK Low Time	6	-	ns
T_{CS}	SCSn High Time	5	-	ns