Vector instructions

Wojciech Muła, 0x80.pl January 2021

Thanks to Roman Kurc & Daniel Lemire for valuable feedback

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- What are **vector instructions**/**SIMD instructions**
- Why are they important
- How do they work
- What are they good for

Where can we find vectors?

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  $v = (1, 2, 3) \Rightarrow$ `int v[3] = {1, 2, 3};` (C/C++/Java)
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  $v = (1, 2, 3) \Rightarrow$ `v = [1, 2, 3]` (Python)
- An array can hold anything, not only bare numbers, but also pixels (images), samples (sound), points (3D models), characters (text)

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$$b = (7, 1, 4, 2, 3, 5, 1, 0)$$

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Suppose we have two vectors of size 8:

$$a = (1, 2, 3, 4, 5, 6, 7, 8)$$

$$b = (7, 1, 4, 2, 3, 5, 1, 0)$$

Their sum c is:

$$c = a + b = (8, 3, 7, 6, 8, 11, 8, 8)$$

How would we add two vectors? – part 3

A program that performs vector addition is quite simple:

```
c[0] = a[0] + b[0]
c[1] = a[1] + b[1]
c[2] = a[2] + b[2]
c[3] = a[3] + b[3]
c[4] = a[4] + b[4]
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c[7] = a[7] + b[7]
```

It can be written with a loop:

```
for (int i=0; i < 8; i++)
    c[i] = a[i] + b[i];
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Despite the form, the number of basic instruction is:

- 16 loads from memory (`a[0..7]` and `b[0..7]`)
- 8 additions (+)
- 8 stores to memory (`c[0..7]`)

Hardware dedicated to vector operations

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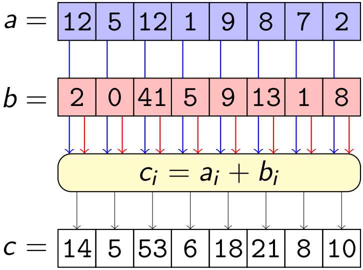
- GPUs usually have SIMD execution units
- Vector instructions are not the only mean of speeding up vector calculation, there are CPUs having *vector architectures* built entirely around the concept of arbitrary length vectors

How vector operations work?

Suppose vectors have 8 elements
Operation is $c = a + b$



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- Most **CPU cores** work in SISD model: *Single Instruction, Single Data*

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Va = vector_load(a);        // Va holds 8 elements
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Vc = vector_add(Va, Vb);    // execute 8 additions
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- Not for all operations such nice scaling is possible
- ...but we can expect significant boost over most of regular CPU instructions

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- Some CPU architectures support only integer operations

Hardware vs software vectors

For instance a 256-bit vector can be used in a program as the following vectors (C/C++ types)

- `int8_t[32]`, `uint8_t[32]`
- `int16_t[16]`, `uint16_t[16]`
- `int32_t[8]`, `uint32_t[8]`
- `int64_t[4]`, `uint64_t[4]`
- `float[8]`
- `double[4]`

Existing SIMD implementations

cryptic name	vendor	year	vector width [bits]
MMX	Intel	1997	64
3DNow	AMD	1998	64
AltiVec	many	1998	128
SSE	Intel	1999	128
—	ARM	2002	32
SSE2	Intel	2001	128
SSE3	Intel	2004	128
SSSE3	Intel	2006	128
SSE4	Intel	2007	128
AVX	Intel	2008	256
XOP	AMD	2010	128
Neon	ARM	2011	64
AVX2	Intel	2013	256
Neon	ARM	2014	128
AVX-512	Intel	2015	512
SVE	ARM	???	1024-4096

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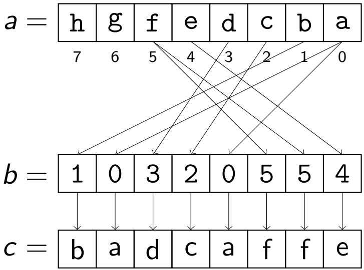
- integer addition / subtraction / type casts using **saturated arithmetic**

Example of shuffle — arbitrary order of elements

Operation is $c = \mathrm{shuffle}(a, b)$



Example of shuffle — reverse

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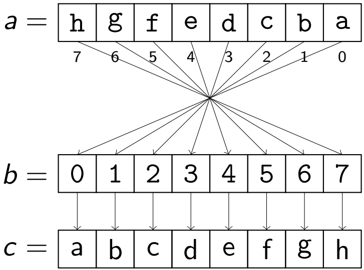

Example of shuffle — broadcast

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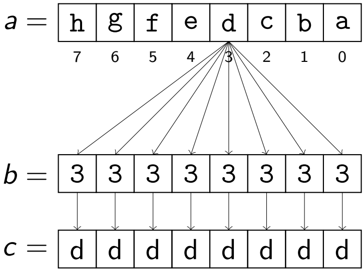
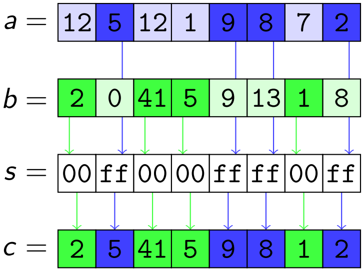


Example of blend

Operation is $c = s \, ? \, a : b$



As a raw bit operations $c = (s \,\mathrm{and}\, a) \,\mathrm{or} (\mathrm{not}\, s \,\mathrm{and}\, b)$

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- Saturated arithmetic is as fast as wrap-around one

Saturated addition example — increase image brightness

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Function `vector_add` can rewritten (*vectorized*) as:

```
void vector_add(float* a, float* b, float* c, size_t N) {
    for (size_t i=0; i < N; i += 8) {
        auto Va = vector_load(a + i);
        auto Vb = vector_load(b + i);
        auto Vc = vector_add(Va, Vb);
        vector_store(c + i, Vc);
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- What if we wanted to port it for another CPU, which is capable to process 16, 32 or 64 numbers?

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- SIMD requires designed data structures to use full power
- ...typical example: instead of a single array of records use separate array for each record's field

More realistic example — signal mixing

Following vector code mixes two signals (image, sound) using linear interpolation

$$c = a \cdot p + b \cdot (1 - p), p \in [0, 1]$$

```
void vector_lerp(float* a, float* b, float* c, size_t N, float p) {
    auto Vp = vector_broadcast(p);      // Vp = [p, ..., p]
    auto Vq = vector_broadcast(1 - p);  // Vq = [1-p, ..., 1-p]
    for (size_t i=0; i < N; i += 8) {
        auto Va  = vector_load(a + i);
        auto Vb  = vector_load(b + i);
        auto Vt0 = vector_mul(Va, Vp); // a * p
        auto Vt1 = vector_mul(Vb, Vq); // b * (1 - p)
        auto Vc  = vector_add(Vt0, Vt1);
        vector_store(c + i, Vc);
    }

    for (size_t i=(N / 8) * 8; i < N; i++)
        c[i] = (a[i] * p) + (b[i] * (1 - p));
}
```

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- Compilers can **autovectorize** loops — they do similar transformation as we did to `vector_add`
- Autovectorization is not as smart as human, but is decent

Signal mixing in practise

This is actual C++ code for signal mixing which uses Intel intrinsics functions for AVX2 extension (full list on Intrinsics Guide)

```
#include <immintrin.h>

void vector_lerp(float* a, float* b, float* c, size_t N, float p) {
    __m256 Vp = _mm256_set1_ps(p);
    __m256 Vq = _mm256_set1_ps(1 - p);
    for (size_t i=0; i < N; i += 8) {
        __m256 Va  = _mm256_loadu_ps(a + i);
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        __m256 Vt0 = _mm256_mul_ps(Va, Vp);
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```

It compiles! `gcc -mavx2 -c vector-lerp-avx2.cpp`

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- . . . our mental model is different
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- Luckily compilers are getting better in autovectorization
- More and more software libraries use SIMD instructions, we can benefit from it without changing our code