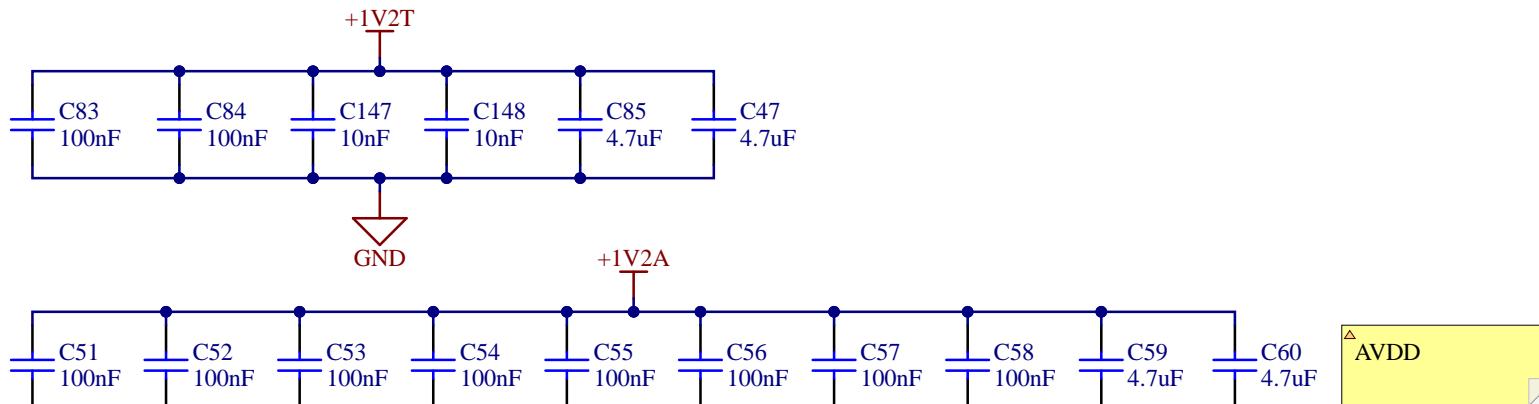
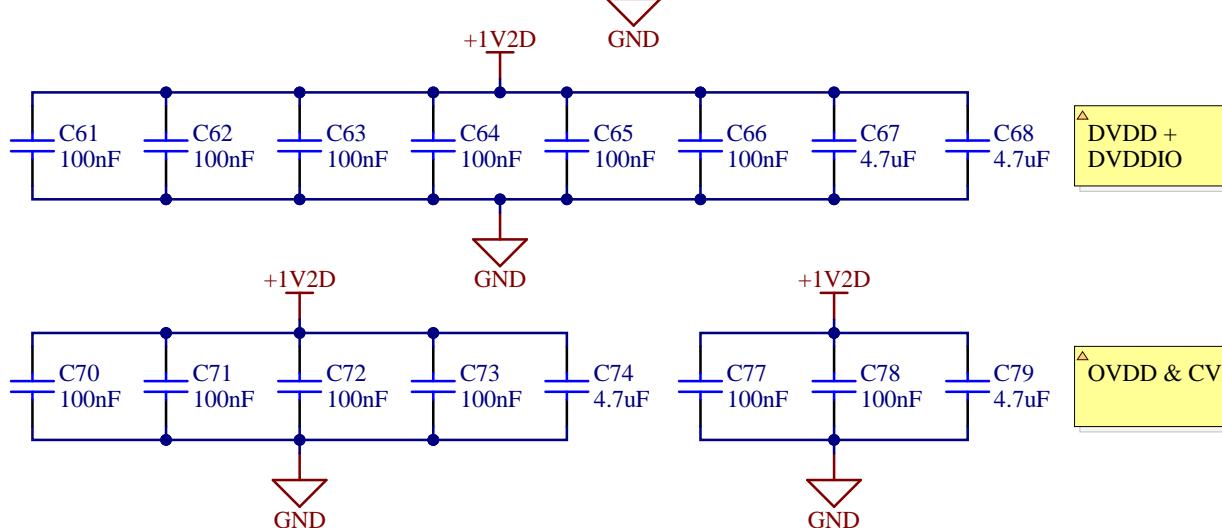


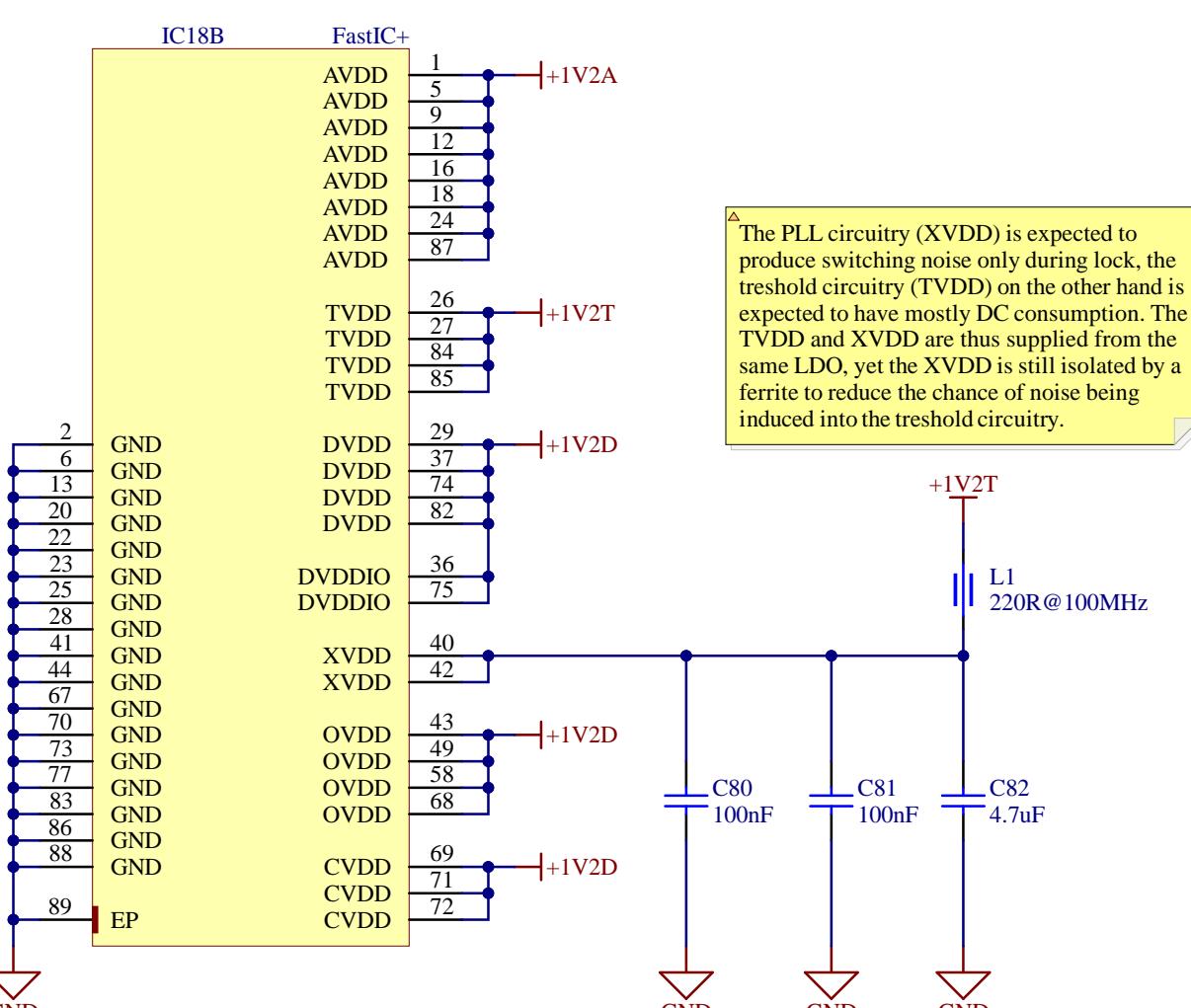
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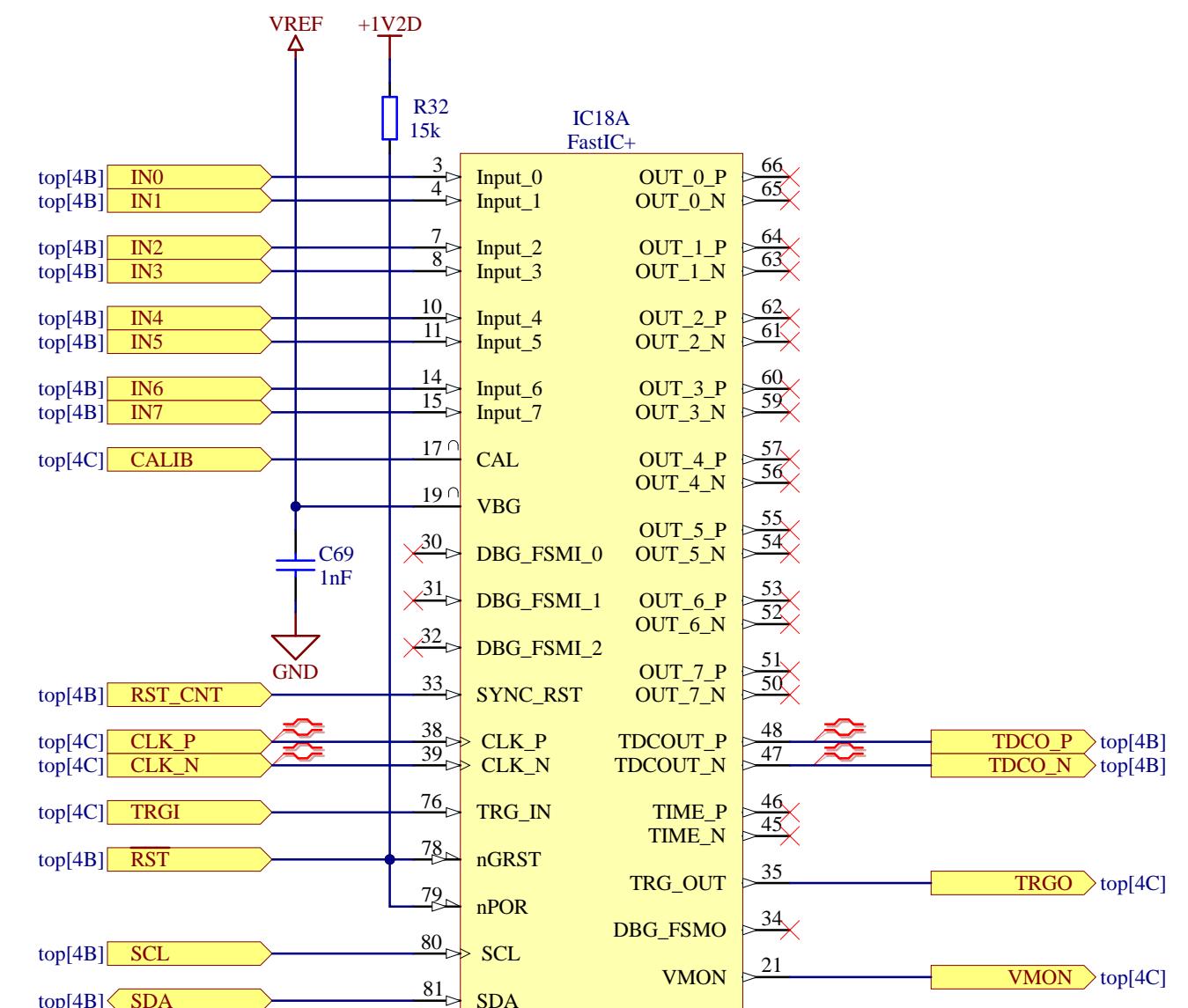
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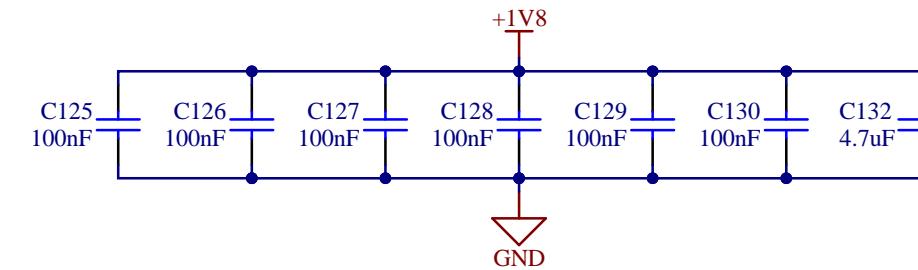
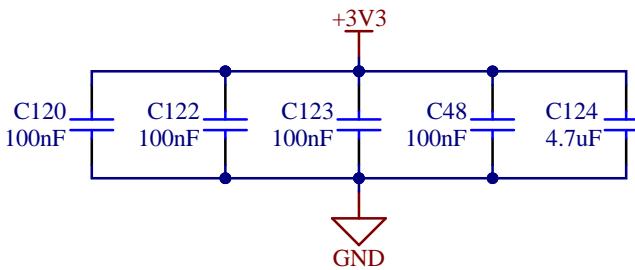
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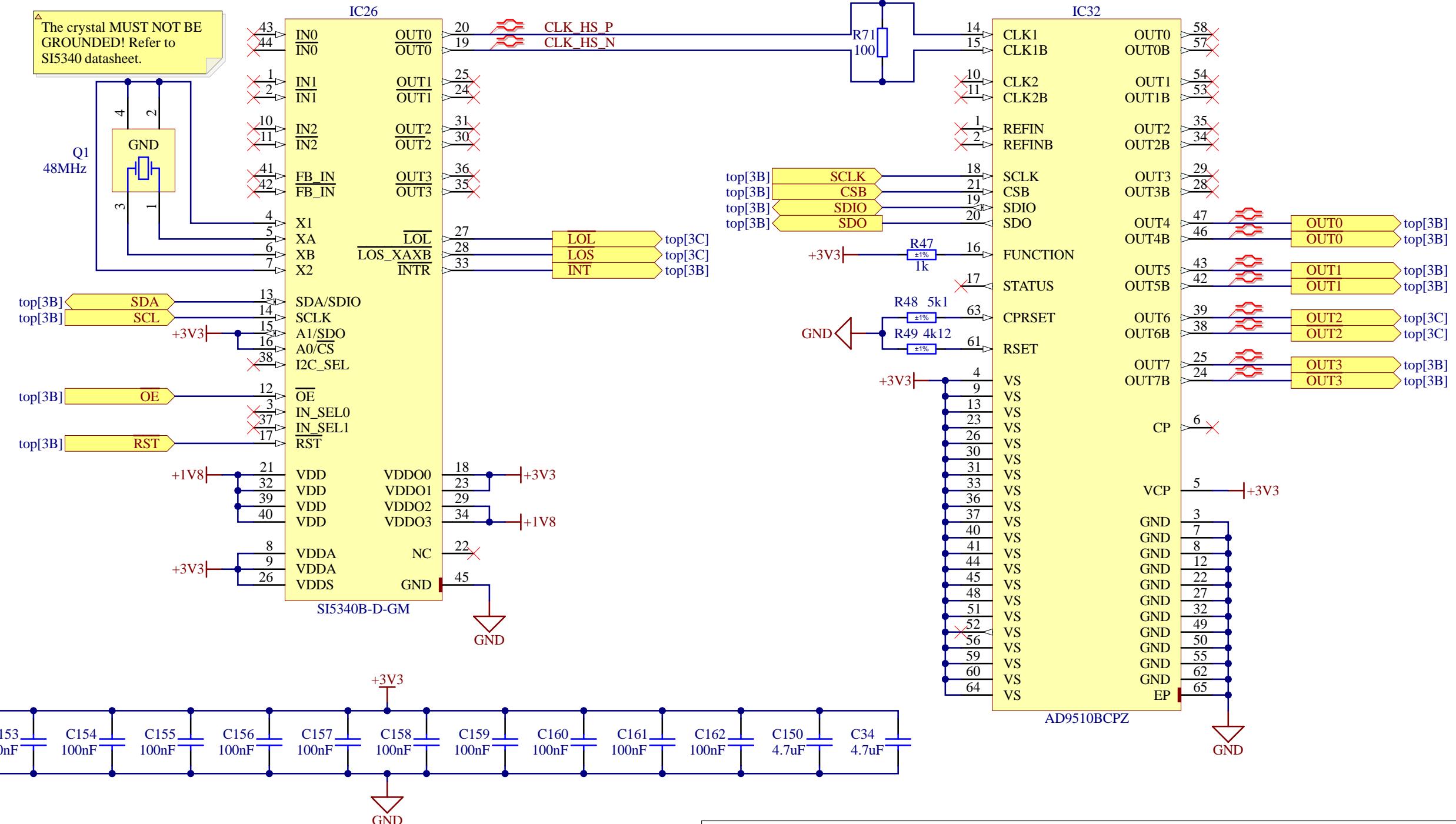
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Document		Fast Timing			
EP-ESE		Fast Timing			
Designer	Vojtech Vosahlo				
Drawn by	Vojtech Vosahlo				
Check by	Jerome A. Alozy				
Last Mod.	11/15/2024				
File	fastic.SchDoc				
Print Date	11/15/2024 9:51:44 AM				
Sheet	2 of 6				
Size	A4				
Rev	1.0				

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OUT0 - Clock for SPI1 sampling the Aurora bus (80/160MHz) - phase adjustable
 OUT1 - Clock for SPI2 sampling the Aurora bus (80/160MHz) - phase adjustable
 OUT2 - Clock for FastIC1 (40MHz) - delay & phase adjustable
 OUT3 - Clock for FastIC2 (40MHz) - delay & phase adjustable

B



C

D

E

A

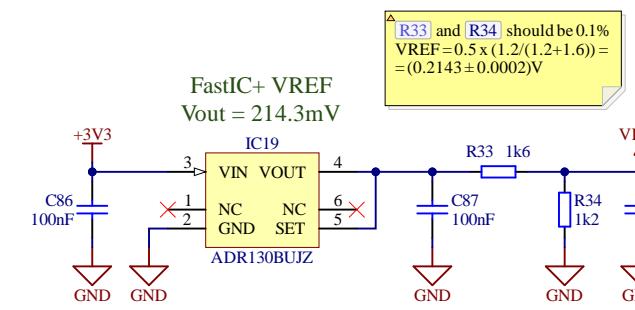
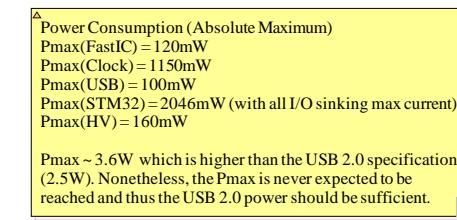
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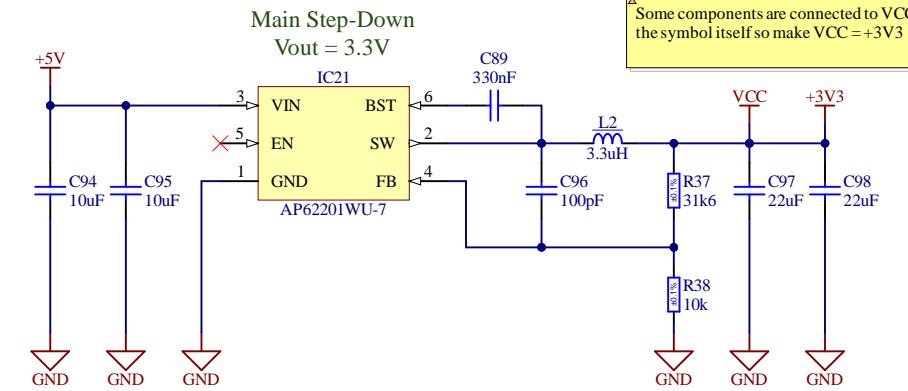
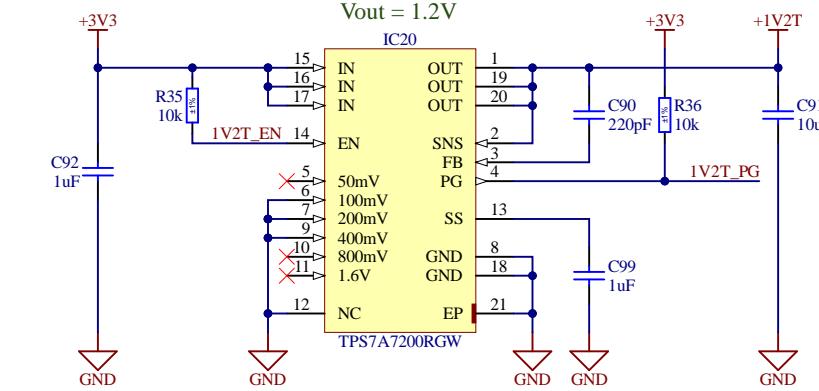
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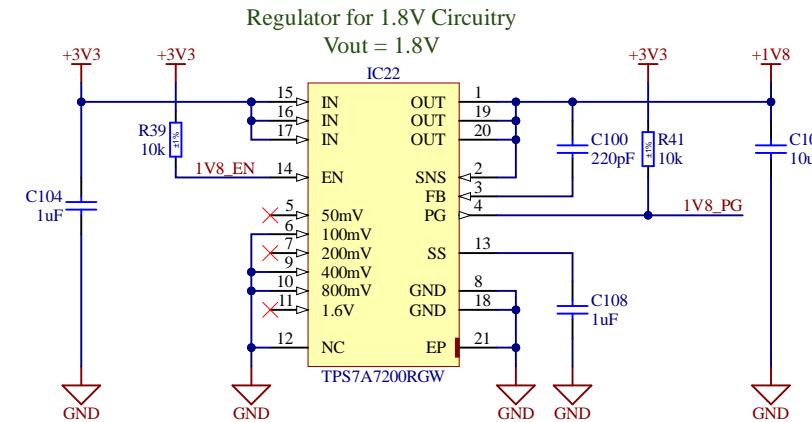
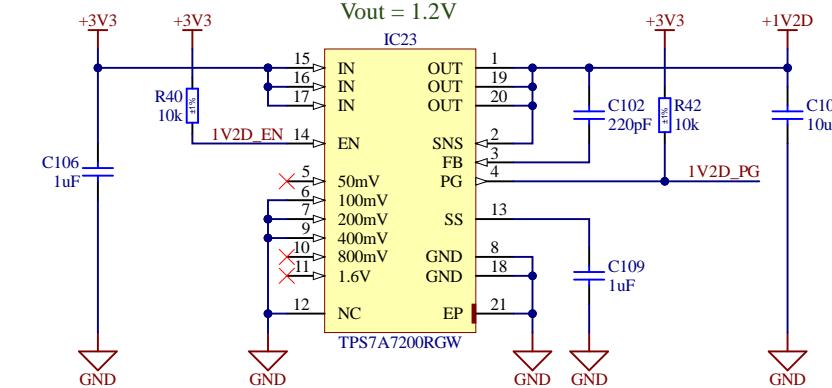
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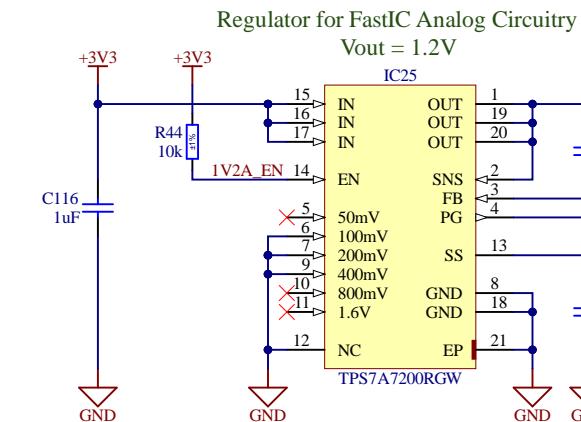
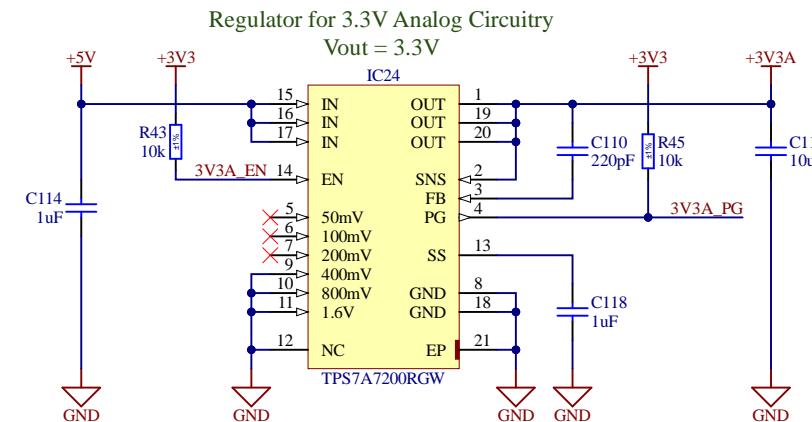
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**Regulator for FastIC PLL and Threshold Circuitry**

C

**Regulator for FastIC Digital Circuitry**

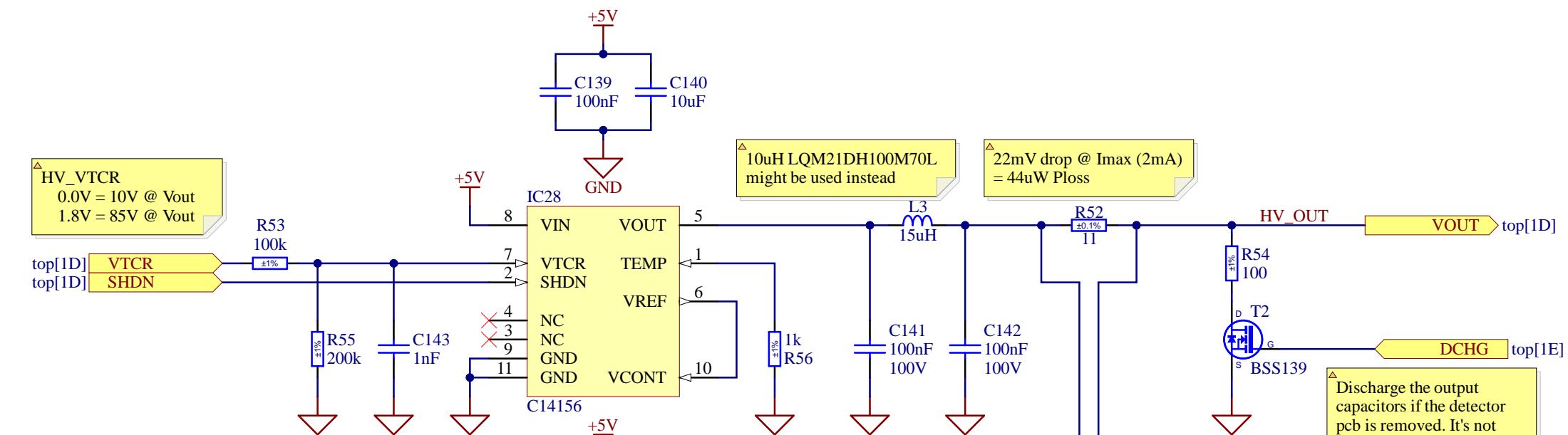
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**Project/Equipment****Fast Timing****Document****EP-ESE****FastIC+ readout**

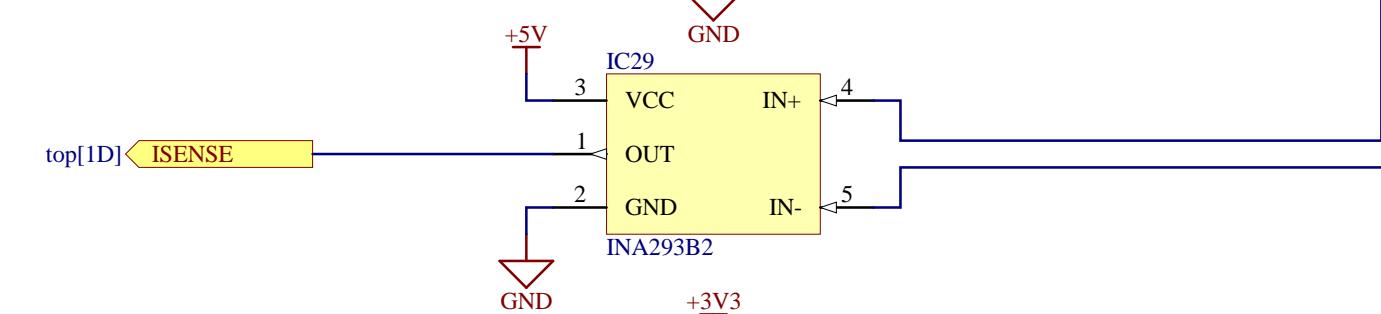
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Drawn by	Vojtech Vosahlo
Check by	Jerome A. Alozy
Last Mod.	11/15/2024
File	power.SchDoc
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Rev	-

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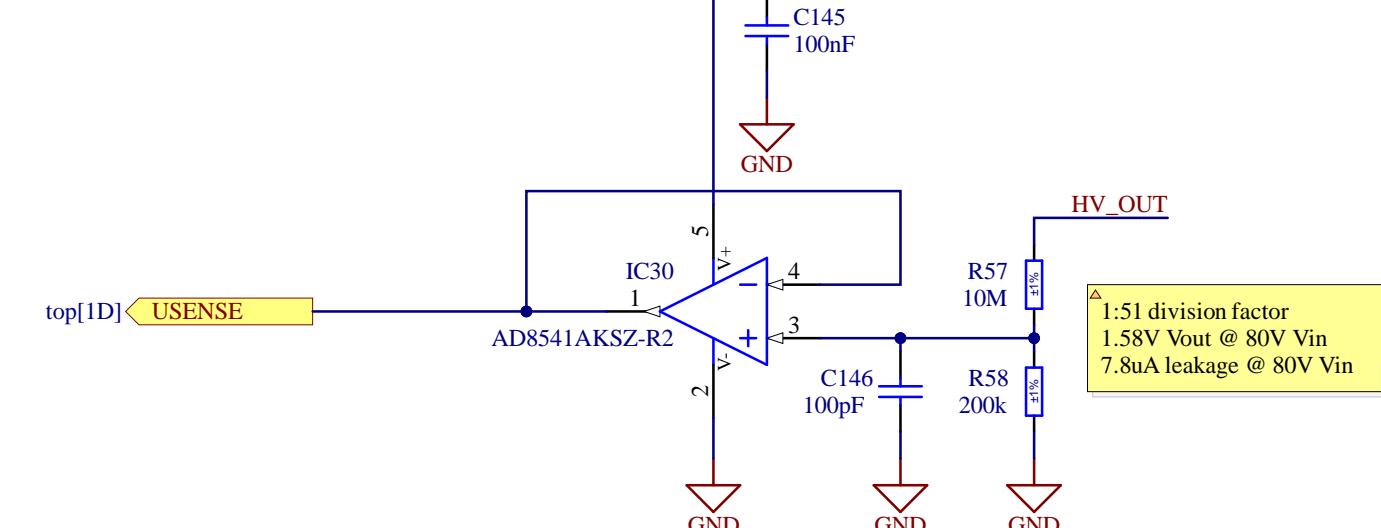
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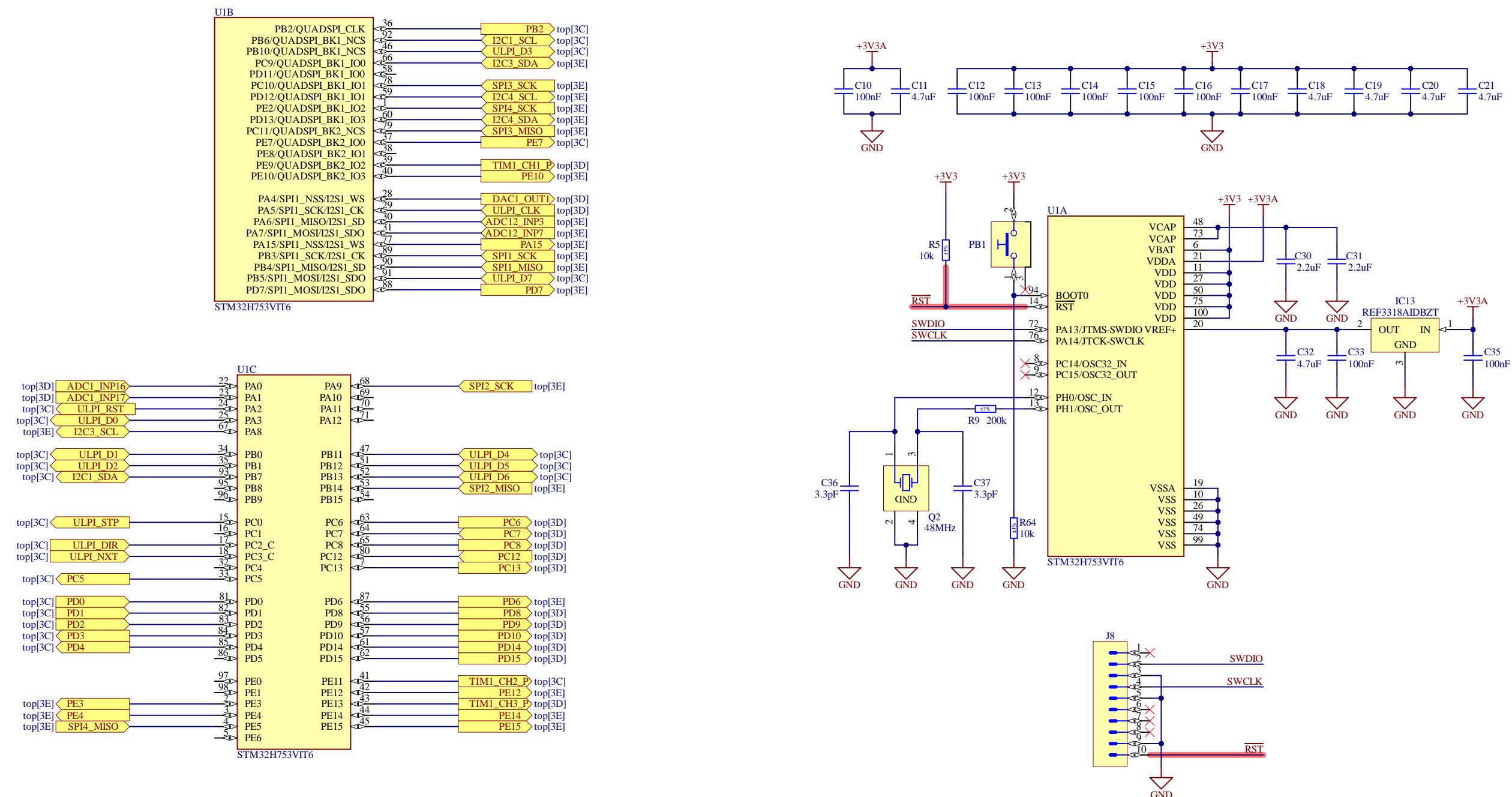
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Project/Equipment		Fast Timing	
Document	EP-ESE	Designer	Vojtech Vosahlo
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Last Mod.		Last Mod.	11/15/2024
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Project/Equipment	Fast Timing	Designer	Vojtech Vosahlo
Document		Drawn by	Vojtech Vosahlo
EP-ESE	FastIC+ readout	Check by	Jerome A. Alozy
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