1. Description

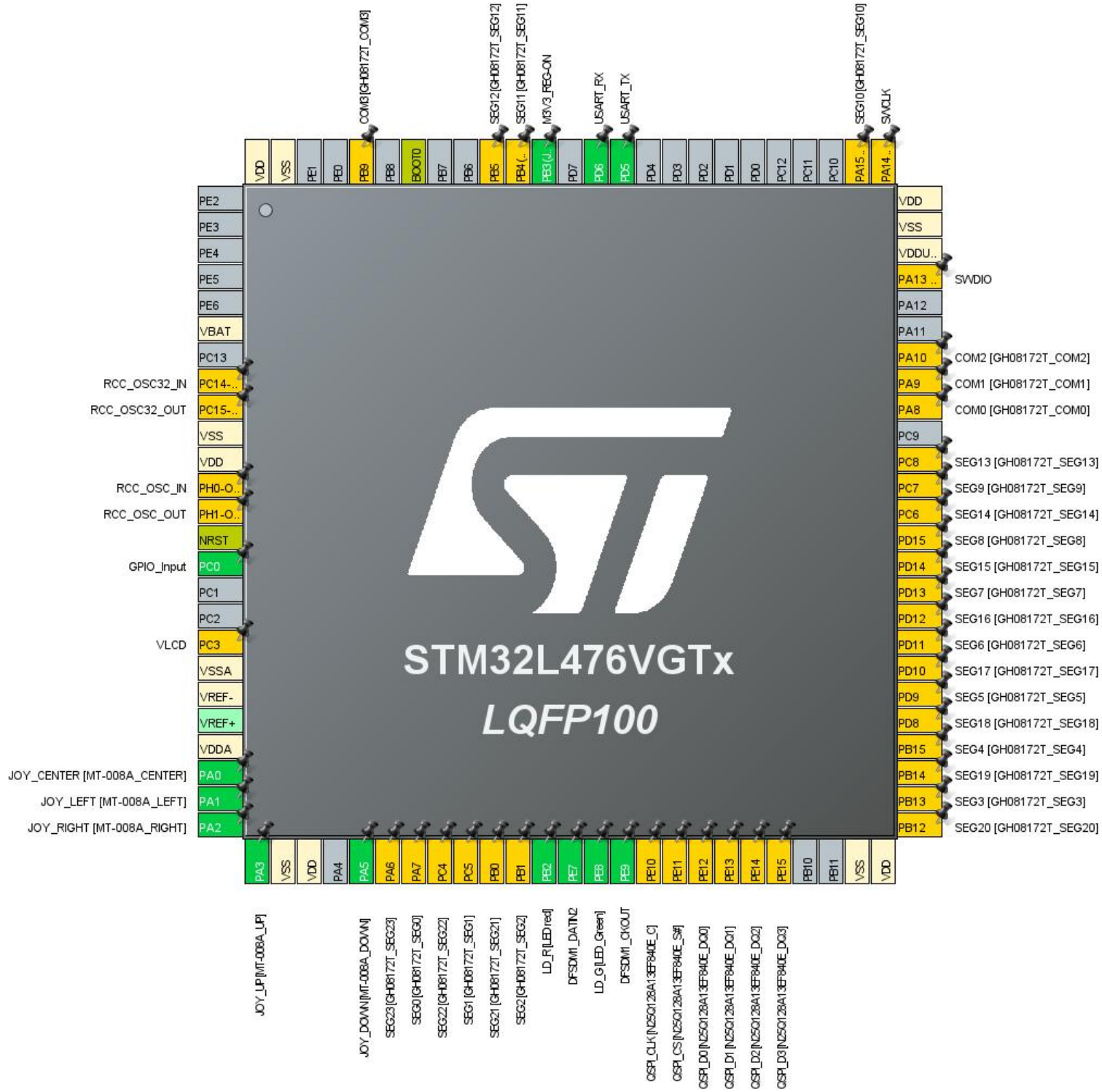
1.1. Project

Project Name	Discovery_clean
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 5.6.0
Date	04/17/2020

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
8	PC14-OSC32_IN (PC14) *	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15) *	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0) *	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 **	I/O	GPIO_Input	
18	PC3 *	I/O	LCD_VLCD	VLCD
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0 **	I/O	GPIO_Input	JOY_CENTER [MT-008A_CENTER]
24	PA1 **	I/O	GPIO_Input	JOY_LEFT [MT-008A_LEFT]
25	PA2 **	I/O	GPIO_Input	JOY_RIGHT [MT-008A_RIGHT]
26	PA3 **	I/O	GPIO_Input	JOY_UP [MT-008A_UP]
27	VSS	Power		
28	VDD	Power		
30	PA5 **	I/O	GPIO_Input	JOY_DOWN [MT-008A_DOWN]
31	PA6 *	I/O	LCD_SEG3	SEG23 [GH08172T_SEG23]
32	PA7 *	I/O	LCD_SEG4	SEG0 [GH08172T_SEG0]
33	PC4 *	I/O	LCD_SEG22	SEG22 [GH08172T_SEG22]
34	PC5 *	I/O	LCD_SEG23	SEG1 [GH08172T_SEG1]
35	PB0 *	I/O	LCD_SEG5	SEG21 [GH08172T_SEG21]
36	PB1 *	I/O	LCD_SEG6	SEG2 [GH08172T_SEG2]
37	PB2 **	I/O	GPIO_Output	LD_R [LED red]
38	PE7	I/O	DFSDM1_DATIN2	
39	PE8 **	I/O	GPIO_Output	LD_G [LED_Green]
40	PE9	I/O	DFSDM1_CKOUT	
41	PE10 *	I/O	QUADSPI_CLK	QSPI_CLK [N25Q128A13EF840E_C]

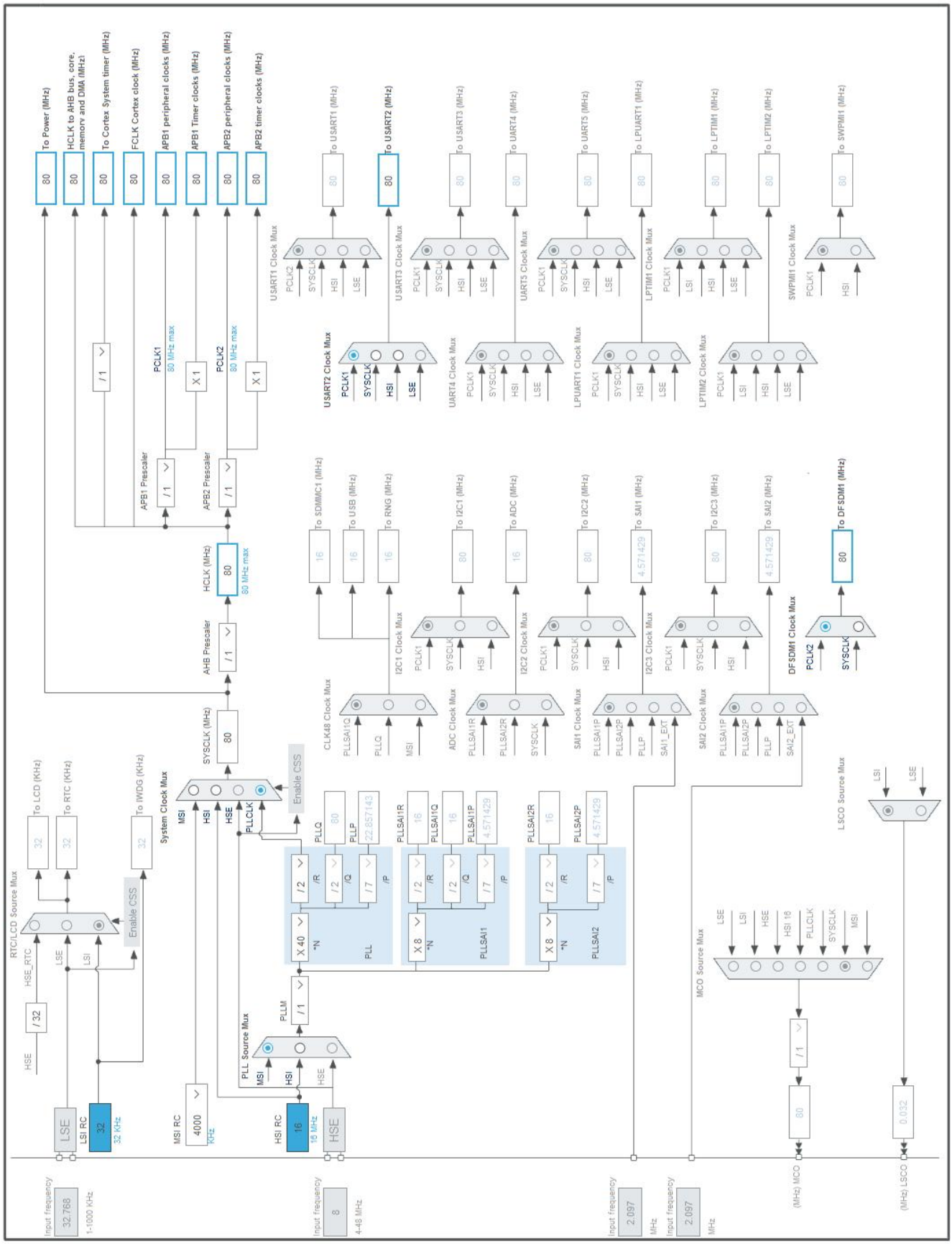
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PE11 *	I/O	QUADSPI_NCS	QSPI_CS [N25Q128A13EF840E_S#]
43	PE12 *	I/O	QUADSPI_BK1_IO0	QSPI_D0 [N25Q128A13EF840E_DQ0]
44	PE13 *	I/O	QUADSPI_BK1_IO1	QSPI_D1 [N25Q128A13EF840E_DQ1]
45	PE14 *	I/O	QUADSPI_BK1_IO2	QSPI_D2 [N25Q128A13EF840E_DQ2]
46	PE15 *	I/O	QUADSPI_BK1_IO3	QSPI_D3 [N25Q128A13EF840E_DQ3]
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	LCD_SEG12	SEG20 [GH08172T_SEG20]
52	PB13 *	I/O	LCD_SEG13	SEG3 [GH08172T_SEG3]
53	PB14 *	I/O	LCD_SEG14	SEG19 [GH08172T_SEG19]
54	PB15 *	I/O	LCD_SEG15	SEG4 [GH08172T_SEG4]
55	PD8 *	I/O	LCD_SEG28	SEG18 [GH08172T_SEG18]
56	PD9 *	I/O	LCD_SEG29	SEG5 [GH08172T_SEG5]
57	PD10 *	I/O	LCD_SEG30	SEG17 [GH08172T_SEG17]
58	PD11 *	I/O	LCD_SEG31	SEG6 [GH08172T_SEG6]
59	PD12 *	I/O	LCD_SEG32	SEG16 [GH08172T_SEG16]
60	PD13 *	I/O	LCD_SEG33	SEG7 [GH08172T_SEG7]
61	PD14 *	I/O	LCD_SEG34	SEG15 [GH08172T_SEG15]
62	PD15 *	I/O	LCD_SEG35	SEG8 [GH08172T_SEG8]
63	PC6 *	I/O	LCD_SEG24	SEG14 [GH08172T_SEG14]
64	PC7 *	I/O	LCD_SEG25	SEG9 [GH08172T_SEG9]
65	PC8 *	I/O	LCD_SEG26	SEG13 [GH08172T_SEG13]
67	PA8 *	I/O	LCD_COM0	COM0 [GH08172T_COM0]
68	PA9 *	I/O	LCD_COM1	COM1 [GH08172T_COM1]
69	PA10 *	I/O	LCD_COM2	COM2 [GH08172T_COM2]
72	PA13 (JTMS-SWDIO) *	I/O	SYS_JTMS-SWDIO	SWDIO
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK-SWCLK) *	I/O	SYS_JTCK-SWCLK	SWCLK
77	PA15 (JTDI) *	I/O	LCD_SEG17	SEG10 [GH08172T_SEG10]
86	PD5	I/O	USART2_TX	USART_TX

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
87	PD6	I/O	USART2_RX	USART_RX
89	PB3 (JTDO-TRACESWO) **	I/O	GPIO_Output	M3V3_REG-ON
90	PB4 (NJTRST) *	I/O	LCD_SEG8	SEG11 [GH08172T_SEG11]
91	PB5 *	I/O	LCD_SEG9	SEG12 [GH08172T_SEG12]
94	BOOT0	Boot		
96	PB9 *	I/O	LCD_COM3	COM3 [GH08172T_COM3]
99	VSS	Power		
100	VDD	Power		

** The pin is affected with an I/O function

* The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	Discovery_clean
Project Folder	C:\Users\Nieke\STM32CubeIDE\workspace_1.3.0\Discovery_clean
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.15.1

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	025976_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

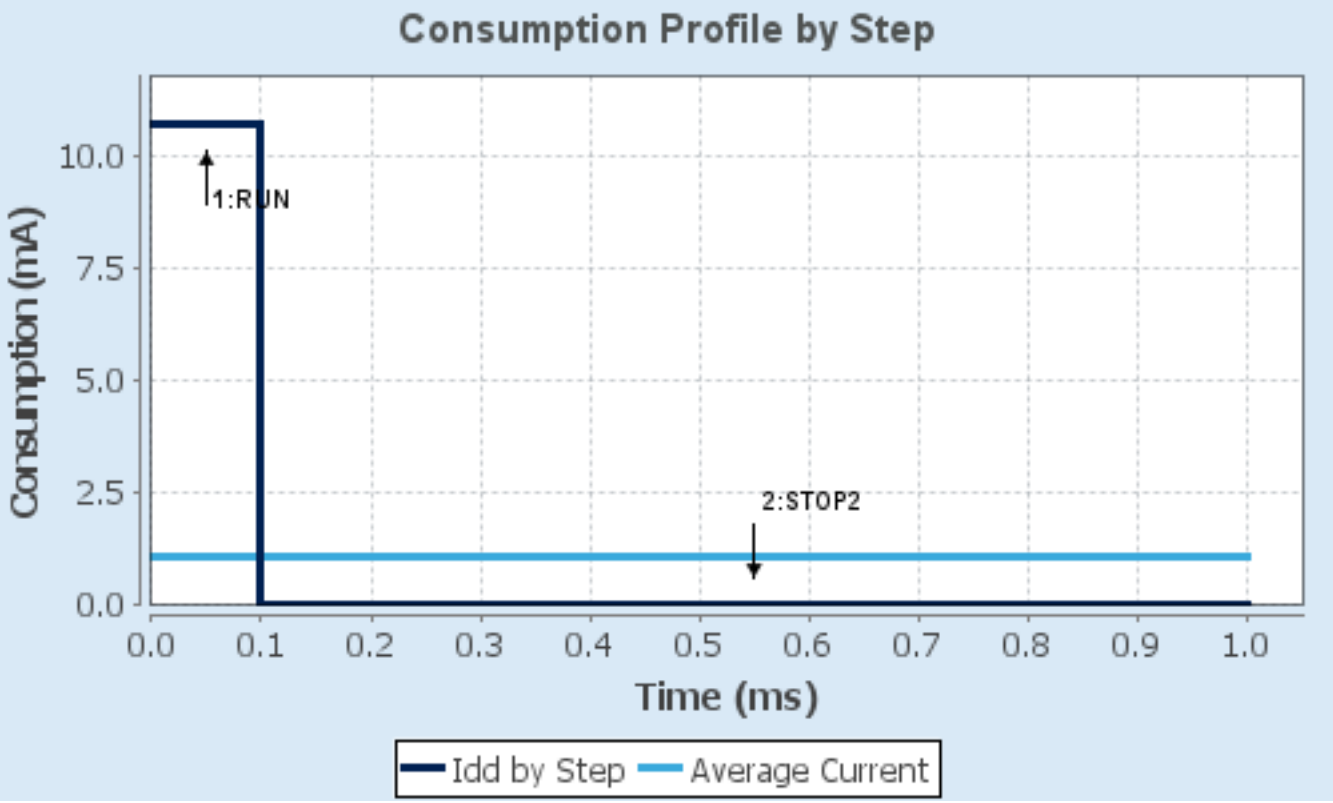
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.65	105
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
10.0
7.5
5.0
2.5
0.0
1:RUN
2:STOP2
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. DFSDM1

mode: PDM/SPI input from ch2 and internal clock

mode: CKOUT

7.1.1. Filter 0:

regular channel selection:

regular channel selection	**Channel 2 ***
Continuous Mode	Continuous Mode
Trigger to start regular conversion	Software trigger
Fast Mode	**Enable ***
Dma Mode	**Enable ***

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

Filter parameters:

Sinc Order	**Sinc 3 filter type ***
Fosr	**250 ***
Iosr	1

7.1.2. Filter 1:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable

Channel7 as injected channel	Disable

7.1.3. Filter 2:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.1.4. Filter 3:

regular channel selection:

regular channel selection	- None -

injected channel selection:

Channel0 as injected channel	Disable
Channel1 as injected channel	Disable
Channel2 as injected channel	Disable
Channel3 as injected channel	Disable
Channel4 as injected channel	Disable
Channel5 as injected channel	Disable
Channel6 as injected channel	Disable
Channel7 as injected channel	Disable

7.1.5. Output Clock:

Output Clock parameters:

Selection	Source for ouput clock is system clock
Divider	**40 ***

7.1.6. Channel 2:

Channel 2 parameters:

Type	SPI with rising edge
Spi Clock	Internal SPI clock
Offset	0
Right Bit Shift	**0x00 ***

Analog watchdog parameters:

Filter Order	FastSinc filter type
Oversampling	1

7.2. GPIO

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

Timebase Source: SysTick

7.5. USART2

Mode: Asynchronous

7.5.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DFSDM1	PE7	DFSDM1_DATIN2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE9	DFSDM1_CKOUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_TX
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	USART_RX
Single Mapped Signals	PC14-OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT (PC15)	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PC3	LCD_VLCD	Alternate Function Push Pull	No pull-up and no pull-down	Low	VLCD
	PA6	LCD_SEG3	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG23 [GH08172T_SEG23]
	PA7	LCD_SEG4	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG0 [GH08172T_SEG0]
	PC4	LCD_SEG22	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG22 [GH08172T_SEG22]
	PC5	LCD_SEG23	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG1 [GH08172T_SEG1]
	PB0	LCD_SEG5	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG21 [GH08172T_SEG21]
	PB1	LCD_SEG6	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG2 [GH08172T_SEG2]
	PE10	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_CLK [N25Q128A13EF840E_C]
	PE11	QUADSPI_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_CS [N25Q128A13EF840E_S#]
	PE12	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	QSPI_D0 [N25Q128A13EF840E_DQ0]
	PE13	QUADSPI_BK1_I	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	QSPI_D1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
		O1			*	[N25Q128A13EF840E_DQ1]
	PE14	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	QSPI_D2 [N25Q128A13EF840E_DQ2]
	PE15	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	QSPI_D3 [N25Q128A13EF840E_DQ3]
	PB12	LCD_SEG12	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG20 [GH08172T_SEG20]
	PB13	LCD_SEG13	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG3 [GH08172T_SEG3]
	PB14	LCD_SEG14	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG19 [GH08172T_SEG19]
	PB15	LCD_SEG15	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG4 [GH08172T_SEG4]
	PD8	LCD_SEG28	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG18 [GH08172T_SEG18]
	PD9	LCD_SEG29	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG5 [GH08172T_SEG5]
	PD10	LCD_SEG30	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG17 [GH08172T_SEG17]
	PD11	LCD_SEG31	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG6 [GH08172T_SEG6]
	PD12	LCD_SEG32	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG16 [GH08172T_SEG16]
	PD13	LCD_SEG33	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG7 [GH08172T_SEG7]
	PD14	LCD_SEG34	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG15 [GH08172T_SEG15]
	PD15	LCD_SEG35	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG8 [GH08172T_SEG8]
	PC6	LCD_SEG24	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG14 [GH08172T_SEG14]
	PC7	LCD_SEG25	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG9 [GH08172T_SEG9]
	PC8	LCD_SEG26	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG13 [GH08172T_SEG13]
	PA8	LCD_COM0	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM0 [GH08172T_COM0]
	PA9	LCD_COM1	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM1 [GH08172T_COM1]
	PA10	LCD_COM2	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM2 [GH08172T_COM2]
	PA13 (JTMS-SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14 (JTCK-SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
	PA15 (JTDI)	LCD_SEG17	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG10 [GH08172T_SEG10]
	PB4 (NJTRST)	LCD_SEG8	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG11 [GH08172T_SEG11]
	PB5	LCD_SEG9	Alternate Function Push Pull	No pull-up and no pull-down	Low	SEG12

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
						[GH08172T_SEG12]
	PB9	LCD_COM3	Alternate Function Push Pull	No pull-up and no pull-down	Low	COM3 [GH08172T_COM3]
GPIO	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PA0	GPIO_Input	Input mode	**Pull-down ***	n/a	JOY_CENTER [MT-008A_CENTER]
	PA1	GPIO_Input	Input mode	**Pull-down ***	n/a	JOY_LEFT [MT-008A_LEFT]
	PA2	GPIO_Input	Input mode	**Pull-down ***	n/a	JOY_RIGHT [MT-008A_RIGHT]
	PA3	GPIO_Input	Input mode	**Pull-down ***	n/a	JOY_UP [MT-008A_UP]
	PA5	GPIO_Input	Input mode	**Pull-down ***	n/a	JOY_DOWN [MT-008A_DOWN]
	PB2	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_R [LED red]
	PE8	GPIO_Output	Output Push Pull	**Pull-up ***	**Very High ***	LD_G [LED_Green]
	PB3 (JTDO-TRACESWO)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	M3V3_REG-ON

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DFSDM1_FLT0	DMA1_Channel4	Peripheral To Memory	Low
USART2_RX	DMA1_Channel6	Peripheral To Memory	Low
USART2_TX	DMA1_Channel7	Memory To Peripheral	Low

DFSDM1_FLT0: DMA1_Channel4 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Word
Memory Data Width:	Word

USART2_RX: DMA1_Channel6 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Channel7 DMA request Settings:

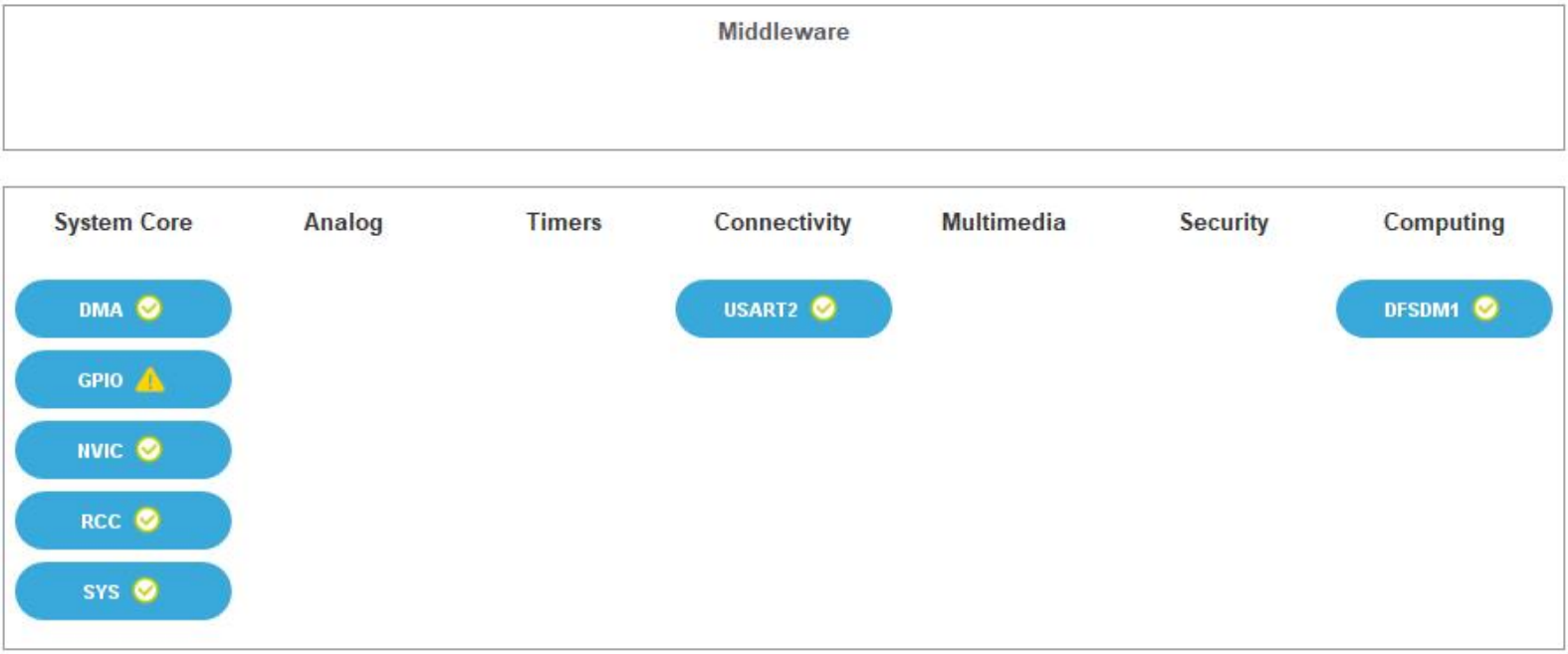
Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel4 global interrupt	true	0	0
DMA1 channel6 global interrupt	true	0	0
DMA1 channel7 global interrupt	true	0	0
USART2 global interrupt	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
DFSDM1 filter0 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report