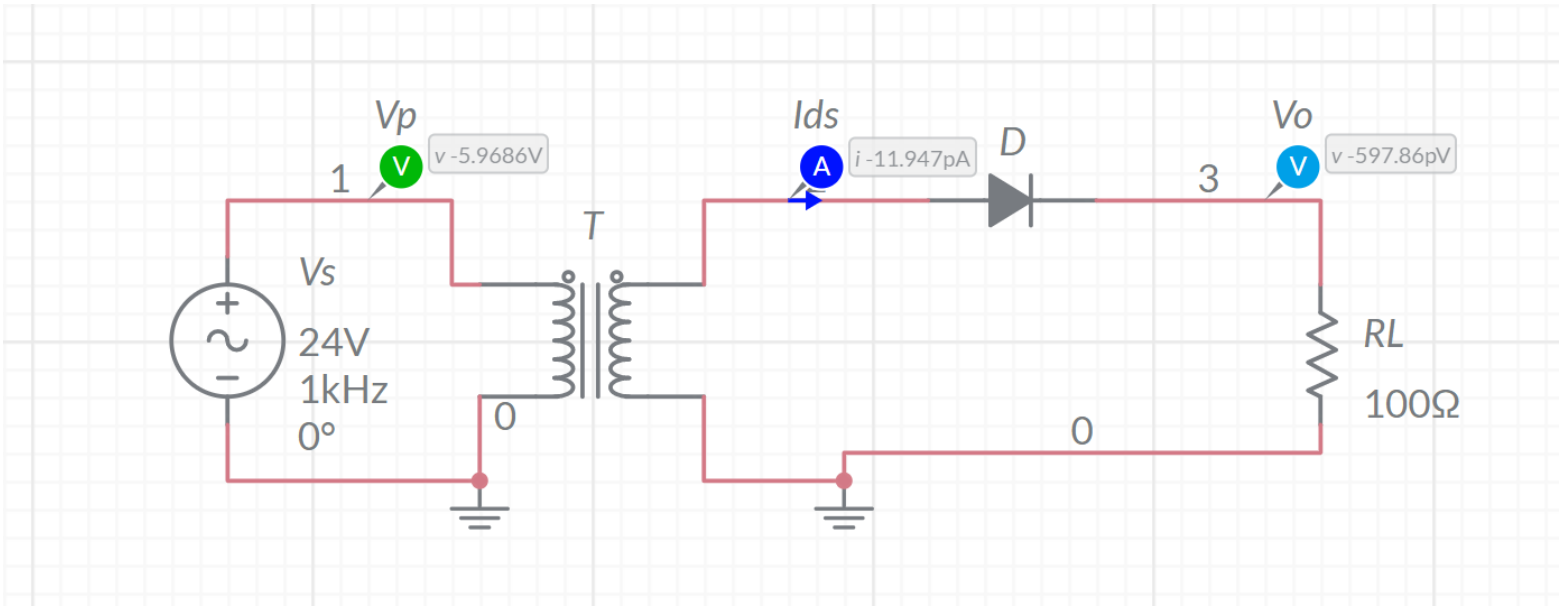
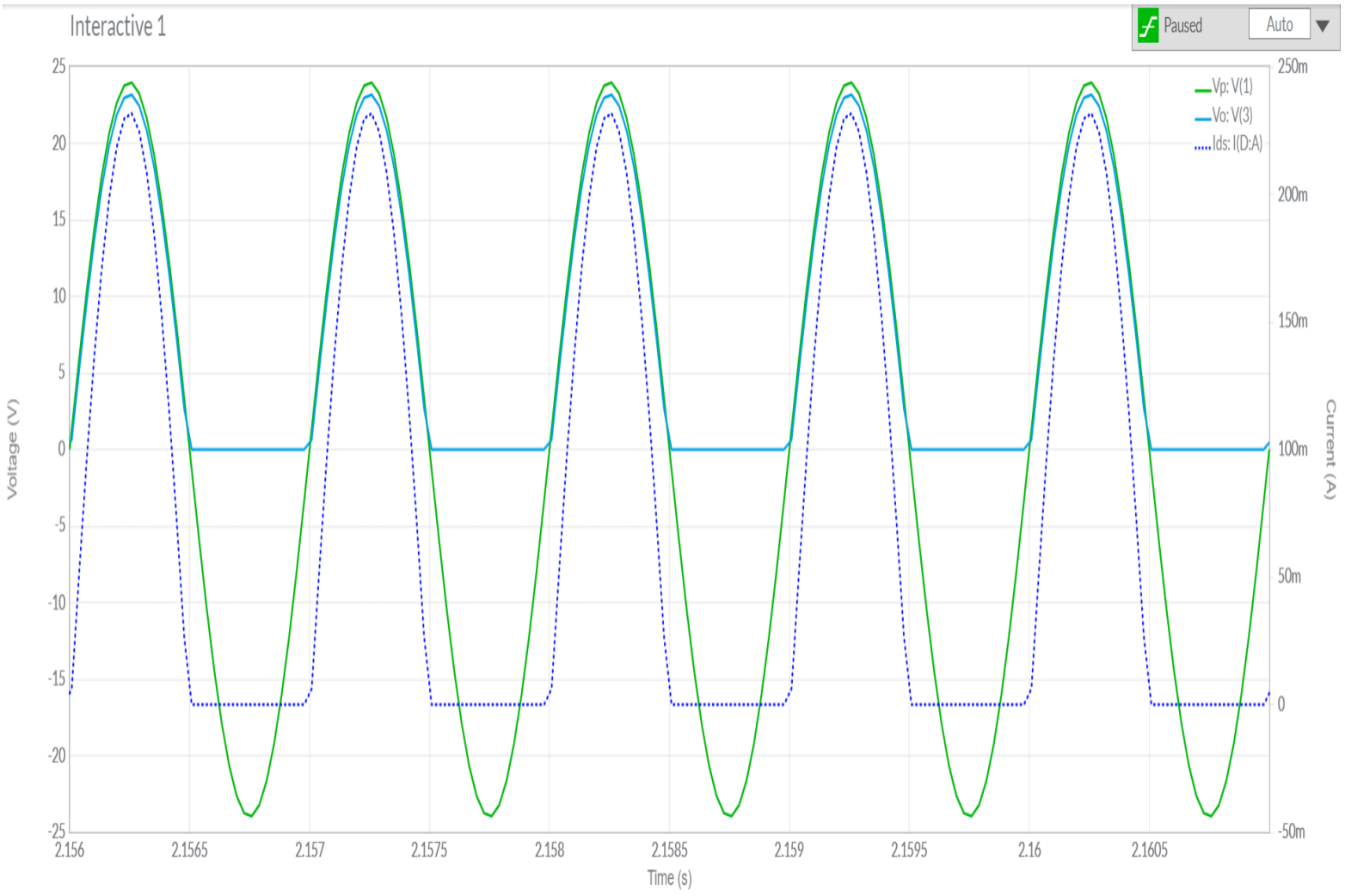
Question 1

Design a half wave rectifier fed with a sinusoidal input voltage of 24V peak-to-peak amplitude, zero average, and 1kHz frequency. Assume the diode to be ideal. Let the load resistance R = 100 ohms and capacitor C = 100 uF. Find the average dc output voltage, the average diode current during conduction and the maximum current. Verify all your results by simulation. Paste your calculation and simulated circuits (with and without filter capacitor) along with the graphs in the PDF document.





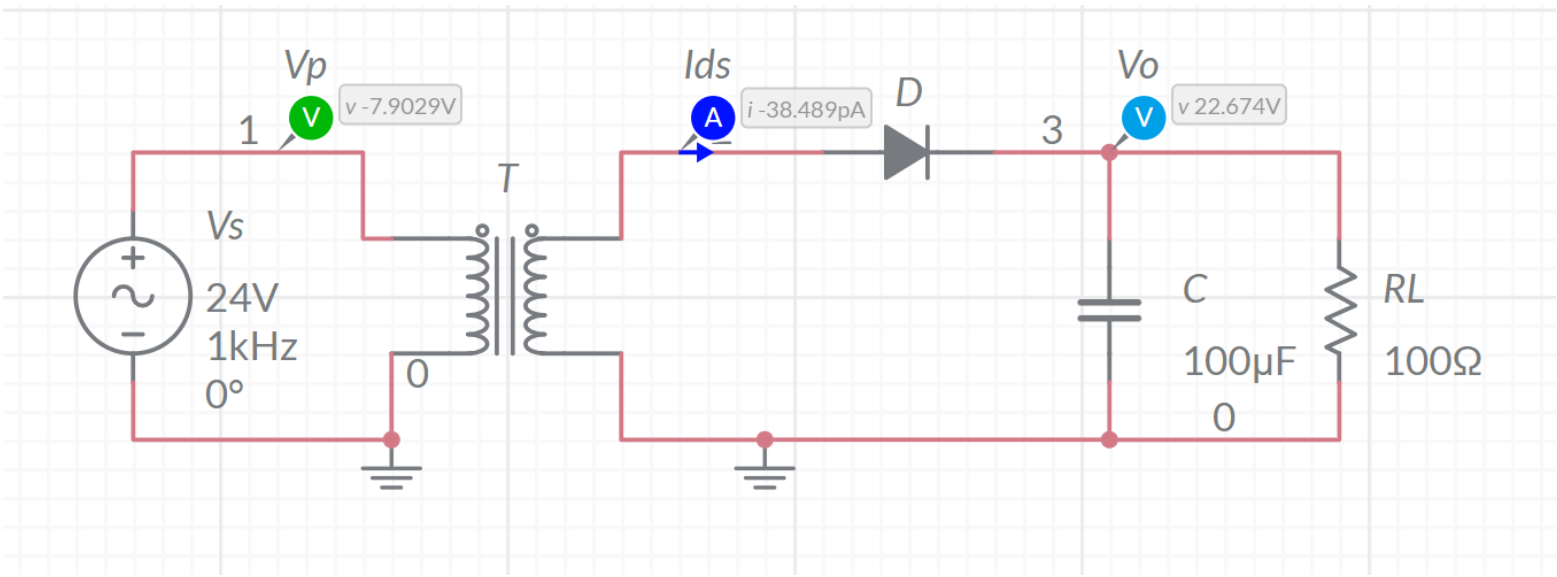
Without filter

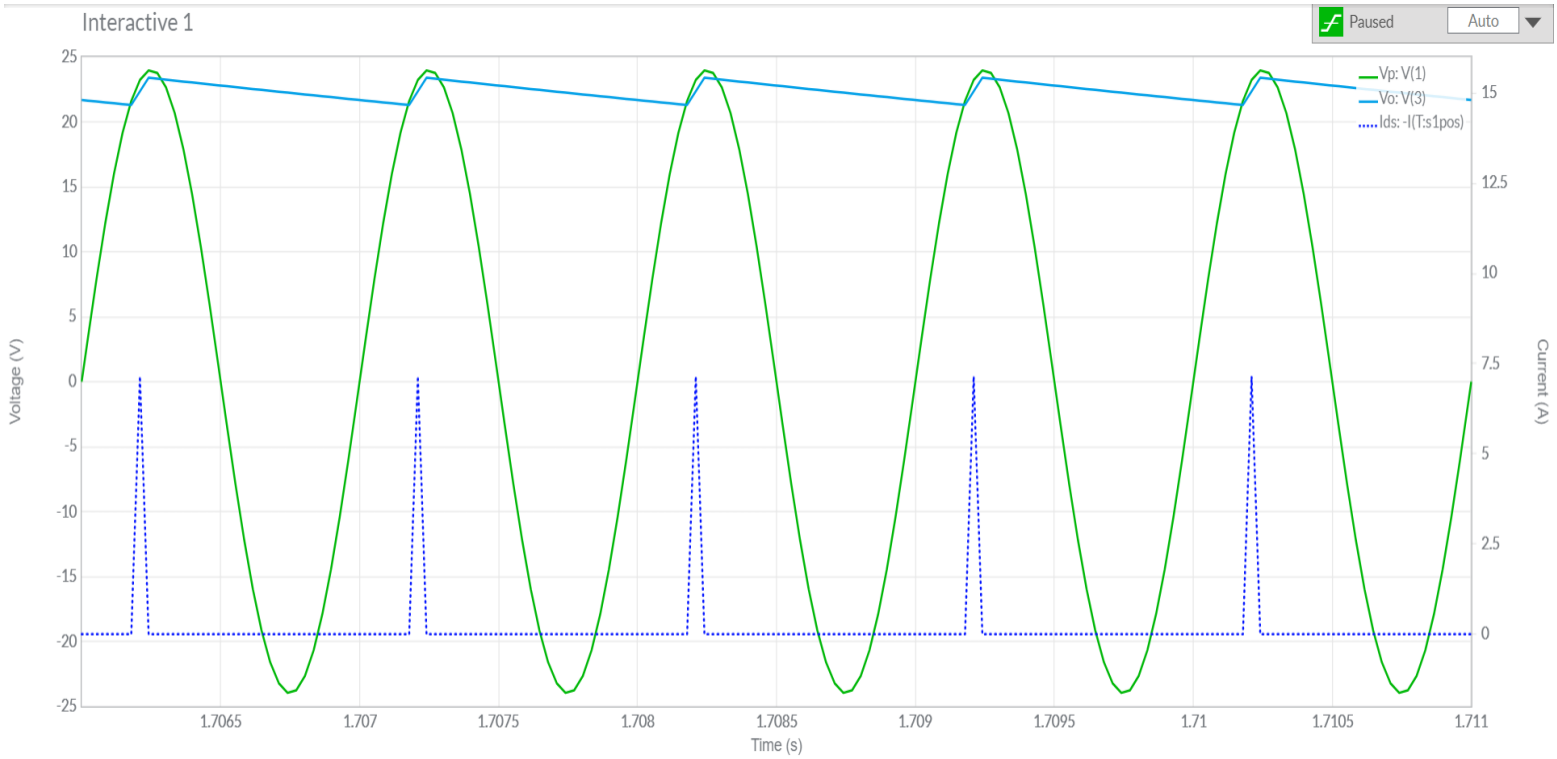
$V_p = 24\ V$

$V_{dc\ out\ avg} = \frac{V_p}{\pi} = \frac{24}{\pi} = 7.639\ V$

$i_{d\,avg} = i_{L\,avg} = \frac{V_{dc\ out\ avg}}{R} = \frac{7.639}{100} = 0.07639\ A.$

$i_{max} = \frac{V_p}{R} = \frac{24}{100} = 0.24\ A.$





With filter

$$V_p = 24\ V$$

$$V_r = \frac{V_p}{fRC} = \frac{24}{100 \times 100 \times 100 \times 10^{-6}} = 2.4\ V$$

$$V_{dc\ out} = V_p - V_r$$

$$= 24 - 2.4 = 21.6\ V$$

$$V_{dc\ out\ avg} = \frac{V_{dc\ out}}{\pi} = \frac{21.6}{\pi} = 6.875\ V$$

$$i_L = \frac{V_p}{R} = \frac{24}{100} = 0.24\ A$$

$$i_{d\ avg} = i_L \left(1 + \pi \sqrt{\frac{2V_p}{V_r}} \right)$$

$$= 0.24 \left(1 + \pi \sqrt{\frac{2 \times 24}{2.4}} \right)$$

$$= 3.611\ A$$

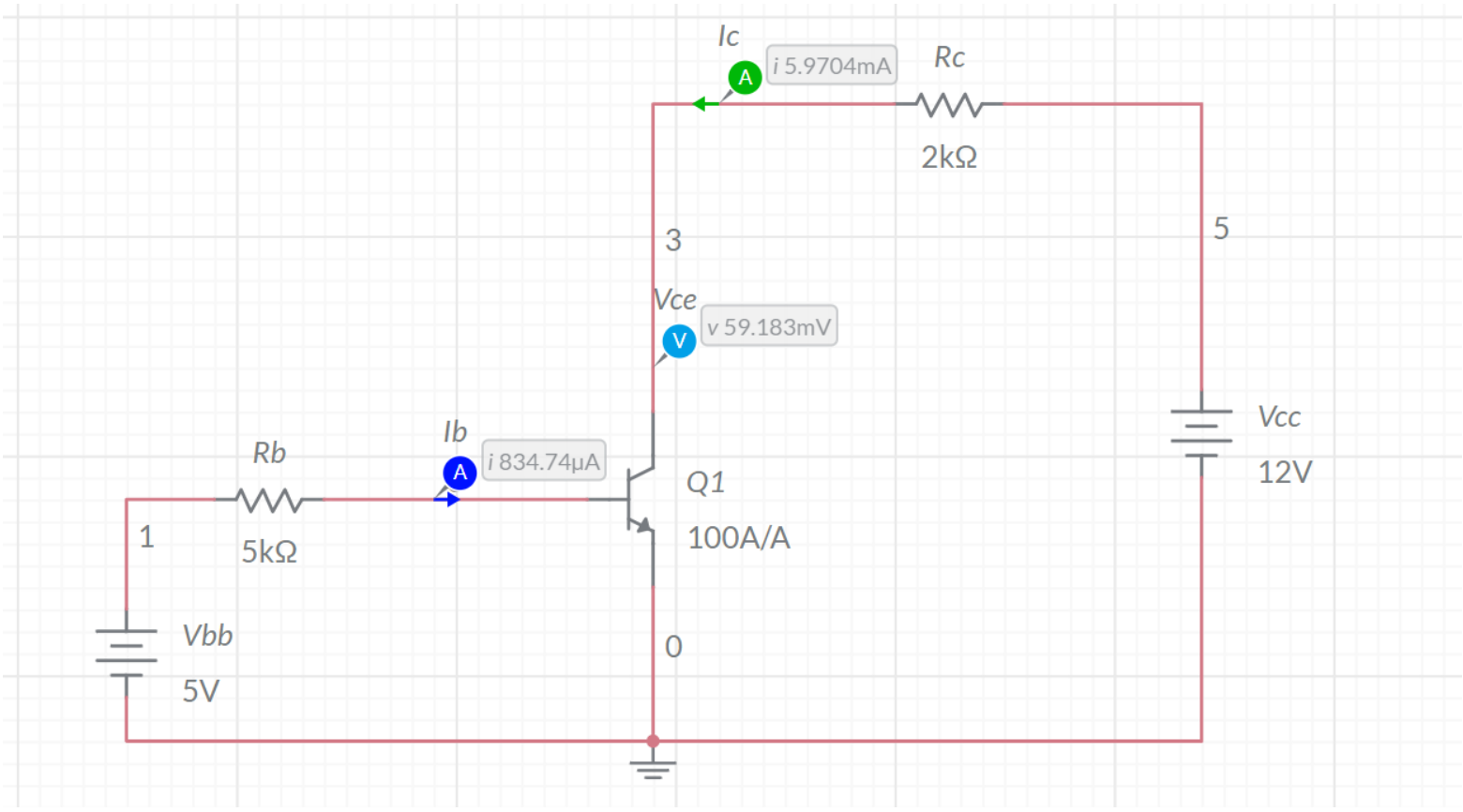
$$i_{max} = i_L \left(1 + 2\pi \sqrt{\frac{2V_p}{V_r}} \right)$$

$$= 0.24 \left(1 + 2\pi \sqrt{\frac{2 \times 24}{2.4}} \right)$$

$$= 6.983\ A$$

Question 2

Design the common emitter configuration of BJT. Take Vcc = 12V, Rc = 2 Kohm, Rb = 5 Kohm. Take Vbb = 0.2V, 0.7, 1V, 2.5V and 5V and measure Ic, Vce and Ib. Take screenshots of each reading. Using these data, find out the value of current gain (Beta) in the active region. Perform all the necessary calculations and attach the screenshots of circuit, all the readings and graphs in a PDF document.



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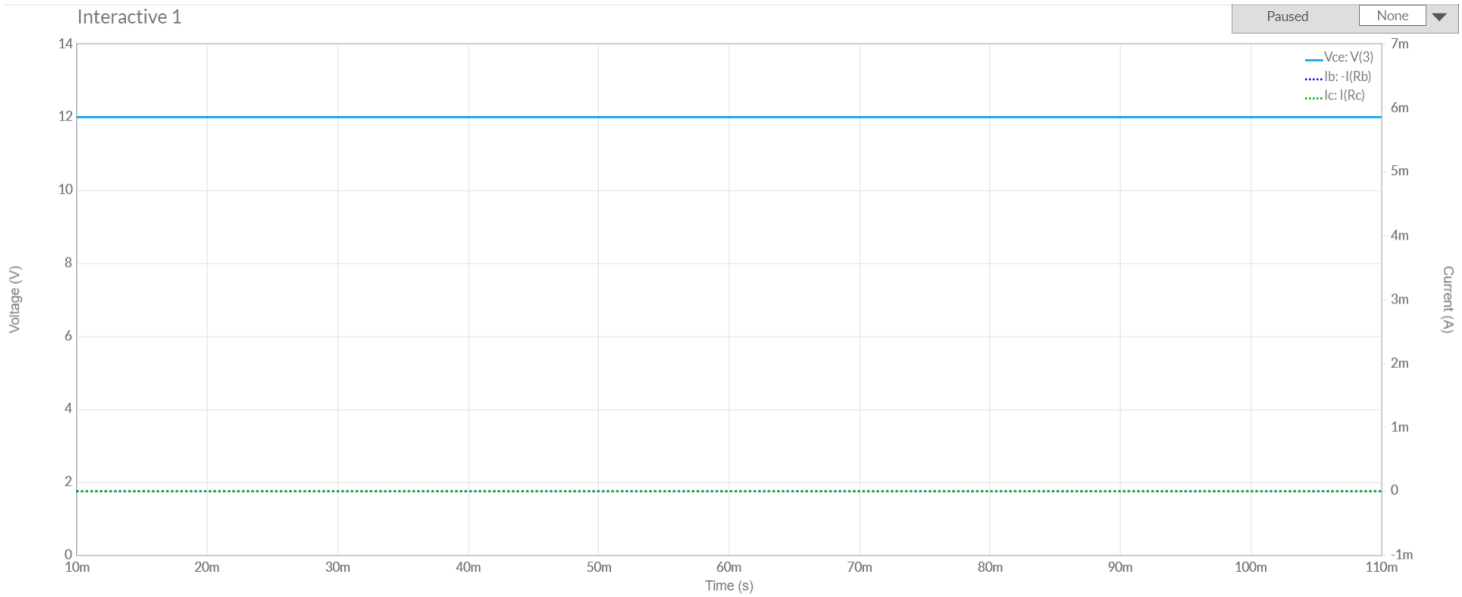
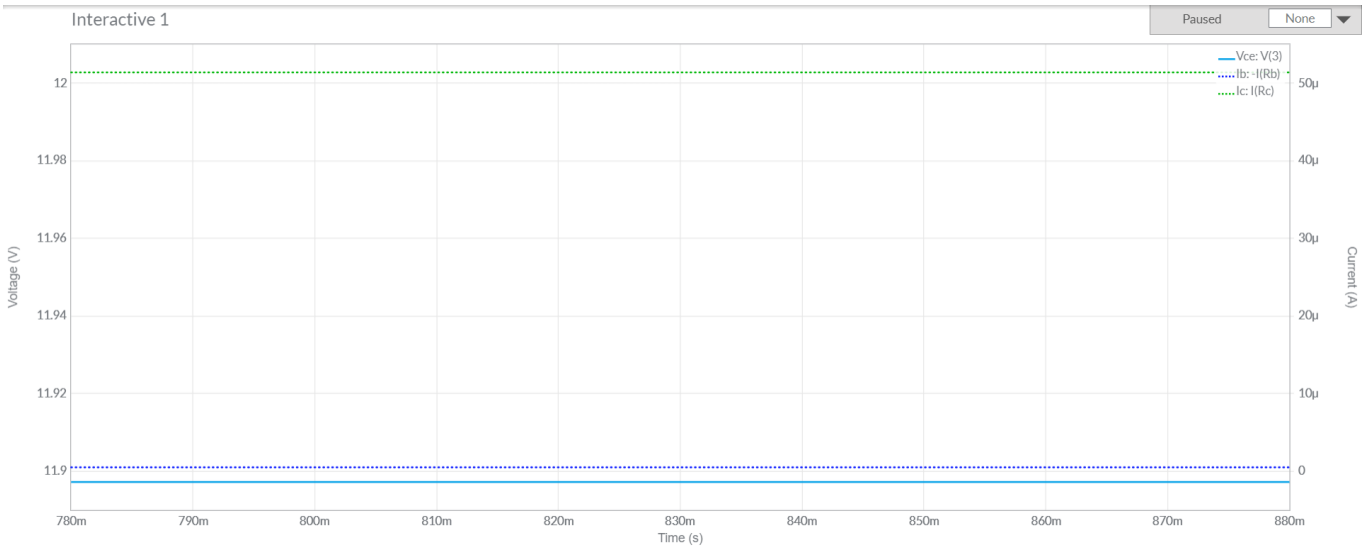
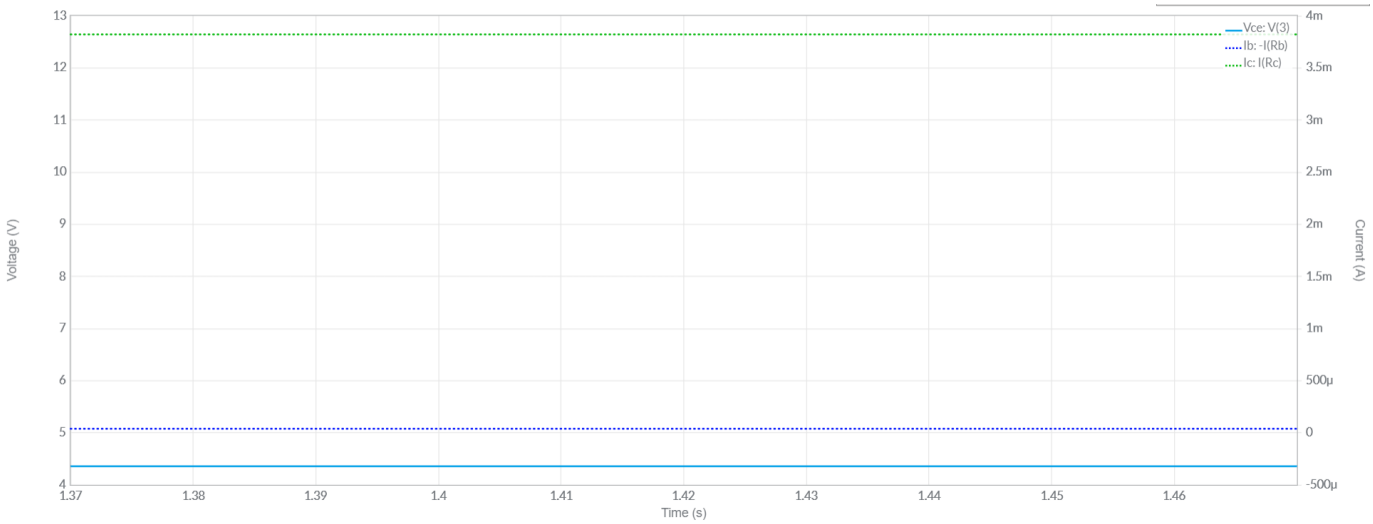
When Vbb = 0.2V **Ib = 11.596pA** **Ic = 36.028pA** **Vce = 12V** **β= Ic/Ib = 3.106**



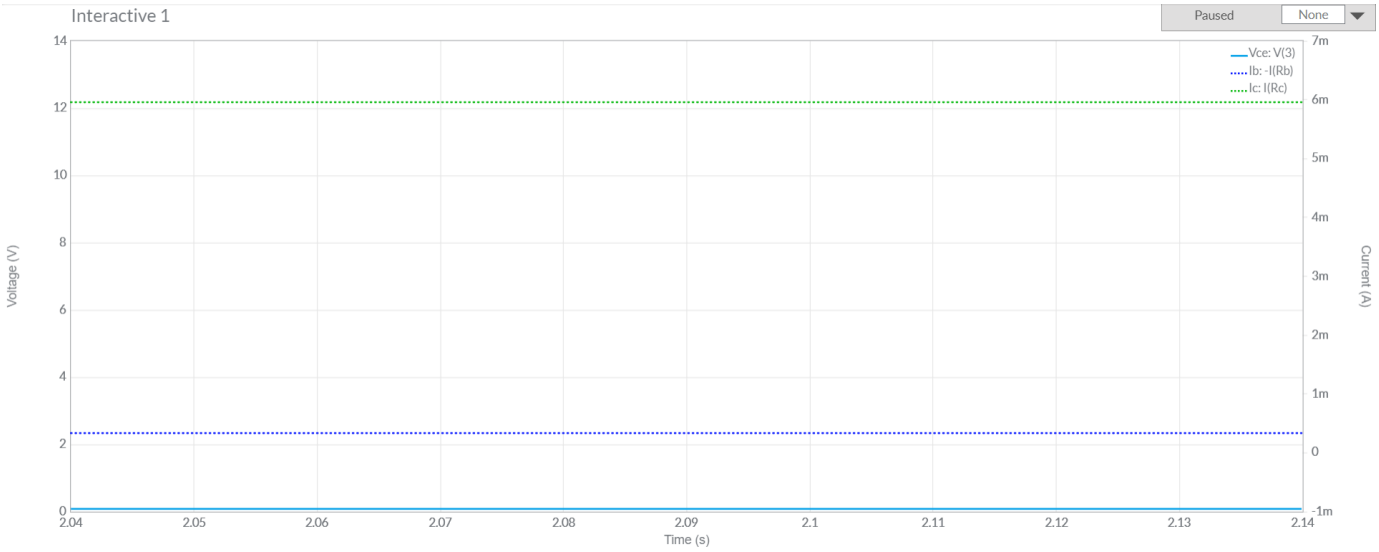
When Vbb = 0.7V **Ib = 513.8nA** **Ic = 51.381µA** **Vce = 11.897V** **β= Ic/Ib = 100**



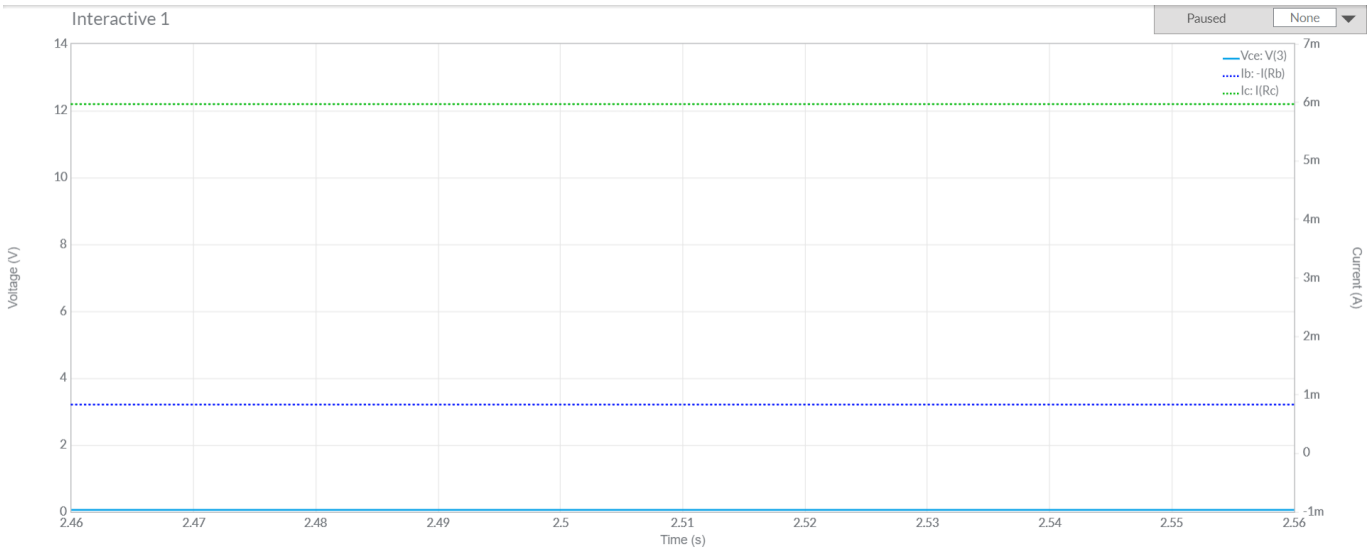
When Vbb = 1V **Ib = 38.222µA** **Ic = 3.822mA** **Vce = 4.355V** **β= Ic/Ib = 100**



When Vbb = 2.5V **Ib = 335.48µA** **Ic = 5.958mA** **Vce = 82.231mV** **β= Ic/Ib = 17.759**



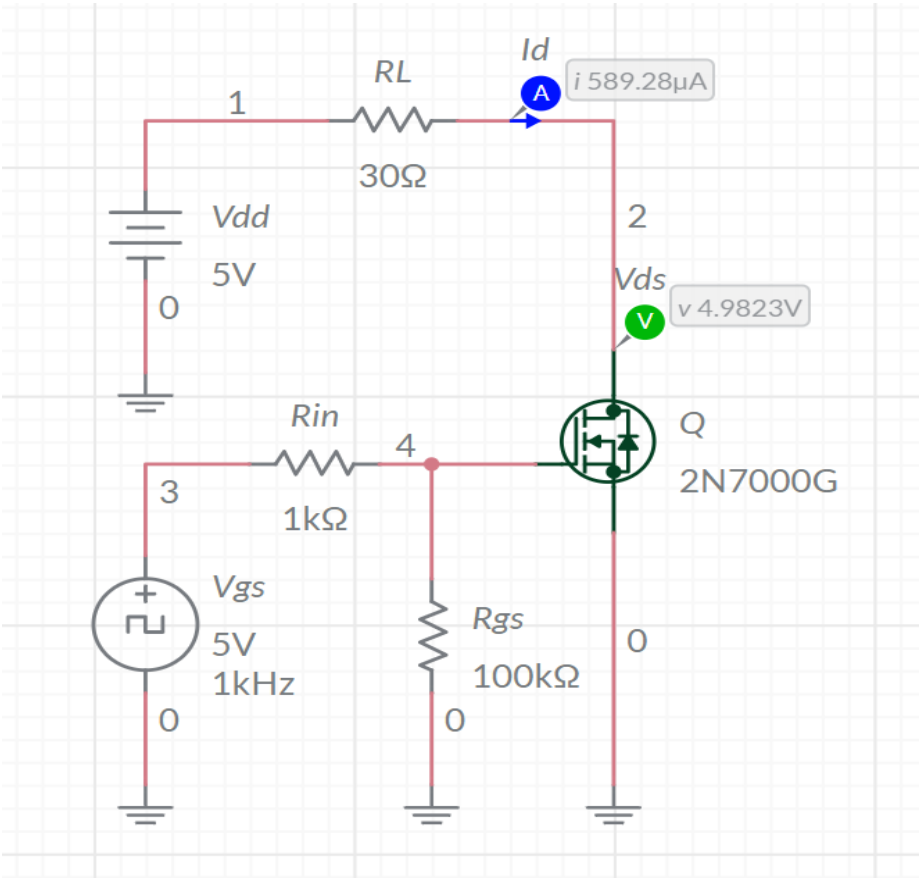
When Vbb = 5V **Ib = 834.74µA** **Ic = 5.970mA** **Vce = 59.183mV** **β= Ic/Ib = 7.151**



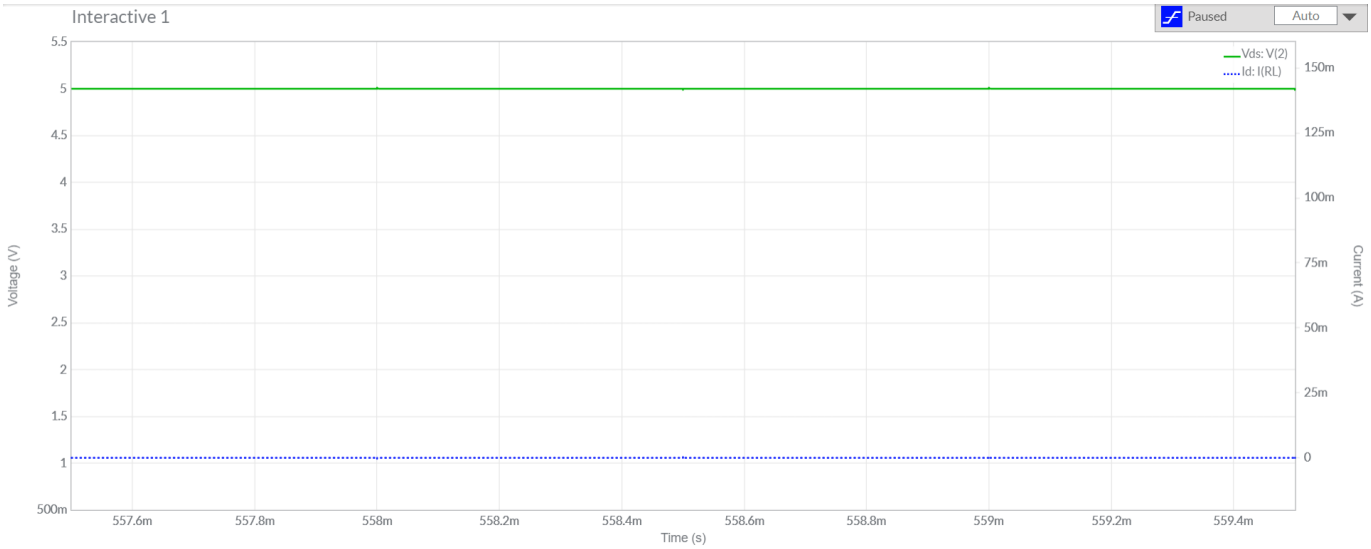
$$\beta \text{ avg} = \frac{3.106 + 100 + 100 + 17.759 + 7.151}{5} = 45.603$$

Question 3

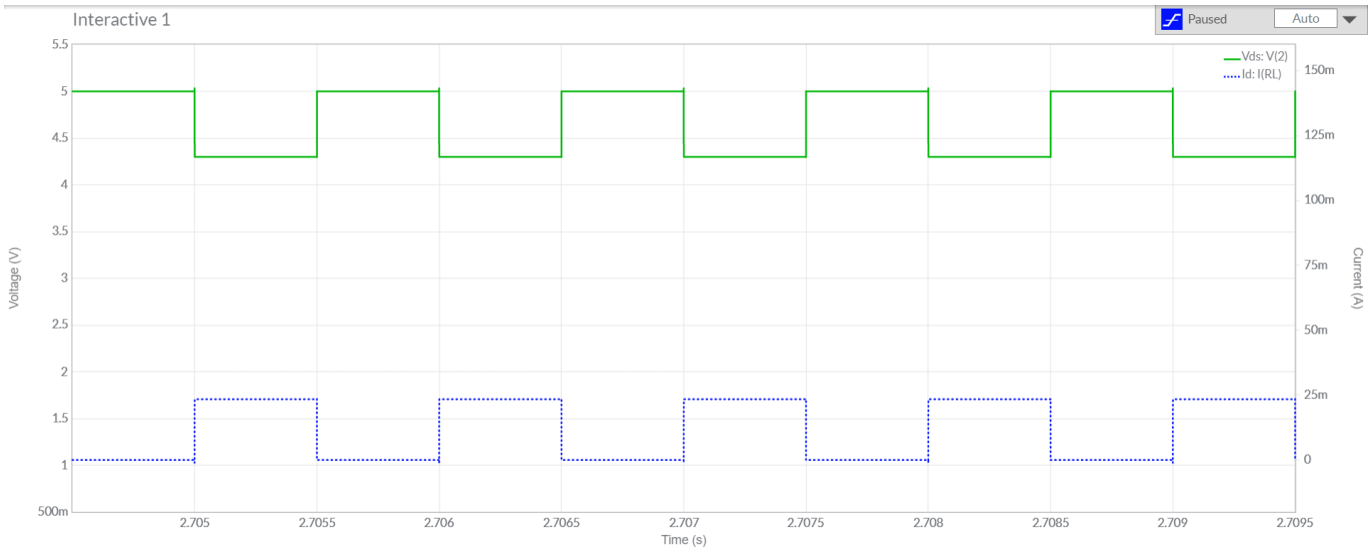
Design and simulate a MOSFET switching circuit using the model 2N7000G (An enhancement type N – channel MOSFET available in Multisim live). Values are VDD = 5V, RL = 30Ω (Load Resistance), Rin (rather say Rg) = 1kΩ. Now use Vgs = 1V, 3V, 5V, 10V and 25V separately. Use probes to measure id and Vds. Observe the changes in circuit. Take snapshots of Schematic as well as graphs. Find the approximate integer value of Vth by observing the graphs. Also describe the working of this circuit. Put it all together in a PDF document.



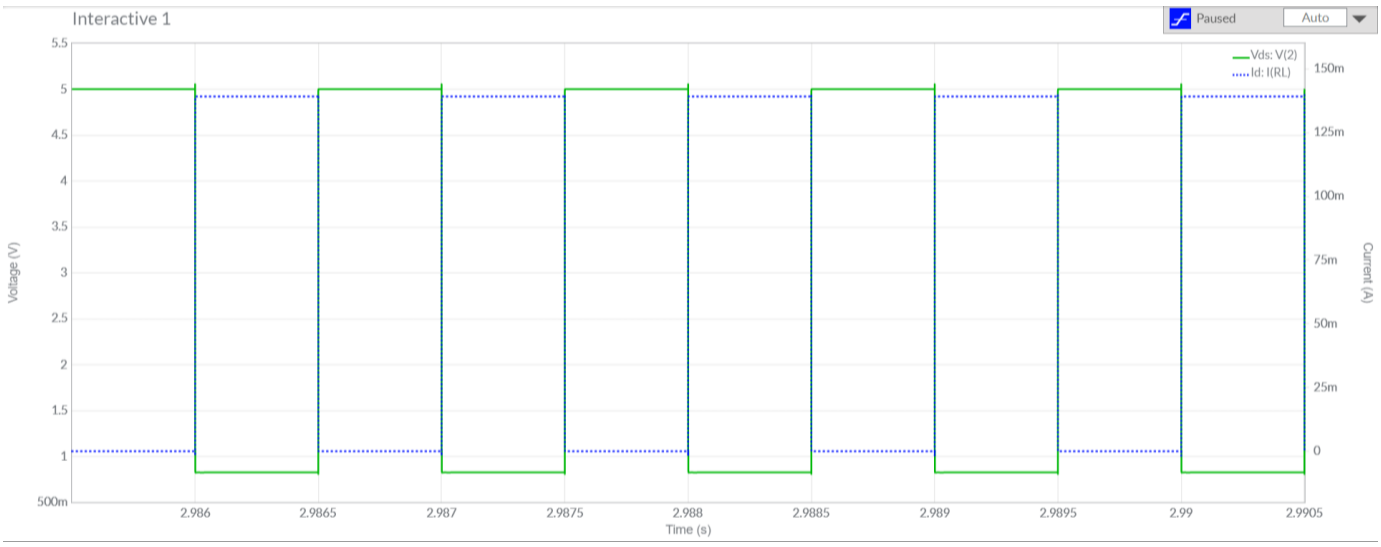
When Vgs = 1V



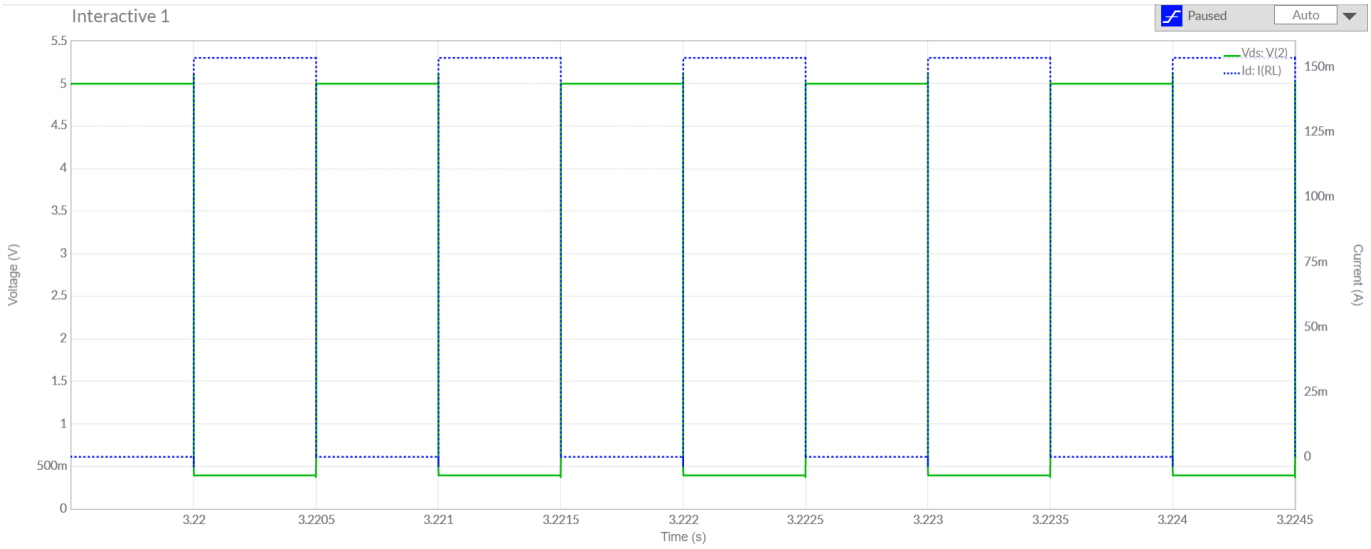
When Vgs = 3V



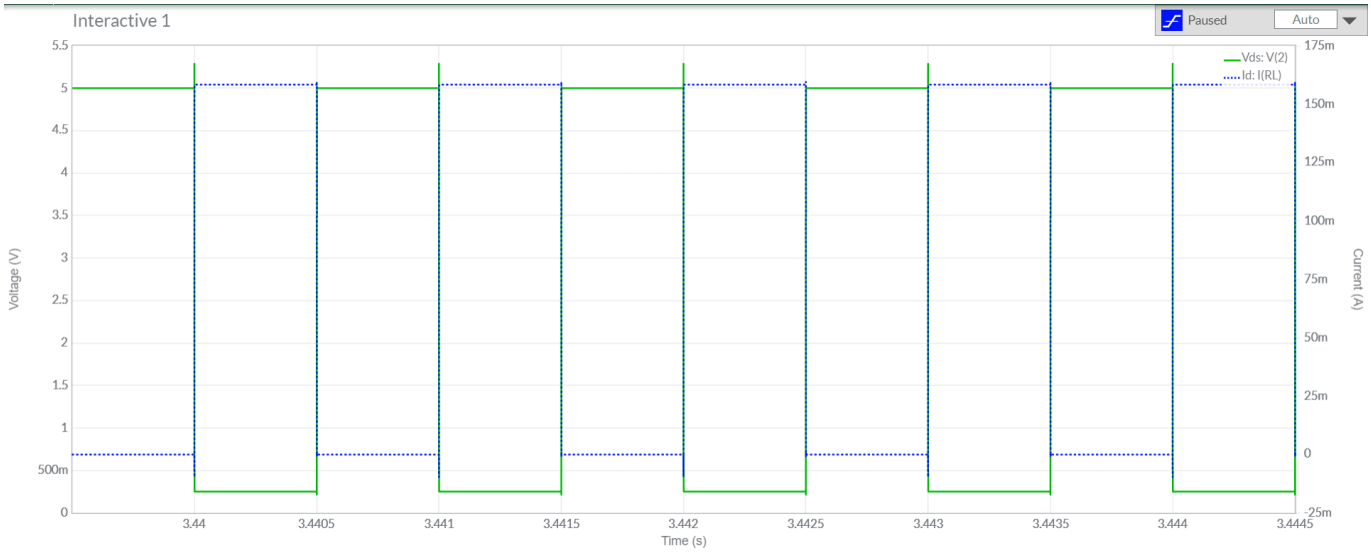
When Vgs = 5V



When Vgs = 10V



When Vgs = 25V



From above graphs we observe that the approximate integer value of Vth is 3V (Actual is somewhere around 2.1V-2.5V)

Working Of N Channel Enhancement Type MOSFET as a Switch

In the above circuit arrangement, an Enhancement mode N channel MOSFET is being used as a switch to turn the device “ON” and “OFF”. The gate input voltage Vgs is taken to an appropriate positive voltage level to turn the device and therefore the load either “ON”, (Vgs = +ve) or at a zero-voltage level that turns the device “OFF”, (Vgs = 0V).

Cut-off Region

Here the operating conditions of the transistor are zero input gate voltage (Vgs), zero drain current Id and output voltage Vds = Vdd. Therefore, for an enhancement type MOSFET the conductive channel is closed, and the device is switched “OFF”.

Cut-off Characteristics

- The input and Gate are grounded (0V)
- Gate-source voltage less than threshold voltage Vgs < Vth
- MOSFET is “OFF” (Cut-off region)
- No Drain current flows (Id = 0A)
- Vout = Vds = Vdd = ”1″
- MOSFET operates as an “open switch”

Then we can define the cut-off region or “OFF mode” when using a MOSFET as a switch as being, gate voltage, Vgs < Vth thus Id = 0

Saturation Region

In the saturation or linear region, the transistor will be biased so that the maximum amount of gate voltage is applied to the device which results in the channel resistance Rds being as small as possible with maximum drain current flowing through the MOSFET switch. Therefore, for the enhancement type MOSFET the conductive channel is open, and the device is switched “ON”.

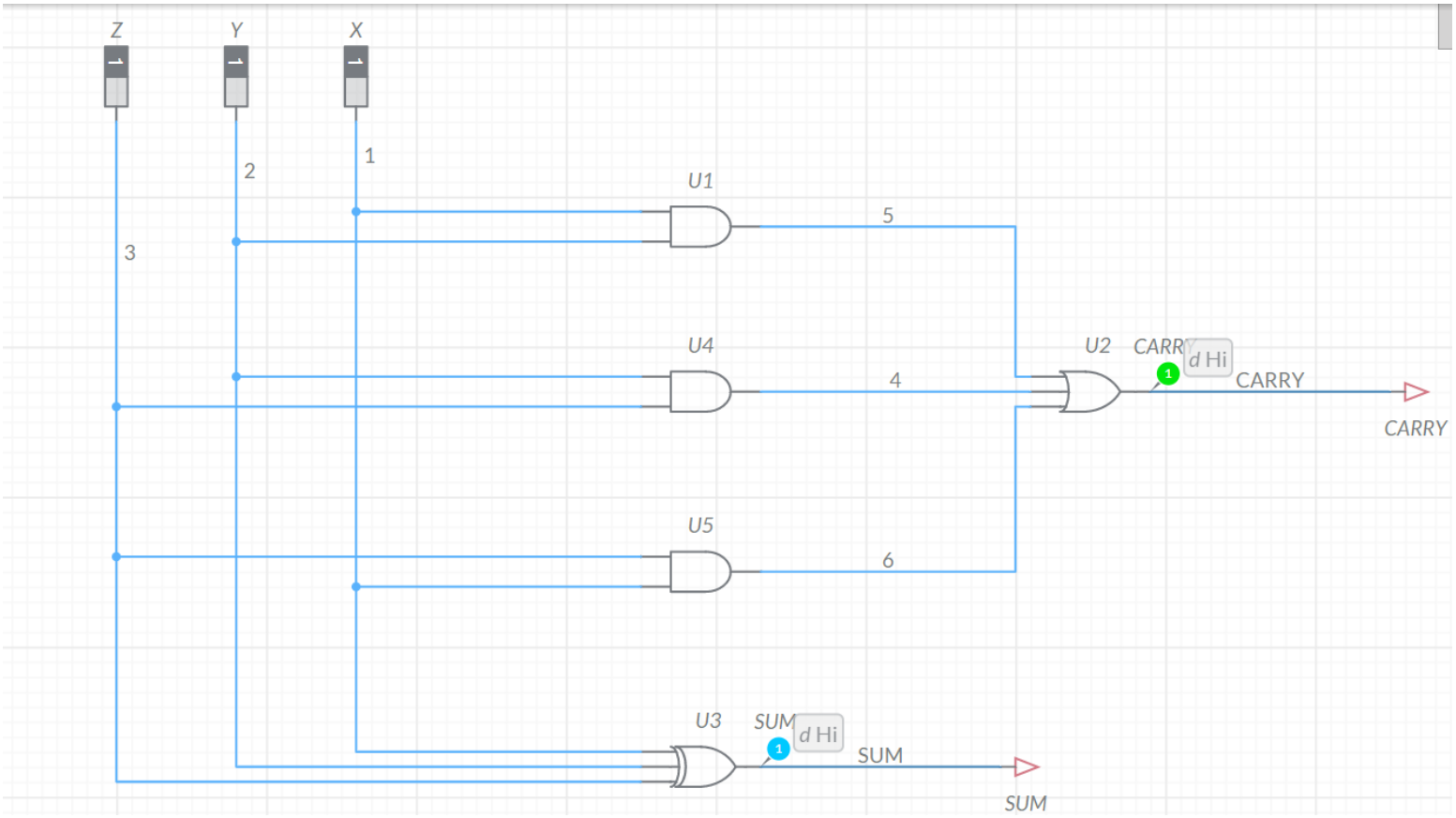
Saturation Characteristics

- The input and Gate are connected to Vdd
- Gate-source voltage is much greater than threshold voltage Vgs > Vth
- MOSFET is “ON” (saturation region)
- Max Drain current flows (Id = Vdd / RL)
- Vds = 0V (ideal saturation)
- Min channel resistance Rds < 0.1Ω
- Vout = Vds ≅ 0.2V due to Rds
- MOSFET operates as a low resistance “closed switch”

Then we can define the saturation region or “ON mode” when using a MOSFET as a switch as gate-source voltage, Vgs > Vth thus Id = Maximum.

Question 4

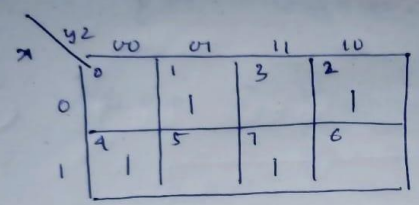
Design a full adder circuit using logic gates. Make the truth table and derive the simplified Boolean expression using K-map. Show the derivations. Take snapshots of Schematic. Put it all together in a PDF document.

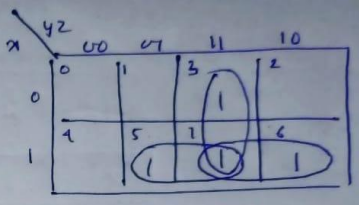


Full adder Truth table.

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full Adder k map





$S = x'y'z + x'yz' + xy'z' + xyz$

$= z'(xy' + x'y) + z(xy + x'y')$

$= z'(xy' + x'y) + z(xy' + x'y)'$

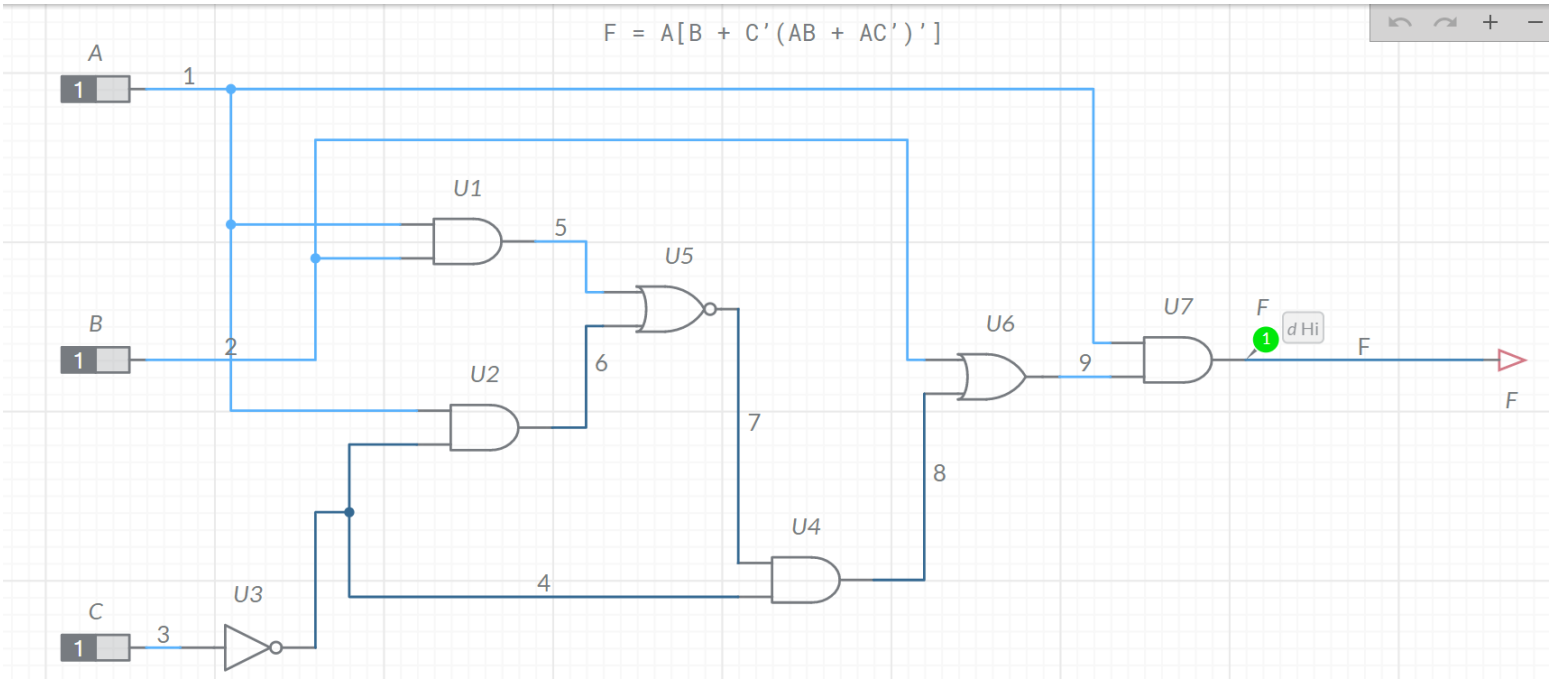
$= z \oplus (x \oplus y)$

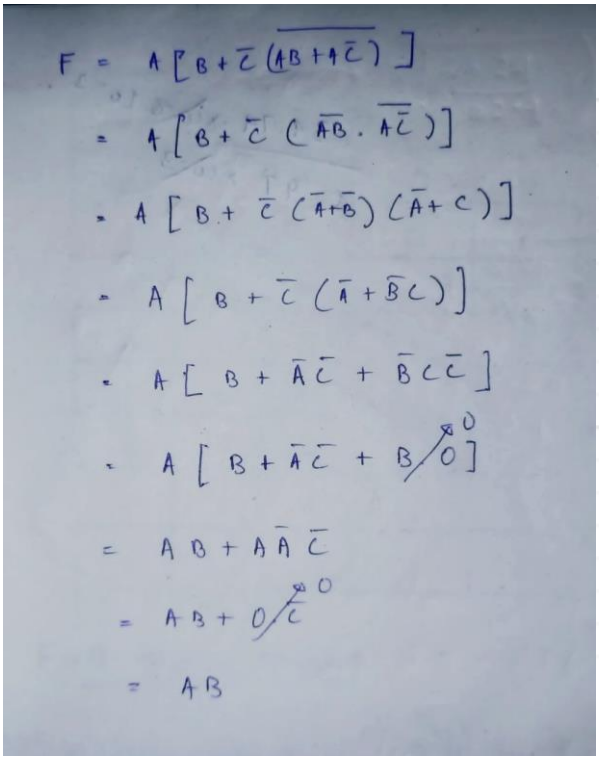
$= x \oplus y \oplus z$

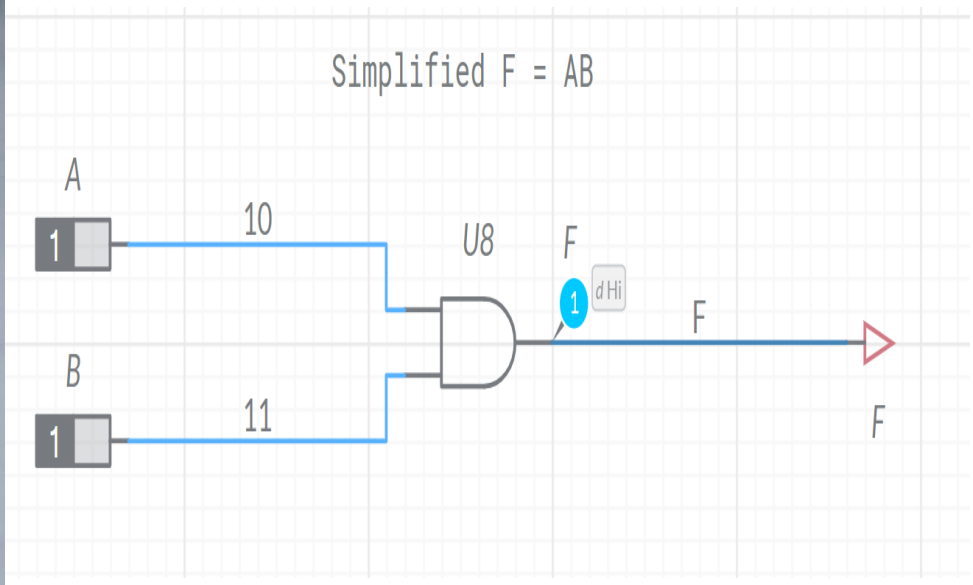
$C = xy + yz + zx$

Question 5

Reduce the expression F = A[B + C'(AB + AC')'] and show the derivation. Design and simulate a circuit for the expression and verify the reduced expression. Take snapshots of Schematic and derivation. Put it all together in a PDF document.







LINK TO MY CIRCUITS

Question 1 - Half Wave Rectifier Without Filter

Half Wave Rectifier Without Filter - Multisim Live

Half Wave Rectifier With Filter

Half Wave Rectifier With Filter - Multisim Live

Question 2 - BJT Common Emitter

BJT Common Emitter - Multisim Live

Question 3 - n-MOSFET as Switch

n-MOSFET as Switch - Multisim Live

Question 4 - Full Adder

Full Adder - Multisim Live

Question 5 - Logic Expression

Logic Expression - Multisim Live