

DSF 4/6 1.1-1.3

0 1 1 0 ⑥

$$\begin{array}{r} 1110 \\ 1011 \end{array} \quad \begin{array}{c} (-2) \\ (+3) \end{array}$$

-1 1 0 1 0 ⑦

10001 ①

Joy's DSF NOTES SP21

$z^4 \dots z^2$

$$A = (-1)^{n-1} \sum_{i=0}^{N-1} a_i z^i$$

10011₂

10000 ⑧

Take 2's complements

$i=0$

sign bit.

$16 + 2 + 1$

flips sign.

that condition

invert bits

0 1 1 0

\downarrow

add.

1 0 0 1

-6 1110

64 + 8 + 2 + 1

1 0 0 0

$3_{10} = 0011\cancel{1}2$

0 1 1 1

invert 5 1 0 0

(1010)

1000 4 A F₁₆

$$\begin{array}{r} + \\ - \\ \hline -3 \end{array} \quad 1101$$

0 0 0 0

$\begin{array}{c} 4 \\ 16 \\ 16 \end{array}$

$\begin{array}{c} 1 \\ 16 \end{array}$

Two's complement Numbers.

进位

$$\text{negative} \quad A = a_{n-1}(-2^{n-1}) + \sum_{i=0}^{N-2} a_i z^i$$

$$\begin{array}{r} 1011 \\ 0011 \\ \hline 1100 \end{array}$$

sign

one's com

two's

comp

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$$\begin{array}{r} 010 \\ 011 \\ 010 \\ 011 \\ 010 \\ 011 \end{array}$$

$i = \text{neg.}$

$0 = \text{positive}$

most ⑨ 4-bit

$$\begin{array}{r} 0101 \\ 1110 \\ \hline 1001 \end{array}$$

7 0 1 1 1

most ⑩

$$\begin{array}{r} 0110 \\ 1000 \\ \hline 1000 \end{array}$$

8 to 7.

①

2.1 Logic gates.

~~sign~~ sign extension

inversion (NOT, AND, OR, NAND).

$$A \rightarrowtail Y \\ y = \bar{A}$$

BUF.

$$A \rightarrowtail Y \\ y = A$$

Something backwards
also works

4-bit 1 0 1 1

8-bit 1 1 1 1 0 1 1

specify same sign.

$$\bar{A}, \sim A, \neg A, A' \quad \begin{matrix} 0 & 0 \\ 1 & 1 \end{matrix}$$

$$\text{unsigned val} = \sum_{i=0}^{n-1} b_i z^i$$



and

or (short)

$$\begin{matrix} D \\ \text{unparticularity} \\ \text{c "and"} \end{matrix}$$

$$A \cdot B \\ A \vee B$$

$$A \wedge B$$

$$\overline{A \oplus B}$$

signed: 2's complement.

$$\text{val} = -b_{N-1} z^{N-1} - \sum_{i=0}^{N-2} b_i z^i$$

unassigned fractional

$$\text{val} = \sum_{i=-F}^{N-F-1} b_i z^i$$

$$b_1 \ b_0 \ b_1 \ b_{-2}$$

$$' \ 0 \ 0 \ 1 = 2.25$$

$$2 \ 1 \ \frac{1}{2} \ \frac{1}{4}$$

xor

exclusive or

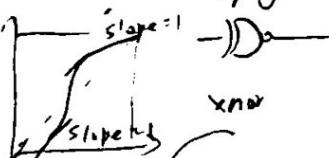


nand
always gets 1 if times at least 1 0.

B.T.R. and

$$\rightarrowtail \Delta$$

unity gain pts.



signed fraction: 1 0 . 0 1 = -1.75

$$\text{neg. MSB. } \overrightarrow{-2} \\ -b_{N-F-1} z^{N-F-1} + \sum_{i=-F}^{N-F-2} b_i z^i$$

$$i=-F$$

xnor
not exclusive or

$$\rightarrowtail \Delta$$

T.Z.

$$\rightarrowtail \Delta$$

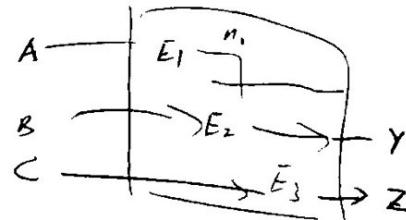
2C Power = $\frac{\text{Energy}}{\text{time}} = \frac{\text{Edynamic + static}}{\text{time}}$ static power consumption
 $P = \frac{1}{2} C V_{DD}^2 f + I_{DD} V_{DD}$ $V_P = IV$

Energy from C to V_{DD} is CV_{DD}^2
freq f
 $\frac{f}{2}$ times per second. Dynamic = $\frac{1}{2} CV_{DD}^2 f$
charged f^2 times / s. \rightarrow # of charges over time.

Ch 2:

Boolean Eq's., Boolean Alg, Logic to Gates, Multilevel Combinational Logic,
X's and Z's, Karnaugh Maps \vdash 逻辑图 - combinational building blocks, timing

$$\begin{array}{c} \bar{A} \bar{B} \bar{C} \\ A \bar{A} B \bar{B} C \bar{C} \\ \text{Implicant} \\ \text{minterm} \rightarrow AB\bar{C}, A\bar{B}C, \bar{A}BC \\ \text{maxterm} \quad A+B+C, \bar{A}+\bar{B}+C, \end{array}$$



Each minterm is "TRUE" for that row.
(max. = false) for that row.

$$(A+B)(A+B) = \prod_{\Delta} (0, 2)$$

not open not only. will eat

A	B	Y	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB	Y
0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0
1	0	0	0	0	1	0	0
1	1	1	0	0	0	1	1

one and only one output.
so P

target outputs

$$Y = M_1 + M_3 = \bar{A}\bar{B} + AB = B \cdot \Sigma(1,3)$$

A	B	$\bar{A}+\bar{B}$	$\bar{A}+B$	$A+\bar{B}$	$A+B$	\oplus means <u>OR</u> , not actual <u>OR</u> .	Y sum of m_1 and m_3
0	0	1	1	1	0	0	0
0	1	0	1	0	1	0	0
1	0	1	0	0	1	1	0
1	1	0	1	1	1	0	1

or $1+1 \rightarrow$ work.

$$Y = M_1 \cdot M_3 = M_0 \cdot M_2 = (\bar{A}+B) \cdot (A+B) = \prod_{\Delta} (0, 2)$$

3A Matlab conversion & Logic Equivalences

edit dec2xxx.m

randi [0 255], 1)

dec2bin(24)

dec2bin(24,8)

bin2dec('00011000')

dec2hex(24)

hex2dec('18')

dec2bin(-24)

dec2bin(-129)

dec2bin(-24,16)

b/in 2dec('11101000')

"help bin2dec."

bin2dec('0b1110100058')

dec2bin(71)

base = 2

$e = \lceil \log_2 d \rceil / \log(\text{base})$.

$e = 7$.

numDigits = max(e, numDigits);

powers = base.^((1:numDigits) : 0);

digits = rem(floor(d * powers), base);

rem is remainder.

Boolean Algebra.

A1 $B=0$ if $B \neq 1$ Axioms

A2 $\bar{0} = 1$ $T=0$

A3 $1 \cdot 1 = 1$ $1+1=1$

A4 $0 \cdot 0 = 0$ $0+0=0$

As $0 \cdot 1 = 1 \cdot 0 = 0$ $1+0 = 0+1=1$

And

or. replace
- w. t.
0 w. l.
Dual.

A

Theorems.

T1 $B \cdot 1 = B$ Identity

T2 $B \cdot 0 = 0$ Null elem.

T3 $B \cdot B = B$ Idempotency

(4) T4 $\bar{\bar{B}} = B$ Involution

$\rightarrow B+1=1$

$\rightarrow B+B=B$

$\rightarrow \bar{B}=B$

T5 $B \cdot \bar{B} = 0$ complements. $\rightarrow B+\bar{B}=1$ complements.

hex2dec('FFFF')

dual: replace • with +, 0 with 1.

T6 $B \cdot C = C \cdot B$ comm $B+C=C+B$

T7 $B \cdot C \cdot D = B \cdot (C \cdot D)$ assoco. $B+C+D=B+(C+D)$

T8 $B \cdot (C+C) = (B \cdot C) + (B \cdot C)$ distrib. $B+(C+C)=B+(C+C)=B$

T9 $B \cdot (B+C) = B$ covering $B+(B \cdot C)=B$

T10 $(B \cdot C) + (B \cdot \bar{C}) = B$ complement. $(B \cdot C) \cdot (B \cdot \bar{C})=0$

T11 $(B \cdot C) + (\bar{B} \cdot D) + (C \cdot D) = (B \cdot C) \cdot (\bar{B} \cdot D)$

$= (B \cdot C) + (\bar{B} \cdot D)$ consensus

$B \cdot (B+C) = B \cdot B + B \cdot C$ Distrib.

$= B + B \cdot C$ Idempotency

$= B \cdot (1+C)$ Distributivity

$= B \cdot 1$ Null elem. $= B$ identity.

simplification thm.

$$\begin{aligned} PA + \bar{A} &= P + \bar{A} \\ &\downarrow \\ &= PA + (\bar{A} + \bar{A}P) \quad \text{covering} \times \times \\ &= PA + P\bar{A} + \bar{A} \quad \text{comm.} \end{aligned}$$

$$= P(A + \bar{A}) + \bar{A} = P(1) + \bar{A} = P + \bar{A}$$

$$\text{or: } PA + \bar{A} = (\bar{A} + A)(A + P) \quad T8' \\ = \bar{A} + P = P + \bar{A}$$

def. happens.

Ex1 $P\bar{A} + PA = P$ combining thm.

$$\begin{aligned} Y &= AB + A\bar{B} \\ &\downarrow \text{combining.} \\ Y &= A \end{aligned}$$

$$\begin{aligned} \text{Ex2 } Y &= (ACAB + ABC) \\ &= ACABC(1+C) \\ &= ACAB(1) \\ &= AA \cdot B \\ &= AB. \end{aligned}$$

$$\begin{aligned} \text{Ex3 } Y &= A'BC + A' \\ &= \bar{A}(BC + 1) \\ &= \bar{A} \cdot 1 \\ &= \bar{A} \end{aligned}$$

$$4) Y = A\bar{B}C + ABC + \bar{A}BC$$

$$\begin{aligned} &= \cancel{(\bar{B} + B)} \cancel{AC} + \bar{A}BC \\ &= AC + \bar{A}BC \\ &= \cancel{AC} \\ &= C(A + \bar{A}B) \\ &= \cancel{C} \end{aligned}$$

$$\begin{aligned} 5) Y &= \underline{AB} + \underline{BC} + \underline{B'D'} + \underline{AC'D'} + \underline{AD'} \quad \text{(redundant or?)} \\ &= \cancel{AB} + BC + \cancel{B'D'} + \cancel{AD'} \quad \checkmark \text{ covering.} \\ &= AB + BC + B'D' \quad \checkmark \text{ redundant.} \end{aligned}$$

$$TII: (B \cdot C) + (\bar{B} \cdot D) + (C \cdot D)$$

$$= (B \cdot C) + (\cancel{C \cdot D}) + (\bar{B} \cdot D)$$

$$= (B \cdot C) + (\bar{B} + C) \cdot D$$

redundant term.

① 3 vars

② each var presented twice.

③ At least one complement.

$$TII: B \cdot C + \bar{B}D + CD$$

$$P\bar{A} + A = P + A$$

$$= B \cdot C + \bar{B}D + CD \cdot 1$$

$$PA + \bar{A} = P + \bar{A}$$

$$= BC + \bar{B}D + CD(B + \bar{B})$$

T8':

$$= BC + \bar{B}D + BCD + \bar{B}CD \quad B + CD$$

$$= BC(1+D) + \bar{B}D(1+C) = (B+C)(B+D)$$

$$= \cancel{BC + \bar{B}D} \quad \checkmark \text{ ??? }$$

$$= BC \cdot 1 + \bar{B}D \cdot 1$$

$$= \boxed{BC + \bar{B}D} \quad \checkmark$$

duplicate.

$$Y = A\bar{B}C + ABC + \bar{A}BC$$

$$= A\bar{B}C + ABC + \bar{A}BC$$

$$= (A\bar{B}C + ABC) + (ABC + \bar{A}BC)$$

$$= AC + BC$$

HW1 Convert binary & hex w. Matlab. 2/10

9) 3.3125_{10} to unsigned fractional bin:

$$\begin{array}{l} \uparrow \\ .3125 \times 2 = 0.625 \Rightarrow 0 \\ 0.625 \times 2 = 1.250 \Rightarrow 1 \end{array}$$

$10) +5.125_{10}$ to signed two's complement frac bin.

$$\begin{array}{r} \oplus \text{sign} \quad 2^2 \quad 2^1 \quad 0^2 \\ \text{---} \quad 0 \quad 1 \quad 0 \quad 1. \quad 0 \quad 0 \quad 1 \end{array}$$

11) -6.8125_{10} to signed 2's comp

$$\begin{array}{l} \text{frac bin: } \quad \begin{array}{ccccccc} 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\ \times 2^{-1} & \times 2^{-2} & \times 2^{-3} & \times 2^{-4} & \times 2^{-5} & \times 2^{-6} & \times 2^{-7} \end{array} \\ \begin{array}{r} 0 \\ 1 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \end{array} \quad \begin{array}{r} 0 \\ 1 \\ 0 \\ 1 \\ 1 \\ 0 \\ 1 \end{array} \quad \begin{array}{r} 0 \\ 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \end{array} \end{array}$$

12) convert 1111.0101_2 to decimal.

$$\begin{array}{r} 3 \quad 2 \quad 2^1 \quad 2^0 \quad 2^{-1} \quad 2^{-2} \quad 2^{-3} \quad 2^{-4} \\ \begin{array}{r} 1 \\ 1 \\ 1 \\ 1 \\ 0 \\ 1 \\ 0 \\ 1 \end{array} \end{array}$$

neg. sign. $\cancel{\overbrace{+ 4+2+1}} \cdot 0.25 + 0.0625 = 11.3125$

13) convert 0110.0011_2 to decimal:

$$\oplus 5.1875$$

$$\begin{array}{r} \boxed{1} \quad \boxed{1} \quad \boxed{1} \quad \boxed{1} \quad \boxed{0} \quad \boxed{0} \quad \boxed{0} \\ \begin{array}{r} 0 \quad 1 \quad 0 \quad 1 \quad | \quad 1 \quad 0 \quad 1 \end{array} \\ + 0 \quad 0 \quad \underline{1} \quad 1 \quad 1 \quad 0 \quad 0 \end{array}$$

$$\boxed{1} \quad \boxed{0} \quad \boxed{1} \quad \boxed{0} \quad \boxed{1} \quad \boxed{1} \quad \boxed{0}$$

$$\begin{array}{r} \sim 1 \quad \sim 0 \quad \sim 1 \quad \sim 0 \quad \sim 1 \quad \sim 0 \quad \sim 1 \\ \begin{array}{r} 0 \quad 0 \quad 1 \quad 0 \quad 0 \quad 1 \quad 0 \end{array} \\ - 0 \quad 0 \quad 1 \quad 1 \quad 1 \quad 0 \quad 0 \\ \hline \sim 1 \quad 0 \quad 0 \quad 1 \quad 0 \quad 0 \quad 1 \\ \sim 1001001 \end{array}$$

1) dec2bin. 9206836_{10} to binary:

$$\text{dec2bin}(9206836)$$

2) bin2dec.

$$\begin{array}{r} 101000111010010111010100 \\ \text{bin2dec}(\dots) \end{array}$$

3) dec2hex 195948557_{10} to bin:

$$\text{dec2hex}(\dots)$$

4) hex2dec FACADE16 to decimal:

$$\text{hex2dec}("FACADE")$$

5) check "help dec2bin" convert -58_{10} to bin. otherwise gives 2's complement.

$$-58_{10} = \text{dec2bin('typecast(luint8(bin2dec('11000110')),'int8'))}$$

6) Convert 234_{10} to base 3:

$$234_{10} = \text{dec2base}(234, 3);$$

$$\begin{array}{r} \hat{d} \quad \hat{n} \\ 5^3 \quad 5^2 \quad 5^1 \quad 5^0 \\ 1 \quad 2 \quad 3 \quad 4 \end{array}$$

7) 1234_s to decimal: 194

8) 1100010100_2 (unsigned) to base 32. OK $\text{bin2dec}(\text{dec2base}(\text{bin2dec}(\dots), 32))$.

• Base 3: ternary 0, 1, 2

Ex: convert 42_{10} to ternary.

$$14_{10}$$

$3 \sqrt{42}$ digit in the "ones place"

$$3 \sqrt[4]{42} \text{ ten's place.}$$

$$\begin{array}{r} \frac{1}{3} \sqrt[4]{42} \text{ last place [0, 2].} \\ \frac{1}{3} \sqrt[4]{42} \text{ hundred's place.} \end{array} \quad \left. \begin{array}{r} 1 \quad 1 \quad 2 \quad 0 \\ \text{④ ③ ② ①} \end{array} \right\}$$

Binary subtraction
borrow | borrow |
1 + 0 0 X 0 + 0 | 3 2 one's

$$\begin{array}{r} -1001101 \\ \hline 1010111 \end{array} \text{ one left over}$$

$\begin{array}{r} 1100+00+00+0 \\ -1001101 \end{array}$

$$\begin{array}{r} -1001101 \\ \hline 101111 \end{array}$$

$\begin{array}{r} 1100+00+00+0 \\ -1001101 \end{array}$

$$\begin{array}{r} \cancel{10}101111 \\ \hline \end{array}$$

$\begin{array}{r} 0100+00+00+101 \\ 0011100 \\ \hline 0110101 \end{array}$

0.03125

Ternary to dec

$$3^3 \quad 3^2 \quad 3^1 \quad 3^0$$

$$1 \quad 1 \quad 2 \quad 0$$

$$27+9+6+10 = 42.$$

basestr = dec2base(D, n)

default base 10 ↑ specify what base.

$$\begin{array}{r} 78 \\ 3 \overline{) 234} \\ 21 \\ \hline 24 \end{array} \quad \begin{array}{r} 26 \\ 3 \overline{) 78} \\ 6 \\ \hline 18 \end{array} \quad \begin{array}{r} 8 \\ 3 \overline{) 26} \\ 24 \\ \hline 24 \end{array} \quad 22200$$

$$3 \overline{) 8} \quad 0.25$$

$$+ 0.0625 \\ \hline 0.1$$

$$125+50+15+4 \\ 140 \quad (194)$$

$$3. \quad 3 \quad 1 \quad 2 \quad 5$$

$$2. \quad 2^{-1} \quad 2^{-2} \quad 2^{-3} \quad 2^{-4}$$

$$0.5 \quad 0.25 \quad 0.125 \quad 2^{-2} \quad 2^{-1} \quad 2^0$$

$$3. \quad 3 \quad 1 \quad 2 \quad 5 \\ 5 \quad 0.3125 \quad 1 \quad 1 \quad 0$$

$$(1) \quad 1_2$$

$$0.3125 \times 2 = 0.6250 \Rightarrow 0$$

$$0.6250 \times 2 = 1.25 \Rightarrow 1$$

$$0.25 \times 2 = 0.5 \Rightarrow 0$$

$$0.5 \times 2 = 1 \Rightarrow 1$$

$$0.0101$$

↓

$$11.0101_2$$

$$4. \quad 2 \quad 1$$

$$0.8125 \times 2 =$$

$$1.625 \Rightarrow (1)$$

$$0.625 \times 2$$

$$= 1.250 \quad (1)$$

$$0.8125 \quad .25 \times 2 = 0.5 \quad (0)$$

$$0.625 \quad 0.5 \times 2 = 1 \quad (1)$$

$$0.0875$$

$$\begin{array}{r} 2^{-1} \quad 2^{-2} \quad 2^{-3} \quad 2^{-4} \\ 0.5 \quad 0.25 \quad 0.125 \quad 0.0625 \\ + 0.0625 \\ \hline 0.1875 \end{array}$$

(1)

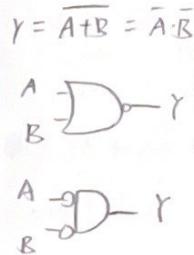
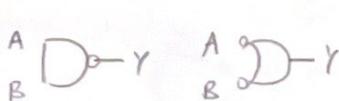
$$\begin{aligned}
 &= (A+C')(B+C')(AB+D)(AB+E) + F \\
 &= (A+C')(B+C')(A+D)(B+D)(A+E)(B+F) + F \\
 &= (A+C'+F)(B+C'+F)(A+D+F)(B+D+F) \\
 &\quad (A+E+F)(B+E+F)
 \end{aligned}$$

DeMorgan's thm.

$$\textcircled{1} \quad \overline{B_0 \cdot B_1 \cdot B_2 \cdot \dots} = \overline{B_0} + \overline{B_1} + \overline{B_2} + \dots$$

$$\textcircled{2} \quad \overline{B_0 + B_1 + B_2 + \dots} = \overline{B_0} \cdot \overline{B_1} \cdot \overline{B_2} \cdot \dots$$

$$Y = \overline{AB} = \bar{A} + \bar{B}$$



$$\text{Ex: } Y = \overline{(A+B)C}$$

$$= \overline{A+B} + \bar{C}$$

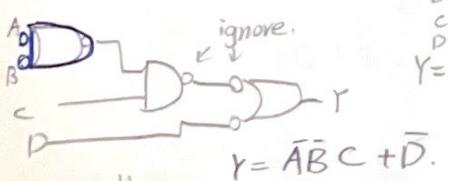
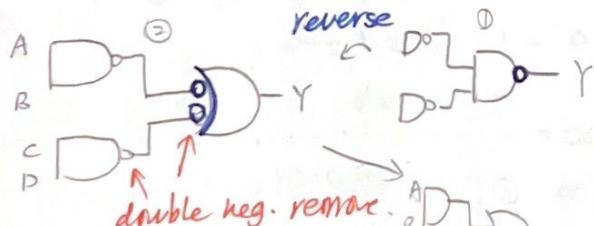
$$= \bar{A} \cdot \bar{B} + C$$

$$= \bar{A} \cdot BD + C$$

schematics.

o inverters.

push bubble forward & backward by Δ operations $-D-$ to $\rightarrow D-$



$$Y = \overline{(ACE + B) + B}$$

$$= \overline{ACE + B} \cdot \bar{B}$$

$$= \overline{ACE} \cdot \bar{B} \cdot \bar{B}$$

$$= (\bar{A}\bar{C} + \bar{E})\bar{B}$$

$$= (ACD + DE)\bar{B}$$

$$= AB\bar{C}D + \bar{B}DE$$

3B. Simplifications, DeMorgan's, Circuits

2/12

$$\begin{array}{r}
 \textcircled{1} : \quad 50 \\
 - 62 \\
 \hline
 + 88
 \end{array}$$

force it to be $\textcircled{1}$

$$\begin{array}{r}
 \textcircled{3} : \quad \begin{array}{c} 1 \\ + 0 \\ \hline 1 \end{array} \quad \begin{array}{c} 0 \\ + 1 \\ \hline 1 \end{array} \\
 - 00 \\
 \hline
 1100
 \end{array}$$

$$\begin{array}{|l}
 \hline
 \text{Simplifying: } T8': B(C+D) = BC + BD \\
 B+CD = (B+C)(B+D) \\
 \hline
 \end{array}$$

$$\text{Ex 6: } Y = (A+BC)(A+DE)$$

$$= (A+X)(A+Y) \quad \text{↓ sub}$$

$$= A + XY \quad \text{↓ } T8' (A+B)(A+C) = A+BC$$

$$= A + BCDE \quad \text{rev. sub.}$$

$$Y = AA + ADE + ABC + BCDE$$

$$= A + ADE + ABC + BCDE$$

$$= A + \underbrace{ABC + BCDE}_{\text{canceling.}}$$

$$= A + BCDE$$

multiplying all to

sum of products form
(SOP). only literals.

$$Y = (A+C+D+E)(A+B) \quad X = (C+D+E)$$

$$= A + BC + BD + BE \quad \text{↓ } T8', A + (C+DFE)B$$

product of sums (POS) $Y = (A+B)(C+D)(E+F)$

connected w. products. only have sum here

$$Y = A + B'C'DE \quad X = B'C \quad Z = BE$$

$$= (A+B'C)(A+DE)$$

multiply.

$$= (A+B')(A+c)(A+D)(A+E)$$

$$Y = AB + C'DE + F \quad W = AB$$

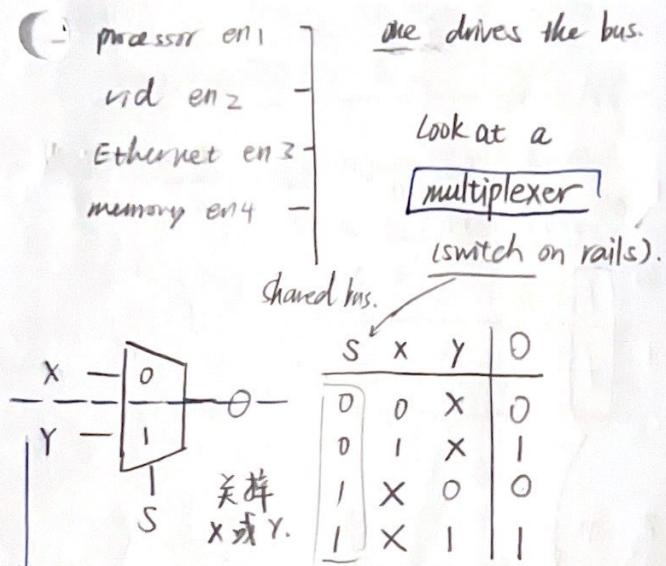
$$X = C' \quad Z = BE$$

$$= W + (CZ) + F$$

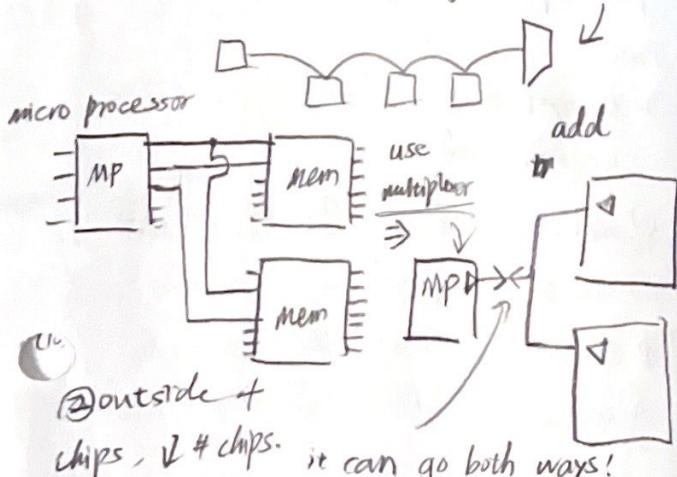
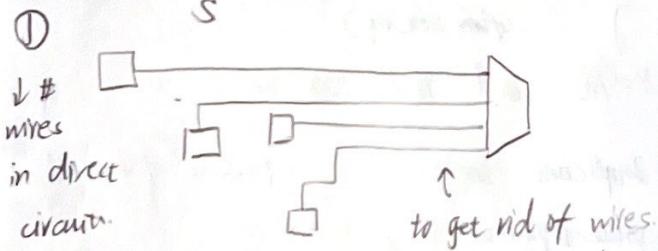
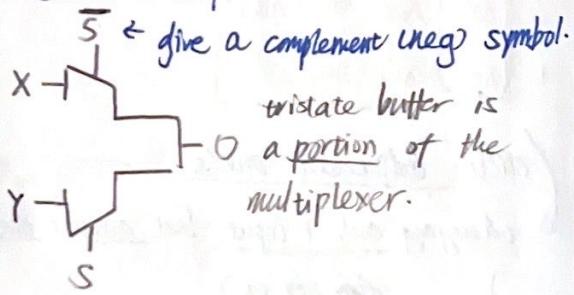
$$= (W+C)(W+Z) + F$$

$$= (AB+C')(AB+DE)F$$

Tristate busses. { many diff drivers
one active at a time.



split the circuit in half.

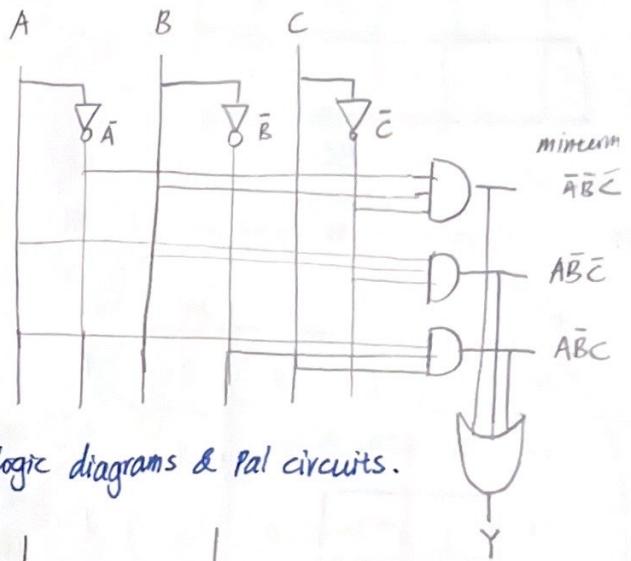


Reduce # of wires practical.

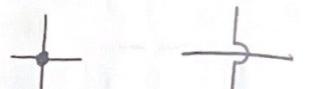
$$\textcircled{4} = \bar{x} \cdot y = \frac{v}{x \cdot y} \quad \text{if } v \neq 0$$

Two-Lv. logic. AND's followed by OR's.

$$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C$$



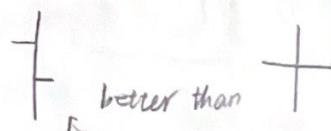
logic diagrams & Pal circuits.



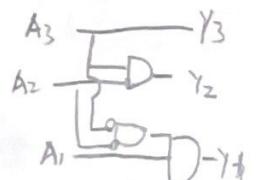
connected



not connected.



better than



Don't cares. cornit plots
that don't matter and
save space). $A_1 = D \cdot Y_0$

3C Tristate busses, K-Maps, Multiplexer

Contention. drives output to 0 or 1. 2/14

↑ power dissipation

$A = 1 - D$ $Y = X$. if inside
 $B = 0 - D$ $Y = X$. ↑ circuit.
↳ X is don't care
and contention

Float: Z.

high impedance. open

A - Z. when buffer is turned off.
tristate buffer. high impedance occurs and
Y becomes Z. Bad output?
(resistor, capacitance, etc.).

⑨
⑩

Ex:

		$\bar{A}B$			
		00	01	11	10
C	0	0	1	0	0
	1	0	1	1	0
		$\bar{B}C$			

Karnaugh Maps (k-maps).

- combining terms.

-graphically minimize equations.

$$-PA + \bar{P}\bar{A} = P$$

		only a 1 bit each time		FLIP	A	B	C	Y
		AB	C		0	0	0	1
		00	01	11	10			
0		1	0	0	0	0	0	1
1		1	0	0	0	0	1	0
						0	1	0
						0	1	1
						1	0	0
						1	0	0
						1	0	1
						1	1	0
						1	1	0
								0

		Y		AB	C	
		00	01	11	10	
		0	1			
0		$\bar{A}\bar{B}C$	$\bar{A}\bar{B}C$	ABC	ABC	
1		$\bar{A}\bar{B}C$	$\bar{A}BC$	ABC	$A\bar{B}C$	

circle adjacent one's.

changing only 1 input but output doesn't ↴

↓ (from set up)

$Y = \overline{AB}$ "and" them together.

Implicant Imply - cants. = product of literals.

prime implicant. largest circle.

Rules

- Q Every 1 must be circled at least once.
Lakhon, all 'on's.

② rect. boxes 口田   } pairs.

③ as large as possible.

④ ok to wrap around edges.

⑦ might circle "don't cares" to fill boxes.

$$Y = \overline{A}C + \overline{A}\overline{B}D + A\overline{B}\overline{C} + \overline{B}\overline{D} \quad \text{minimum rep.}$$

Ex:

AB		CD				
		00	01	11	10	00
00	00	1	0	X	1	
	01	0	X	X	1	
11	1	1	X	X		
10	1	1	X	X	1	

A + C + \bar{BD}

concentrate on
the one's.

Alt: work on

concentrate on
the one's.

Alt: unk

each col has 3 neighbors. 000 { 001
010
110

ABC		Cache Cache								110
D		000	001	011	010	110	111	101	100	
0	0	1	1	1	0	0	0	1	1	
1	0	0	1	1	1	0	0	0	1	

$$Y = \underline{\bar{A}C} + \underline{\bar{A}BD} + \underline{\bar{ABC}} + \underline{\bar{BD}}$$

se are actually neighbors! 1x8 grid not good.

4A Go over HW1. 2/15

HW2 : Boolean Axioms &

Simplifications & k-maps 2/16

#1) Prove T7. w. perfect induction (穷舉法).

$$(10) \quad (x \cdot Y) \cdot Z = x \cdot (Y \cdot Z)$$

X	Y	Z	$x \cdot Y$	$(x \cdot Y) \cdot Z$	$Y \cdot Z$	$x \cdot (Y \cdot Z)$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	1	0
1	0	0	0	0	0	0
1	0	1	0	0	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

#2 Prove T8' $x + (Y \cdot Z) = (x + Y) \cdot (x + Z)$

X	Y	Z	$Y \cdot Z$	$x + (Y \cdot Z)$	$x + Y$	$x + Z$	$(x + Y) \cdot (x + Z)$
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	0	1	1	0	0
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	0	1	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	1

#3. / complement, . AND + OR.

$$(10) \quad /x \cdot Y \cdot Z + /x \cdot Y \cdot /Z \quad \text{rewrite}$$

$$= \underline{\bar{x}} \cdot Y \cdot Z + \underline{\bar{x}} \cdot Y \cdot \bar{Z} \quad \text{J T8 Distribu...}$$

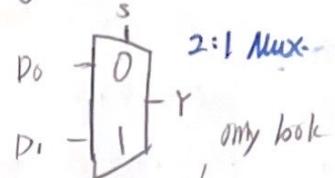
$$\textcircled{2} = (\bar{x} \cdot Y) (Z + \bar{Z}) \quad \text{J T5 complements}$$

$$\textcircled{3} = (\bar{x} \cdot Y) \cdot 1 \quad \text{J T5 complements}$$

$$\textcircled{4} = \bar{x} \cdot Y = \underline{\underline{1}} \cdot \underline{\underline{x}} \cdot \underline{\underline{y}} \quad \text{J T1 identity} \\ = 1 \cdot x \cdot y \cdot z$$

combinational building blocks.

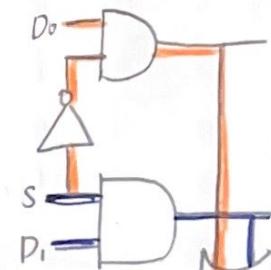
log₂ N-bit select \rightarrow input.



only look at D₀, bc. S=0.

S	D ₁	D ₀	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

More compact.
logic gates.



look at D₁ bc. S=1.

Y	D ₀	D ₁	S
0	0	0	0
0	0	1	1

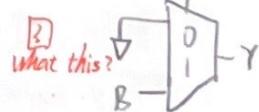
$$Y = D_0 \bar{S} + D_1 S$$

for N-input mux, use N tristates.

Turn on exactly one.

Reduce the size of mux (combine terms).

A	B	Y	A	Y
0	0	0	0	0
0	1	0	0	0
1	0	0	1	B
1	1	1	1	1



11
15

	w	x	y	z	o
v	0	0	0	0	0
					$\bar{xyz} + x \cdot \bar{y}$ <small>demorg.</small>
v	0	0	0	1	0
					$= \bar{x} + \bar{y} + \bar{z} + x \cdot \bar{y}$ <small>T2</small>
v	0	0	1	0	1
					$= \bar{x} + \bar{y} + \bar{z} + x \cdot \bar{y}$ <small>T2</small>
v	0	0	1	1	1
					$= \bar{x} + \bar{y} + \bar{z} + x \cdot \bar{y}$ <small>T2</small>
v	0	1	0	0	1
					$= \bar{x} + \bar{y} + \bar{z}$ <small>T9 covering</small>
v	0	1	0	1	0
v	0	1	1	0	1
v	1	0	0	0	1
v	1	0	0	1	1
v	1	0	1	0	1
v	1	0	1	1	1
v	1	1	0	0	0
v	1	1	0	1	0
v	1	1	1	0	0
v	1	1	1	1	1

Y\Z	00	01	11	10
00	0	1	0	1
01	0	0	0	1
11	1	1	1	1
10	1	1	0	1

$$\begin{aligned}
 &= \bar{w}\bar{z} \cdot \bar{x}, \bar{y} + w\bar{z}(x\bar{y} + x\bar{y} + \bar{x}\bar{y} + \bar{x}\bar{y}) + x \\
 &= [\bar{w}\bar{z} \cdot \bar{x}, \bar{y}] + w\bar{z}x\bar{y} + w\bar{z}\bar{x}\bar{y} + [w\bar{z}\bar{x}\bar{y}] + x \\
 &= \cancel{\bar{w}\bar{z} \cdot \bar{x}\bar{y}} + \cancel{w\bar{z}x\bar{y}} + \cancel{w\bar{z}\bar{x}\bar{y}} + w\bar{z}\bar{x}\bar{y} + x = \text{covering} \\
 &= \bar{z}\bar{x}\bar{y} + w\bar{z}\bar{x}\bar{y} + x \\
 &= (w+\bar{w})\bar{z}\bar{x}\bar{y} + w\bar{z}\bar{x}\bar{y} + x \\
 &= \cancel{w\bar{z}\bar{x}\bar{y}} + \cancel{w\bar{z}\bar{x}\bar{y}} + w\bar{z}\bar{x}\bar{y} + x \\
 &\quad \xrightarrow{\text{no } w \text{ in } \bar{z}\bar{x}\bar{y}} \\
 &\quad \xrightarrow{\text{no } w \text{ in } w\bar{z}\bar{x}\bar{y}}
 \end{aligned}$$

$$\begin{aligned}
 \#4. \quad & /(\bar{x}, \bar{y}, \bar{z}) + x \cdot \bar{y} = \\
 (10) \quad & \overline{XYZ} + x \cdot \bar{y} \quad \downarrow \text{complement T5} \\
 & \text{demorg. } x \quad \downarrow \text{T2} \\
 & = \overline{XYZ} + x \cdot \bar{y} \cdot (\bar{z} + \bar{z}) \\
 & \text{dist. T8} \\
 & = \overline{XYZ} + \overline{x\bar{y}z} + \overline{x\bar{y}\bar{z}} \quad \downarrow \text{T8} \\
 & = (\bar{x} + x)\bar{y}z + x\bar{y}\bar{z} \\
 & = \bar{y}z + x\bar{y}\bar{z} \quad \downarrow \text{covering T9} \\
 & = \bar{y}z \quad \downarrow \text{covering T9} \\
 & = \boxed{1\bar{y}, z}
 \end{aligned}$$

$$\begin{aligned}
 \#5. \quad & /x \cdot y \cdot z + /(\bar{y} \cdot \bar{z}) + y \cdot z \\
 (10) \quad & = \bar{x} \cdot yz + \overline{y \cdot \bar{z}} + yz \\
 & \text{covering} \\
 & = (\bar{x} + 1)yz + \overline{y \cdot \bar{z}} \quad \downarrow \text{T9 covering} \\
 & = yz + \bar{y} + \bar{z} \quad \downarrow \text{T12 DeM.} \\
 & = yz + \bar{y} + \bar{z} \quad \downarrow \text{Involution T4} \\
 & = z + \bar{y} \quad \downarrow \text{covering T9} \\
 & = \boxed{z + \bar{y}}
 \end{aligned}$$

$$\begin{aligned}
 \#6. \quad & /(\bar{w} + x + y) \cdot \bar{z} + w \cdot \bar{z} + x \\
 (10) \quad & = \overline{w+x+y} \cdot \bar{z} + w \cdot \bar{z} + x \quad \downarrow \text{T12 DeM.} \\
 & = \bar{w} \cdot \bar{x} \cdot \bar{y} \cdot \bar{z} + w \cdot \bar{z} + x \\
 & = (\bar{w}\bar{z}) \cdot \bar{x} \cdot \bar{y} + (\bar{w}\bar{z})(x + \bar{x})(y + \bar{y}) + x \\
 & = (\bar{w}\bar{z}) \cdot \bar{x} \cdot \bar{y} + (w\bar{z})(x(y + \bar{y}) + \bar{x}(y + \bar{y})) + x
 \end{aligned}$$

Answer.

$$\begin{array}{ccccc}
 & & & & \\
 & a & & & \\
 & \boxed{(w \cdot \bar{z}) + x + (\bar{y} \cdot x)} & & & \\
 & \downarrow & \downarrow & \downarrow & \downarrow \\
 & 1 & 0 & 0 & 0
 \end{array}$$

$$\#6. \frac{\overline{A+B+C} \cdot D + A \cdot \overline{D} + B}{W+X+Y \cdot Z + W \cdot Z + X}$$

$$= (\overline{W} \cdot \overline{X} \cdot \overline{Y} + W) \cdot \overline{Z} + X$$

$$= \overline{W} \cdot \overline{Z} \cdot \overline{X} \cdot \overline{Y} + WZ + X$$

$$= \overline{W} \cdot \overline{Z} \cdot \overline{X} \cdot \overline{Y} + WZ(X + \overline{X})(Y + \overline{Y}) + X$$

$$= \overline{W} \cdot \overline{Z} \cdot \overline{X} \cdot \overline{Y} + WZ(XY + X\overline{Y} + \overline{X}Y + \overline{X}\overline{Y}) + X$$

$$= \overline{W} \cdot \overline{Z} \cdot \overline{X} \cdot \overline{Y} + \cancel{WZXY} + \cancel{WZ\overline{X}Y} + \cancel{WZ\overline{X}Y} + \cancel{WZ\overline{X}\overline{Y}} + X$$

$$= \cancel{Z\overline{X}\overline{Y}} + WZ \cdot X + WZ \cdot \overline{X}Y + X$$

$$= WZ(X + \overline{X}Y) + X + \cancel{Z\overline{X}\overline{Y}}$$

$$= W(ZX + Z\overline{X}Y) + X + \cancel{Z\overline{X}\overline{Y}}$$

$$= WZ(X + \overline{X}Y) + X + Z(\overline{X} + Y)$$

$\star \overline{AB} + A = B + A$ Absorption rule

#6

$$\overline{W+X+Y} \cdot Z + W \cdot \overline{Z} + X \quad \text{2 dem.}$$

$$\textcircled{1} \overline{W} \cdot \overline{X} \cdot \overline{Y} \cdot Z + WZ + X$$

$$\textcircled{2} \overline{W} \overline{Y} Z + WZ + X \quad \swarrow \text{absorb}$$

$$\textcircled{3} Z(\overline{W}\overline{Y} + W) + X \quad \text{2 T8} \quad \text{2 T5} \quad \overline{A} + \overline{AB} = A + B$$

$$\textcircled{4} Z(\overline{Y} + W) + X \quad \text{2 T8} \quad \text{proof: } \overline{A} + \overline{AB} = AA + \overline{AB} \quad \text{identity}$$

$$\textcircled{5} \overline{Z}\overline{Y} + ZW + X \quad \text{2 T8} \quad \overline{A} + \overline{AB} = (A + \overline{A})(A + B) \quad \text{distribute.}$$

$$= 1(A+B)$$

T8.

$$= A + B. \quad \text{T8}$$

$$x + \overline{x}\overline{W}\overline{Y}Z = (x + \overline{x})(x + \overline{W}\overline{Y}Z) \quad \text{2 T8.}$$

$$= 1(x + \overline{W}\overline{Y}Z)$$

#8.

	W	X	Y	Z
W	00	01	11	10
X	00	0	0	1
Y	01	1	1	0
Z	11	0	1	1
	0	0	0	1

WY

#9.

	WXY	000	001	011	010	110	111	101	100
W	0	1	0	0	1	0	0	0	0
X	0	1	0	0	1	0	0	0	0
Y	1	0	0	1	0	0	0	0	0
Z	0	0	0	0	0	0	0	0	0

$\star \overline{WY}$
↓ ↓ ↓
D10 000

0	1	0	0	1	1
1	1	0	0	1	1
0	0	0	0	0	0
0	0	0	0	0	0

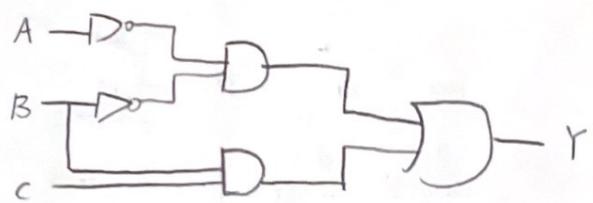
statement:

$$\begin{aligned} A * (A + B) &= A * \overline{A} + A * B \\ &= 0 + A * B \quad \text{2 T8.} \quad A\overline{A} = 0. \\ &= AB \end{aligned}$$

(13)

(15)

Glitches : one input Δ , multiple output Δ

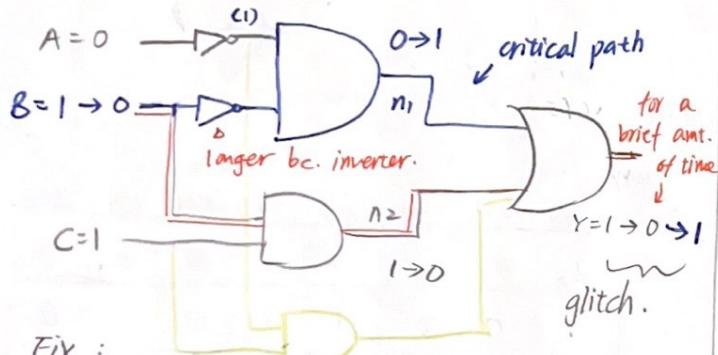


add overlap

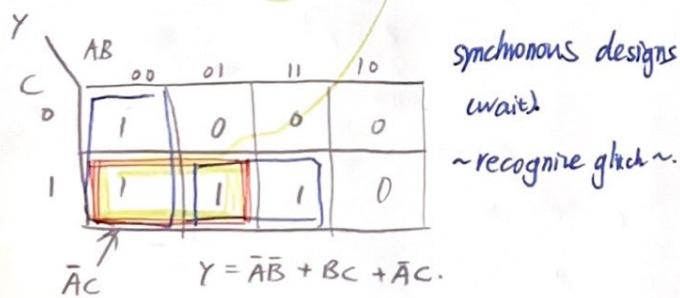
		AB	00	01	11	10
C	0	1	0	0	0	
	1	1	1	1	0	

$$Y = \bar{A}\bar{B} + BC$$

When $A=0, C=1, B$ falls (from 1 to 0)



Fix :



Breadboard.

wirecutter.

pcb matlab function.



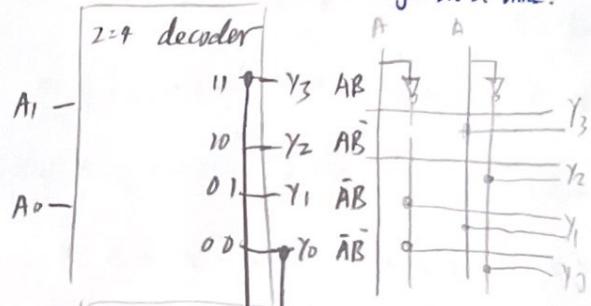
4C Finish ch. 2. Decoder, Propagation

Delay, contamination delay, glitches 2/1

N inputs, 2^N outputs

one-hot outputs

one high at a time.



OR minterms

$$Y = AB + \bar{A}\bar{B}$$

$$= \overline{A \oplus B}$$

Delay. $A \rightarrow y$ what's this?

Propagation delay. $t_{pd} = \text{Max delay range.}$

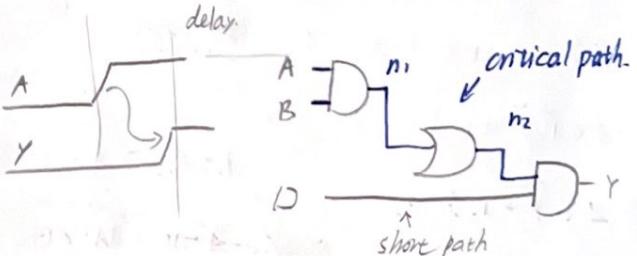
Contamination delay $t_{cd} = \text{Min delay}$ caused by

- capacitance & resistance. $C = 3 \times 10^{-8} \text{ m/s.}$

- rising and falling delays.

- Diff in I/out speeds.

- slows down when hot. slows down when cold. CMOS delay.

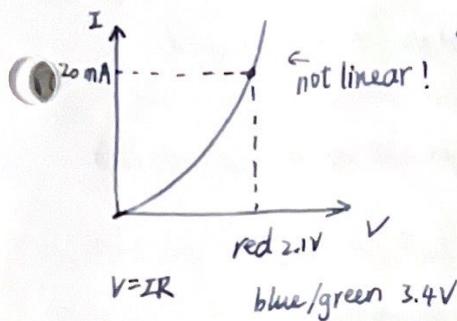


$$t_{pd} = 2t_{pd\text{-AND}} + t_{pd\text{-OR}}$$

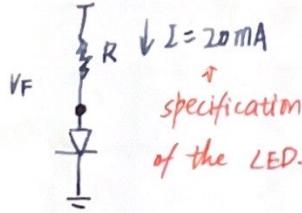
$$\text{short path. } t_{cd} = t_{cd\text{-AND}}$$

not for the entire system.

4C Breadboard and LED's 2/2



LED's operating voltage.

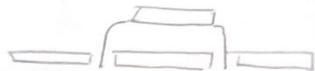
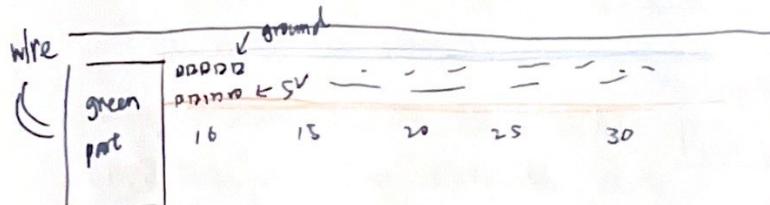


$$R_1 = \frac{V_1}{I_1} = \frac{5V - 3.4V}{20 \text{ mA}} = 80 \Omega$$

$$R_2 = \frac{V_2}{I_2} = \frac{5V - 2.1V}{20 \text{ mA}} = 145 \Omega$$

power budget of the board: 500 mA.

- colored bands encode resistance values.



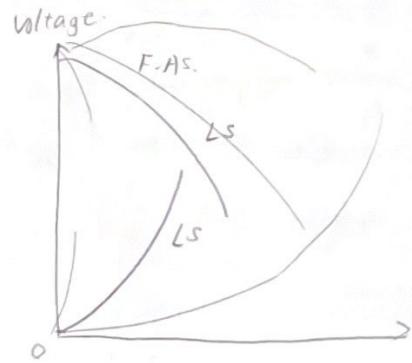
bend the legs straight...

Pin SN74AHC04N Refer to data sheets.

1A	1	14	Vcc
1Y	2	13	6A
2A	3	12	6Y
2Y	4	11	5A
3A	5	10	5Y
3Y	6	9	4A
GND	7	8	4Y

5A Theory, Breadboard, HW3,

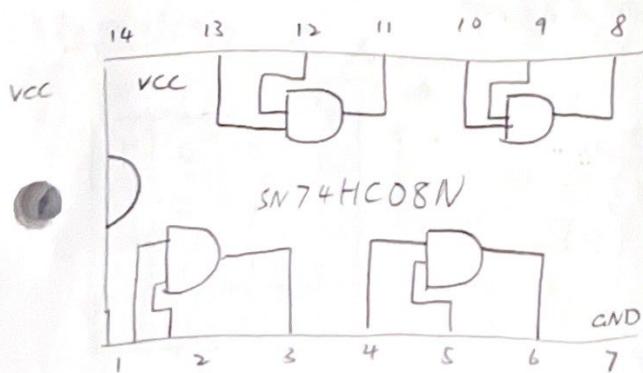
Microcontroller , kMaps. 2/26



The Art of Electronics.

TTL Data Book.

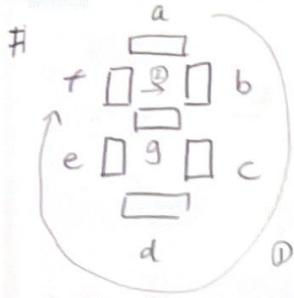
our gate : AND GATE.



$\bar{I}_1 \bar{I}_2 \cdot 4G - 4G LS$

$\bar{I}_1 \bar{I}_2 \cdot 24G - 2S 240$

common anode
common cathode.



Making Numbers! $wxyz$

$wx \backslash yz$	00	01	11	10
00	0	1	1	2
01	4	5	7	6
11	X	X	X	X
10	3	9	X	X

g-section horizontal bar)

$wx \backslash yz$	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$$\bar{y}x + \underline{w} + \bar{x}y + \underline{yz}$$

4 minterms.

$wx \backslash yz$	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	X	X	X	X
10	0	X	X	X

$$\bar{y}wx + \underline{\bar{w}xyz}$$
 2 minterms.

① Make nums in grid and place them in the right binary representations.

② Look at the g. section, for example.

③ choose 0' presentation or 1' representation bc. we have don't care's.

④ Write as few minterms as possible.

SB More K-Maps + HW 2. Prime implicant = the biggest region of 1's.

two+ ways to make the shortest Rep of a k-map.
decide based on reusability & num bits used.

2/26 in one part:
Not out of all.

Decide between b or \bar{b} . & 1's or 0's rep.

$wx \backslash yz$	00	01	11	10
00	1	0	1	1
01	0	1	1	0
11	X	X	X	X
10	1	1	X	X

OR \bar{w} $\bar{x}z$ $\bar{y}z$ $\bar{w}\bar{z}$ $y\bar{z}$
 $w\bar{y}$ $\bar{z}x$ $\bar{w}\bar{x}$ $\bar{y}z$ $\bar{y}\bar{x}$

$$w + xz + \bar{x}z + yz$$

or $w + xz + \bar{x}z + \bar{xy}$

$wx \backslash yz$	00	01	11	10
00	0	0	0	1
01	1	1	0	0
11	0	1	1	1
10	0	0	1	1

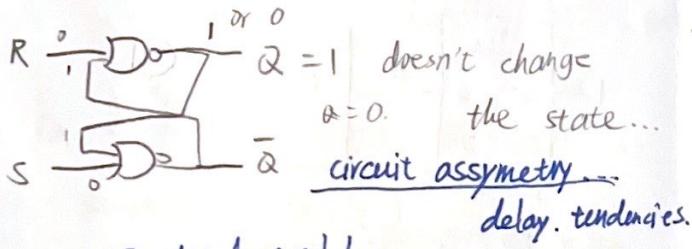
(16)

144

Don't use \bar{Q} !! func.

S	R	Q	\bar{Q}
1	1	0	0
			not valid bc $a \neq \bar{a}$
1	0	1	0
		set	
0	1	0	1
		reset	
0	0	$a = Q_{\text{prev}}$	maintain.

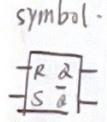
Prev: $S=0, R=0$



SR latch symbol.

Shorthand

Set: $S=1, R=0 \quad a=1$



Reset: $S=0, R=1 \quad a=0$

Don smth to avoid invalid state!!

this is
not complement!!!

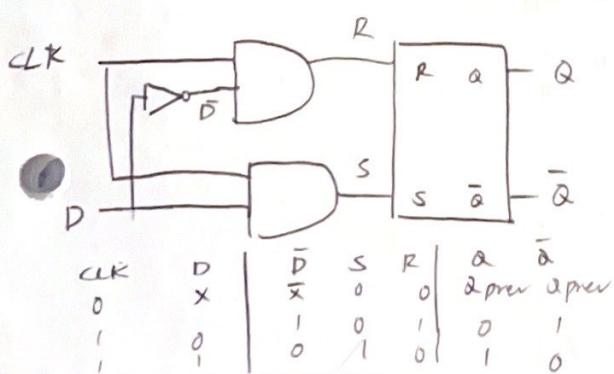
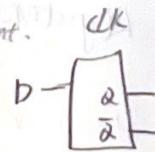
D Latch

- G/E (CLK) clock. enable signal.

- D data input

$CLK=1 \Rightarrow$ goes to Q . (transparent.)

$=0 \Rightarrow$ holds copode.



SC Ch. 3 3/1

Latches, flip flops, sync logic design

- State all input/info about circuit
- latches & flip flops memo elem. one bit of stat
- synchronous sequential circuits
comb. logic followed by flip flops.

- seq. of events, memory, feed back from output to input.

Bi-stable circuit

a, \bar{a}

SR latch

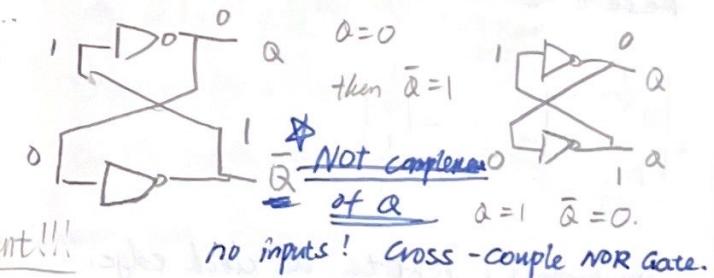
\bar{a}, a

D latch

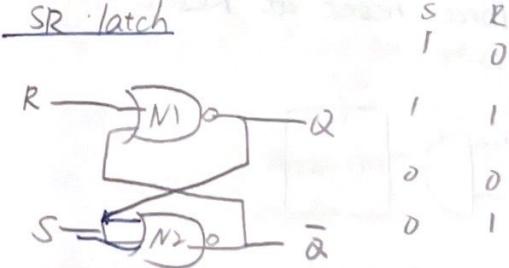
a, \bar{a}

D flip-flop.

a, \bar{a}



SR latch



① $S=1, R=0 \quad a=1 \quad \bar{a}=0$

$Q=0, \bar{Q}=1$

② $R=1, S=0 \quad a=0 \quad \bar{a}=1$

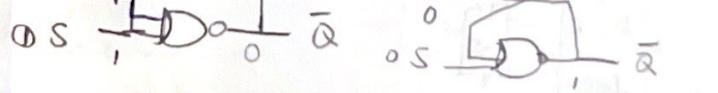
$Q=1, \bar{Q}=0$

③ $R=1, S=1 \quad a=1 \quad \bar{a}=0$

$Q=0, \bar{Q}=1$

④ $R=0, S=1 \quad a=0 \quad \bar{a}=1$

$Q=1, \bar{Q}=0$



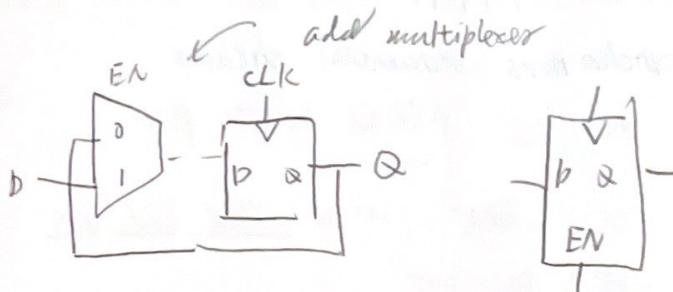
⑤

Enabled flip-flops.

Enable input (EN) ? new data (D) stored.

$EN = 1 \Rightarrow D \rightarrow Q$ on clock edge.

$EN = 0 \Rightarrow$ maintains val.

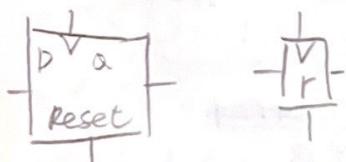


Resettable flip flops.

Inputs: CLK , D , reset.

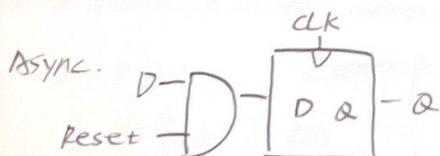
Reset = 1 $\rightarrow Q$ forced to 0

Reset = 0 \rightarrow like ord. D. ff.



Synchronous: resets at clock edge.

Async. Force reset at $reset = 1$.

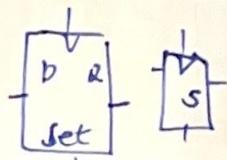
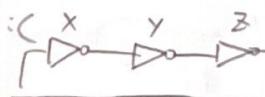


settable ff. CLK , D , Set.

$S=1$: Q is 1
etc.

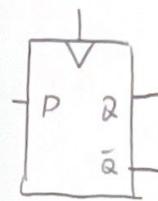
Set = 0: ord. Dff.

sequential logic



D flip flop.

edge triggered.

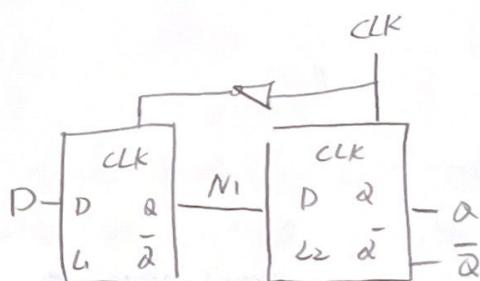


rising edge.

CLK rise from 0-1,
 D transfers to Q .

otherwise holds

Internal circuit.

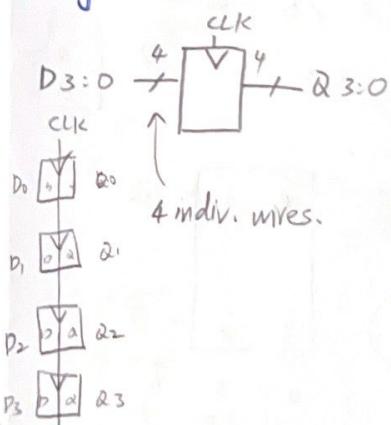


CLK	L_1	L_2	D
0	trans	op	to N_1
1	op	trans	N_1 to Q

D-latch vs. D F.F.

D latch \leftarrow kit. ignores Δ of D , only
① edge triggered the transition of clock
--- \uparrow/\downarrow edge triggered.

Registers: Multi-bit F.F.



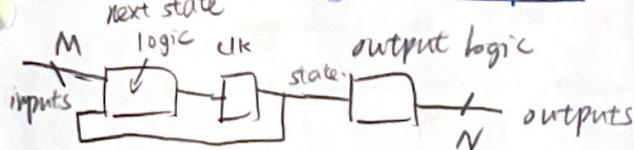
Astable, oscillates
0 inputs & 1-3 outputs.
inverter delay... cyclic path.

(8)

(4)

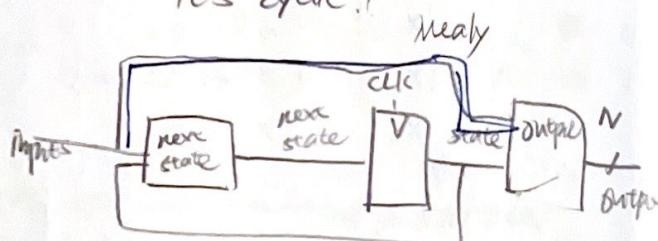
Moore FSM: depend on curr state only

Mealy FSM: curr state & inputs



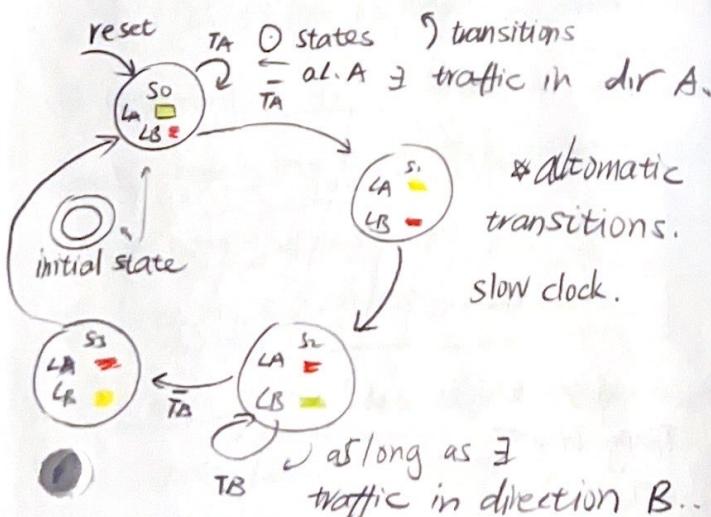
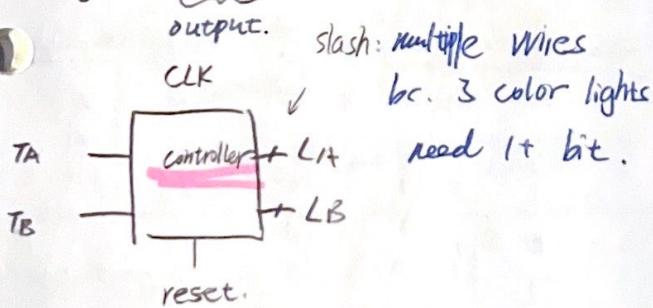
Moore.

it's cyclic!!



Ex: traffic lights. Slides P32

Sensors TA, TB. True when \exists traffic
Lights LA, LB. constantly cycles.



6A Seq. Logic, FSM, Moorm. Mealy, State Trans Diag, 3/3

Project: at home, someone work w- hardware. Have an idea -- calculator, clock, ...
Need to get past this point.

Syn. Seq. Logic Design.

Breaks cyclic paths by adding registers

↳ state of system
↳ clock edge.

Synced to the clock.

Rules:

- Every elem is a register or a combinational circuit.
- At least one is a register
- same clock signal.
- Cyclic path has 1+ register.

Common seq. circuits:

- Finite state machines (FSMs)

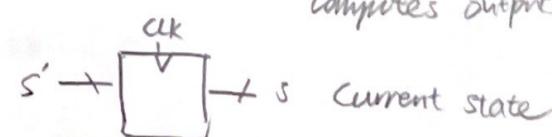
- Pipelines. ↑ comp. capacity / overlap.

parallel approach.

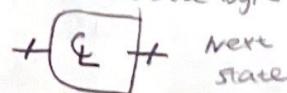
FSM.

state register { stores state
heads next

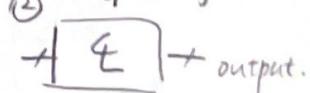
combinational logic { computes next
computes outputs



① next state logic



② output logic



one-hot encoding.

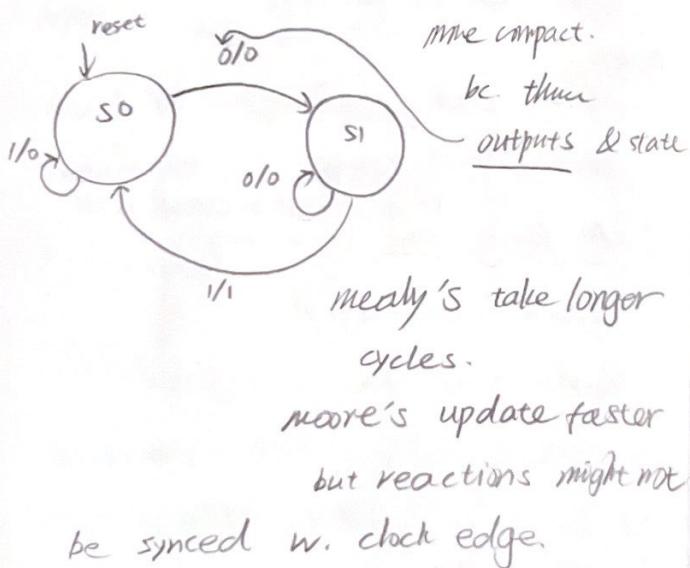
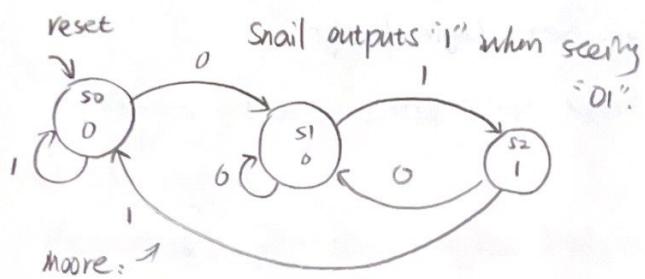
one state bit per state.

one high each time.

choose a good
combo

Easy to fix, need more flip flops.

0001, 0010, 0100, 1000 for 4 states.



Truth table for this ...

curr state	Inputs		Next
S	TA	TB	S'
S0	0	X	S1
S0	1	X	S0
S1	X	X	S2
S2	X	0	S3
S2	X	1	S2
S3	X	X	S0

not looking in
this dir. don't care.
red & yellow.

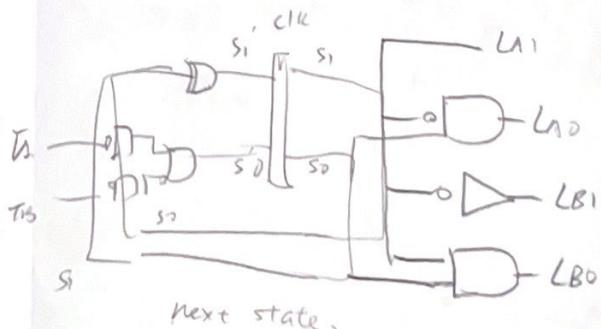
Encoded table. Don't do both bits at once!!!

Figure out S_1' , S_0' from inputs S_1 , S_0 .

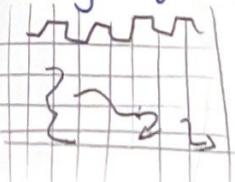
curr state	Outputs				Output	Encoder
S_1 S_0	L_{A1}	L_{A0}	L_{B1}	L_{B0}	green	00
0 0	0	0	1	0	ye	01
0 1	0	1	1	0	red	10
1 0	1	0	0	0		
1 1	1	0	0	1	$L_{B1} = \bar{S}_1$	

$$L_{A1} = S_1 \quad L_{A0} = \bar{S}_1 S_0 \quad L_{B0} = S_1 S_0$$

schem.



Timing Diagram Sequence of events.



6B. HW 3 comments, FSM factoring, signal time constraints. 3/4

Hw last prob: unique 2-input logic gates? 10 or 8.

$x \cdot y$	out	input o-output	x	\bar{x}	y	\bar{y}	input actually has 2 inputs that matter---
0 1	a	0 1	0	1	1	0	
0 0	b	0 1	0	1	0	1	
1 1	c	0 1	1	0	1	0	
1 0	d	0 1	1	0	0	1	

6 are named:

AND / NAND /

or / NOR

XOR / XNOR

what are the remaining 4?

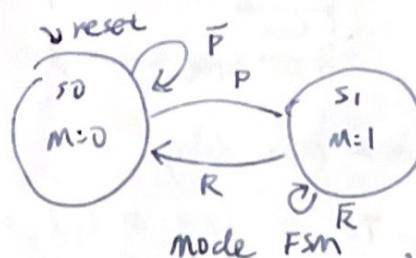
$x \cdot y$	A_1	A_2	A_3	A_4	\leftarrow 2-input nonname.
0 0	1	0	1	0	
0 1	0	1	1	0	
1 0	1	0	0	1	
1 1	1	0	1	0	

they the same!! the same be swapped order of x, y .



Ch. 3 Slides P59-75.

factored FSM's are good for simplifying inputs !!



procedure

① find m & out ② trans diagram ③ table

④ encoding ⑤ For moore -- trans table \rightarrow output

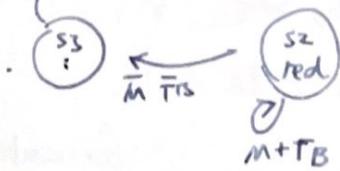
mealy machine : state transition \rightarrow state encodings.

⑥ Boolean equations

⑦ sketch schematic.

Fewer state variables
table

↓
move on.



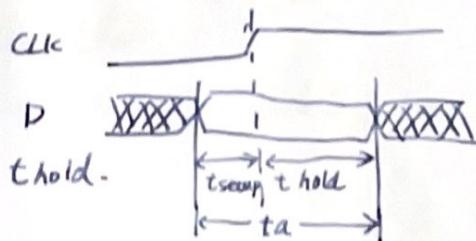
Timing D @ clock edge must be stable around it.

① Setup time t_{setup}

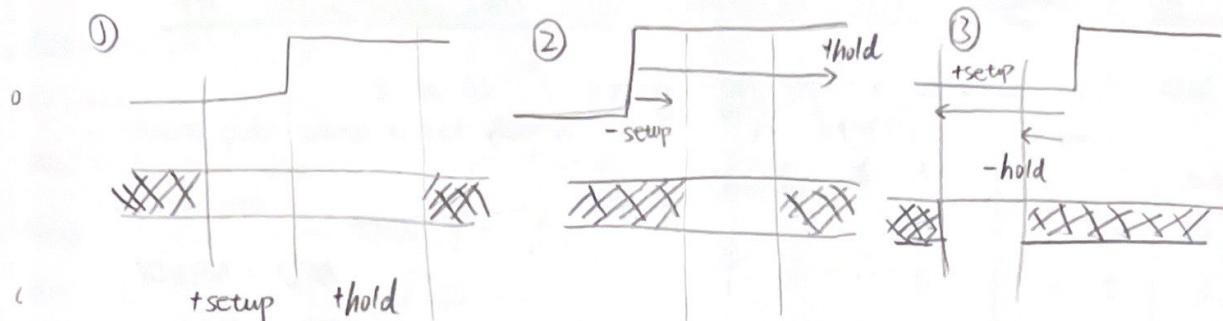
Hold time t_{hold}

Aperture time $t_a = t_{\text{setup}} + t_{\text{hold}}$.

△ tot. "must be stable" time.



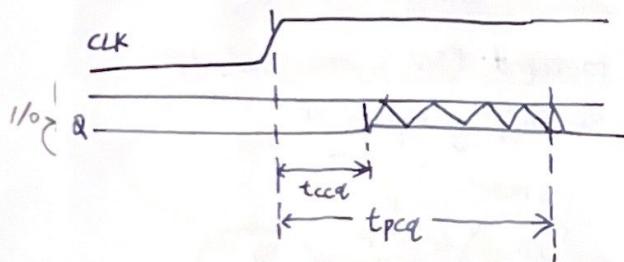
(2)



① hold time on flip flop itself delay on CLK or Dataline . buffered ...
but ② relative to the outside.

Propagation delay t_{pcq} = time after \ominus guaranteed to be stable.

Contamination delay t_{ccq} = time after CLK \ominus might be unstable.



Must be stable during aperture.
(setup & hold).

- At least $t_{\text{set up}}$ before +
- At least t_{hold} after.

Min and Max delay.

$$\text{Ex: } T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

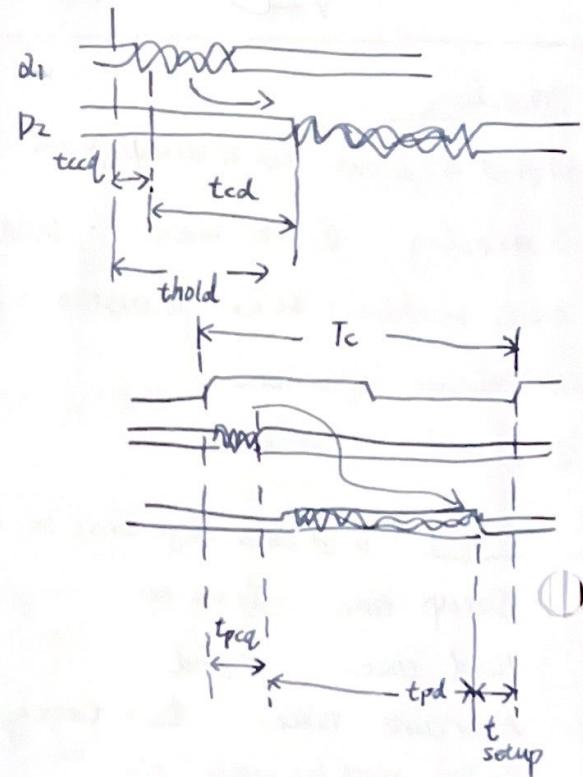
$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}})$$

$$t_{\text{hold}} < t_{ccq} + t_{cd}$$

$$t_{cd} > t_{\text{hold}} - t_{ccq}$$

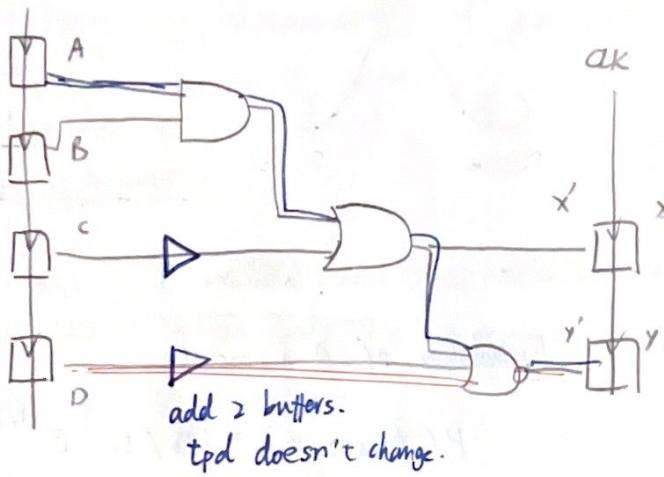
cont. d. we
can control.

contamination thru ff.



6C Timing Analysis, Constraints, synchronizers, Parallelism -End of ch.3

3/6



Timing char:

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 70 \text{ ps}$$

$$\text{per stage } t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$tpd = 3 \times 35 \text{ ps} = 105 \text{ ps} \quad \leftarrow \text{propagation delay based on longest path.} =$$

$$t_{cd} = 25 \text{ ps} \quad \leftarrow \text{cont. delay based on shortest path.}$$

$$\rightarrow t_{cd} = 25 \times 2 = 50 \text{ ps.}$$

Set up constraint

$$T_c > (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = \frac{1}{T_c} = 4.65 \text{ GHz.}$$

② Hold time constraint

$$t_{cd} + t_{cd} > t_{hold} ?$$

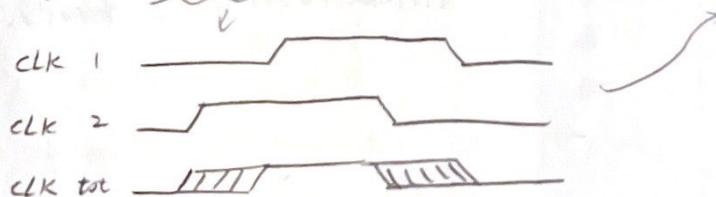
$$(35 + 25) \text{ ps} > 70 \text{ ps} \quad \boxed{\text{NO!}}$$

Fix? Artificially delay.

$$\text{changes to } (35 + 50) \text{ ps} > 70 \text{ ps.} \quad \boxed{\text{YES!}}$$

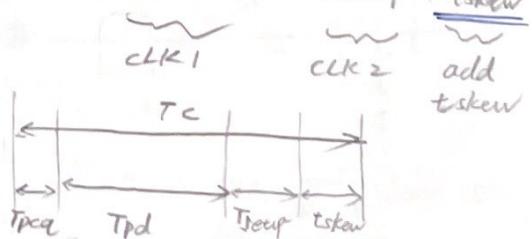
However... clock skew. (diff between 2 clock edges).

Perform worst case analysis!!

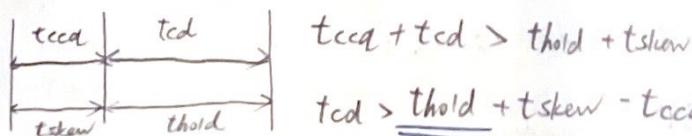


① suppose CLK 2 earlier than CLK 1.

$$T_c > t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$



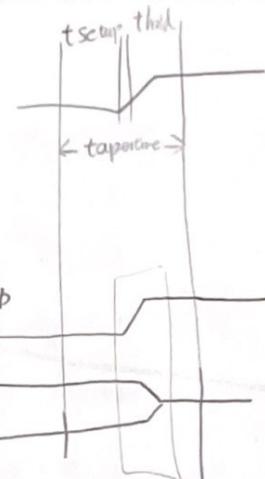
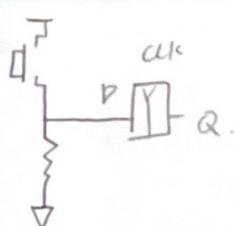
② CLK 1 is later than CLK 2.



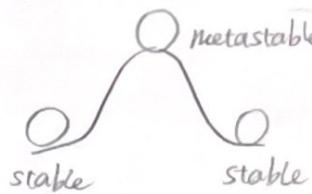
comb. logic between 2 F.F.'s.

23

Asynchronous inputs might violate the dynamic discipline.



Bistable devices has a metastable eq.



f.f. stays there
for an undetermined
amount of time.

Q is somewhere between 1.0. Not resolved.

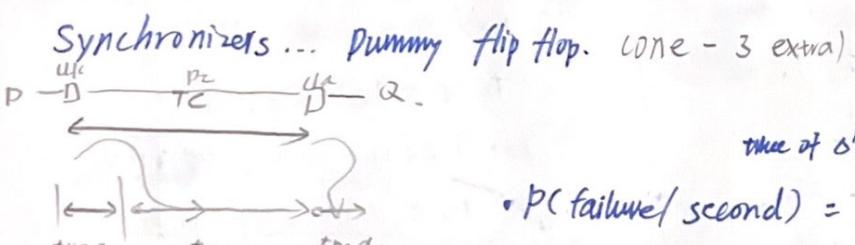
Probability of Q metastable:

$$P(t_{res} > t) = (T_0 / T_c) e^{-t/T_c}$$

t_{res} : time to resolve 1 or 0.

T_0, T_c : properties of the circuit.

the constant
for how fast
f.f. moves
away from
metastability.



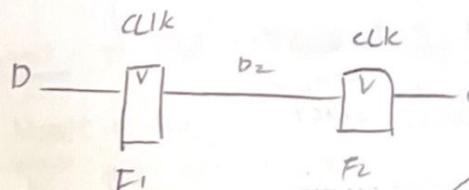
time of 0's/1's input Δ (dummy aperture).

$$\bullet P(\text{failure/second}) = (N T_0 / T_c) e^{-(t - t_{\text{setup}})/T_c}$$

D₂ has $T_c - T_{\text{setup}}$ time
to resolve 1 or 0.

• Mean time between failures MTBF:

$$\text{reciprocal. MTBF} = \frac{1}{P(\text{failure/second})} \quad (\text{unit: hours}).$$



$$T_c = \frac{1}{500 \text{ MHz}} = 2 \text{ ns}$$

$$T_0 = 150 \text{ ps}$$

$$N = 10 \text{ events/s}$$

$$T = 200 \text{ ps}$$

$$t_{\text{setup}} = 100 \text{ ps}$$

slow down clock = increase T_c

$$P(\text{failure}) = (150 \text{ ps} / 2 \text{ ns}) e^{-(1.9 \text{ ns}) / 200 \text{ ps}} = 5.6 \times 10^6$$

$$P(\text{f/second}) = 10 \times 5.6 \times 10^6 = 5.6 \times 10^5 \text{ /s.}$$

$$\text{MTBF} = \frac{1}{P(\text{f/second})} = \frac{1}{5.6 \times 10^5 / \text{s}} \approx 5 \text{ hrs.}$$