CMOS Imager Design with 3-Transistor Pixel, C2MOS Latches, and Operational Transconductance Amplifiers

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***Abstract*— The three-transistor CMOS active pixel sensors (3T-APS) generates voltages in proportion to incident light sensed by photodiodes, which have wide applications in digital image sensing. This project designs and simulates a simple CMOS imager circuit with Cadence. The main components are the single 3-T pixel, two C2MOS shift registers for column and row selections, and a column amplification stage with operational transconductance amplifiers (OTA). The schematic, symbol, layout, and incremental simulation results are presented. The voltage output from a 4 x 4 pixel array is also simulated.**

***Keywords*— CMOS Image Sensor, C2MOS Shift Registers, OTA, Circuit Simulations**

I. Introduction

Complementary metal-oxide semiconductor (CMOS) image sensors are widely used in applications such as digital cameras and biosensors. Using one NMOS transistor to convert photodiode current into output voltage, a CMOS pixel is like an "electronic eye" that converts light levels into voltage signals. With a large array of pixels and column- and row-switching logic, implemented with C2MOS latches, each pixel's output can be read sequentially, allowing other digital components to re-construct the image captured by the camera.

CMOS imagers have several advantages of low power consumption, a single supply voltage, low number of transistors used in each pixel, and the capability for on-chip system integration. To understand the implementation principles of a CMOS imager, this project designs and simulates a three-transistor CMOS pixel array with C2MOS shift registers to achieve sequential voltage readout. To reduce the effects of noise and achieve more accurate readings, a five-transistor OTA is designed for column-level amplification.

A 4-by-4 pixel array is used for voltage output simulations. Then, a layout of a 2.5mm x 2.5mm CMOS imager chip is designed with Cadence, which can fit as many as _____ pixels total.

All the schematics, layouts, and simulations in this project passes the Design Rule Check (DRC) and Layout Vs. Schematic (LVS) check in Cadence Virtuoso. The chip is designed with the TSMC 0.18um CMOS fabrication process. Other specifications adhere strictly to standard practices in the VLSI industry.

II. CMOS Pixel

A. Three-Transistor Pixel Design

The three-transistor Active Pixel Sensor (3T-APS) is the simplest APS configuration. The design is presented in figure 1:

1. The cycle starts when the row select transistor (M3) is turned on. This selects all pixels of a same row of the two-dimensional array. M3 then works like a closed switch and allows the output current to flow through the column output line.

2. The reset transistor (M1) then turns on to take the photodiode to a known maximum voltage (1.8V) to reset the voltage at the critical node (Node 1) to VDD − Vth (supply voltage of 1.8V - MOSFET threshold voltage of about 0.7V).

3. After the reset transistor turns off, integration begins. The photogenerated charge from I_PHOTON discharges the sensing capacitor. The voltage drop at Node 1 is proportional to the incident light intensity.

4. When the current row is selected, the source-follower (SF) transistor M2 buffers the photodiode voltage to the pixel's output at the COL_SEL pin.

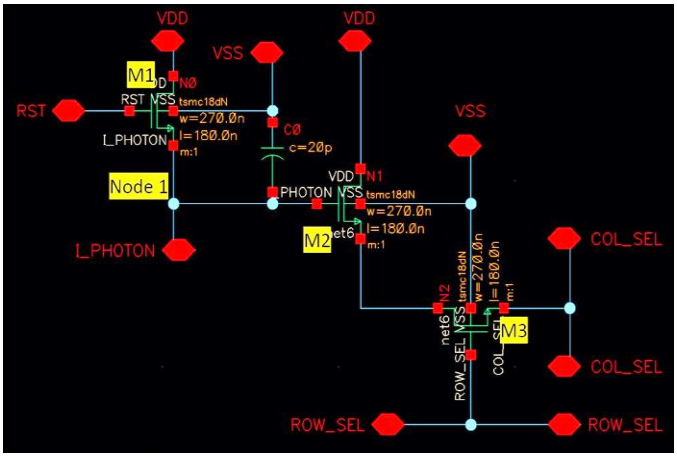


Fig. 1. The pixel schematic with labels.

To maximize the pixel fill-factor, all three transistors have minimal dimensions (3-by-2, 270n * 180n). All transistors are common-source. Therefore, the VSS metal is placed directly above all three source terminals to maximize the fill-factor.

This project treats the photodiode as an input current source for ease of simulation. Therefore, the schematic has an I_PHOTON pin that feeds in a mirrored-current of 1-100 pA, as shown in Fig. 2. The internal capacitance of the photodiode is typically about 70pF and is included in the schematic.

There are 11 pins total: VDD, VSS, COL_SEL, ROW_SEL, RST have 2 pins each, in addition to I_PHOTON. The pin configurations allow multiple pixels to be connected vertically and horizontally, where each row of pixels share the same reset signal. Each column of pixels share the same column output line, since only one pixel in this column is activated at a time.

Fig. 3 shows the pixel layout. The green N_Active region represents the photodiode area that captures incident light. The layout is dimensioned to 10 um * 10 um, with the photodiode occupying 65.379 um^2 out of the 100 um^2 area. Therefore, the fill-factor of this pixel is 65.379 / 100 = 0.6538. The device connectivity information is presented in the extracted view and matches with the schematic.

B. Single Pixel Simulations

A single pixel is tested in a test schematic, shown in Fig. 5. The photo_diode supplies 10 pA current to the pixel. The reset pulse voltage has a peak of 1.8V, a period of 2.5ms, and pulse width of 50us. Fig. 4 and Fig. 5. illustrate the test circuit and simulation results.

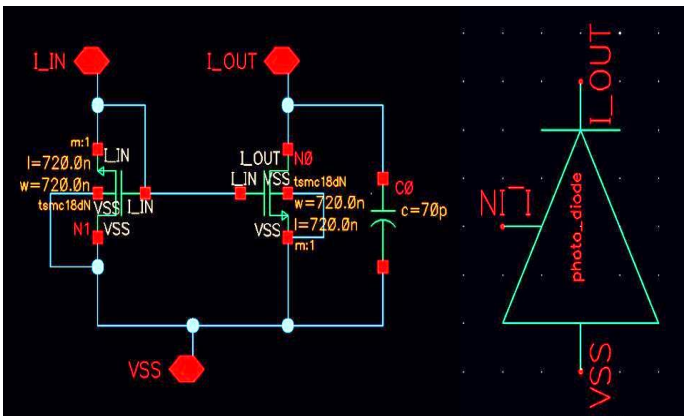
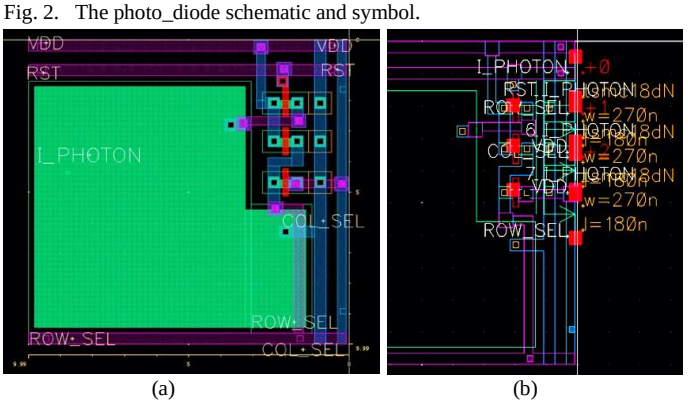


Fig. 2. The photo_diode schematic and symbol.



(a) (b)

Fig. 3. (a) Pixel layout. (b) Layout extracted view (partial).

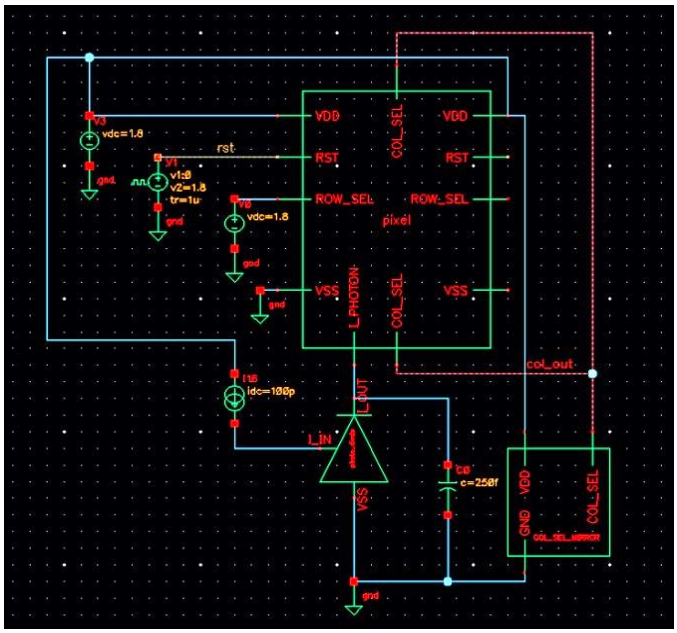


Fig. 4. Single pixel test circuit. The photodiode and colun select modules are both current mirrors.

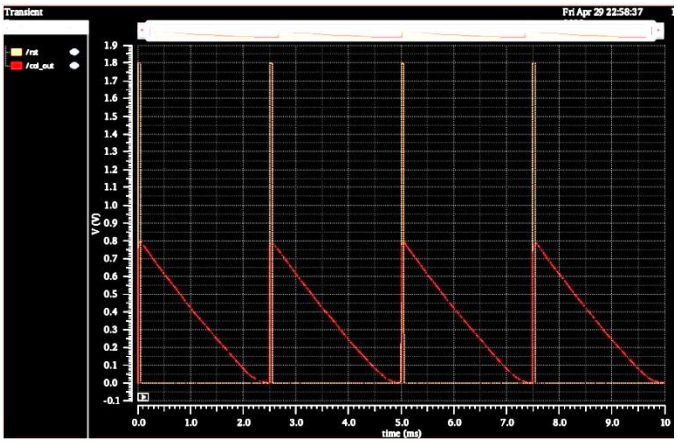


Fig. 5. Single pixel output voltage.

Since the threshold voltage is approximately 1.0V, the maximum reference voltage is expected to be 1.8V – 1.0V = 0.8V. The simulation result shows the output voltage dropping from 0.8V to about 0V throughout the integration time. If the reset pulse period is reduced, the output voltage will be recharged more often and not decrease as much. With the next reset pulse, output rises back to 1.8V and repeats another cycle.

III. C2MOS Shift Registers

A. C2MOS Schematic, Symbol, and Layout Designs

The Clocked CMOS (C2MOS) master-slave negative edge-triggered D flip-flop is an ingenious design that uses only 8 transistors to achieve a wide range of timing patterns. As shown in Fig. 6, the clock (CLK) and inverted clock (CLKN) signals are applied alternately to the PMOS and NMOS transistors. it Only the pull-down networks are enabled during 1-1 overlap and only pull-up networks for the 0-0 overlap. This allows either the master or slave stages (the left and right half of the latch, respectively) to set the circuit output on hold stage, preventing

race conditions. If clock rise and fall times are short enough, the C2MOS latch is insensitive to clock overlaps.

This implementation of the C2MOS flip flop has 4 pins: the input pulse D, CLK and CLKN, and the output pulse Q. Having 4 cascaded flip flops creates a C2MOS shift register, where outputs Q0 – Q3 creates 4 pulses rising and falling in sequence. The schematic, symbol, and layout are shown in Fig. 7.

B. C2MOS Row- and Column-Select Simulations

The main goal of the CMOS pixel array switching logic is to scan through each pixel sequentially. In the sample 4x4 array, the overall voltage outputs from pixels 0–15, respectively.

A total of 8 C2MOS latches are used, 4 for row selection and 4 for column selection. By carefully designing the D input and CLK parameters, the sequential logic is can traverse through the array. Considering clocking delays, transistor noise, and the requirement, the selection outputs shown in Fig. 8 are obtained with the following parameters:

TABLE I. C2MOS INPUT AND CLOCK PARAMETERS

	Time (us)	**D**	**CLK**	**CLKN**
Row	Period	1600	400	400
	Delay	240	250	50
	Pulse Width	400	200	200
Column	Period	400	100	100
	Delay	10	0	50
	Pulse Width	100	50	50

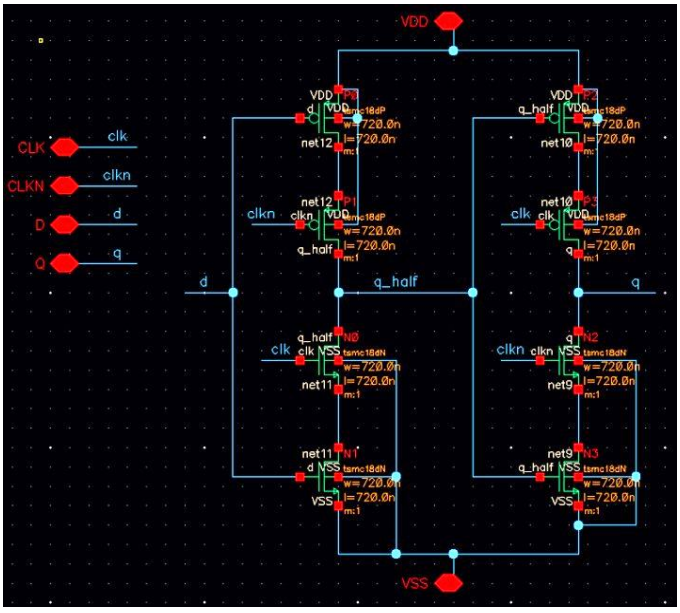


Fig. 6. C2MOS schematic.

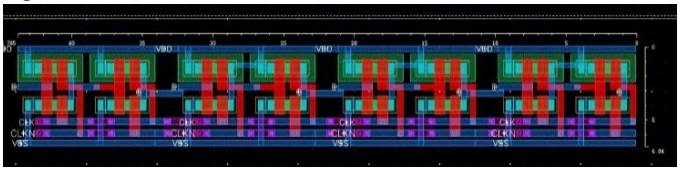


Fig. 7. Shift register layout.

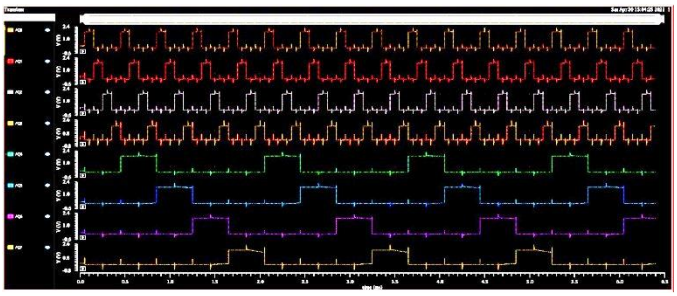


Fig. 8. Row select and column select achieves array traversal.

IV. COLUMN AMPLIFICATION WITH OPERATIONAL TRANSCONDUCTANE AMPLIFIER

A. 5-T OTA Design Parameters and Gain Caluclations

To amplify the voltage outputs, a single-stage 5-transistor operational transconductance amplifier (OTA) is used at the column level. The OTA is an amplifier whose differential input voltages produces and output current. It's a voltage-controlled current source (VCCS). There's also an additional input for bias current to control the transconductance.

In the ideal OTA, the output current

$$I_{out} = (V_{in+} - V_{in-}) * gm \quad (1)$$

$$V_{out} = I_{out} * R_{load} \quad (2)$$

This 5T-OTA uses 4 transistors at the amplifying stage and 2 NMOS transistors for a bias current mirror. There's a 10pF capacitive load at the voltage output and a bias current of 10uA (Fig. 9). A Cadence ADEL XL Local Optimization Simulation is run for transistor dimensions between 400nm to 1um. The configuration shown below produces a DC gain of about 25 dB and the gain bandwidth product of around 5M Hz. An AC analysis with input voltage of 1V gives output voltage of 83V, shown in Fig. 10.

B. 4-by-4 Pixel Array Amplified Result

Fig. 11(a) shows the 16-pixel array test schematic. Each input current ranges from 1-10 pA with the last 4 inputs ranging from 8-10 pA. Four column amplifiers are applied before the column decoder.

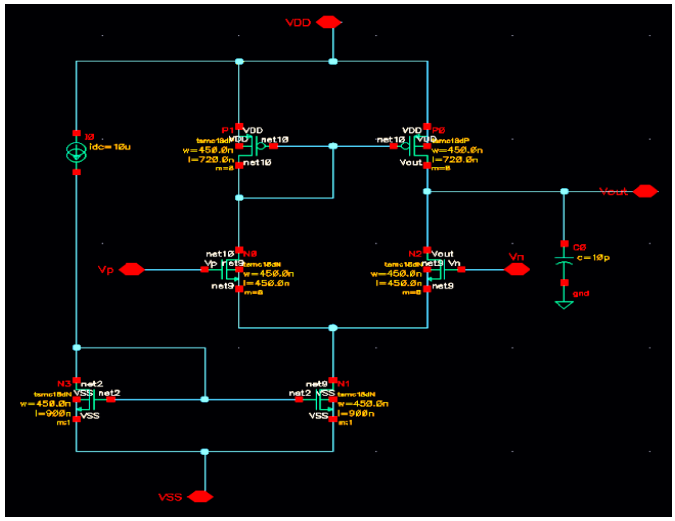


Fig. 9. 5T-OTA schematic.

It is verified that pixel elements are being traversed in order, as pixels with larger input currents see faster voltage drops during integration time. After amplification, voltage outputs are also larger and more distinguishable from their unamplified counterparts, shown in the thin lines near the 700mV range in Fig. 11(b). This allows other digital components to create higher-quality images with better light level detection.

An important next step is to further quantify the amplification gain, as the output voltage seems to be limited at 1.8V. A possible cause of this issue is the NMOS switches at the column decoder (Fig. 12).

V. 2.5mm * 2.5mm Chip Design and Layout

The same pattern shown in Fig. 12 can be repeated to create a larger chip that is 2.5mm by 2.5mm. In this layout, the column decoders, amplifiers, and row shift registers occupy the top left corner to select any pixel. The rest is all occupied by pixels. Considering larger VDD and VSS busses on the left (10-lambda) and other component spacings, this area could still fit 249 column amplifiers, and a total of 249 * 248 = 61752 pixels in the array. Photodiodes occupy 61752 * 65.379 um^2 = 4.037 mm^2, which is 4.037mm^2/ 6.25mm^2 = 64.59% of the total chip area. All layouts are carefully configured with minimized wiring area. The number of vias and metal layers are also minimized.

VI. Global Impacts of IC Design

Due to trends in fabrication techniques for increasingly small geometries, IC fabrication is becoming more energy-costly and complicated, causing large carbon emissions and energy consumptions [1]. The types of metal materials and the number of layers also have significant effects on the IC's carbon footprint. However, a minimum of 72g chemicals and 1600g fossil fuels are required to create a 2-gram microchip; water, silicon, and other secondary products add up to over 600 times

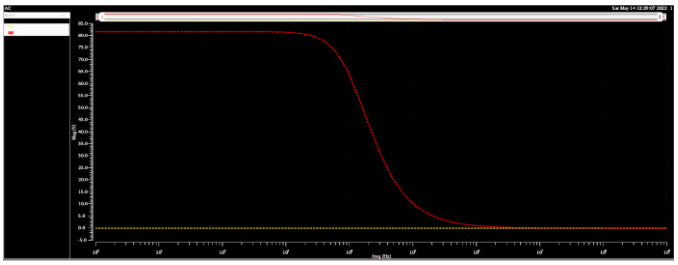
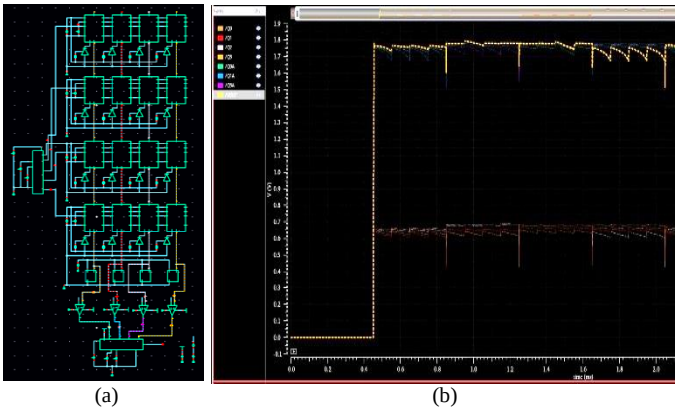


Fig. 10. The Amplifier gain AC sweep from 1-1G Hz.



(a) (b)

Fig. 11. (a) The 16-array schematic. (b) One full cycle of voltage outputs. Integration starts at 440ms. Each 400us segment corresponds to a pixel.

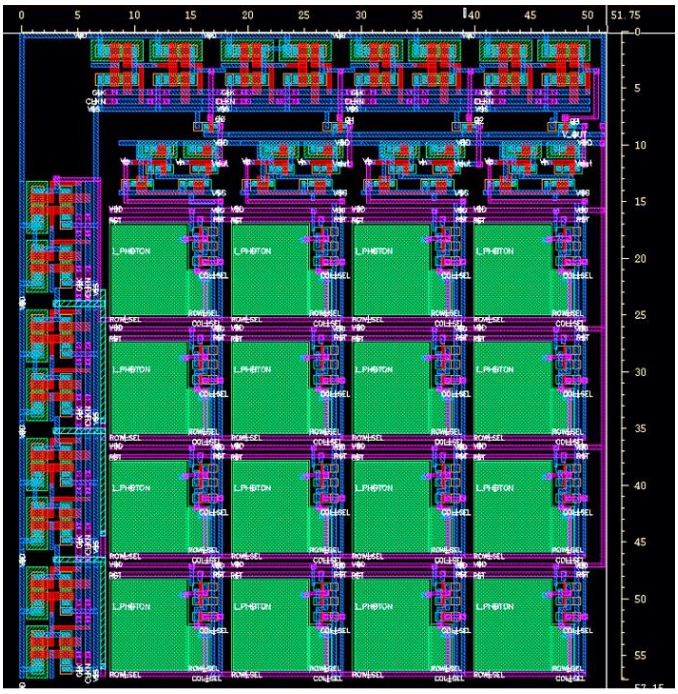


Fig. 12. Layout of the 4-by-4 pixel array. Note that there are 4 NMOS transistors below the column shift registers that control the switching of each column output.

the mass of the final IC product [2]. Although there is more awareness and policy changes on e-waste disposal [3] and global electrical engineering sustainability groups such as the Basel Convention, there is still a considerable amount of work to be done. IC fabrication is essential for global technological developments, but every engineer must be aware of its increasing and negative impact on the environment. From design to production to disposal, every step requires careful consideration and innovations to ensure sustainability.

VII. Engineering Ethics

This project's implementation process upholds the latest IEEE Code of Ethics. All three authors contributed equally to the brainstorming, design, and implementation of all components, usually working in a synchronous, seminar-style manner. All authors engaged fully in a total of 3 in-class presentations and the JHU Design Day poster session to engage in discussions with peers, instructors, and researchers from other engineering departments. Team members actively seek, accept, and offer honest criticism of technical work. Several errors in the schematic and layout design were identified and corrected after the presentations, and each team member contributed original and honest work to present simulation results verified by both the Cadence software design checks and the EN.520.216 Introduction to VLSI instructor team.

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