

WonBin Seo

Dr. Shannon Nicley,

ECE 813 Advanced VLSI Design

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Exam2

Problem 1 – 4-bit Adder Schematic – [MCGA4_Schematic]

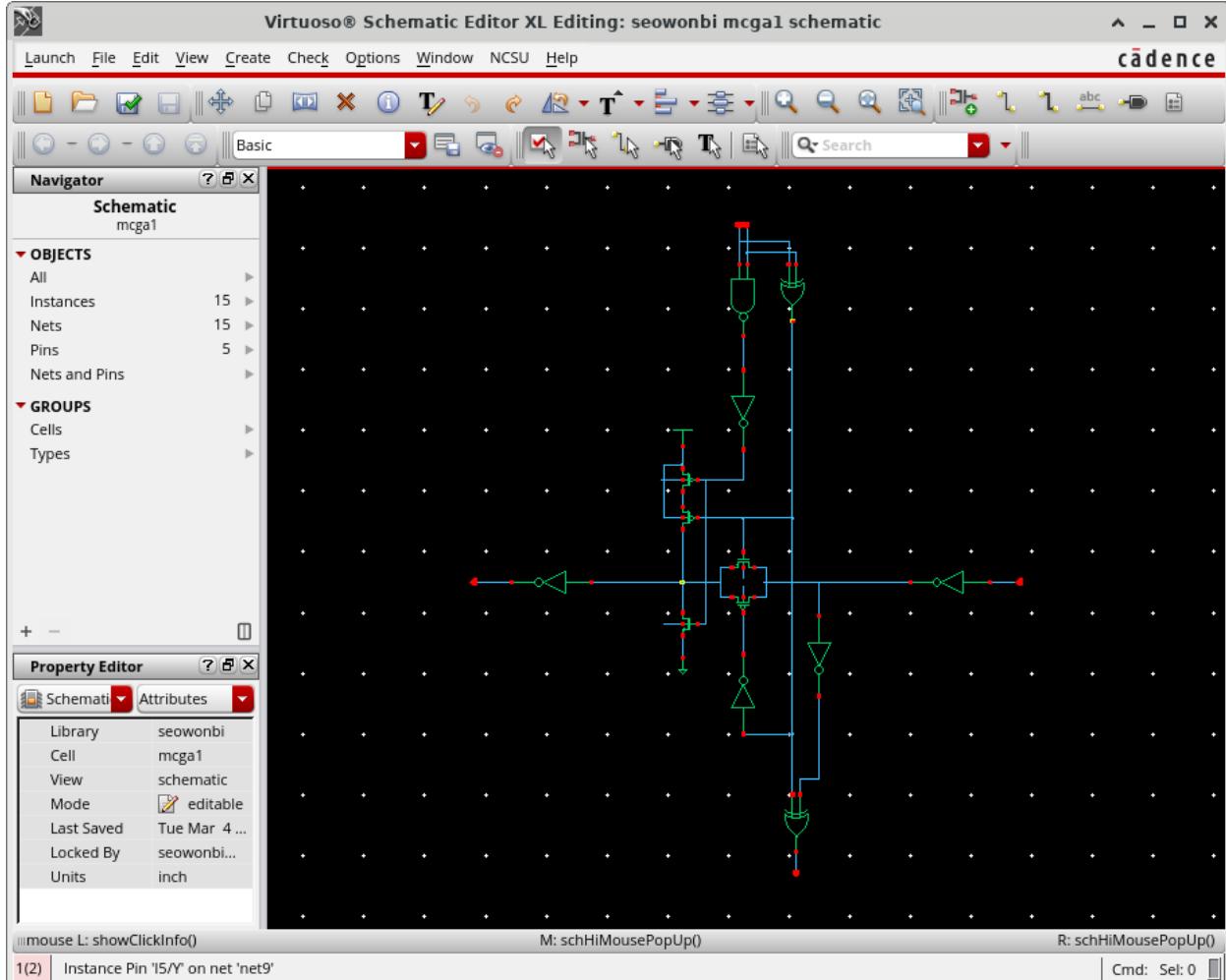


Figure 1. MCGA1_Schematic

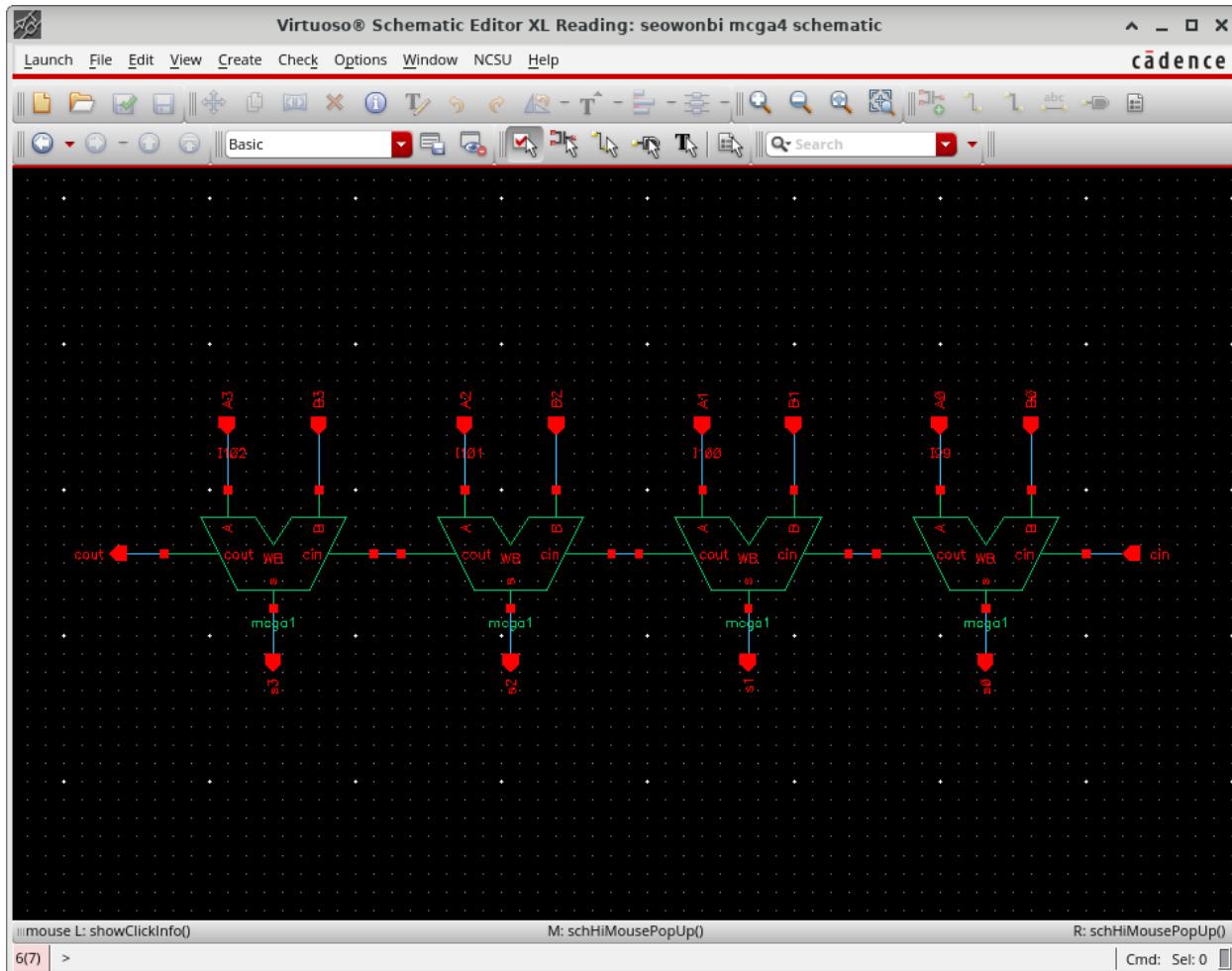


Figure 2. MCGA4_Schematic

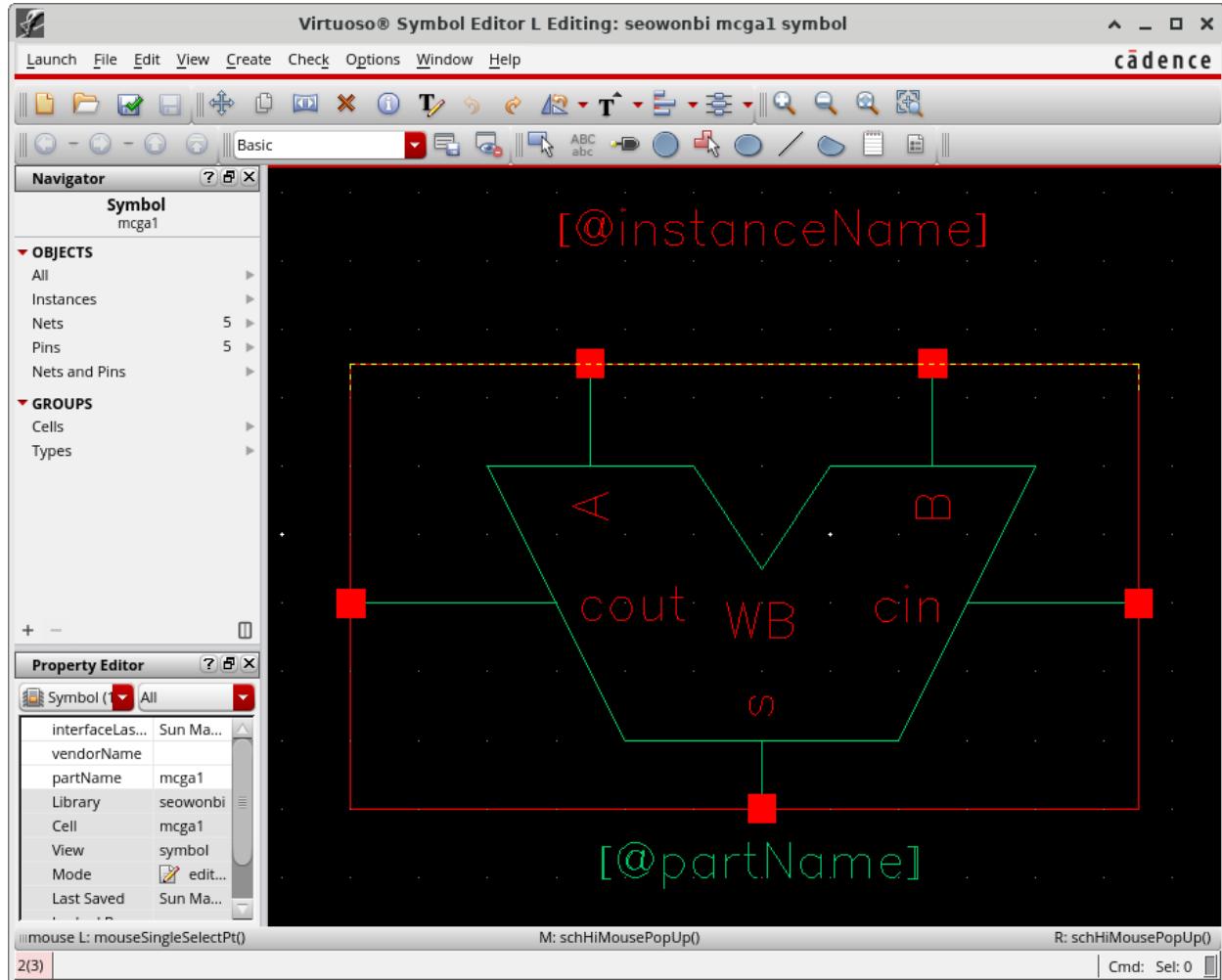
Problem 2 – 4-bit Adder Symbol [MCGA4_Symbol]

Figure 3. MCGA1_Symbol

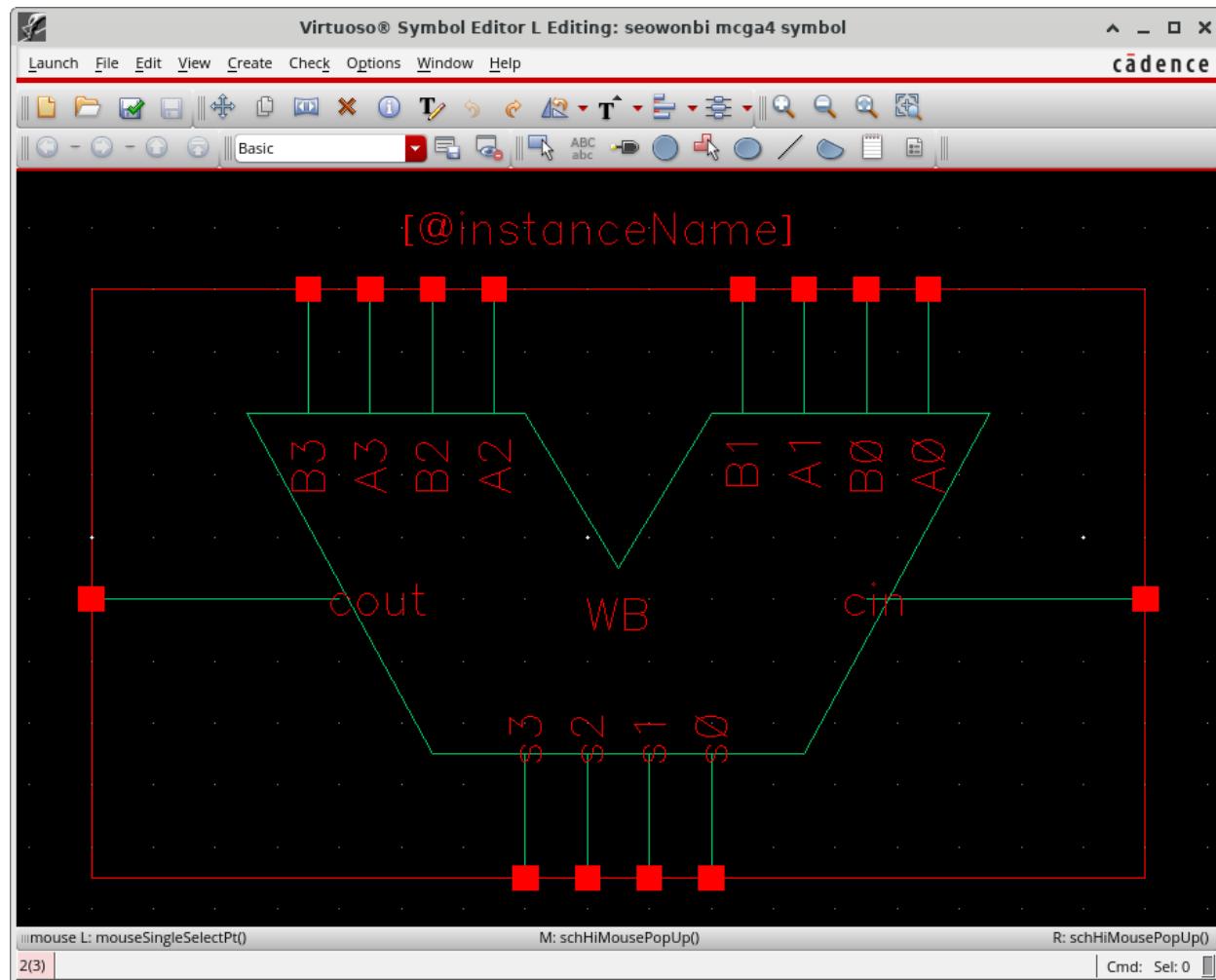


Figure 4. MCGA4_Symbol

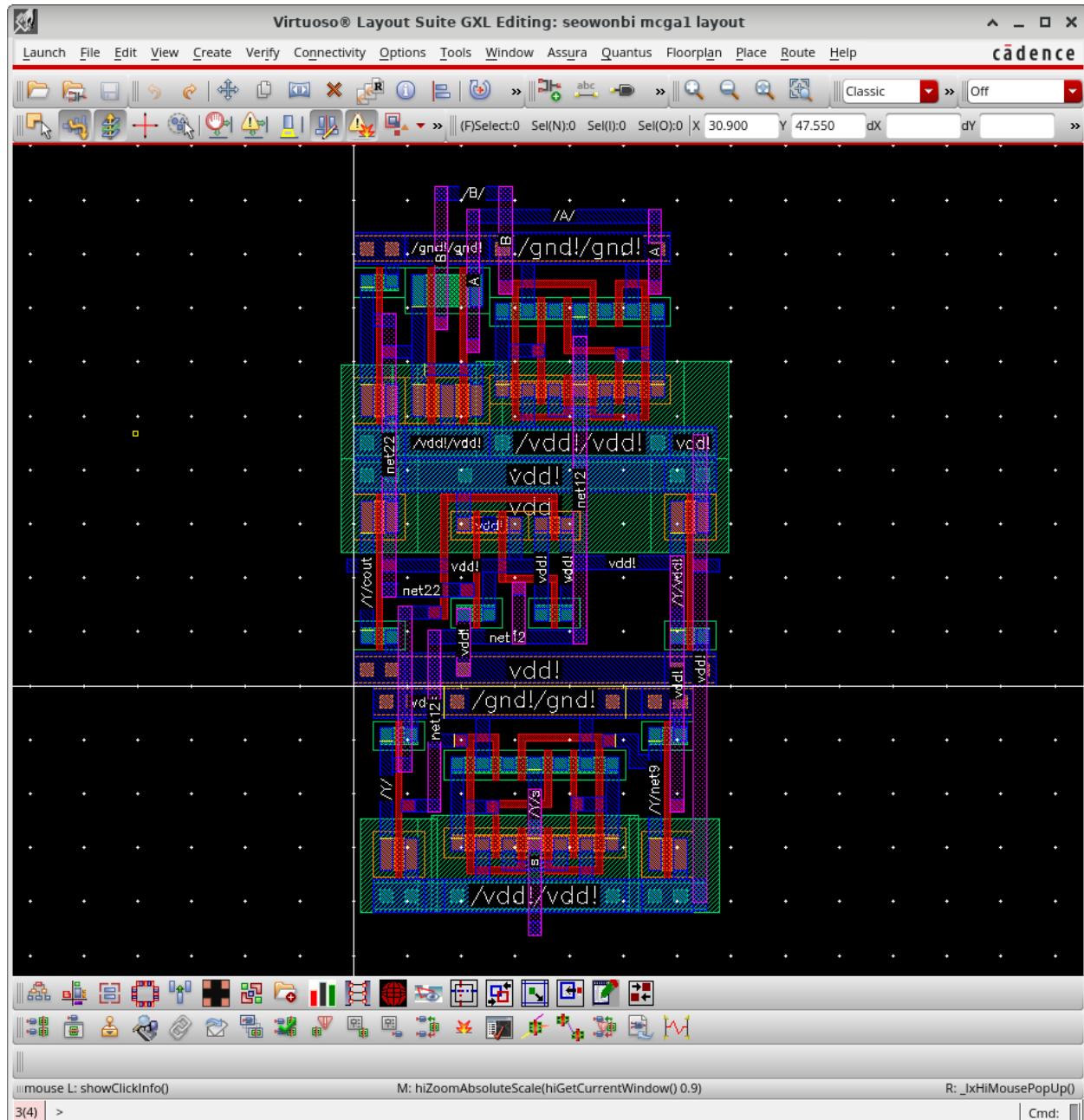
Problem 3 – 4-bit Adder Layout - [MCGA4_Layout]

Figure 5. MCGA1_Layout

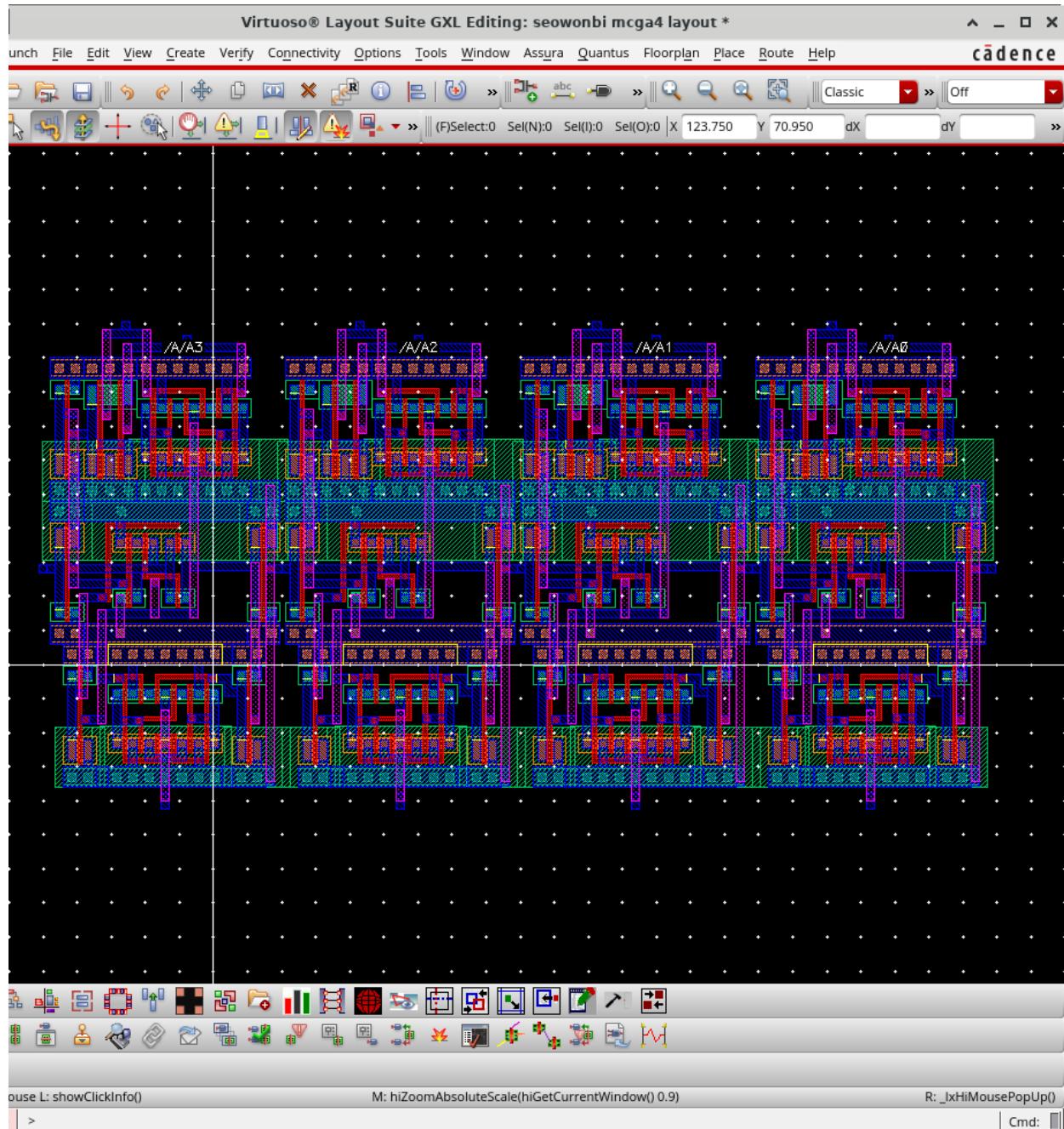


Figure 6. MCGA4_Layout

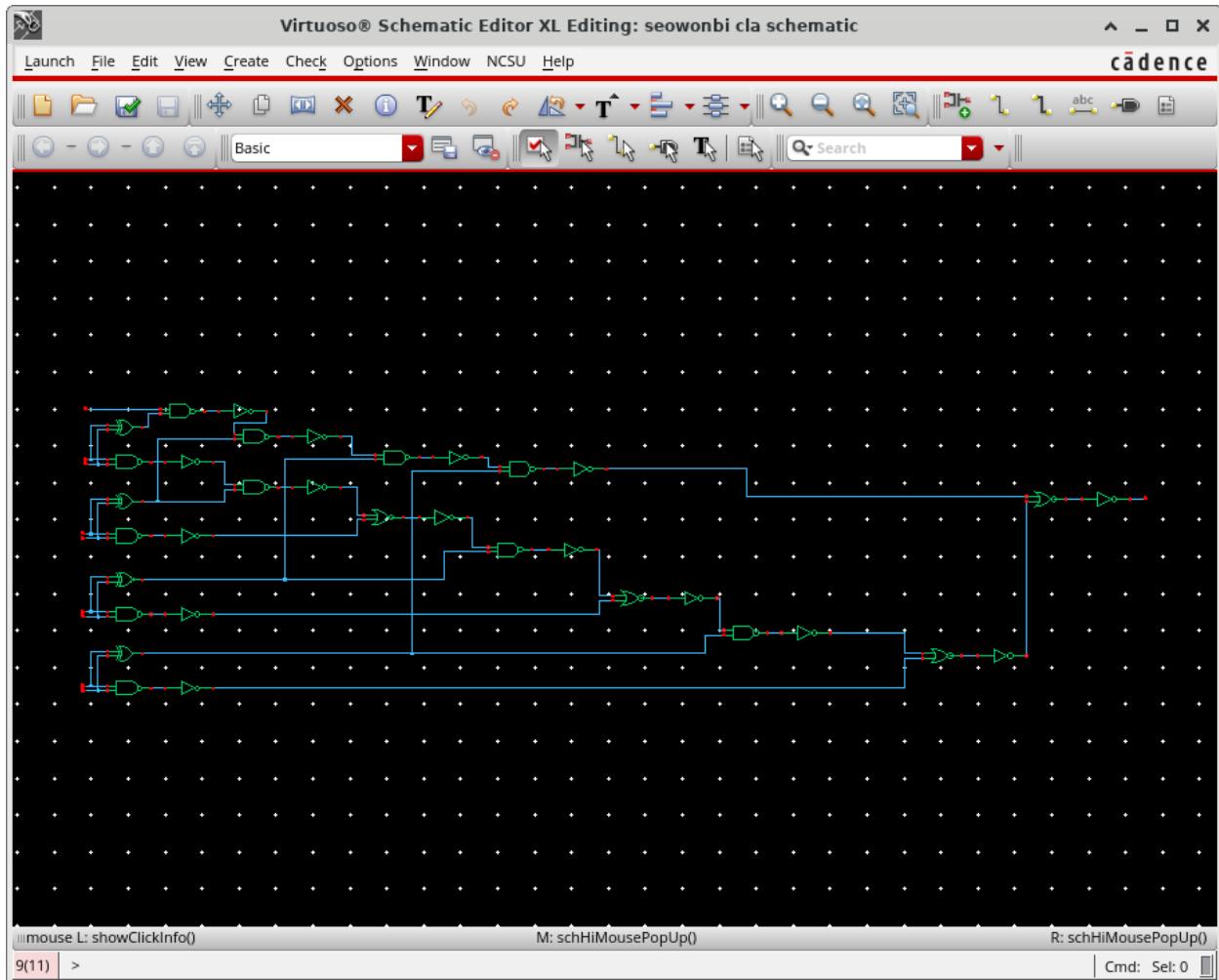
Problem 4 – Carry Lookahead Schematic – [CLA_Schematic]

Figure 7. Carry Lookahead Schematic

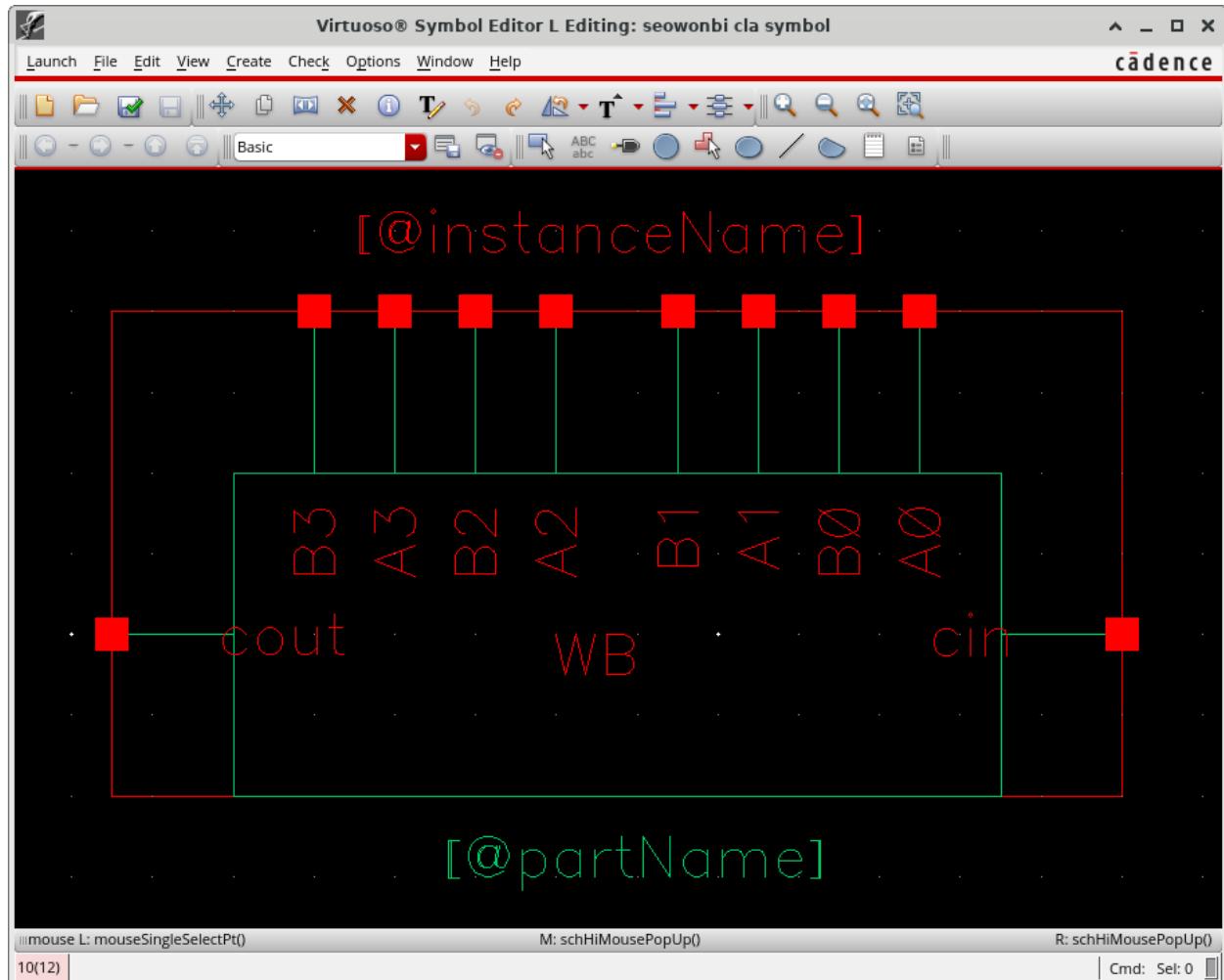
Problem 5 – Carry Lookahead Symbol [CLA_Symbol]

Figure 8. Carry Lookahead Symbol

Problem 6 – Carry Lookahead Layout - [CLA_Layout]

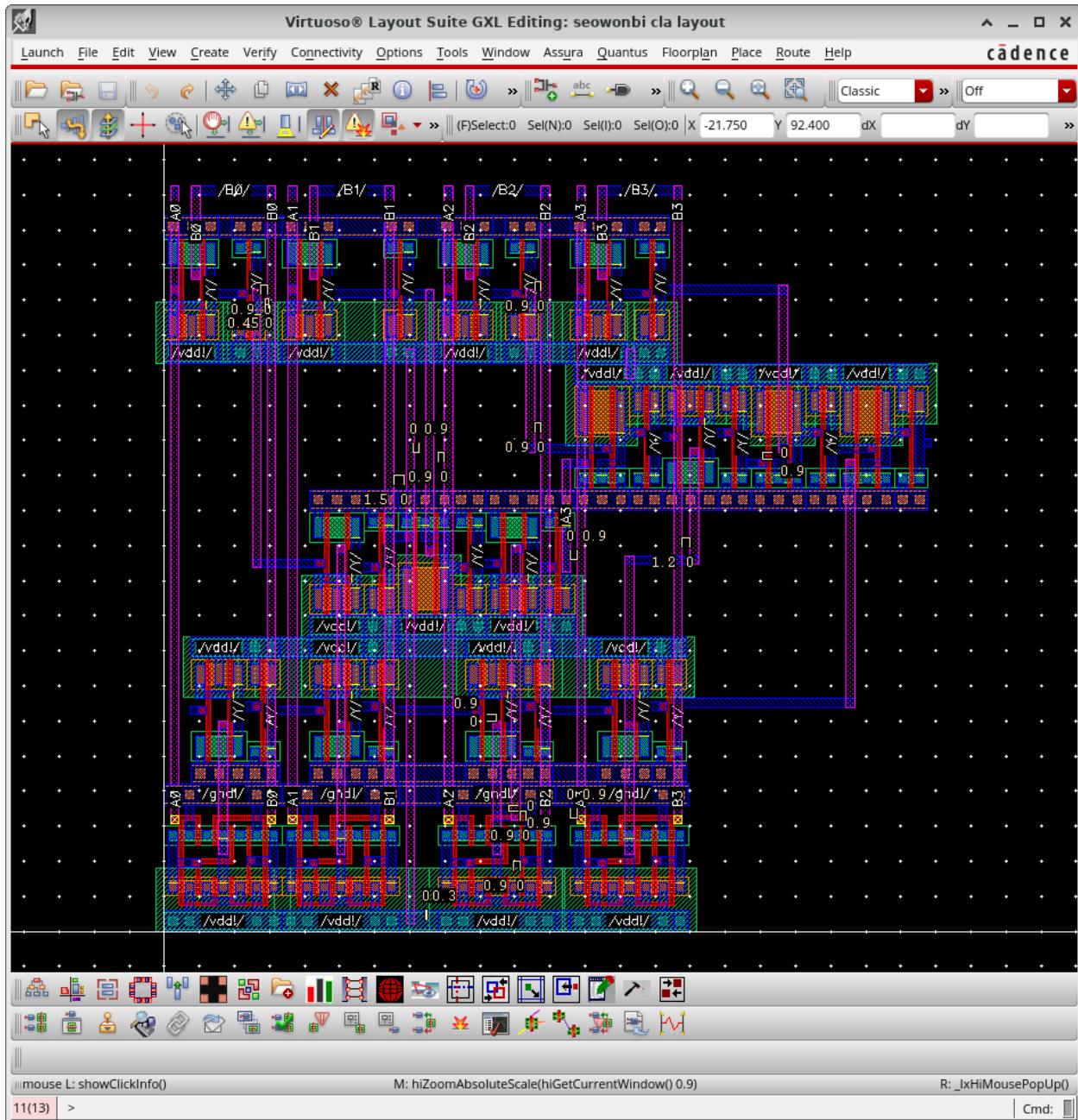


Figure 9. Carry Lookahead Layout

Problem 7 – 8-bit Adder Schematic – [MCGACLA8_Schematic]

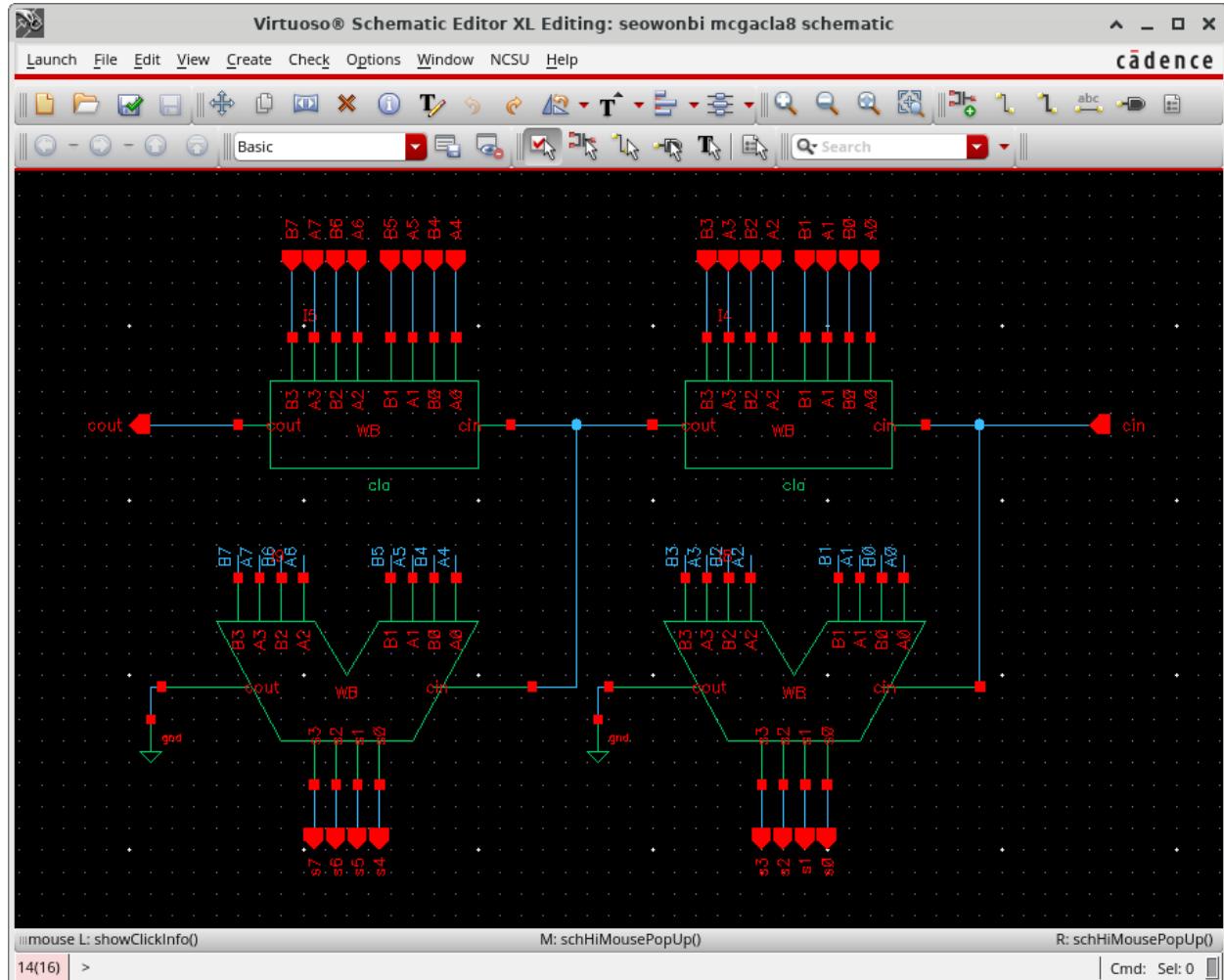


Figure 10. 8-bit Manchester Carry Generation Carry Lookahead Adder Schematic

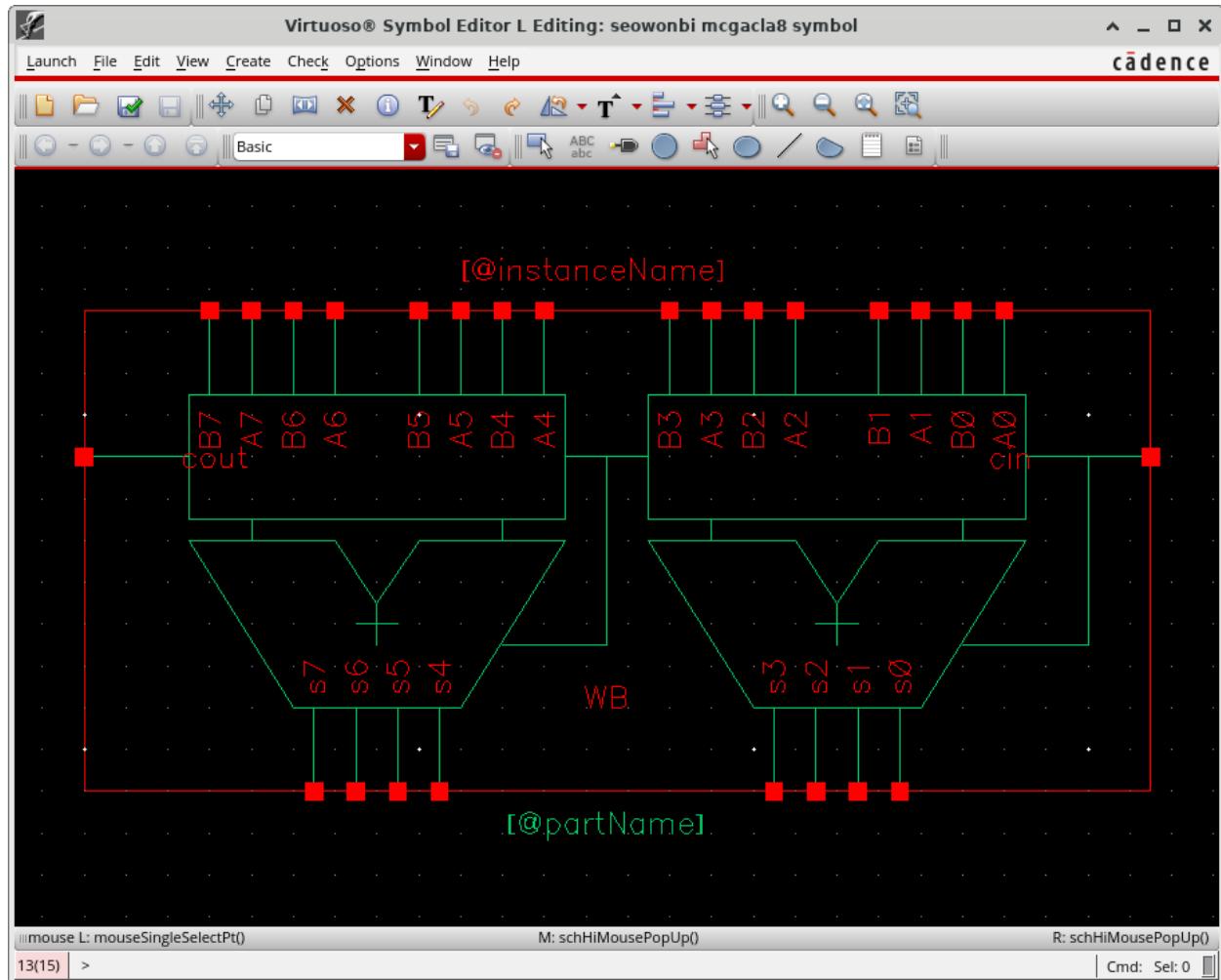
Problem 8 – 8-bit Adder Symbol – [MCGACLA8_Symbol]

Figure 11. 8-bit Adder Symbol

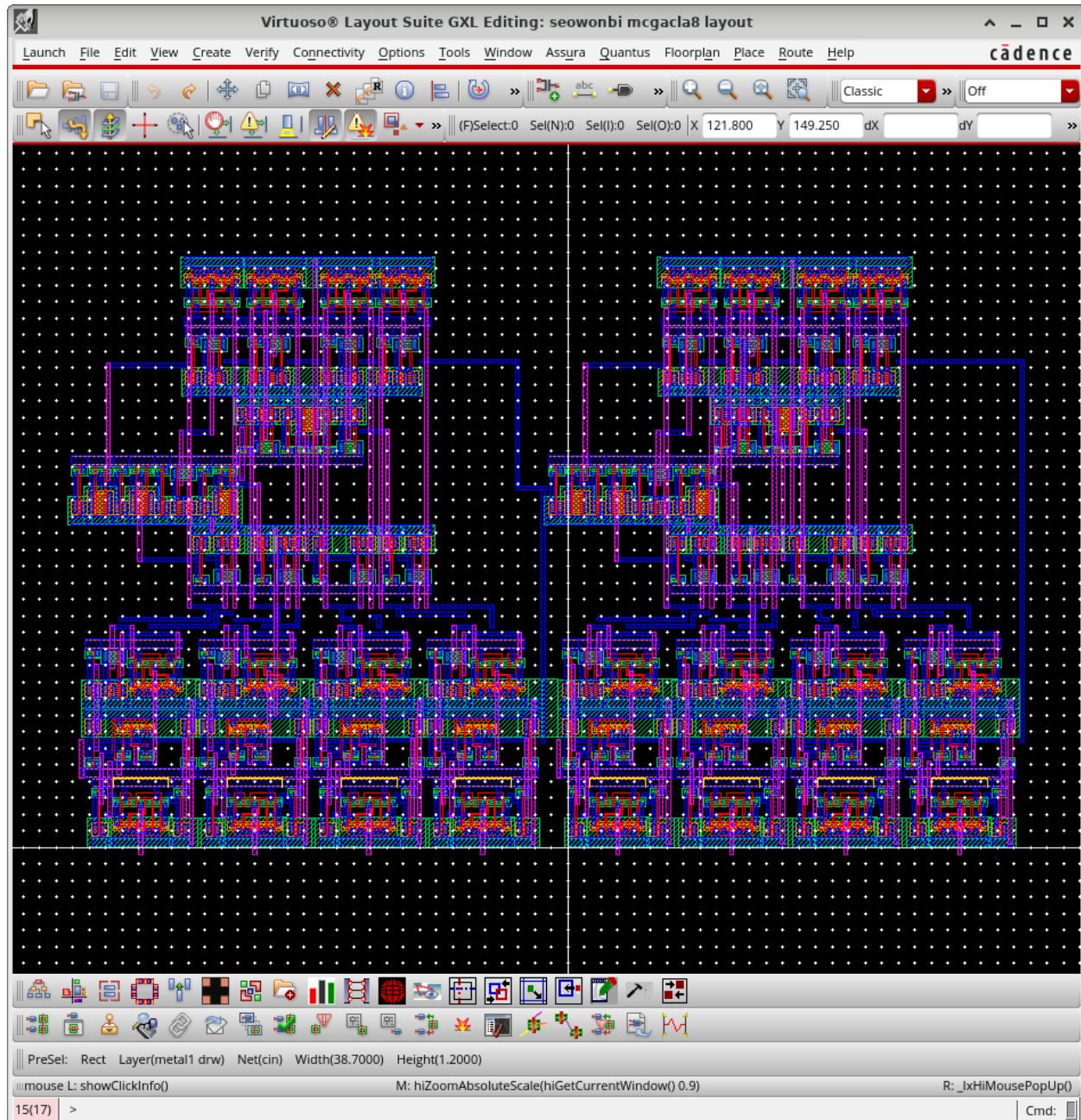
Problem 9 – 8-bit Adder Layout - [MCGACLA8_Layout]

Figure 12. 8-bit Adder Layout

Problem 10 – 8-bit Adder LVS

The screenshot shows the Cadence Virtuoso LVS interface. The terminal window displays the output of the LVS command, which compares the layout and schematic netlists. Key statistics include:

- Net-list summary for /egr/courses/unix/ECE/813/sewonobi/virtuoso/LVS/layout/netlist:**
 - Count: 323 nets, 26 terminals, 314 pins, 308 nodes.
 - Terminal correspondence points: N014, N2 A0; N033, N3 A1; N032, N4 A2; N303, N5 A3; N300, N6 A4; N292, N7 A5; N298, N8 A6; N297, N9 A7; N232, N10 A8; N211, N16 B1; N320, N15 B2; N311, N14 B3; N318, N13 B4; N317, N12 B5; N313, N11 B6; N315, N10 B7; N314, N19 cin; N313, N18 cout; N312, N20 s0; N311, N21 s1; N313, N22 s2; N309, N23 s3; N303, N24 s4; N307, N25 s5; N306, N26 s6; N305, N27 s7.
- Devices in the netlist but not in the rules:** None listed.
- Devices in the rules but not in the netlist:** None listed.
- The net-lists match.**
- layout schematic instances:** un-matched 0, required 0, size errors 0, primitive 0, active 620 620, total 620 620.
- un-matched nets:** merged 0 0.

Figure 13. 8-bit Adder LVS

Problem 11 – 8-bit Adder Simulation

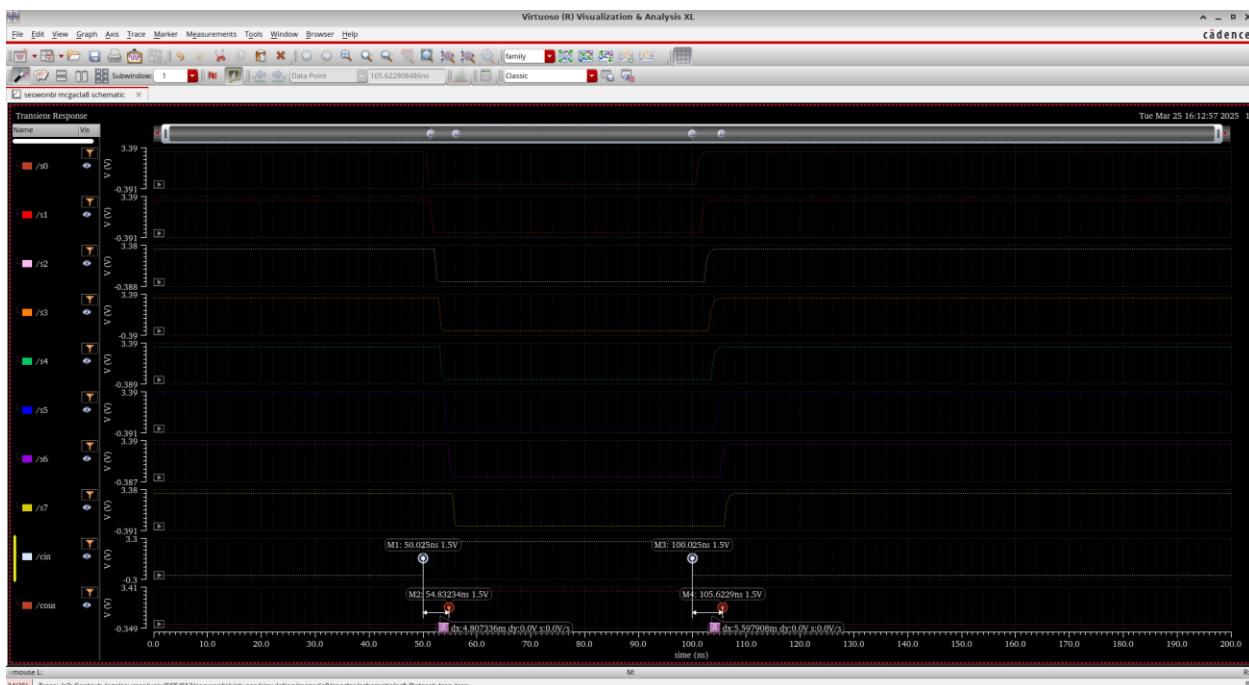


Figure 14. 8-bit Adder Simulation

Rise time delay: 4.807336ns, Falling time delay: 5.597908ns

A	B	Cin	s0	s1	s2	s3	s4	s5	s6	s7	cout
1	0	0	1	1	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0	0	0	0	1
1	0	0	1	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1	0

Figure 15. Truth Table of the 8-bit Adder