

WonBin Seo

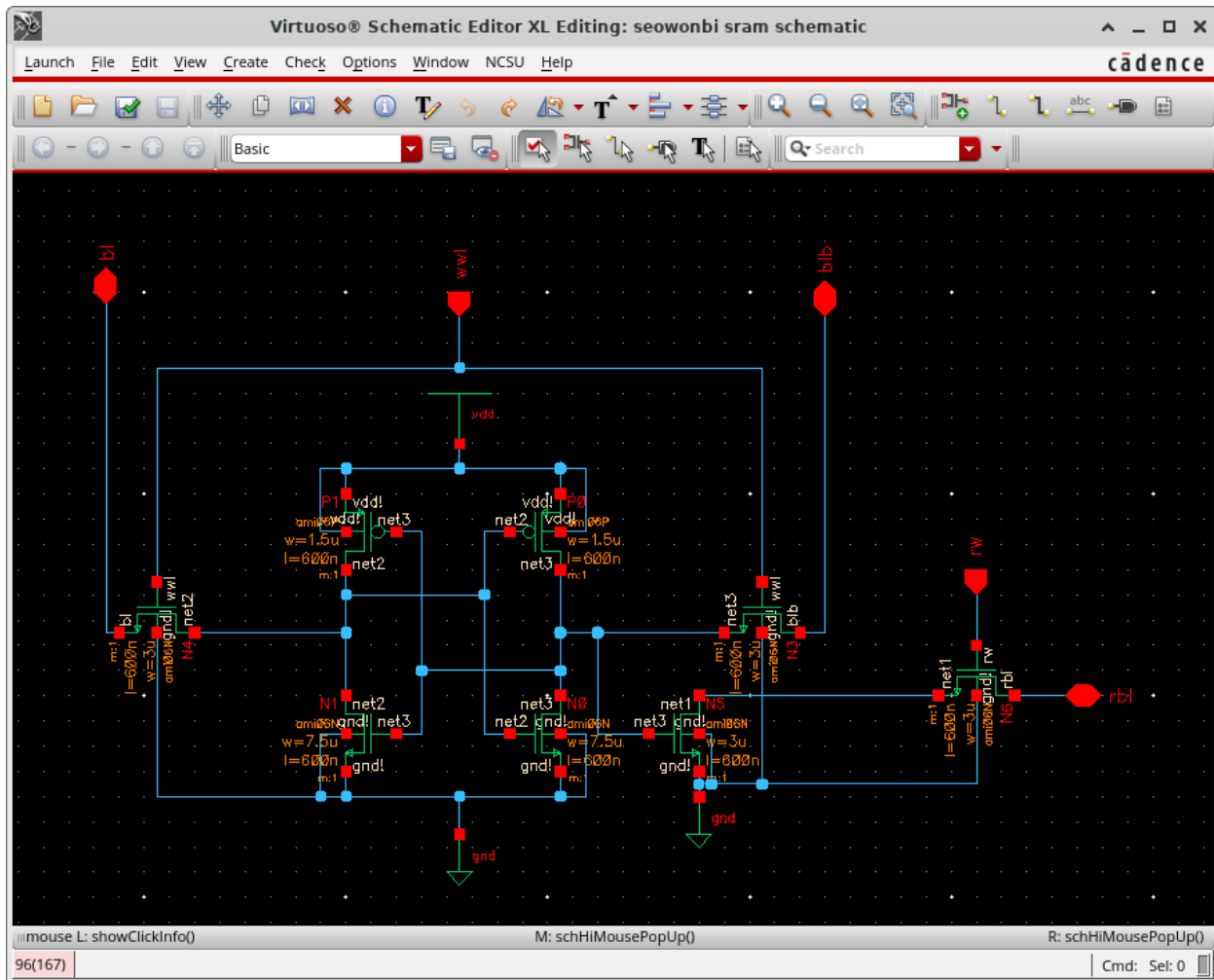
Dr. Shannon Nicley,

ECE 813 Advanced VLSI Design

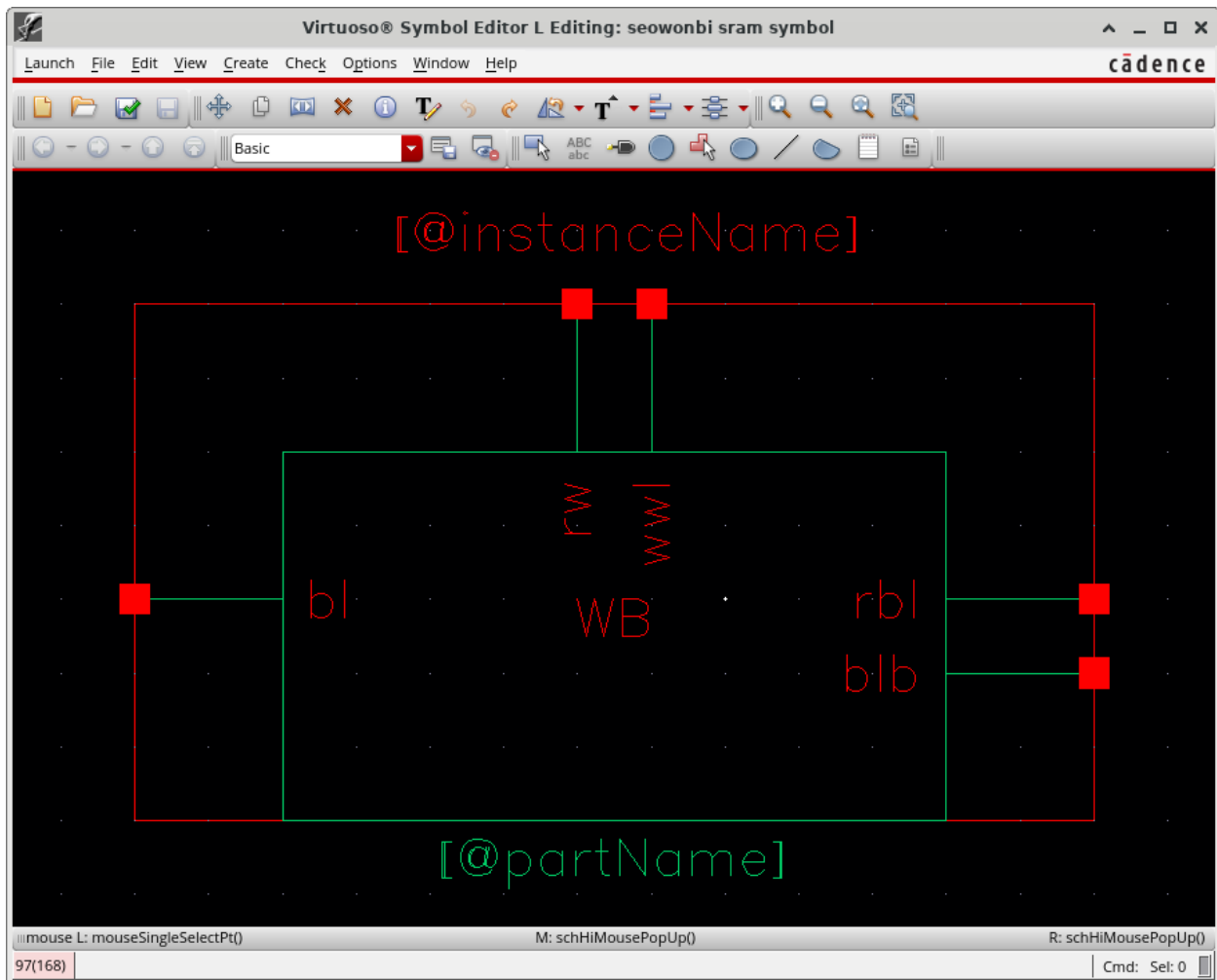
16 April 2025

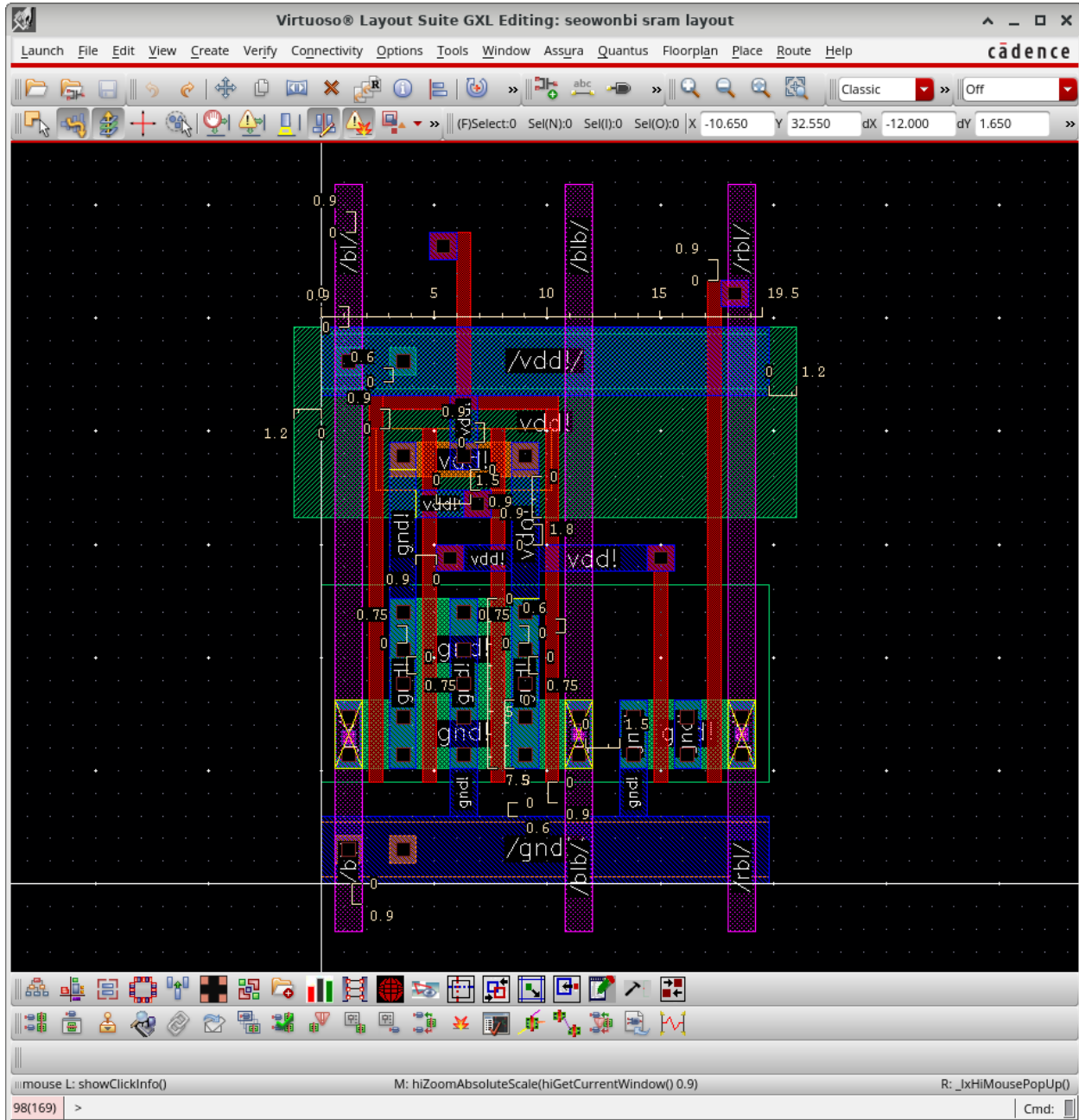
Exam3

Problem 1 – 1-bit SRAM Schematic

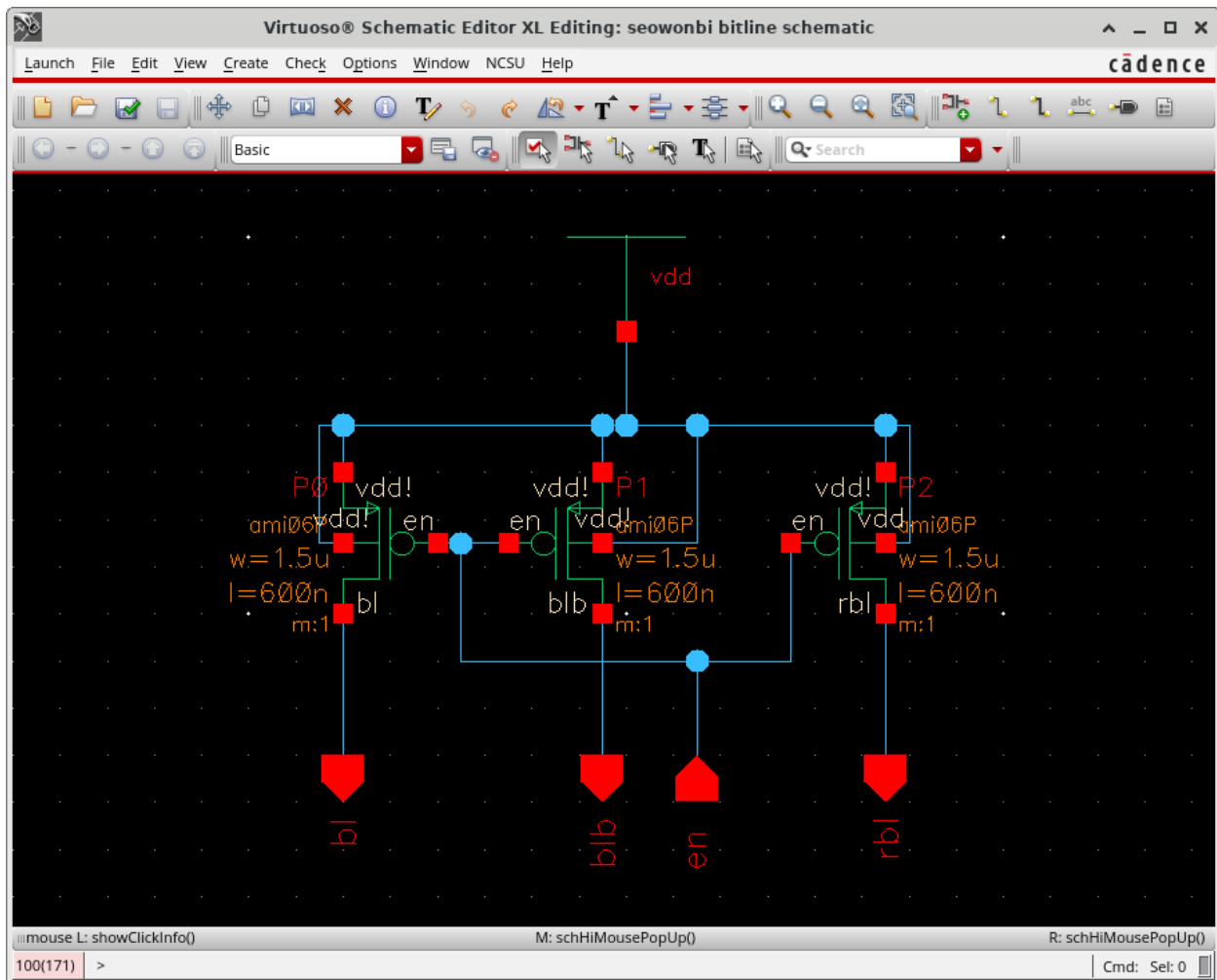


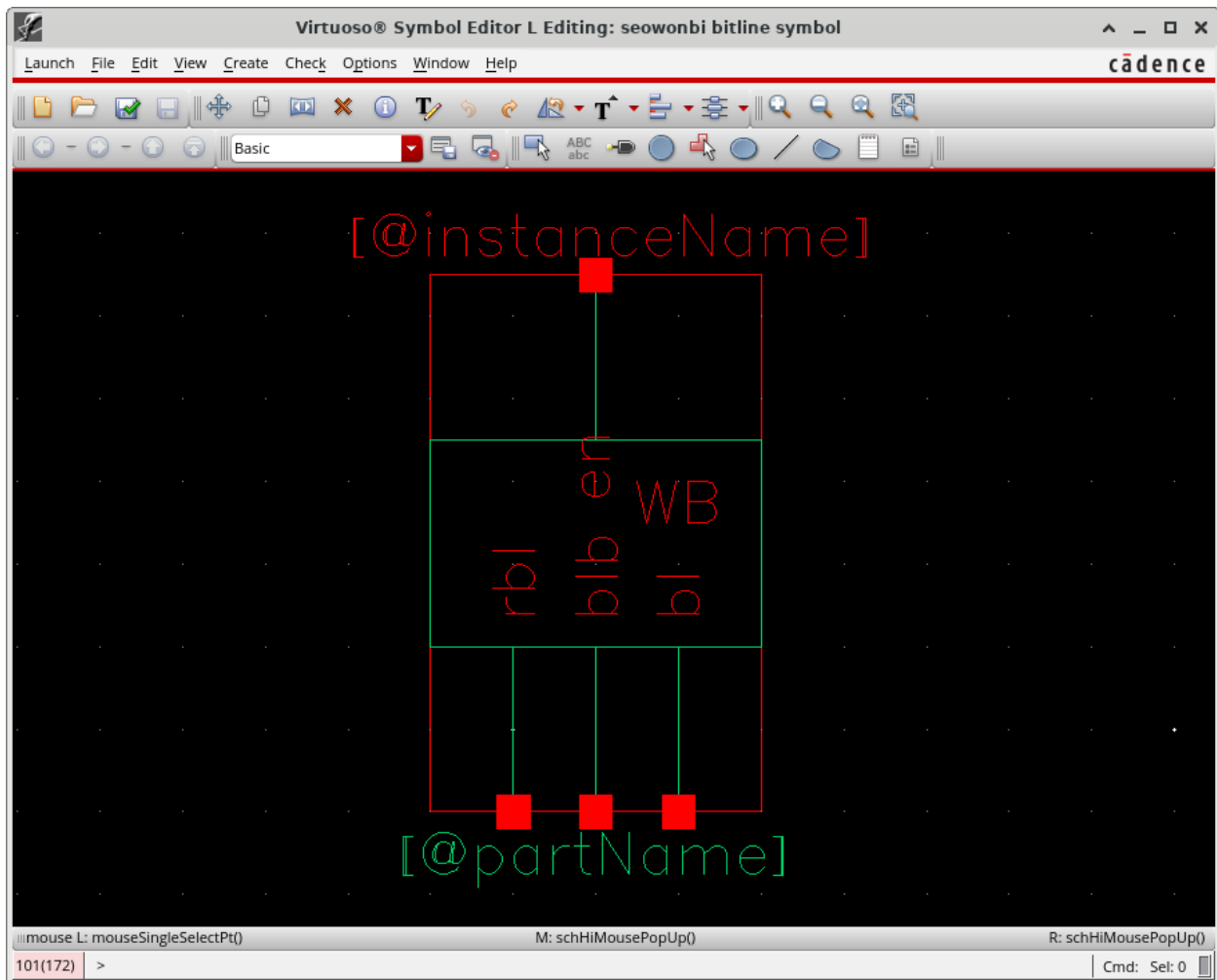
Problem 1 – 1-bit SRAM Symbol

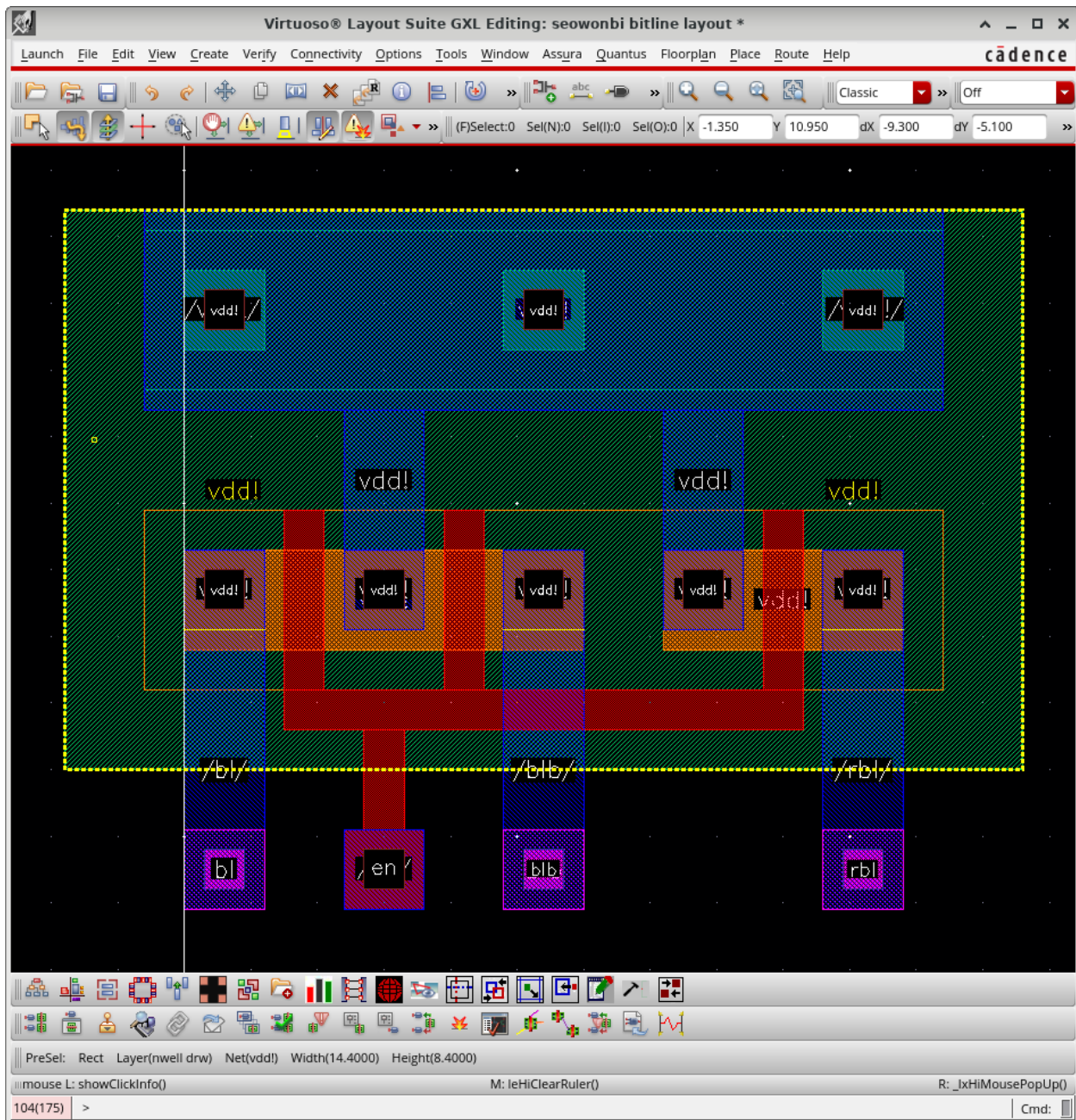


Problem 1 – 1-bit SRAM Layout

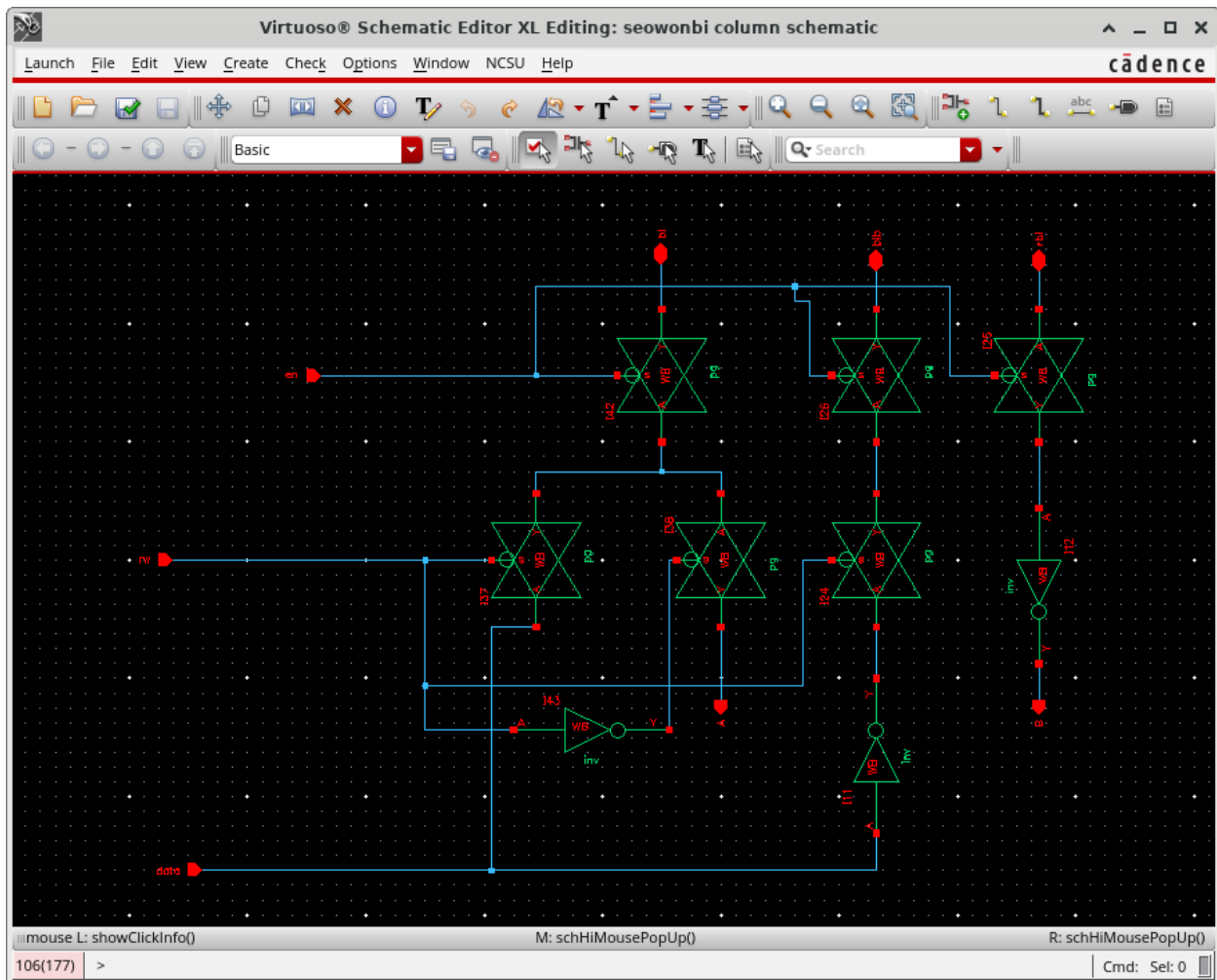
Problem 2 – Bitline Conditioning Schematic

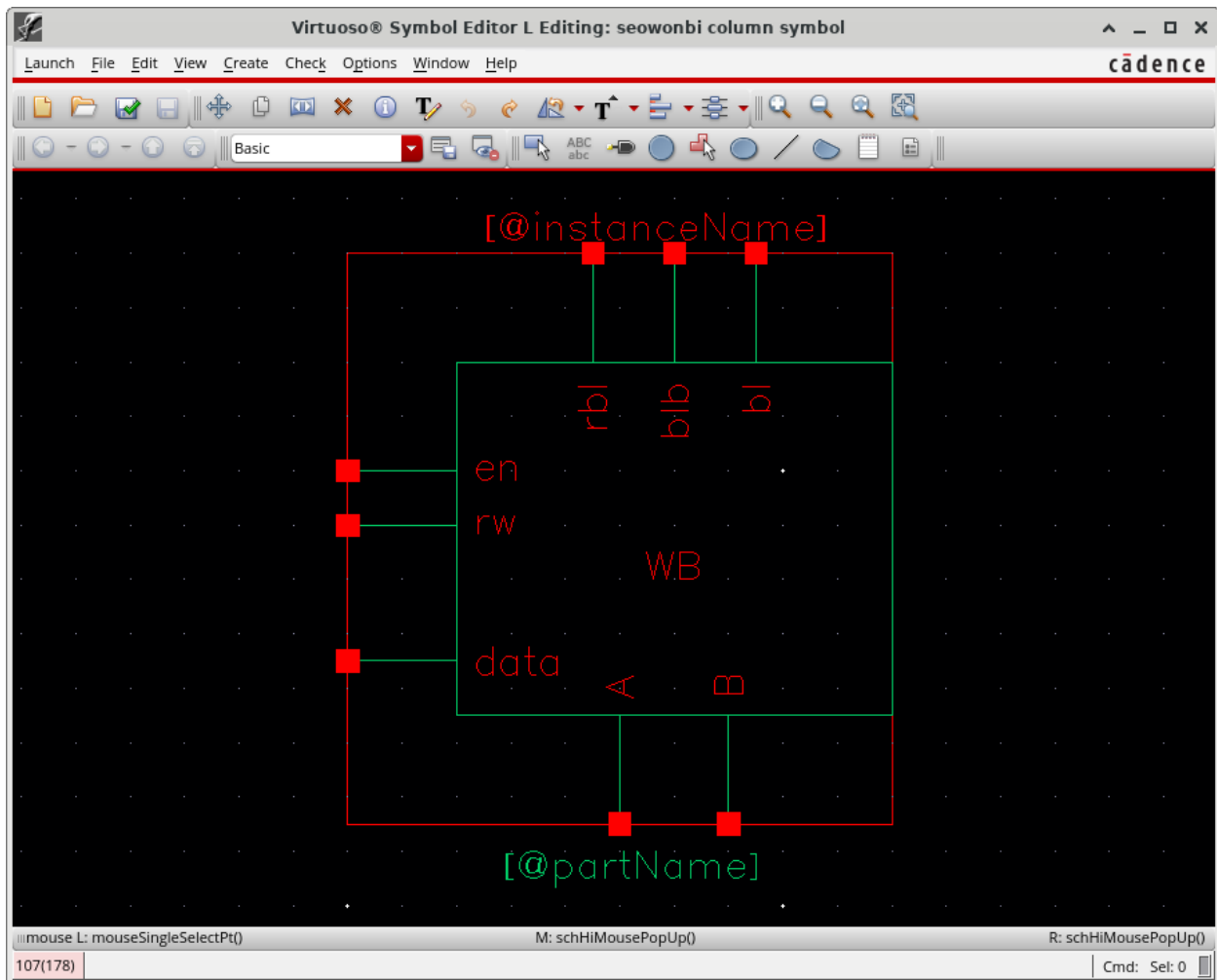


Problem 2 – Bitline Conditioning Symbol

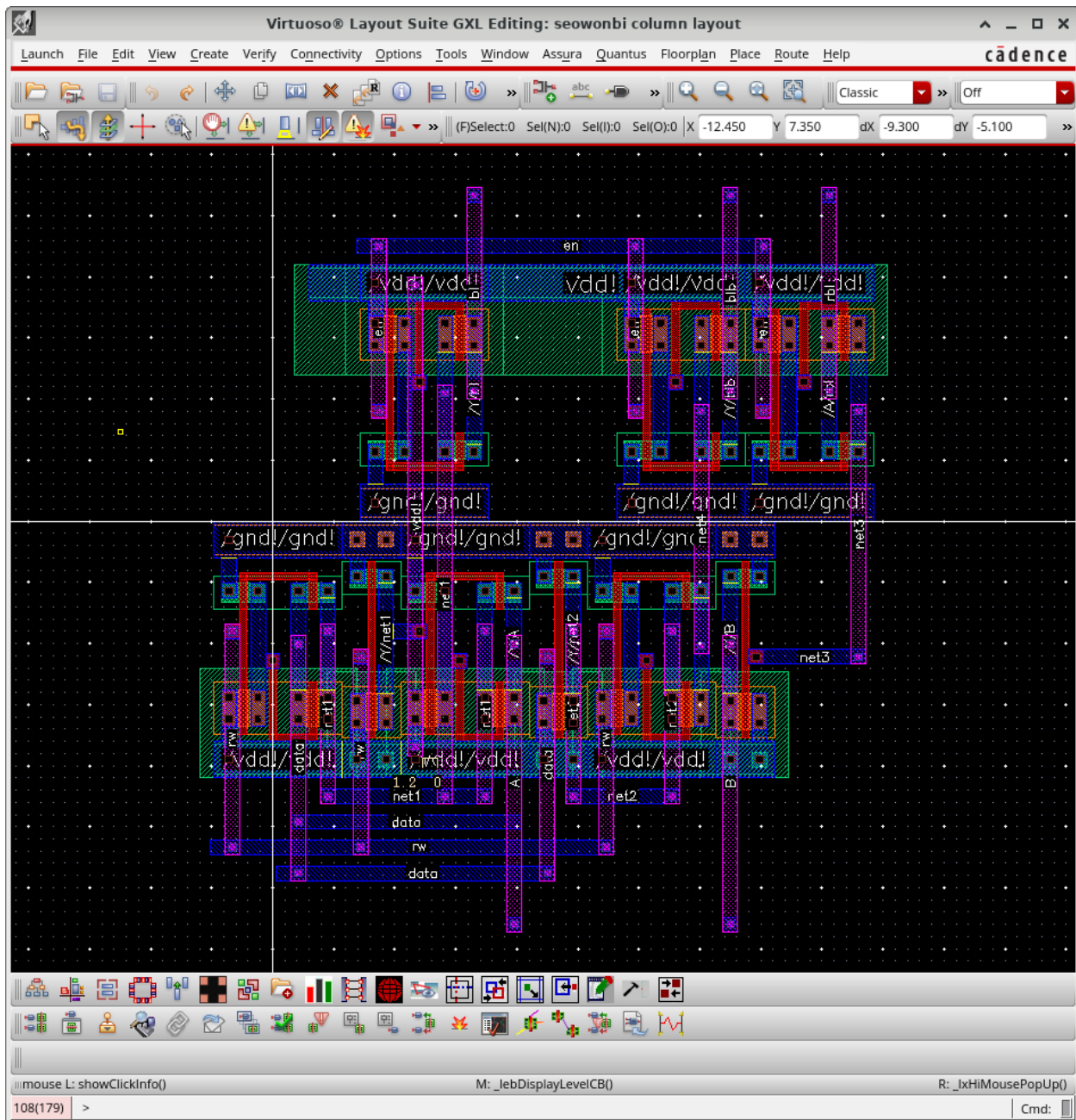
Problem 2 – Bitline Conditioning Layout

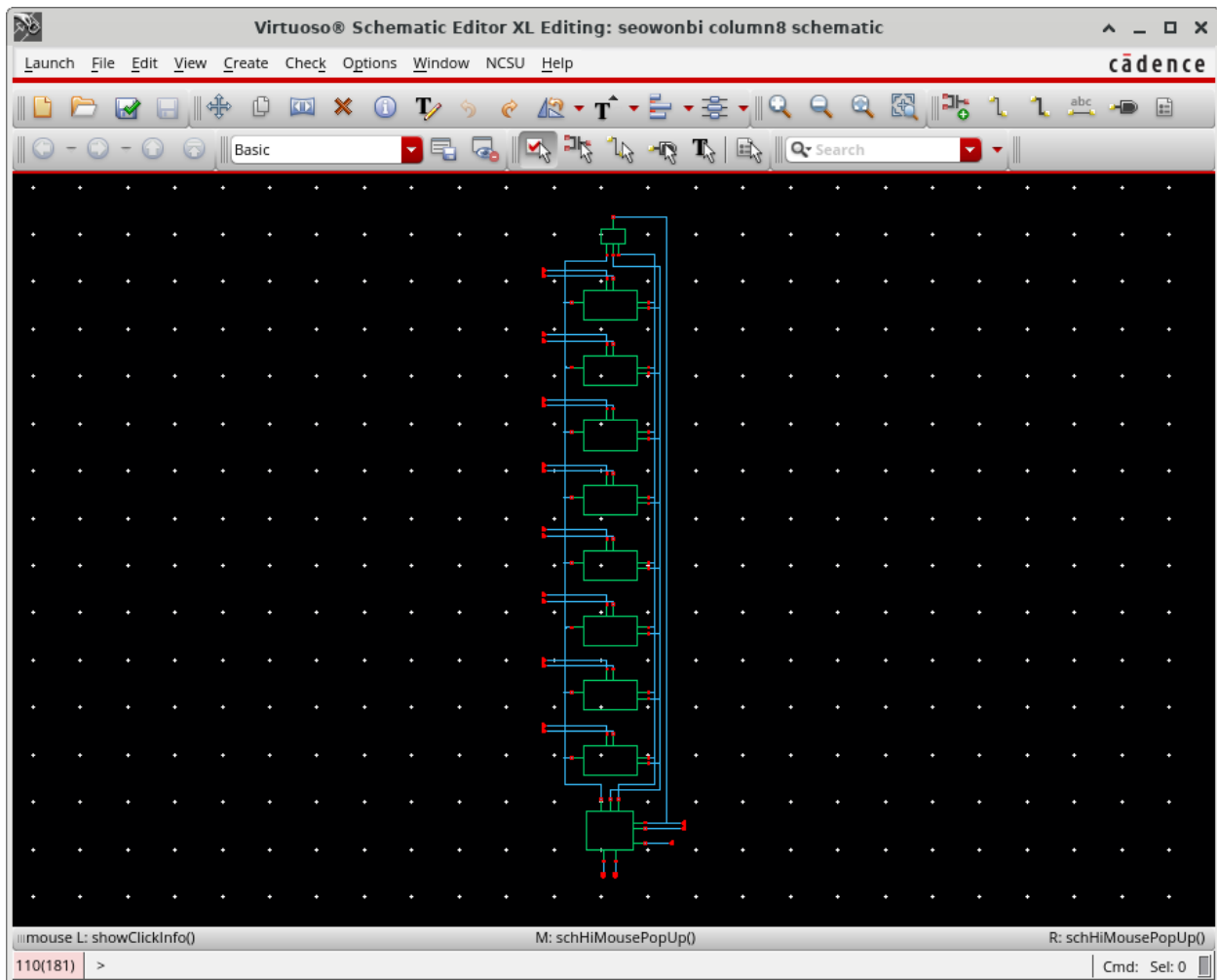
Column Circuitry Schematic

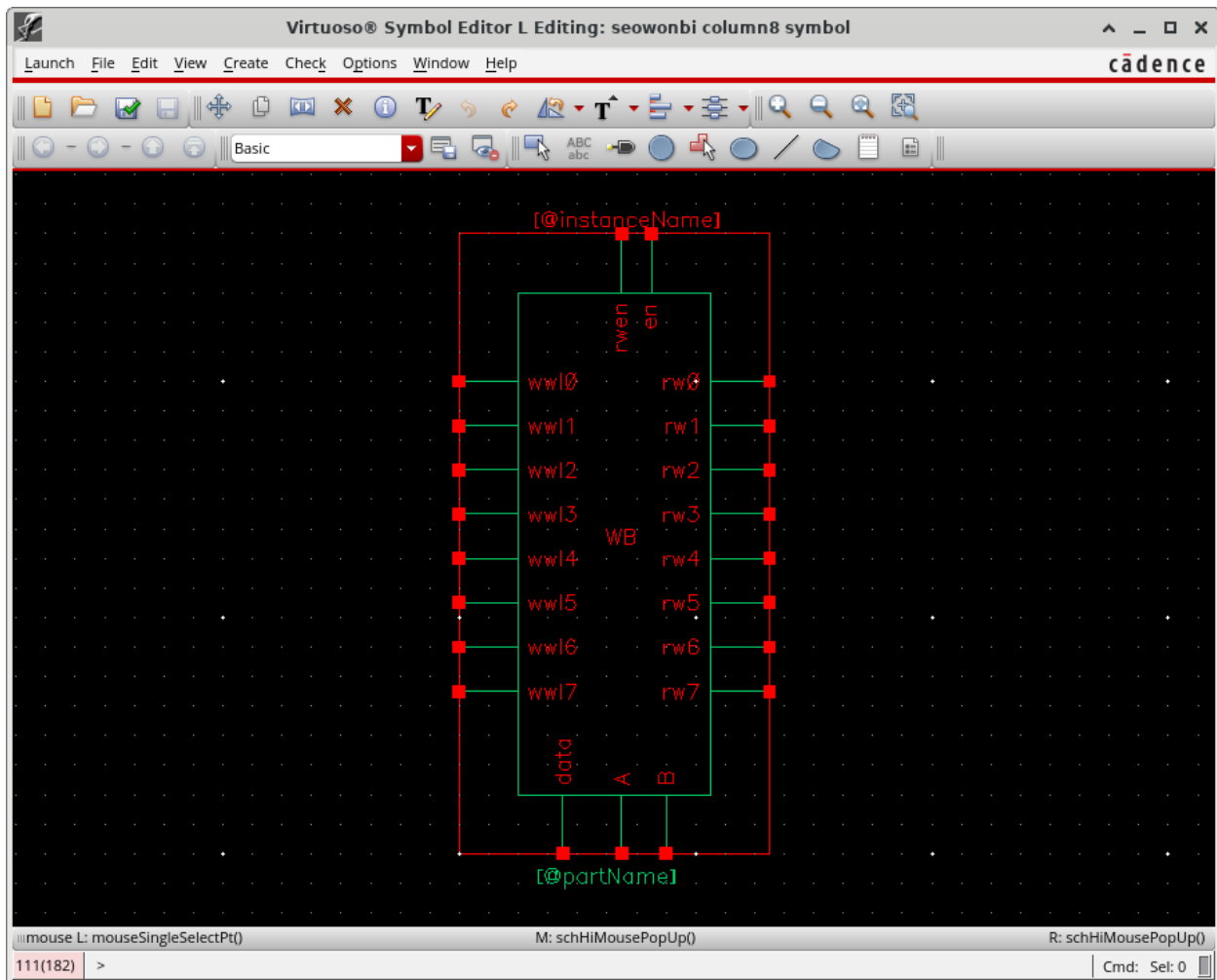


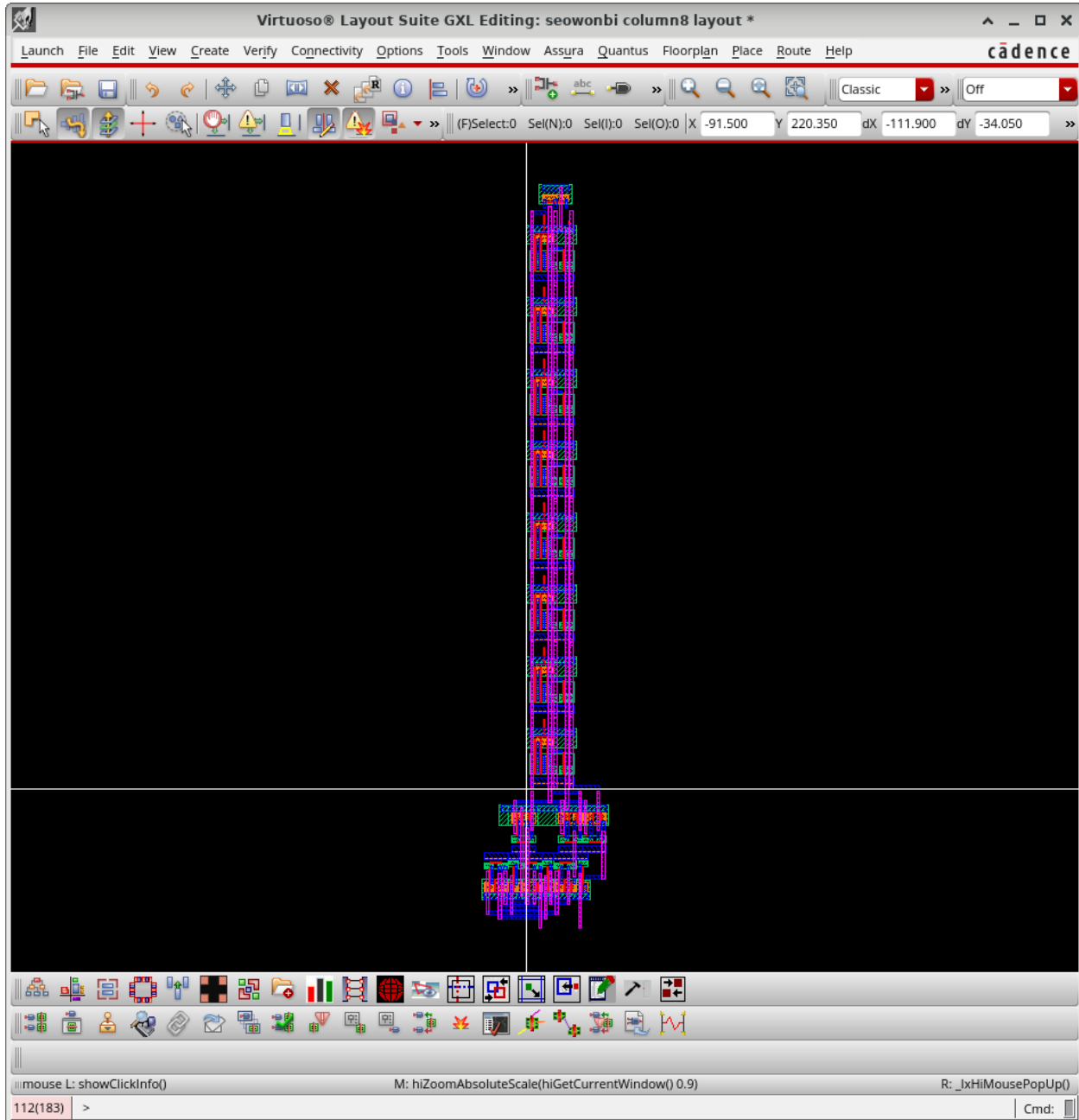
Problem 3 – Column Circuitry Symbol

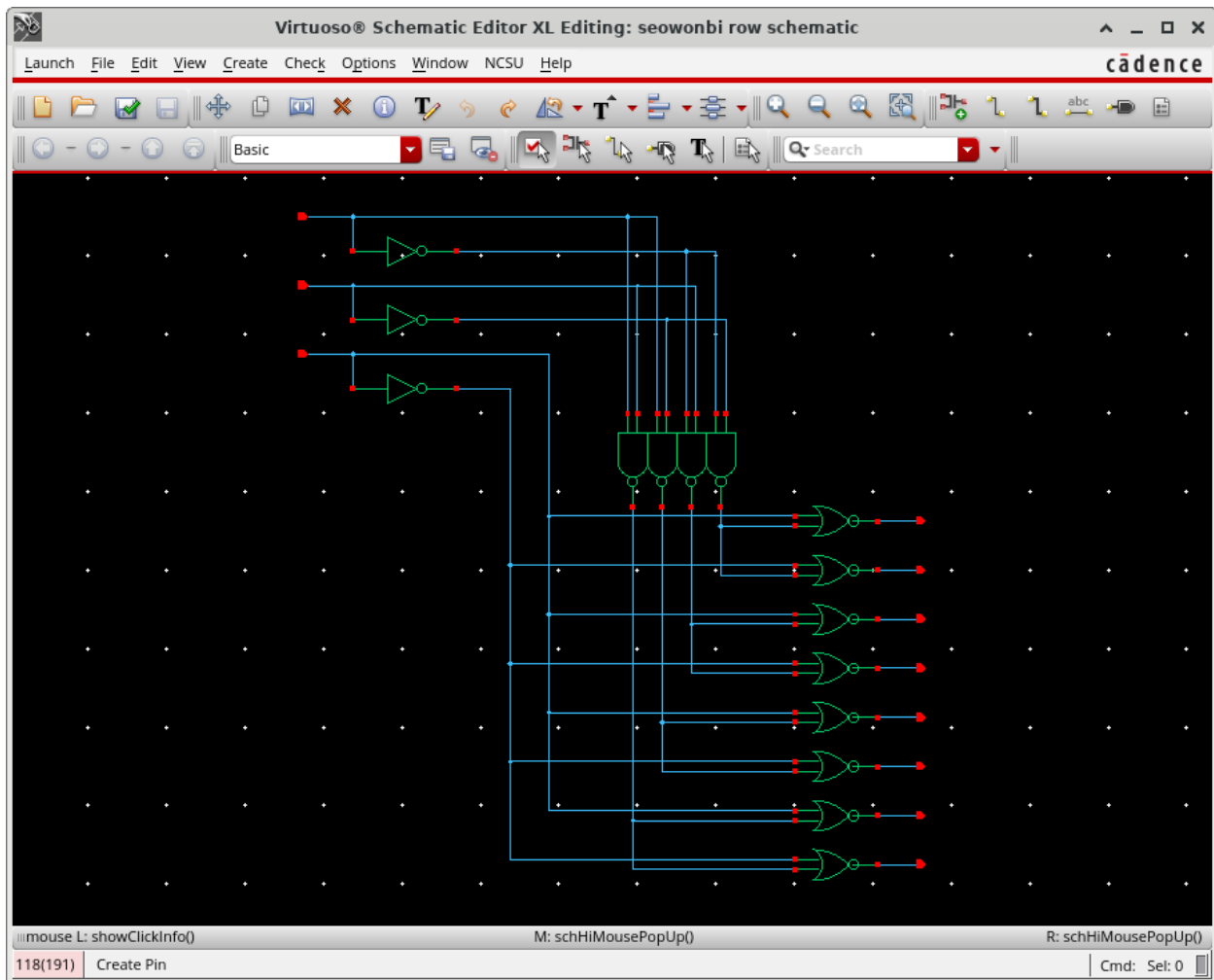
Problem 3 – Column Circuitry Layout

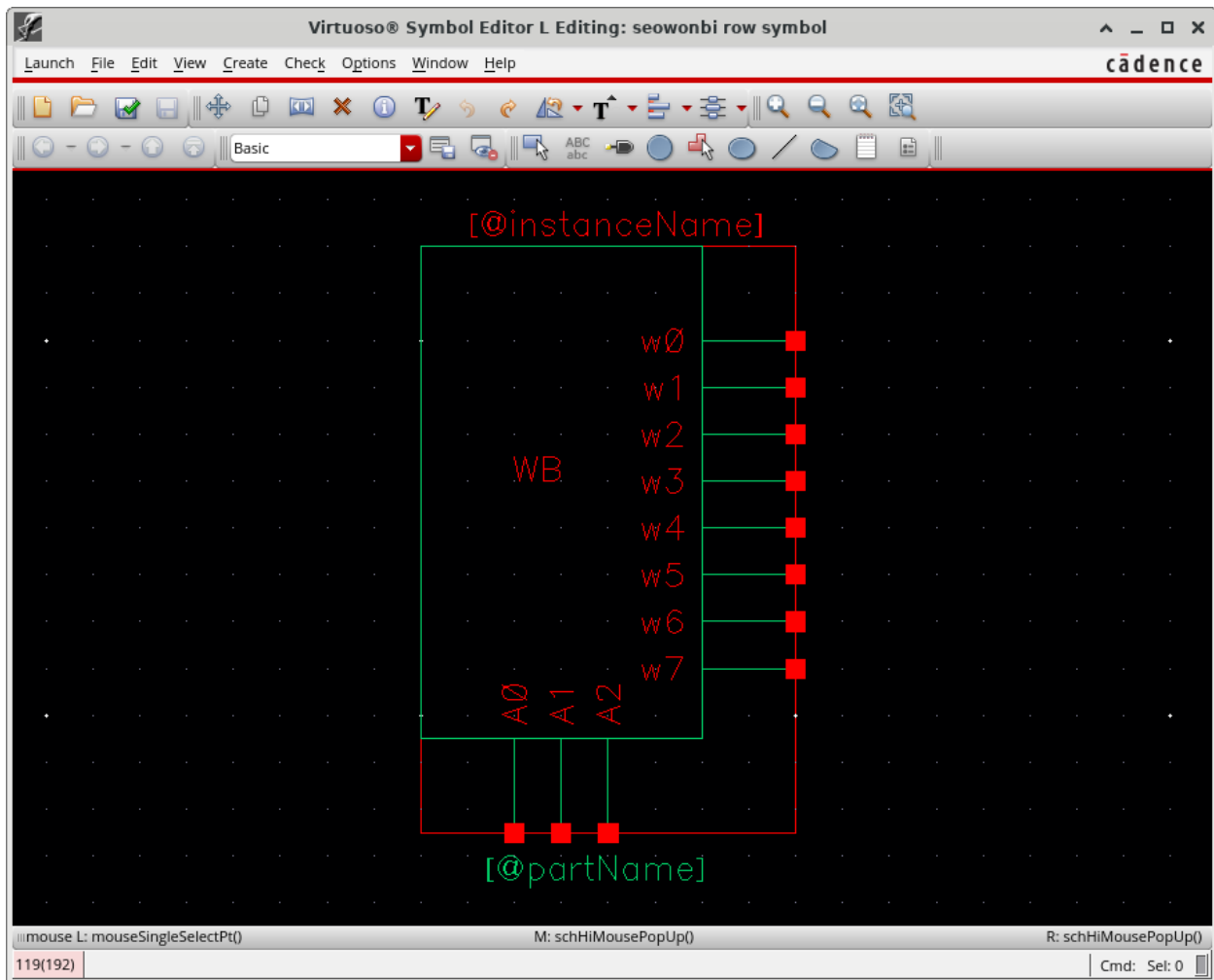


Problem 4 – 8-bit SRAM Column Schematic

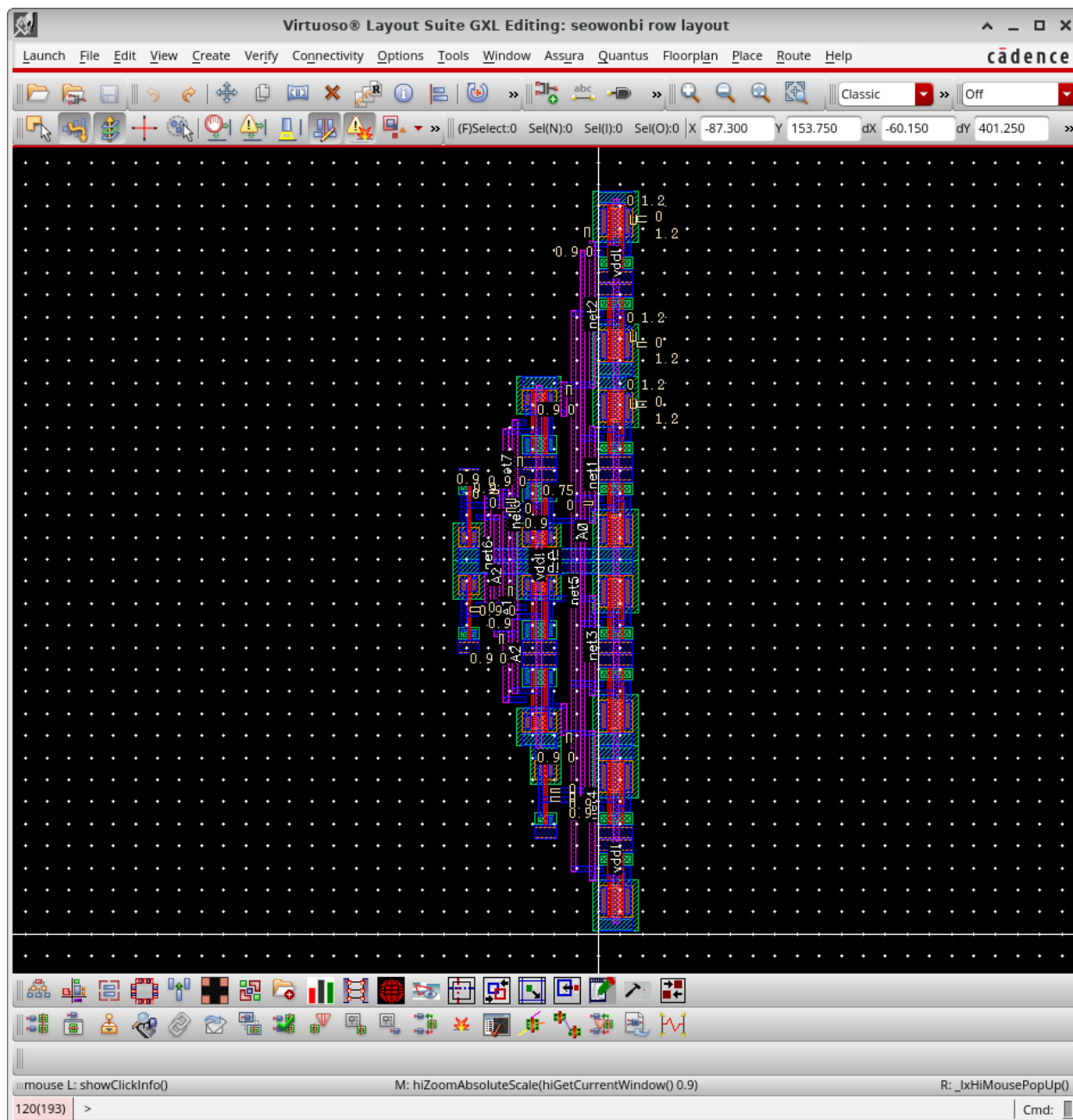
Problem 4 – 8-bit SRAM Column Symbol

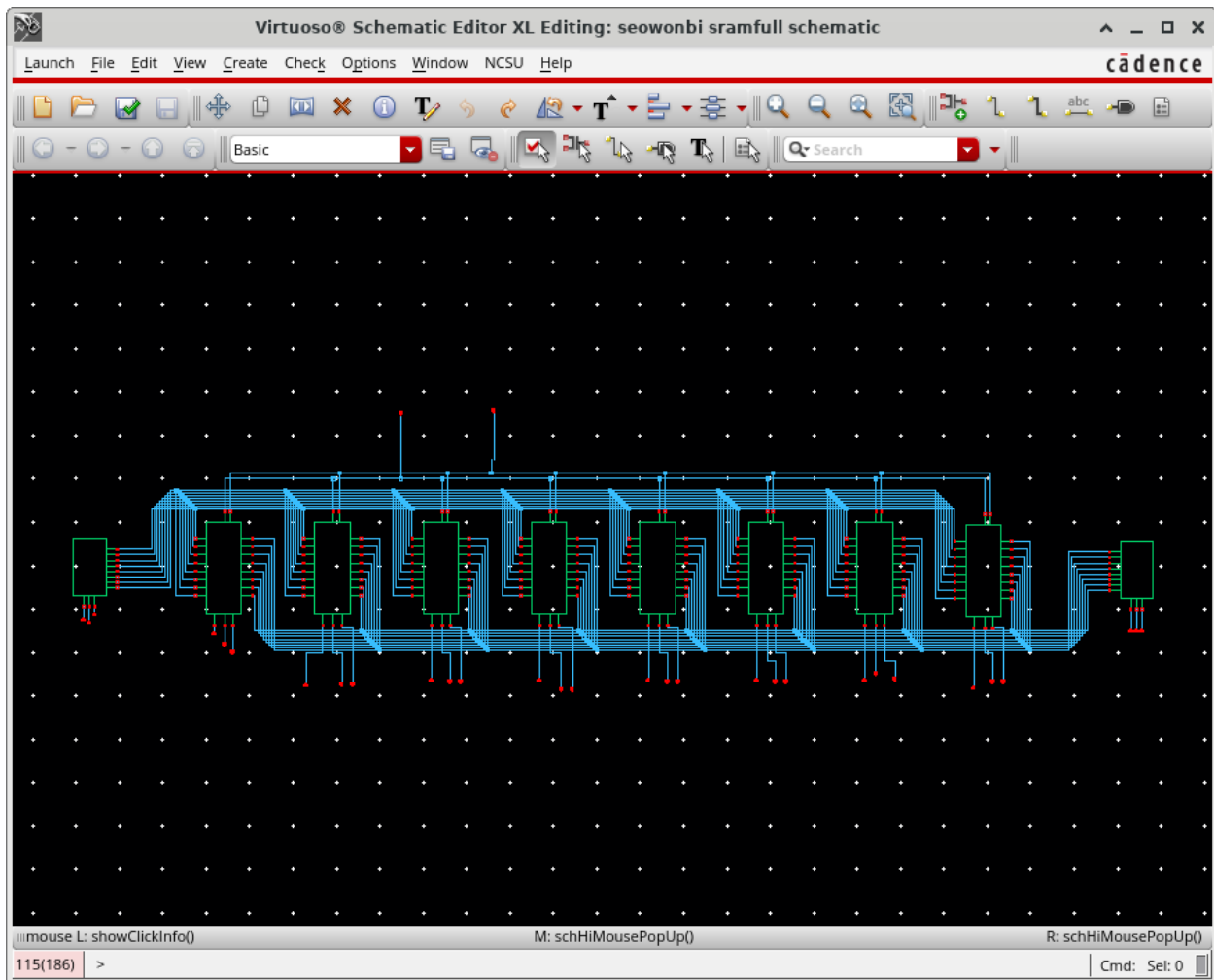
Problem 4 – 8-bit SRAM Column Layout

Problem 5 – Address Decoder Schematic

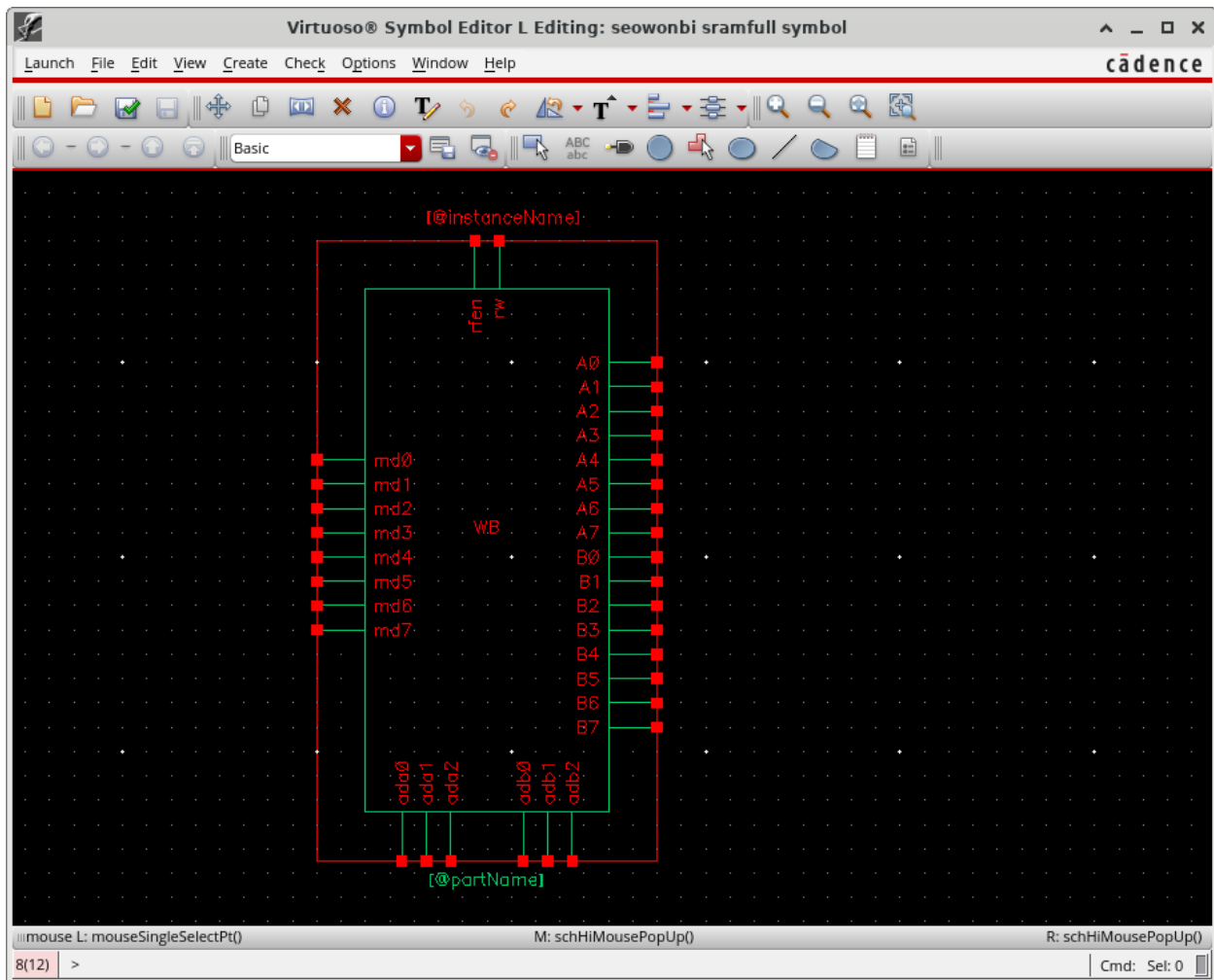
Problem 5 – Address Decoder Symbol

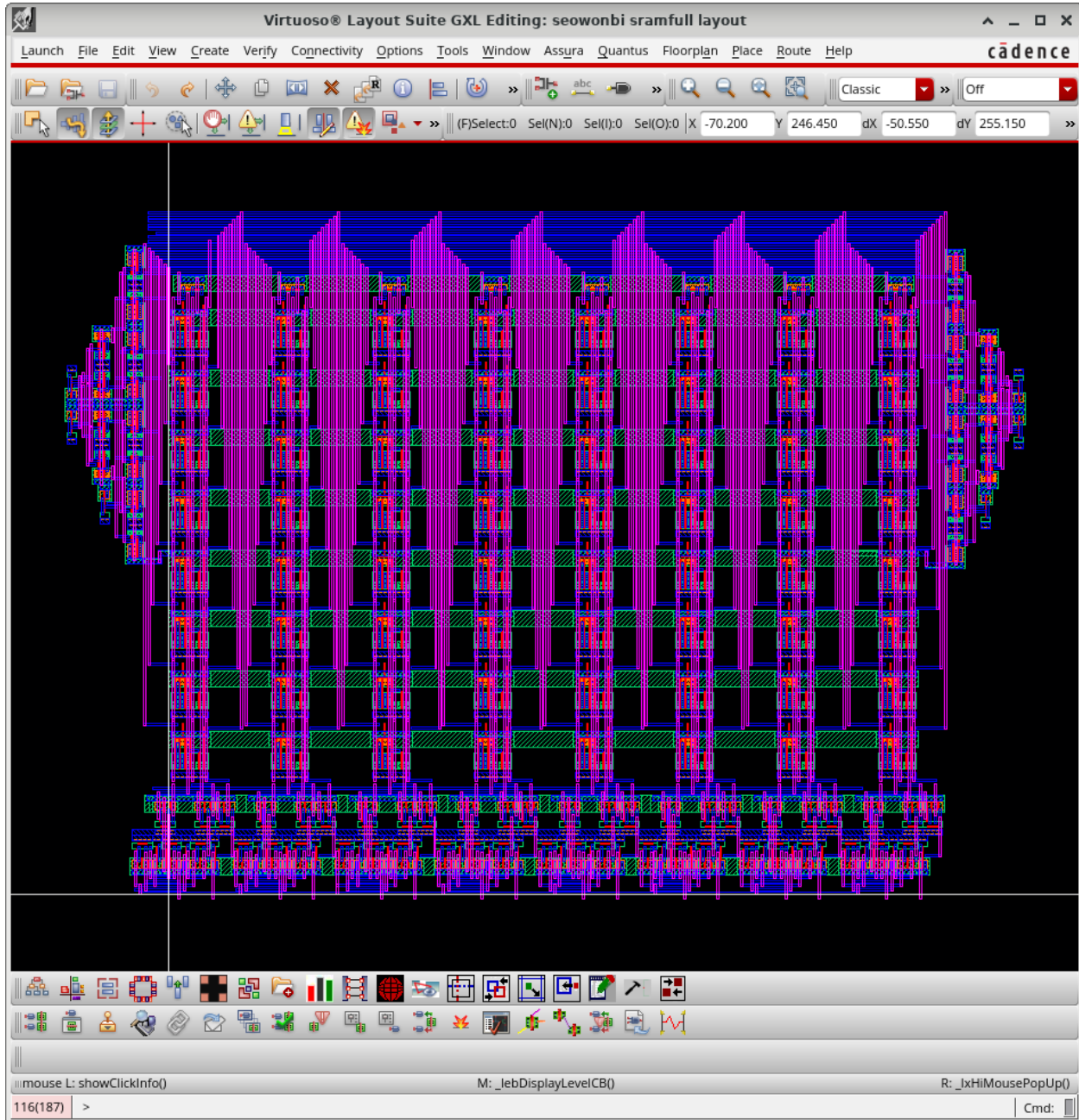
Problem 5 – Address Decoder Layout



Problem 6 – 8x8 SRAM Schematic

Problem 6 – 8x8 SRAM Symbol



Problem 6 – 8x8 SRAM Layout

Problem 6 – 8x8 SRAM LVS

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C /egr/courses/unix/ECE/813/seowonbi/virtuoso/LVS/sl.out
File Edit View Help
cadence

W@18G05: LVS version 6.1.8-64b 10/11/2023 09:34 (cpgbl007) $
Command line: /egr/soft/soft/Cadence/IC618/tools.lnx64/cell/bin/64bit/LVS -l -s -t /egr/courses/unix/ECE/813/seowonbi/virtuoso/LVS/layout /egr/courses/unix/ECE/813/seowonbi/virtuoso/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

Net-list summary for /egr/courses/unix/ECE/813/seowonbi/virtuoso/LVS/layout/netlist
count
392 nets
22 terminals
326 pmos
558 nmos

Net-list summary for /egr/courses/unix/ECE/813/seowonbi/virtuoso/LVS/schematic/netlist
count
392 nets
24 terminals
326 pmos
558 nmos

Terminal correspondence points
N373 N16 A0
N372 N18 A1
N371 N20 A2
N370 N22 A3
N369 N24 A4
N368 N26 A5
N366 N28 A6
N364 N30 A7
N369 N17 B0
N368 N19 B1
N367 N21 B2
N366 N23 B3
N365 N25 B4
N364 N27 B5
N362 N29 B6
N360 N31 B7
N363 N5 ad00
N361 N6 ad01
N379 N7 ad02
N377 N2 ad00
N376 N3 ad01
N375 N4 ad02
N367 N8 ad0
N365 N9 ad1
N363 N10 ad2
N362 N11 ad3
N361 N12 ad4
N360 N13 ad5
N351 N14 ad6
N350 N15 ad7
N374 N33 rfm
N378 N32 rw

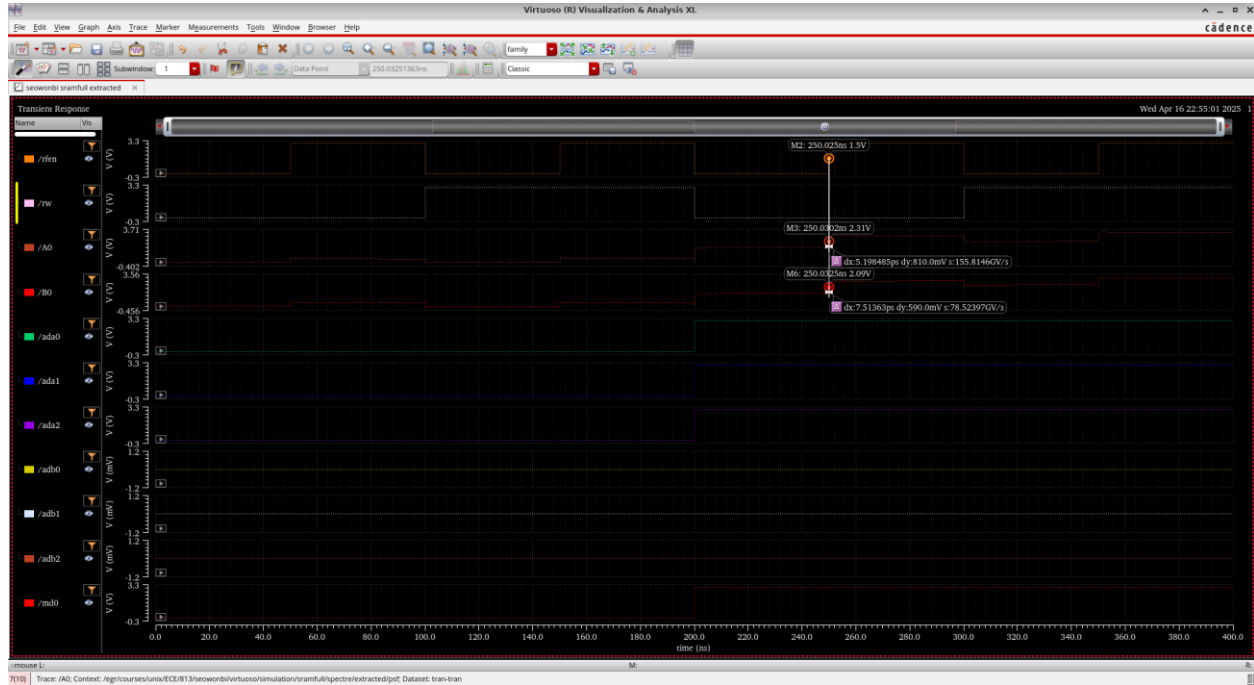
Devices in the netlist but not in the rules:
prospector
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

Layout schematic
instances
un-matched 0 0
required 0 0
size errors 0 0
pruned 0 0

```

Problem 7 – 8x8 SRAM Simulation



Problem 7 – 8x8 SRAM Stimulus File

simulator lang=spectre

global gnd!

parameters t0=25n tt=0.050n

Vdd (vdd! 0) vsource dc=3

Gnd (gnd! 0) vsource dc=0

v1 (ada0 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+]

v2 (ada1 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+]

v3 (ada2 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+]

v4 (adb0 0) vsource type=pwl wave = \[
+ (0*t0) 0
+]

v5 (adb1 0) vsource type=pwl wave = \[
+ (0*t0) 0
+]

```
v6 (adb2 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ ]
```

```
v7 (md0 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ (8*t0) 0  
+ (8*t0+tt) 3  
+ ]
```

```
v8 (md1 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ (8*t0) 0  
+ (8*t0+tt) 3  
+ ]
```

```
v9 (md2 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ (8*t0) 0  
+ (8*t0+tt) 3  
+ ]
```

```
v10 (md3 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ (8*t0) 0  
+ (8*t0+tt) 3  
+ ]
```

```
v11 (md4 0) vsource type=pwl wave = \[  
+ (0*t0) 0  
+ (8*t0) 0  
+ (8*t0+tt) 3  
+ ]
```

```
v12 (md5 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+ ]
```

```
v13 (md6 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+ ]
```

```
v14 (md7 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (8*t0) 0
+ (8*t0+tt) 3
+ ]
```

```
v15 (rw 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (4*t0) 0
+ (4*t0+tt) 3
+ (8*t0) 3
+ (8*t0+tt) 0
+ (12*t0) 0
+ (12*t0+tt) 3
+ ]
```

```
v16 (rfen 0) vsource type=pwl wave = \[
+ (0*t0) 0
+ (2*t0) 0
+ (2*t0+tt) 3
```

+ (4*t0) 3
 + (4*t0+tt) 0
 + (6*t0) 0
 + (6*t0+tt) 3
 + (8*t0) 3
 + (8*t0+tt) 0
 + (10*t0) 0
 + (10*t0+tt) 3
 + (12*t0) 3
 + (12*t0+tt) 0
 + (14*t0) 0
 + (14*t0+tt) 3
 +]

c0 (0 A0) capacitor c=3f
 c1 (0 B0) capacitor c=3f
 c2 (0 A1) capacitor c=3f
 c3 (0 B0) capacitor c=3f
 c4 (0 A2) capacitor c=3f
 c5 (0 B2) capacitor c=3f
 c6 (0 A3) capacitor c=3f
 c7 (0 B3) capacitor c=3f
 c8 (0 A4) capacitor c=3f
 c9 (0 B4) capacitor c=3f
 c10 (0 A5) capacitor c=3f
 c11 (0 B5) capacitor c=3f
 c12 (0 A6) capacitor c=3f
 c13 (0 B6) capacitor c=3f

c14 (0 A7) capacitor c=3f

c15 (0 B7) capacitor c=3f