ECE 813 - Spring 2025

Design Checkpoint 1 Report

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(Due Date) 4/11/2025

Summary: A quick summary of what you have completed since the last Design Checkpoint (DCP)

Tasks Completed

Cell	Cellview or Simulation Completed	Notes
8x8 SRAM	Schematic, Symbol, Layout, and Simulation (Exam3)	Checked simulation results Passing LVS for all Layouts
Shifter: 8-bit row	Schematic, Symbol, Layout, and Simulation	Done with LVS
ALU	Schematic, Symbol, Simulation (Adder – Schematic, Symbol, Simulation, and Layout – Done) (16-bit XOR – Schematic, Symbol, Simulation, and Layout – Done) (16-bit NOR – Schematic, Symbol, Simulation, and Layout – Done) (16-bit NAND – Schematic, Symbol, Simulation, and Layout – Done) (16-bit INV – Schematic, Symbol, Simulation, and Layout – Done)	All done in LVS and Simulation Need to make ALU Layout and LVS.

Changes to Work Plan

Please summarize the changes if any to the work plan in your proposal. Please list and comment on any cells you planned to complete by the current DCP and did not. Please describe any difficulties that have caused delays in your intended schedule.

I have completed the designs for SRAM and Shifter, and only the wiring for ALU remains. After that, I will proceed with the design and wiring of the latch and the mux. These tasks will be carried out in parallel with passing the layout LVS for ALU. The schematics for SRAM, Shifter, and ALU have all been completed, and simulations have confirmed that they operate correctly. Once the wiring is done as described, the integration should proceed smoothly.