ECE 813 - Spring 2025

Design Checkpoint 1 Report

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(Due Date) 4/4/2025

Summary: A quick summary of what you have completed since the last Design Checkpoint (DCP) (or for DCP1, since you turned in the draft proposal)

Tasks Completed

Cell	Cellview or Simulation Completed	Notes
SRAM: 1-bit SRAM	Layout (For Exam3)	Done schematic. Try Layout and LVS (8T SRAM)
Shifter: 8-bit row	Schematic, Symbol and Layout	Done with LVS
Adder	Layout	Struggling with LVS, something went wrong in hierarchy design.

Changes to Work Plan

Please summarize the changes if any to the work plan in your proposal. Please list and comment on any cells you planned to complete by the current DCP and did not. Please describe any difficulties that have caused delays in your intended schedule.

I tried to complete ALU but there were some errors in my design when I checked the whole adder. For Exam3, I will make SRAM first and fix the error of the Adder and complete ALU. After that, I will connect all the others.