ECE 813 - Spring 2025

Design Checkpoint 1 Report

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(Due Date) 4/18/2025

Summary: A quick summary of what you have completed since the last Design Checkpoint (DCP)

Tasks Completed

Cell	Cellview or Simulation Completed	Notes
8x8 SRAM	Schematic, Symbol, Layout, and Simulation (Exam3)	Checked simulation results Passing LVS for all Layouts Extracted Simulation Problem
Shifter: 8-bit row	Schematic, Symbol, Layout, and Simulation	Done with LVS Extracted Simulation Problem
ALU	Schematic, Symbol, Simulation (Adder – Schematic, Symbol, Simulation, and Layout – Done) (16-bit XOR – Schematic, Symbol, Simulation, and Layout – Done) (16-bit NOR – Schematic, Symbol, Simulation, and Layout – Done) (16-bit NAND – Schematic, Symbol, Simulation, and Layout – Done) (16-bit INV – Schematic, Symbol, Simulation, and Layout – Done)	All done in LVS and Simulation Need to make ALU Layout and LVS. Extracted Simulation Problem
8-bit latch	Done	
Wiring	Schematic, Symbol Need to do Layout	How about Extracted Simulation?

Changes to Work Plan

Please summarize the changes if any to the work plan in your proposal. Please list and comment on any cells you planned to complete by the current DCP and did not. Please describe any difficulties that have caused delays in your intended schedule.

Changing in shifter logic

Left	F5	F4	F3	Operation
0	0	0	0	Pass
0	0	0	1	LSR1
0	0	1	0	LSR2
0	0	1	1	LSR3
0	1	0	0	LSR4
0	1	0	1	LSR5
0	1	1	0	LSR6
0	1	1	1	LSR7
1	0	0	0	Pass
1	0	0	1	LSL1

1	0	1	0	LSL2
1	0	1	1	LSL3
1	1	0	0	LSL4
1	1	0	1	LSL5
1	1	1	0	LSL6
1	1	1	1	LSL7

I have implemented the 8-bit operation of the shifter by adding the left signal. The current design is complete, but there have been issues with the extracted simulation of individual components, and I need to continue attempting to resolve the problem. I haven't identified the exact cause yet, and I'm unsure how to fix it.