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ECE 813 Advanced VLSI Design

26 March 2025

Exam2

Problem 1 – 4-bit Adder Schematic – [MCGA4_Schematic]

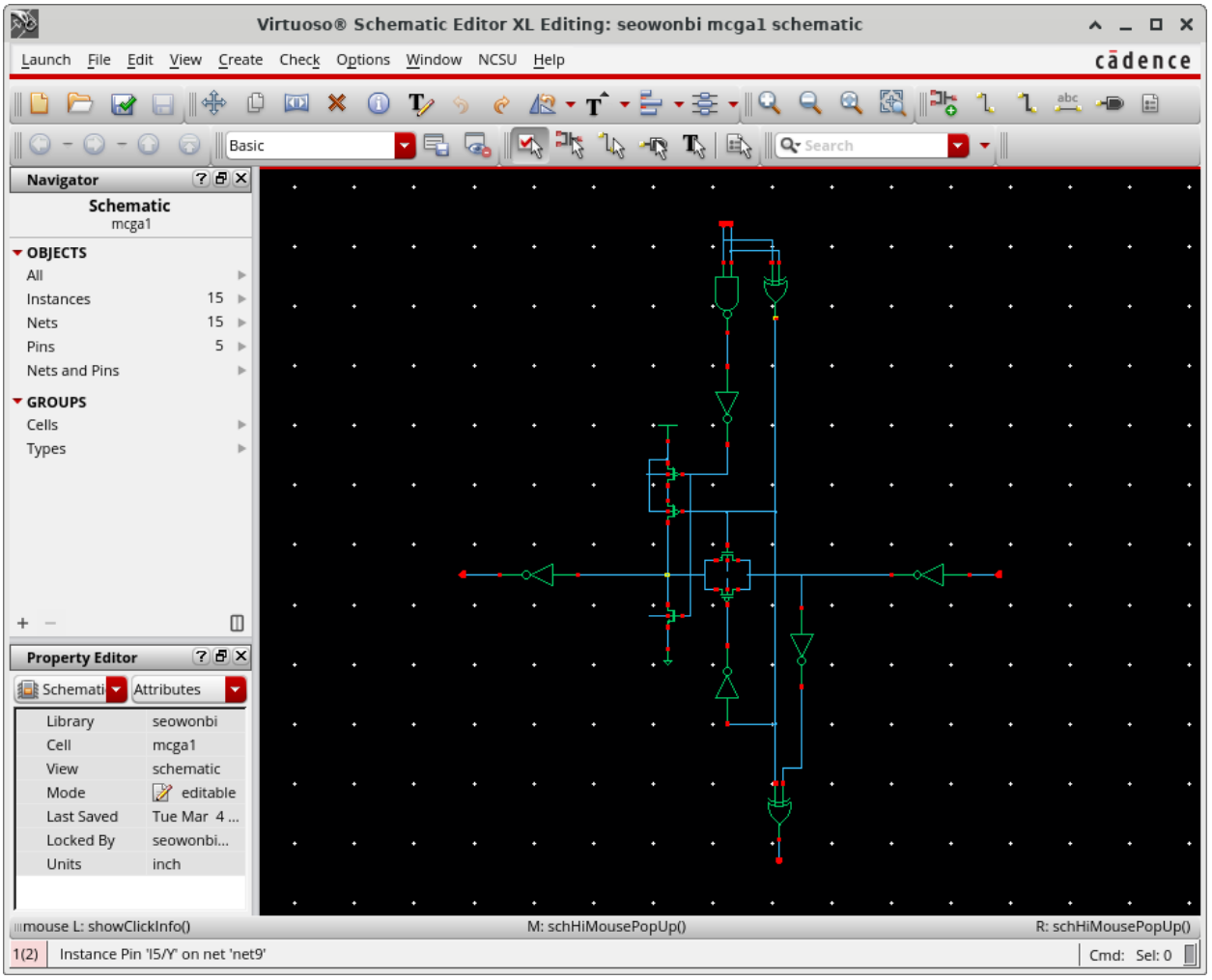

Figure 1. MCGA1_Schematic

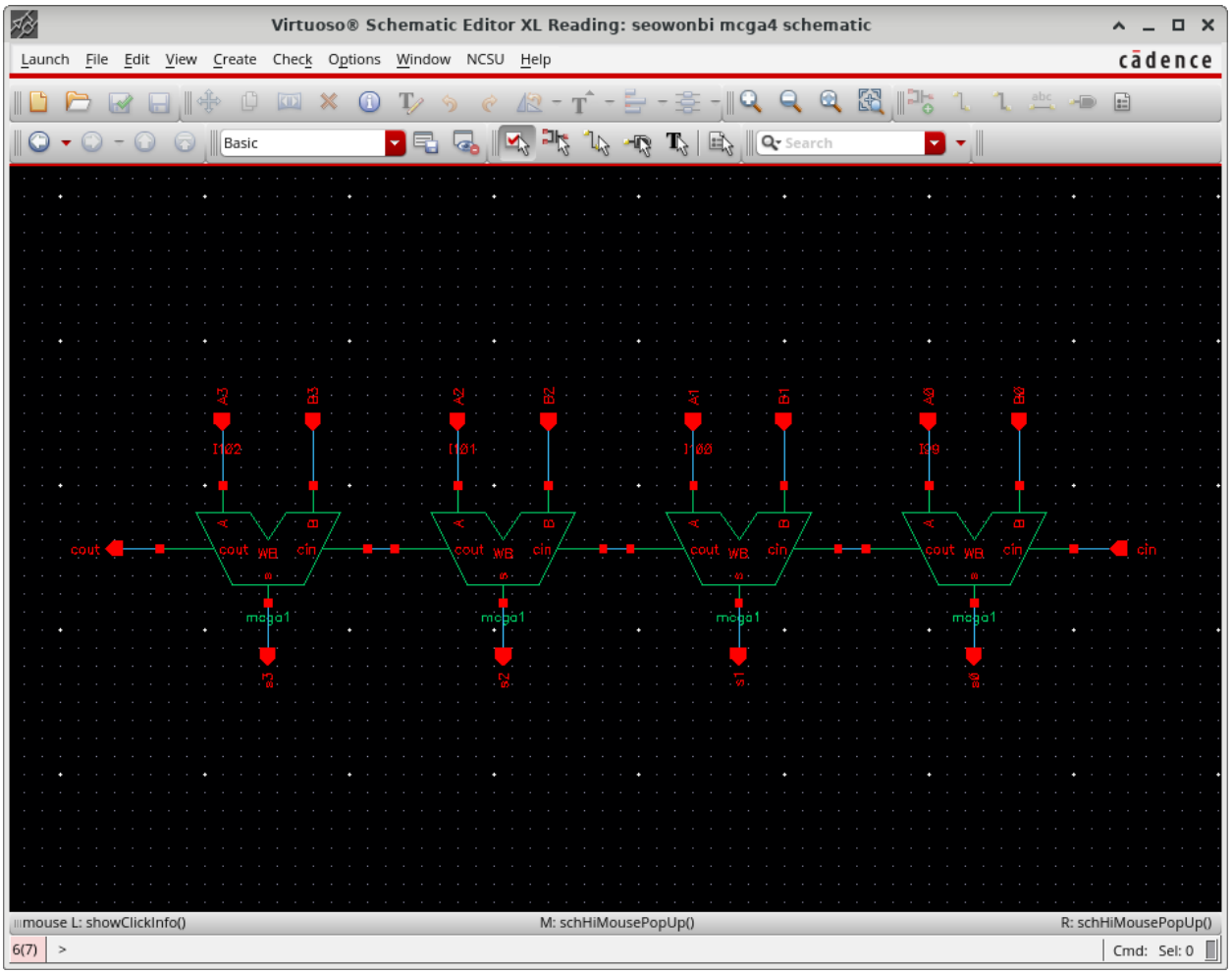

Figure 2. MCGA4_Schematic

Problem 2 – 4-bit Adder Symbol [MCGA4_Symbol]

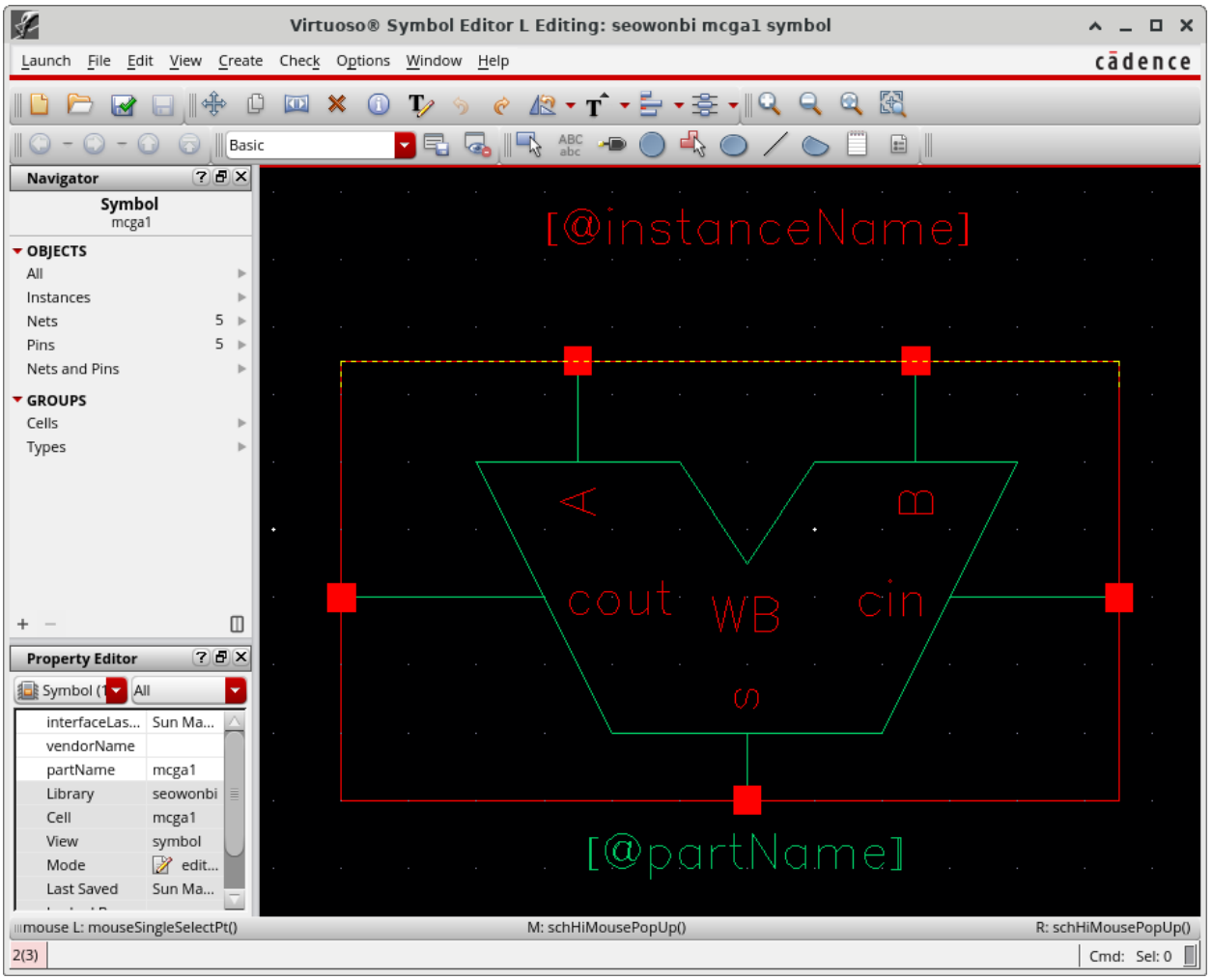

Figure 3. MCGA1_Symbol

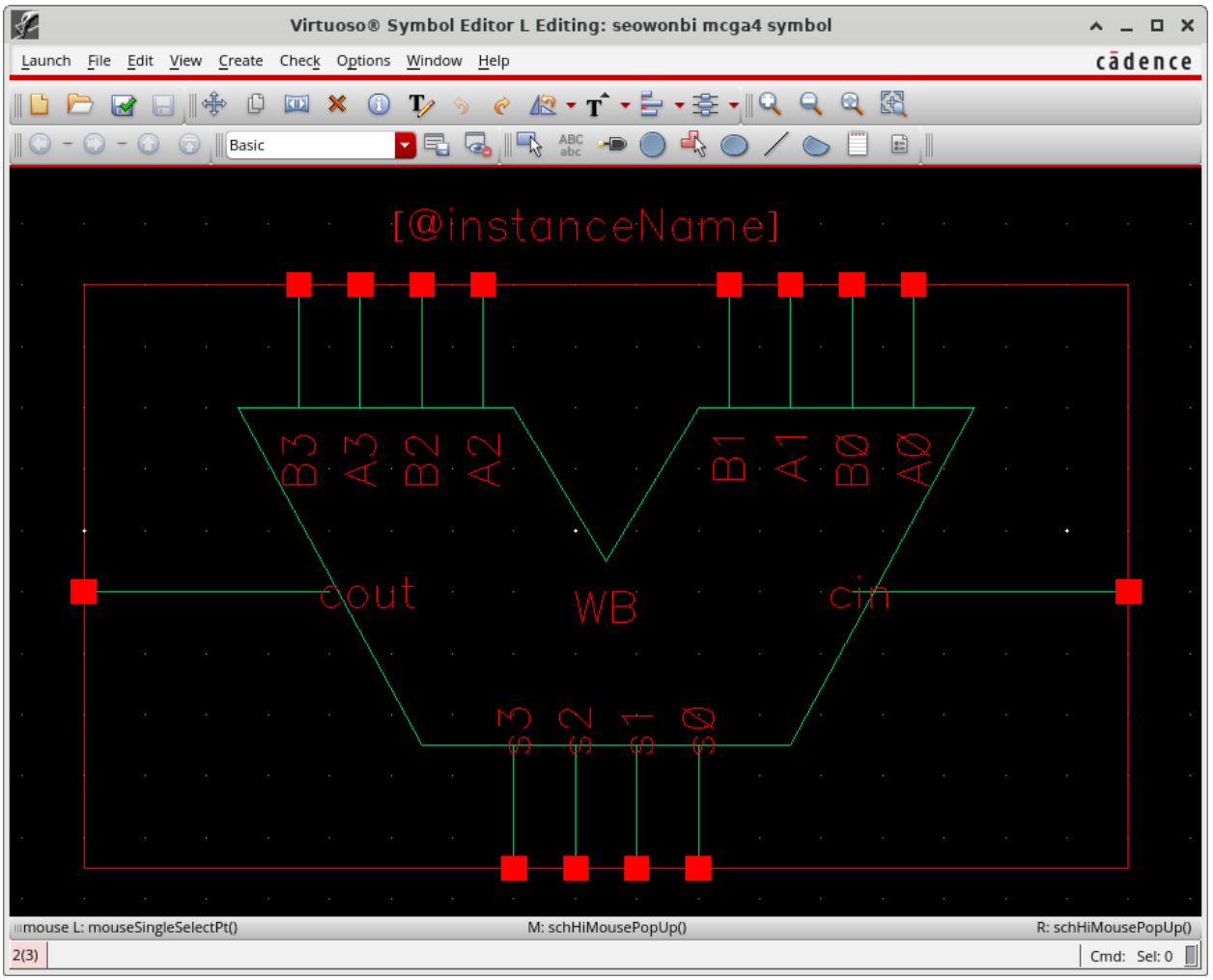

Figure 4. MCGA4_Symbol

Problem 3 – 4-bit Adder Layout - [MCGA4_Layout]

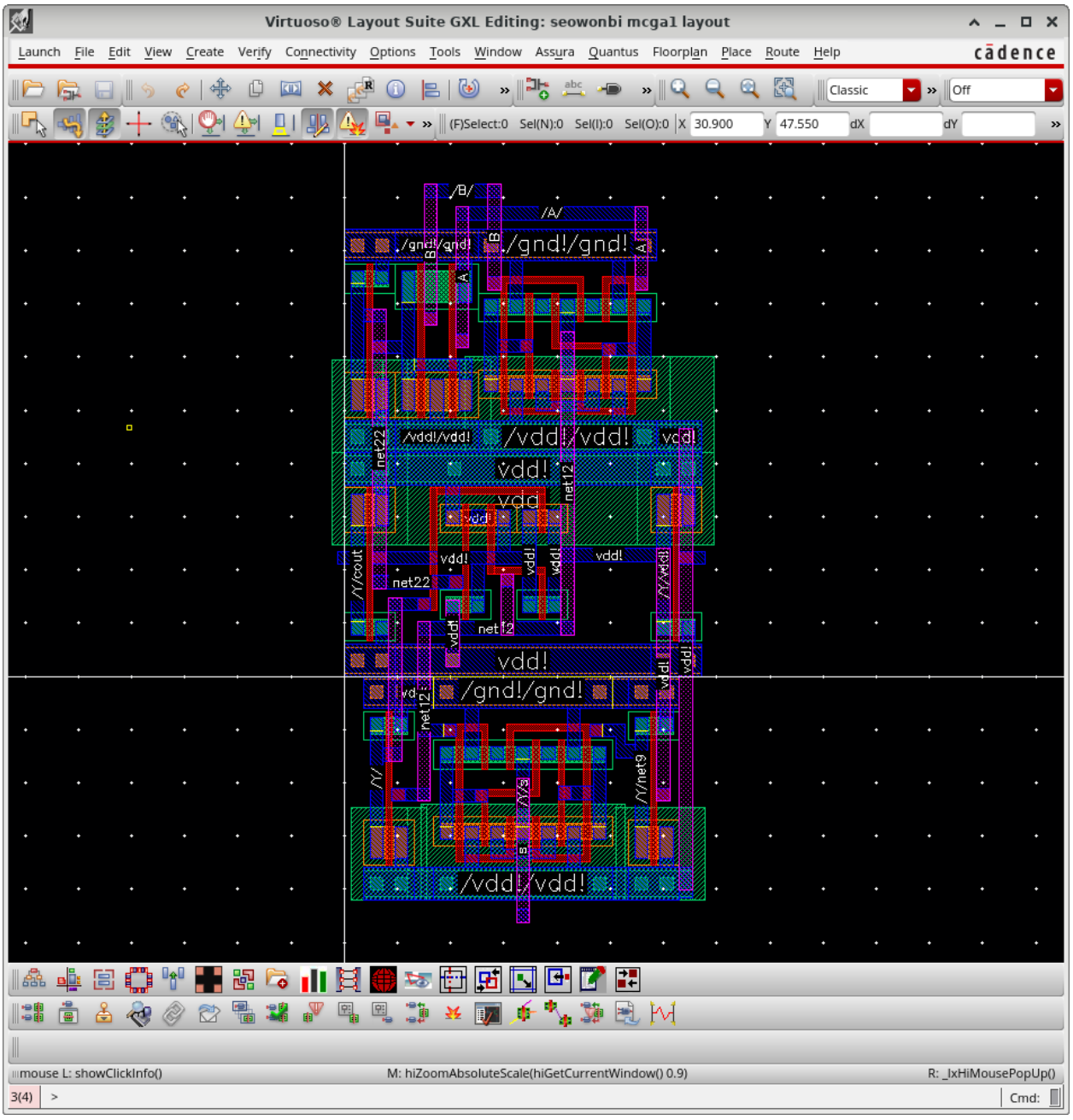

Figure 5. MCGA1_Layout

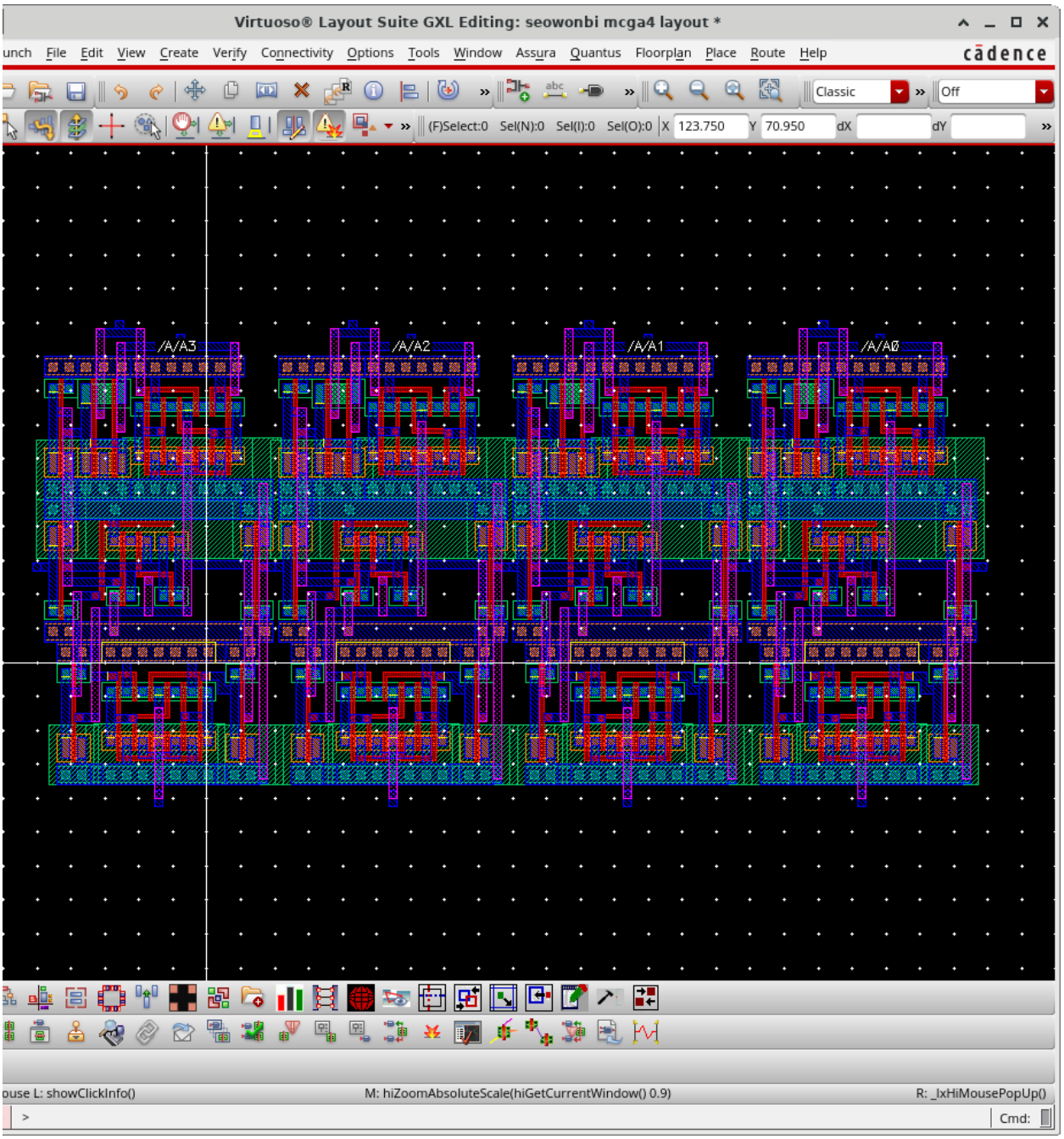

Figure 6. MCGA4_Layout

Problem 4 – Carry Lookahead Schematic – [CLA_Schematic]

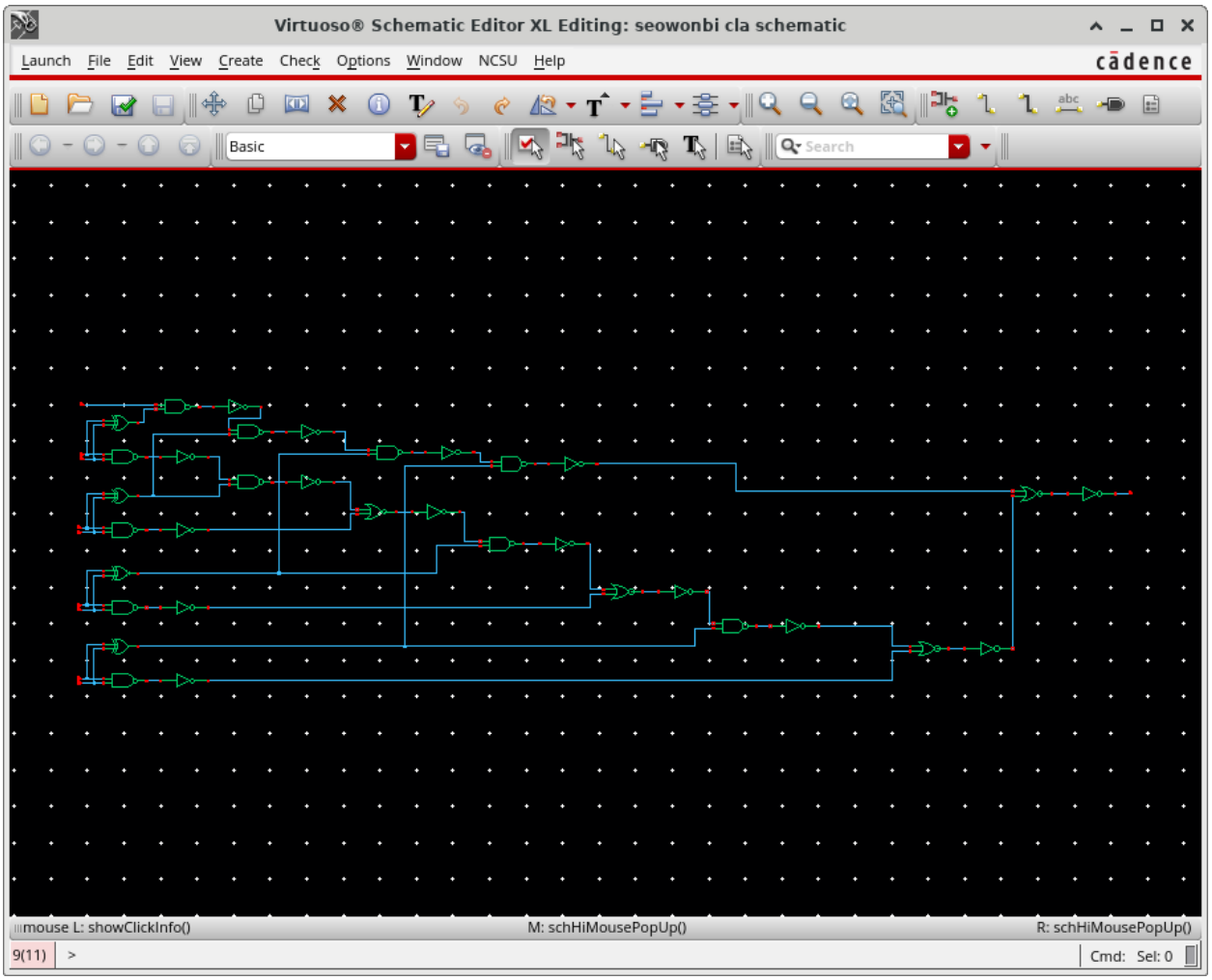

Figure 7. Carry Lookahead Schematic

Problem 5 – Carry Lookahead Symbol [CLA_Symbol]

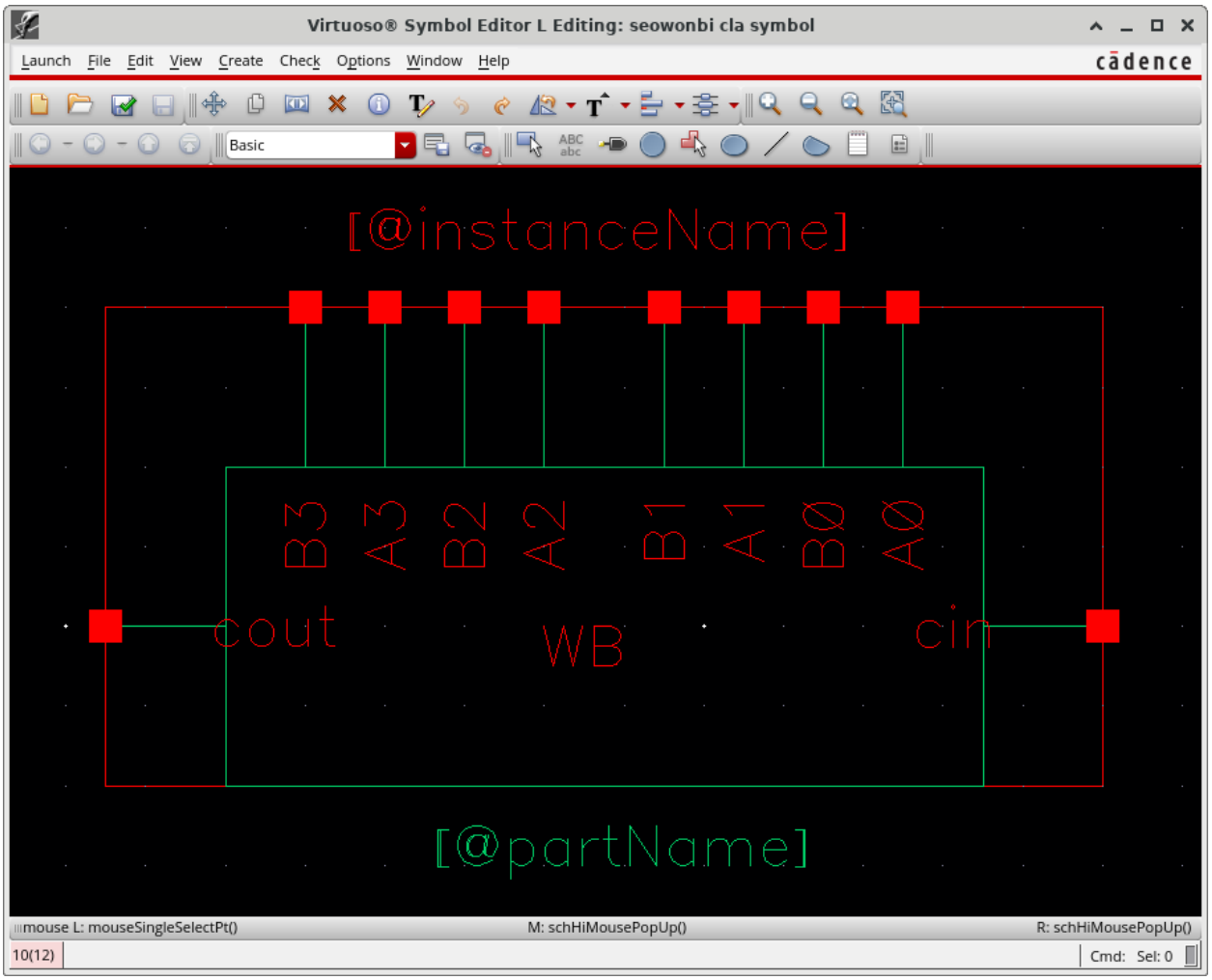

Figure 8. Carry Lookahead Symbol

Problem 6 – Carry Lookahead Layout - [CLA_Layout]

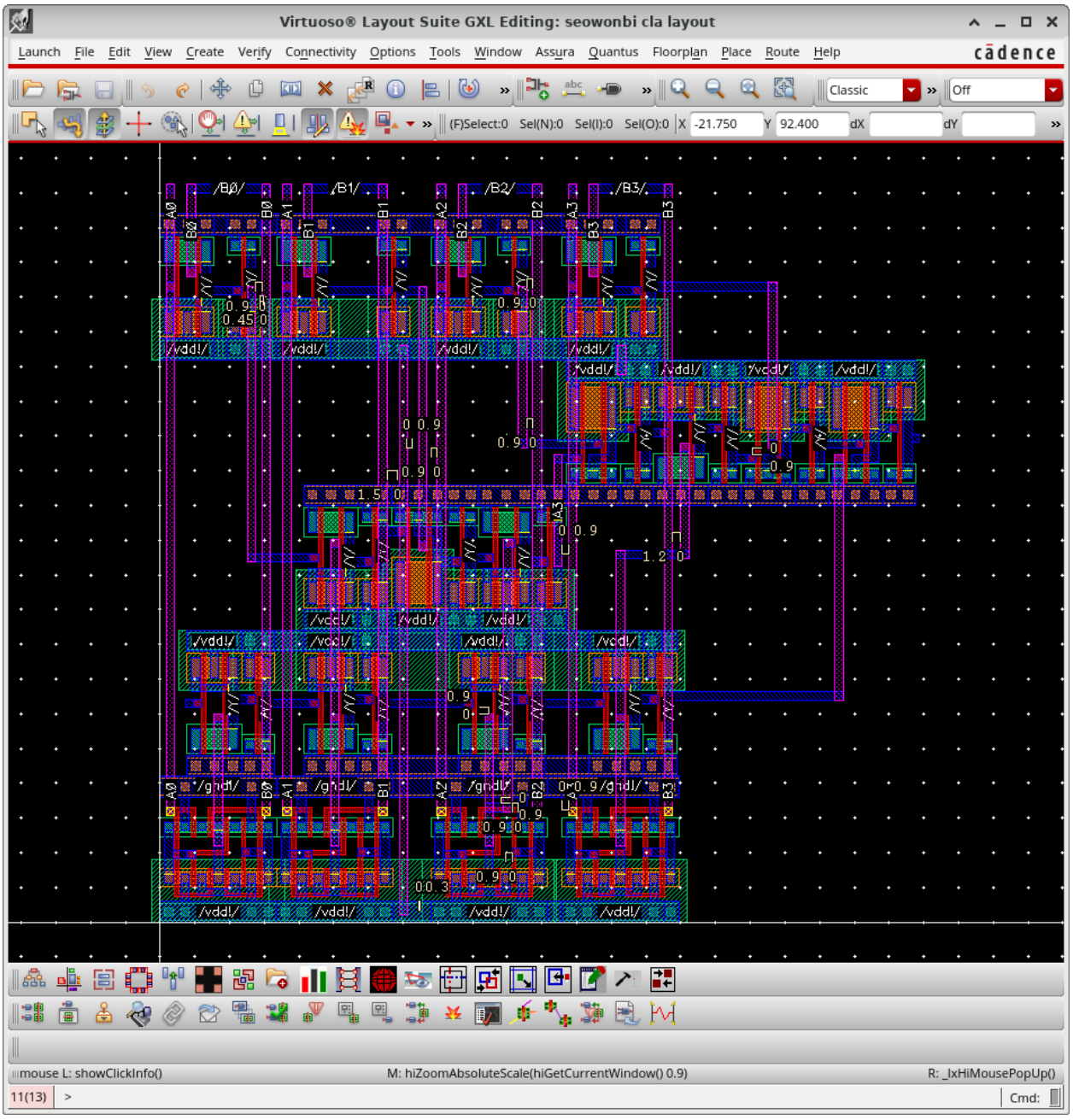

Figure 9. Carry Lookahead Layout

Problem 7 – 8-bit Adder Schematic – [MCGACLA8_Schematic]

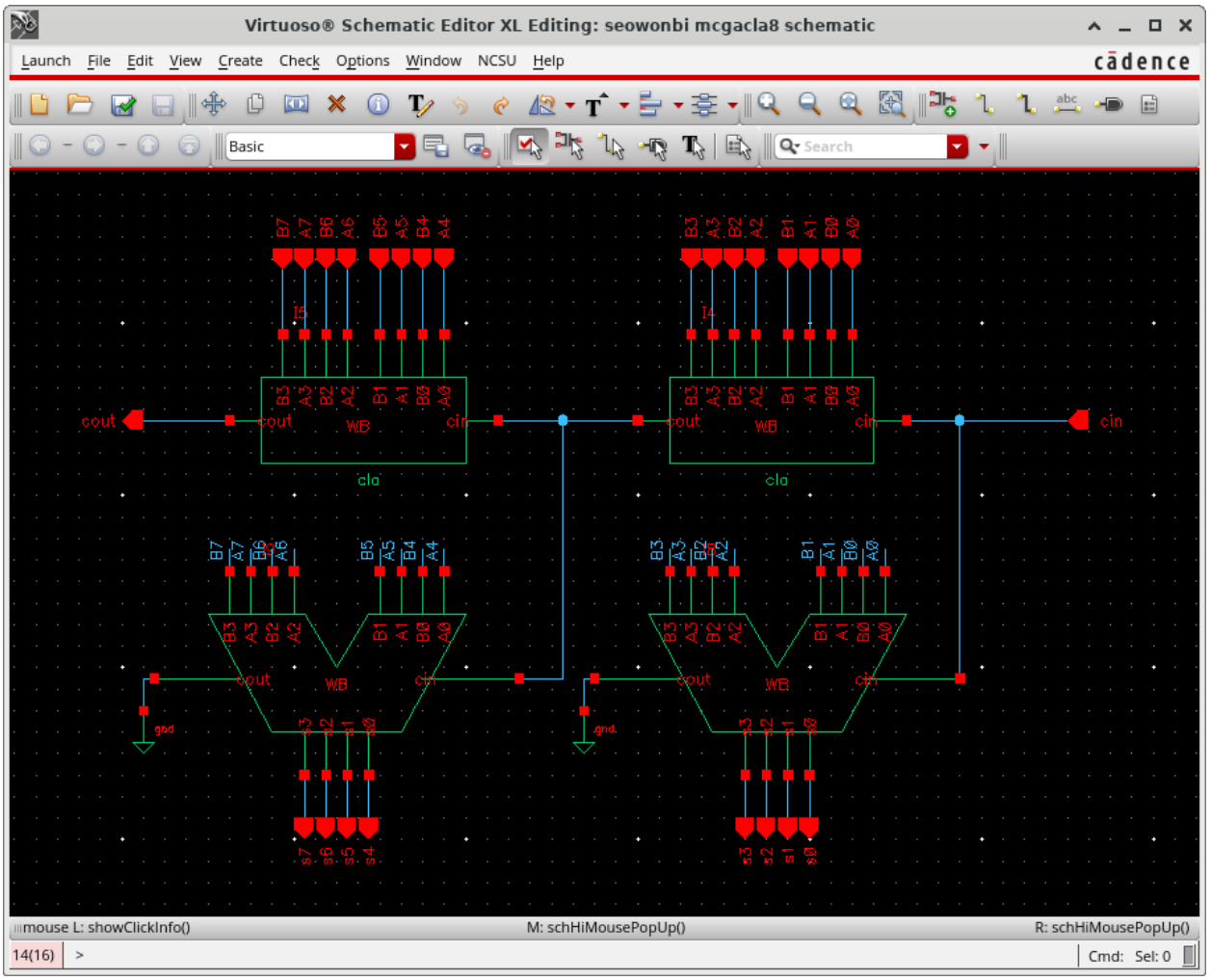

Figure 10. 8-bit Manchester Carry Generation Carry Lookahead Adder Schematic

Problem 8 – 8-bit Adder Symbol – [MCGACLA8_Symbol]

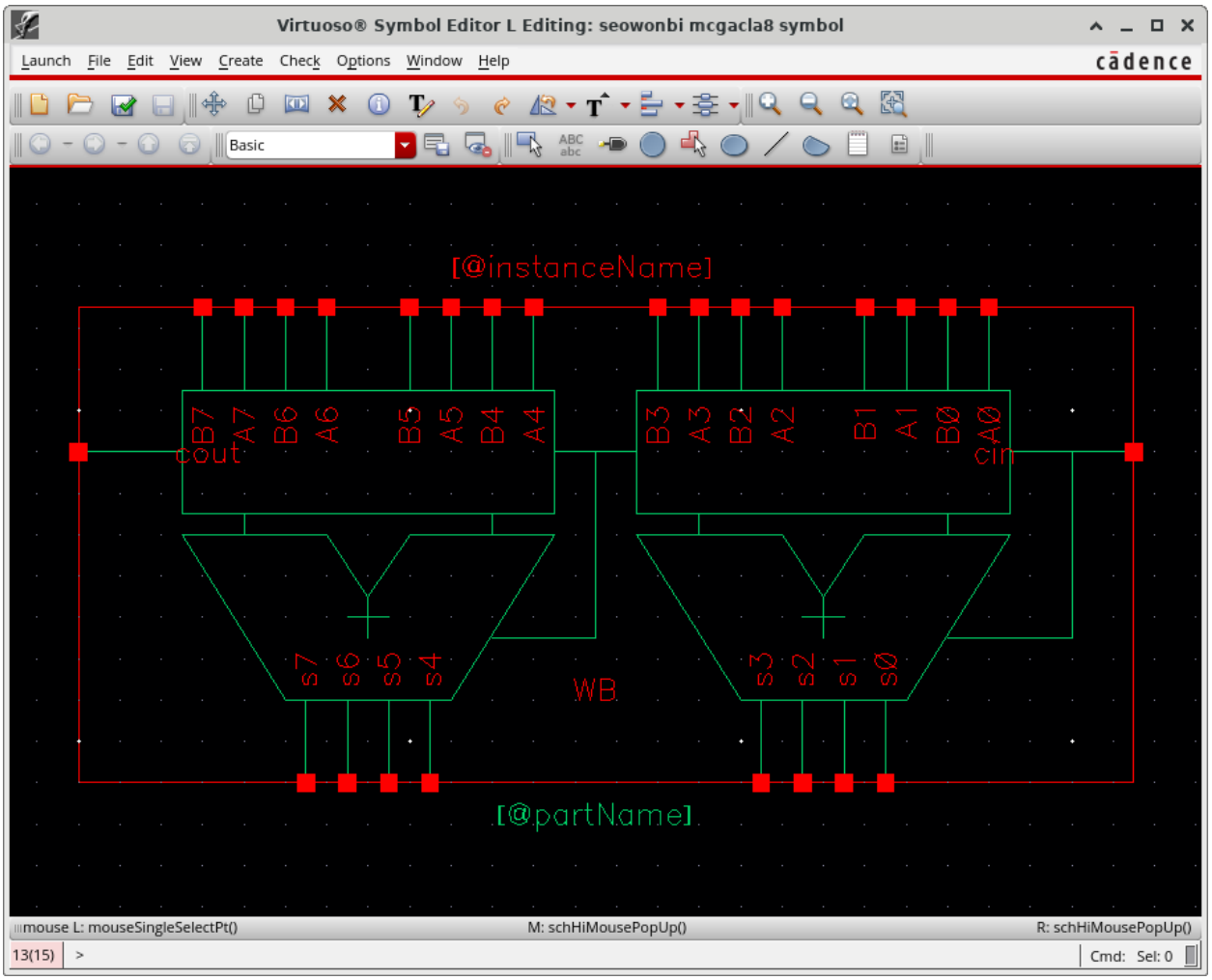

Figure 11. 8-bit Adder Symbol

Problem 9 – 8-bit Adder Layout - [MCGACLA8_Layout]

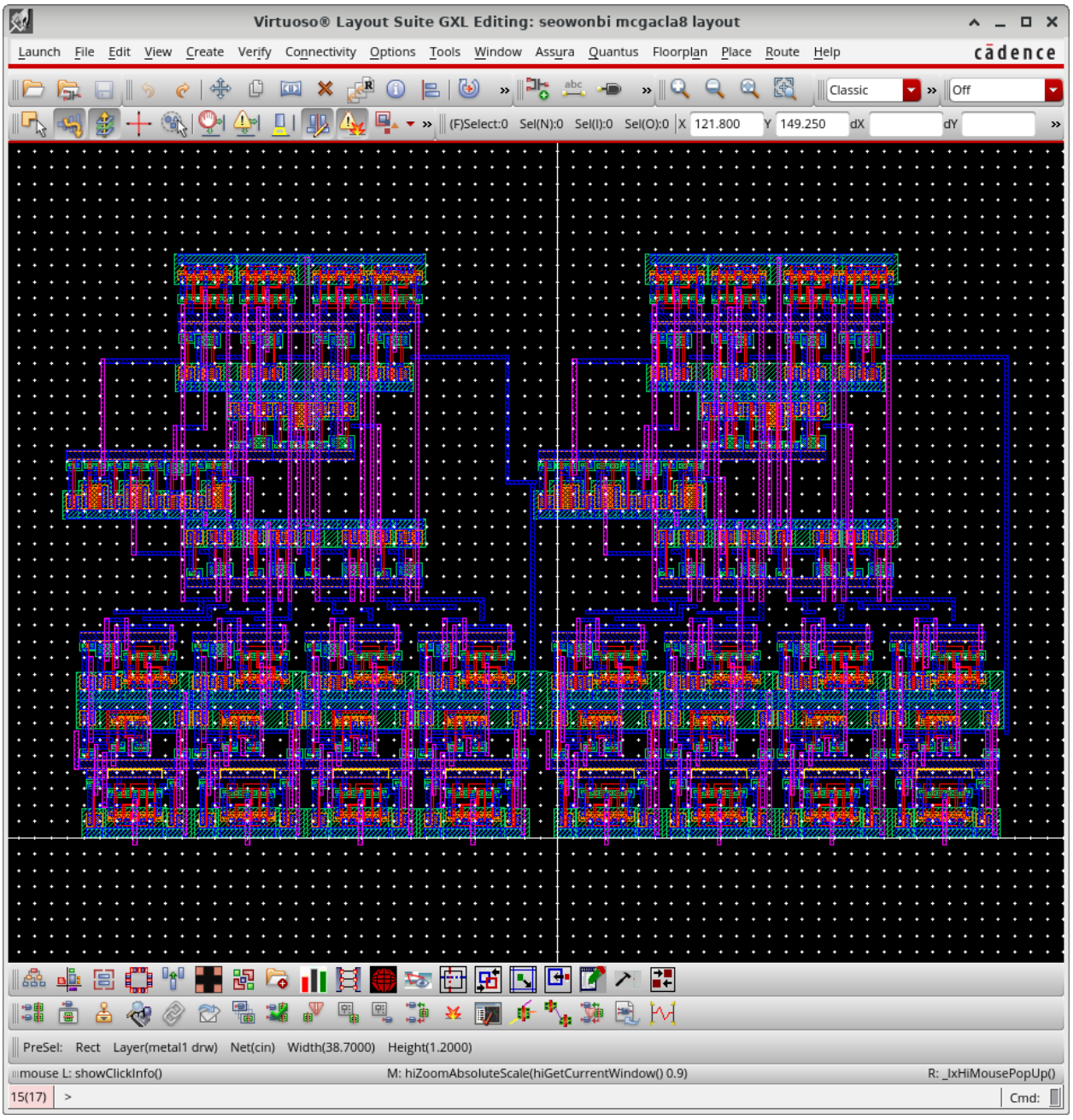

Figure 12. 8-bit Adder Layout

Problem 10 – 8-bit Adder LVS

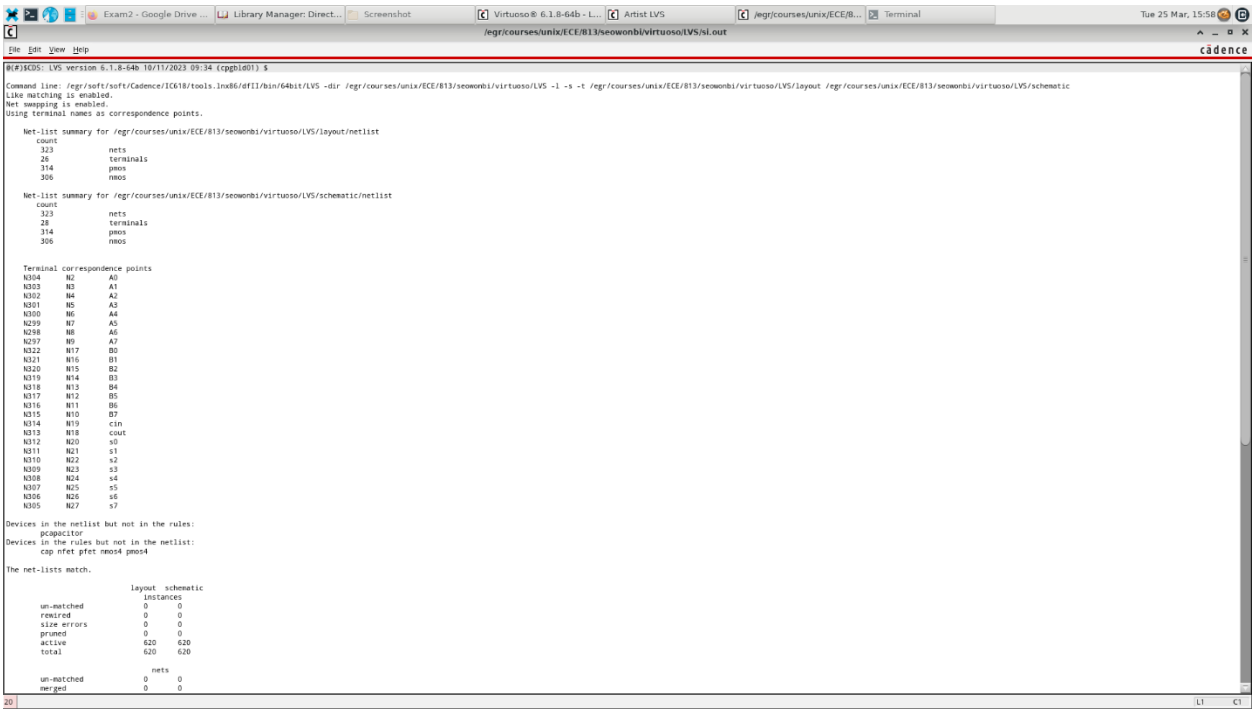

Figure 13. 8-bit Adder LVS

Problem 11 – 8-bit Adder Simulation

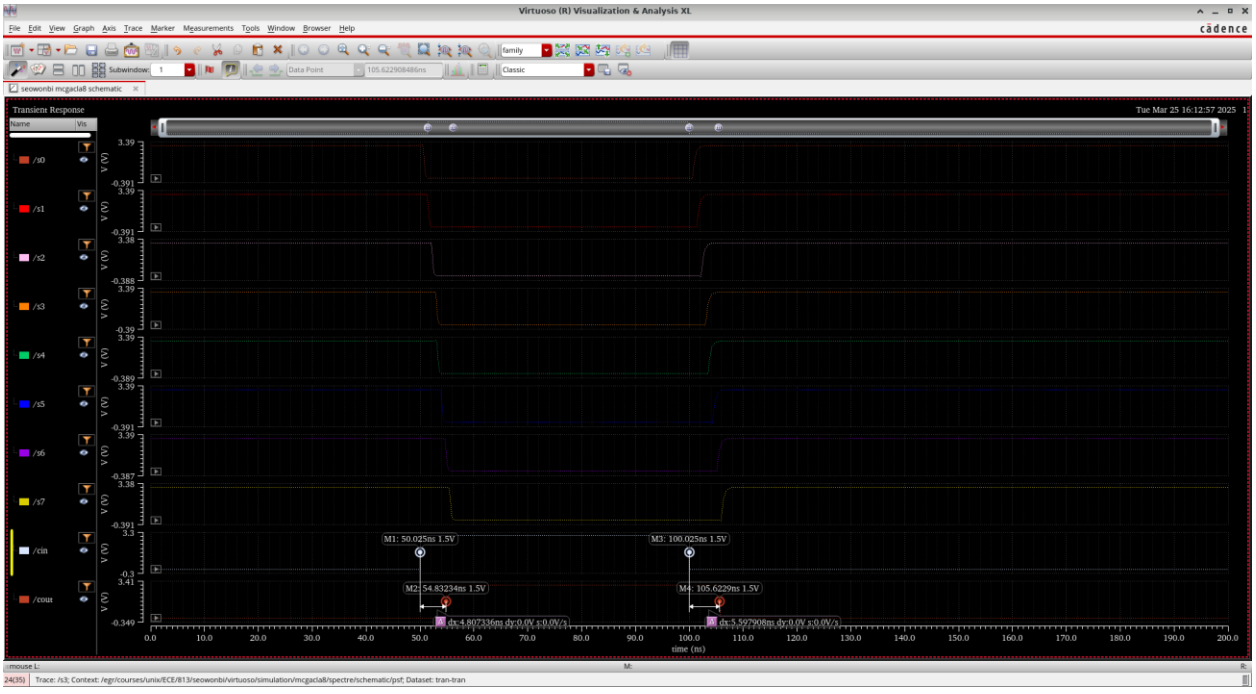

Figure 14. 8-bit Adder Simulation

Rise time delay: 4.807336ns, Falling time delay: 5.597908ns

A	B	Cin	s0	s1	s2	s3	s4	s5	s6	s7	cout
1	0	0	1	1	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0	0	0	0	1
1	0	0	1	1	1	1	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1	1	0

Figure 15. Truth Table of the 8-bit Adder