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Revisions

Rev	Description	Date	Approved
X1	Original Release	APR-17-2015	O. Romero
A	Production Release	APR-29-2015	O. Romero
B	2nd Production Release	JUL-20-2015	O. Romero

FREEDOM+S32K144

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ICAP Classification: FCP: FIUO: X PUBI:

Designer: Osvaldo Romero	Drawing Title: FRDMPK144-Q100
Drawn by: Osvaldo Romero	Page Title: TITLE PAGE
Approved: APPROVER	Size C / Document Number SCH-28810 PDF: SPF-28810 / Rev B
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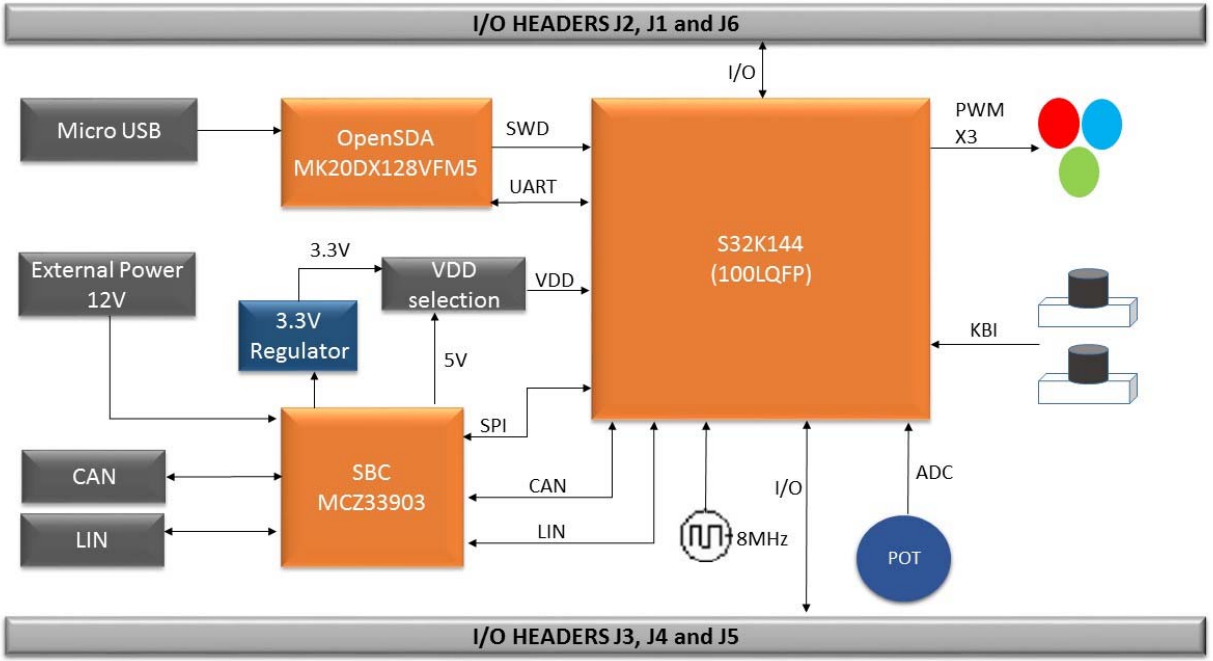
1. Unless Otherwise Specified:
   All resistors are in ohms, 1% and 5 %
   All capacitors are in uF, 10% , 20 % and 5%
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.



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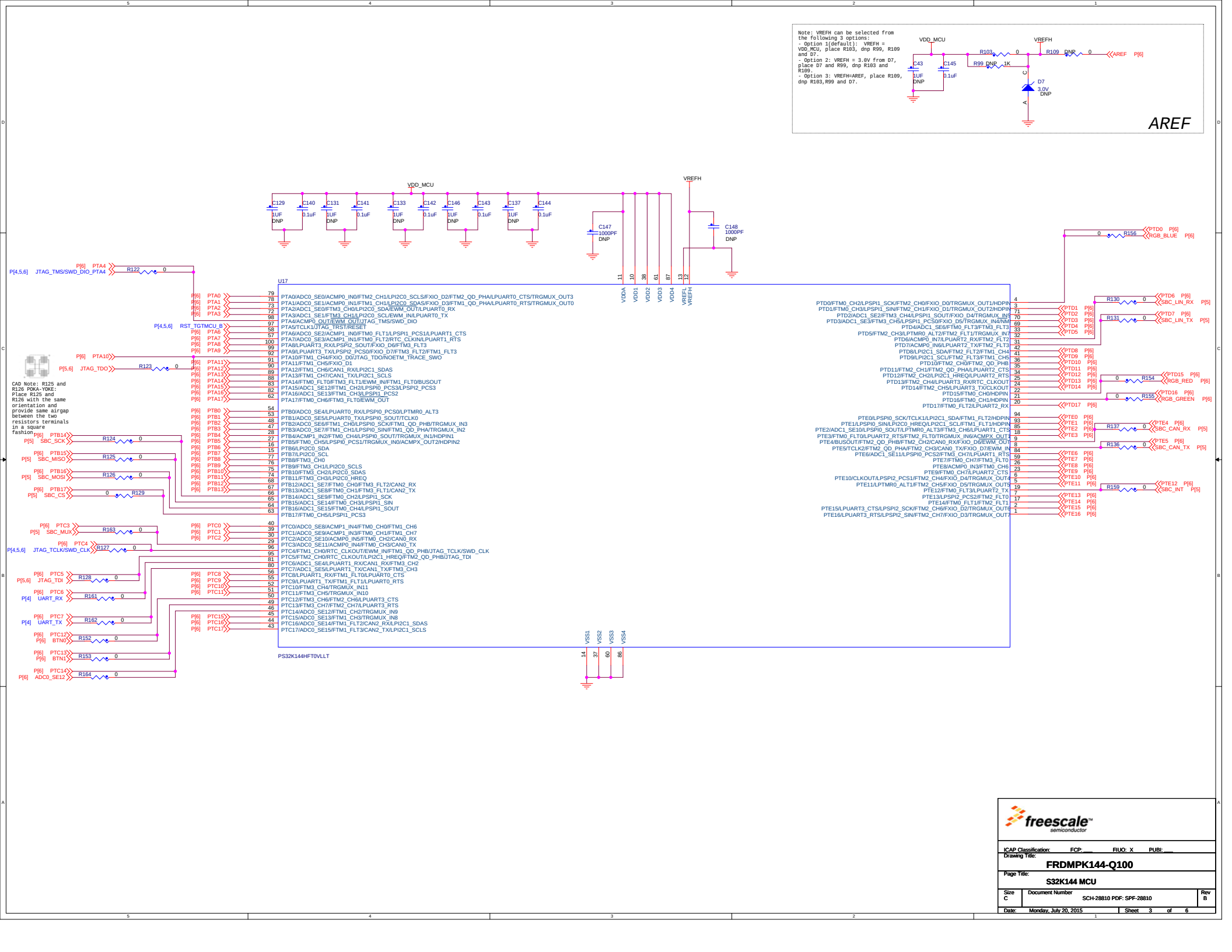
Note: VREFH can be selected from the following 3 options:
- Option 1(default): VREFH = VDD_MCU, place R103, dnp R99, R109 and D7.
- Option 2: VREFH = 3.0V from D7, place D7 and R99, dnp R103 and R109.
- Option 3: VREFH=AREF, place R109, dnp R103,R99 and D7.
VDD_MCU
VREFH
R103 0
R109 DNP 0
AREF P[6]
C43 1UF DNP
C145 0.1uF
R99 DNP 1K
D7 3.0V DNP
AREF
VDD_MCU
C129 1UF DNP
C140 0.1uF
C131 1UF DNP
C141 0.1uF
C133 1UF DNP
C142 0.1uF
C146 1UF DNP
C143 0.1uF
C137 1UF DNP
C144 0.1uF
C147 1000PF DNP
C148 1000PF DNP
VREFH
U17
VDDA VDD1 VDD2 VDD3 VDD4 VREFL VREFH
PTA0/ADC0_SE0/ACMP0_IN0/FTM2_CH1/LPI2C0_SCLS/FXIO_D2/FTM2_QD_PHA/LPUART0_CTS/TRGMUX_OUT3
PTA1/ADC0_SE1/ACMP0_IN1/FTM1_CH1/LPI2C0_SDAS/FXIO_D3/FTM1_QD_PHA/LPUART0_RTS/TRGMUX_OUT0
PTA2/ADC1_SE0/FTM3_CH0/LPI2C0_SDA/EWM_OUT/LPUART0_RX
PTA3/ADC1_SE1/FTM3_CH1/LPI2C0_SCL/EWM_IN/LPUART0_TX
PTA4/ACMP0_OUT/EWM_OUT/JTAG_TMS/SWD_DIO
PTA5/TCLK1/JTAG_TRST/RESET
PTA6/ADC0_SE2/ACMP1_IN0/FTM0_FLT1/LPSPI1_PCS1/LPUART1_CTS
PTA7/ADC0_SE3/ACMP1_IN1/FTM0_FLT2/RTC_CLKIN/LPUART1_RTS
PTA8/LPUART3_RX/LPSPI2_SOUT/FXIO_D6/FTM3_FLT3
PTA9/LPUART3_TX/LPSPI2_PCS0/FXIO_D7/FTM3_FLT2/FTM1_FLT3
PTA10/FTM1_CH4/FXIO_D0/JTAG_TDO/NOETM_TRACE_SWO
PTA11/FTM1_CH5/FXIO_D1
PTA12/FTM1_CH6/CAN1_RX/LPI2C1_SDAS
PTA13/FTM1_CH7/CAN1_TX/LPI2C1_SCLS
PTA14/FTM0_FLT0/FTM3_FLT1/EWM_IN/FTM1_FLT0/BUSOUT
PTA15/ADC1_SE12/FTM1_CH2/LPSPI0_PCS3/LPSPI2_PCS3
PTA16/ADC1_SE13/FTM1_CH3/LPSPI1_PCS2
PTA17/FTM0_CH6/FTM3_FLT0/EWM_OUT
PTB0/ADC0_SE4/LPUART0_RX/LPSPI0_PCS0/LPTMR0_ALT3
PTB1/ADC0_SE5/LPUART0_TX/LPSPI0_SOUT/TCLK0
PTB2/ADC0_SE6/FTM1_CH0/LPSPI0_SCK/FTM1_QD_PHB/TRGMUX_IN3
PTB3/ADC0_SE7/FTM1_CH1/LPSPI0_SIN/FTM1_QD_PHA/TRGMUX_IN2
PTB4/ACMP1_IN2/FTM0_CH4/LPSPI0_SOUT/TRGMUX_IN1/HDPIN1
PTB5/FTM0_CH5/LPSPI0_PCS1/TRGMUX_IN0/ACMPX_OUT2/HDPIN2
PTB6/LPI2C0_SDA
PTB7/LPI2C0_SCL
PTB8/FTM3_CH0
PTB9/FTM3_CH1/LPI2C0_SCLS
PTB10/FTM3_CH2/LPI2C0_SDAS
PTB11/FTM3_CH3/LPI2C0_HREQ
PTB12/ADC1_SE7/FTM0_CH0/FTM3_FLT2/CAN2_RX
PTB13/ADC1_SE8/FTM0_CH1/FTM3_FLT1/CAN2_TX
PTB14/ADC1_SE9/FTM0_CH2/LPSPI1_SCK
PTB15/ADC1_SE14/FTM0_CH3/LPSPI1_SIN
PTB16/ADC1_SE15/FTM0_CH4/LPSPI1_SOUT
PTB17/FTM0_CH5/LPSPI1_PCS3
PTC0/ADC0_SE8/ACMP1_IN4/FTM0_CH0/FTM1_CH6
PTC1/ADC0_SE9/ACMP1_IN3/FTM0_CH1/FTM1_CH7
PTC2/ADC0_SE10/ACMP0_IN5/FTM0_CH2/CAN0_RX
PTC3/ADC0_SE11/ACMP0_IN4/FTM0_CH3/CAN0_TX
PTC4/FTM1_CH0/RTC_CLKOUT/EWM_IN/FTM1_QD_PHB/JTAG_TCLK/SWD_CLK
PTC5/FTM2_CH0/RTC_CLKOUT/LPI2C1_HREQ/FTM2_QD_PHB/JTAG_TDI
PTC6/ADC1_SE4/LPUART1_RX/CAN1_RX/FTM3_CH2
PTC7/ADC1_SE5/LPUART1_TX/CAN1_TX/FTM3_CH3
PTC8/LPUART1_RX/FTM1_FLT0/LPUART0_CTS
PTC9/LPUART1_TX/FTM1_FLT1/LPUART0_RTS
PTC10/FTM3_CH4/TRGMUX_IN11
PTC11/FTM3_CH5/TRGMUX_IN10
PTC12/FTM3_CH6/FTM2_CH6/LPUART3_CTS
PTC13/FTM3_CH7/FTM2_CH7/LPUART3_RTS
PTC14/ADC0_SE12/FTM1_CH2/TRGMUX_IN9
PTC15/ADC0_SE13/FTM1_CH3/TRGMUX_IN8
PTC16/ADC0_SE14/FTM1_FLT2/CAN2_RX/LPI2C1_SDAS
PTC17/ADC0_SE15/FTM1_FLT3/CAN2_TX/LPI2C1_SCLS
PS32K144HFT0VLLT
VSS1 VSS2 VSS3 VSS4
PTD0/FTM0_CH2/LPSPI1_SCK/FTM2_CH0/FXIO_D0/TRGMUX_OUT1/HDPIN
PTD1/FTM0_CH3/LPSPI1_SIN/FTM2_CH1/FXIO_D1/TRGMUX_OUT2/HDPIN
PTD2/ADC1_SE2/FTM3_CH4/LPSPI1_SOUT/FXIO_D4/TRGMUX_IN5
PTD3/ADC1_SE3/FTM3_CH5/LPSPI1_PCS0/FXIO_D5/TRGMUX_IN4/NMI
PTD4/ADC1_SE6/FTM0_FLT3/FTM3_FLT3
PTD5/FTM2_CH3/LPTMR0_ALT2/FTM2_FLT1/TRGMUX_IN7
PTD6/ACMP0_IN7/LPUART2_RX/FTM2_FLT2
PTD7/ACMP0_IN6/LPUART2_TX/FTM2_FLT3
PTD8/LPI2C1_SDA/FTM2_FLT2/FTM1_CH4
PTD9/LPI2C1_SCL/FTM2_FLT3/FTM1_CH5
PTD10/FTM2_CH0/FTM2_QD_PHB
PTD11/FTM2_CH1/FTM2_QD_PHA/LPUART2_CTS
PTD12/FTM2_CH2/LPI2C1_HREQ/LPUART2_RTS
PTD13/FTM2_CH4/LPUART3_RX/RTC_CLKOUT
PTD14/FTM2_CH5/LPUART3_TX/CLKOUT
PTD15/FTM0_CH0/HDPIN
PTD16/FTM0_CH1/HDPIN
PTD17/FTM0_FLT2/LPUART2_RX
PTE0/LPSPI0_SCK/TCLK1/LPI2C1_SDA/FTM1_FLT2/HDPIN
PTE1/LPSPI0_SIN/LPI2C0_HREQ/LPI2C1_SCL/FTM1_FLT1/HDPIN
PTE2/ADC1_SE10/LPSPI0_SOUT/LPTMR0_ALT3/FTM3_CH6/LPUART1_CTS
PTE3/FTM0_FLT0/LPUART2_RTS/FTM2_FLT0/TRGMUX_IN6/ACMPX_OUT1
PTE4/BUSOUT/FTM2_QD_PHB/FTM2_CH2/CAN0_RX/FXIO_D6/EWM_OUT
PTE5/TCLK2/FTM2_QD_PHA/FTM2_CH3/CAN0_TX/FXIO_D7/EWM_IN
PTE6/ADC1_SE11/LPSPI0_PCS2/FTM3_CH7/LPUART1_RTS
PTE7/FTM0_CH7/FTM3_FLT0
PTE8/ACMP0_IN3/FTM0_CH6
PTE9/FTM0_CH7/LPUART2_CTS
PTE10/CLKOUT/LPSPI2_PCS1/FTM2_CH4/FXIO_D4/TRGMUX_OUT4
PTE11/LPTMR0_ALT1/FTM2_CH5/FXIO_D5/TRGMUX_OUT5
PTE12/FTM0_FLT3/LPUART2_TX
PTE13/LPSPI2_PCS2/FTM2_FLT0
PTE14/FTM0_FLT1/FTM2_FLT1
PTE15/LPUART3_CTS/LPSPI2_SCK/FTM2_CH6/FXIO_D2/TRGMUX_OUT6
PTE16/LPUART3_RTS/LPSPI2_SIN/FTM2_CH7/FXIO_D3/TRGMUX_OUT7
R156 0 PTD0 P[6] RGB_BLUE P[6]
R130 0 PTD6 P[6] SBC_LIN_RX P[5]
R131 0 PTD7 P[6] SBC_LIN_TX P[5]
R154 0 PTD15 P[6] RGB_RED P[6]
R155 0 PTD16 P[6] RGB_GREEN P[6]
R137 0 PTE4 P[6] SBC_CAN_RX P[5]
R136 0 PTE5 P[6] SBC_CAN_TX P[5]
R159 0 PTE12 P[6] SBC_INT P[5]
P[6] PTA4 P[4,5,6] JTAG_TMS/SWD_DIO_PTA4 R122 0
P[4,5,6] RST_TGTMCU_B
P[6] PTA10 P[5,6] JTAG_TDO R123 0
CAD Note: R125 and R126 POKA-YOKE: Place R125 and R126 with the same orientation and provide same airgap between the two resistors terminals in a square fashion
P[6] PTB14 P[5] SBC_SCK R124 0
P[6] PTB15 P[5] SBC_MISO R125 0
P[6] PTB16 P[5] SBC_MOSI R126 0
P[6] PTB17 P[5] SBC_CS R129 0
P[6] PTC3 P[5] SBC_MUX R163 0
P[6] PTC4 P[4,5,6] JTAG_TCLK/SWD_CLK R127 0
P[6] PTC5 P[5,6] JTAG_TDI R128 0
P[6] PTC6 P[4] UART_RX R161 0
P[6] PTC7 P[4] UART_TX R162 0
P[6] PTC12 P[6] BTN0 R152 0
P[6] PTC13 P[6] BTN1 R153 0
P[6] PTC14 P[6] ADC0_SE12 R164 0
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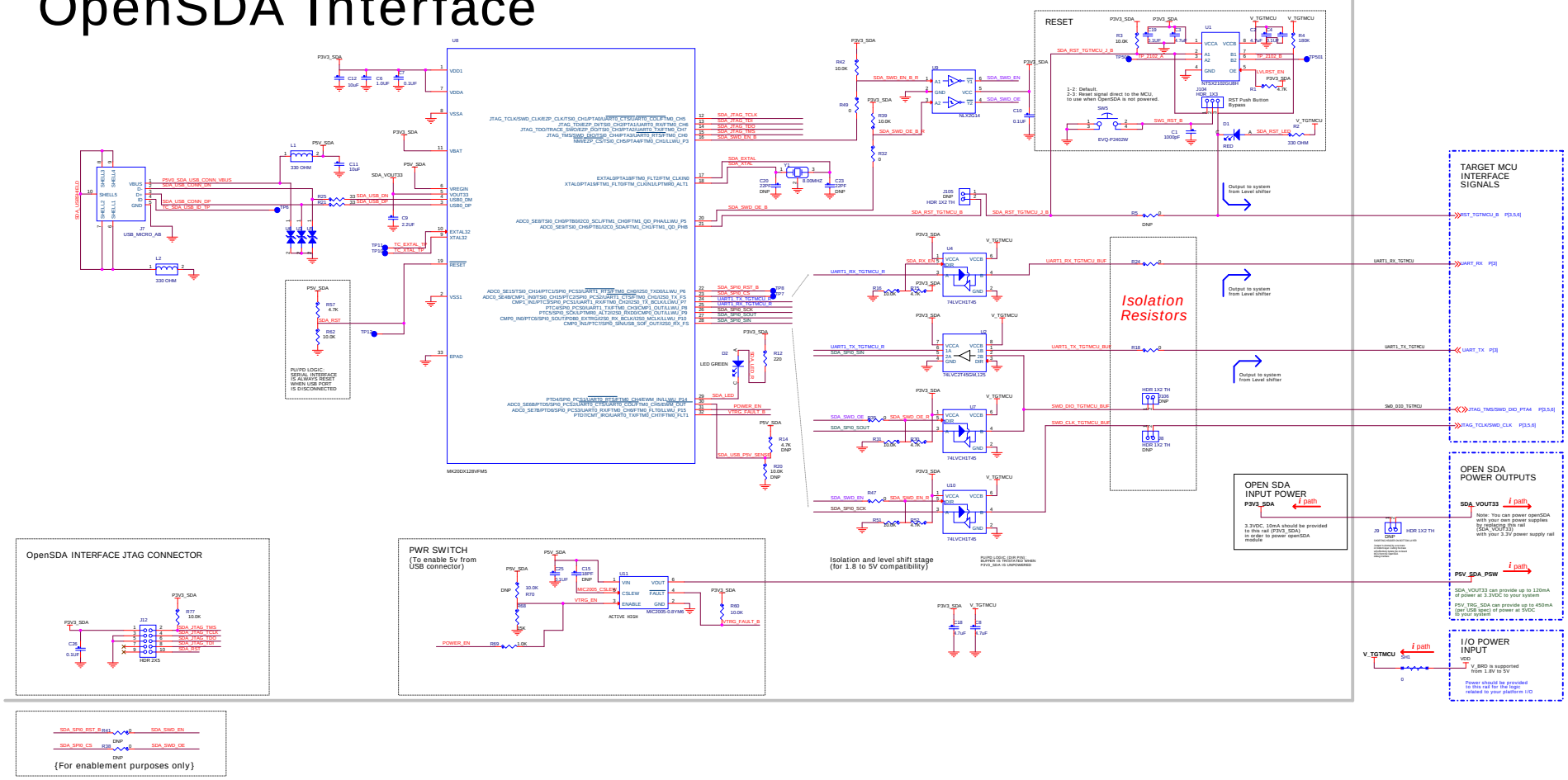
OpenSDA Interface



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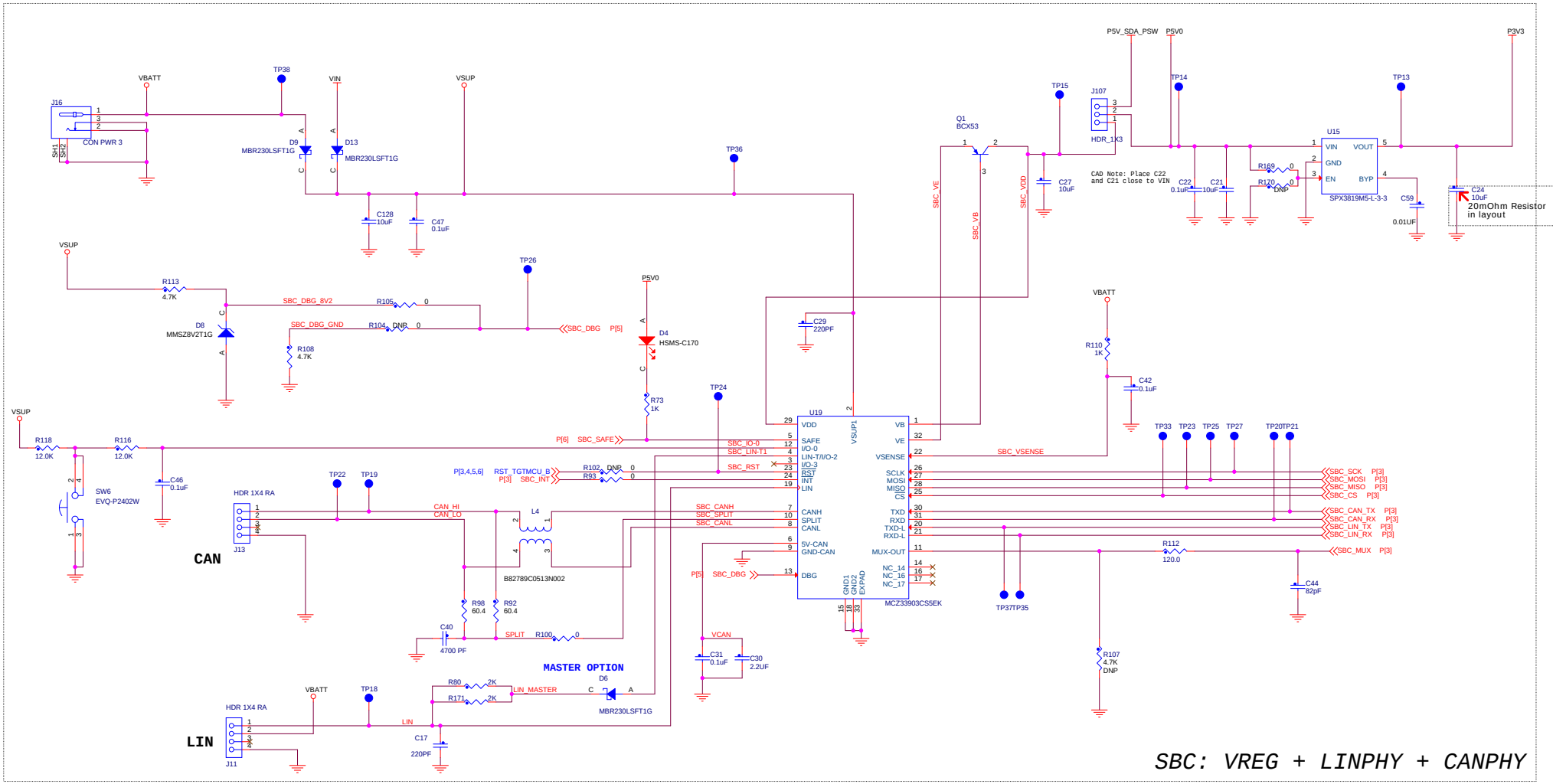

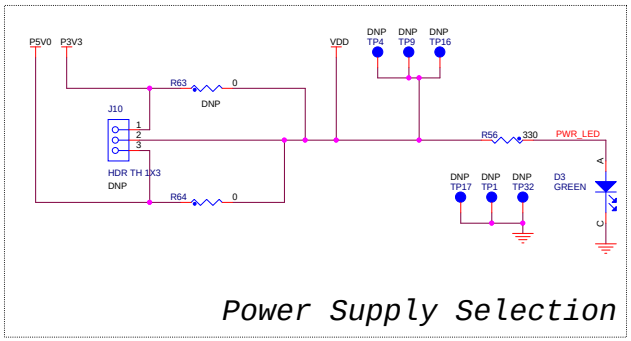

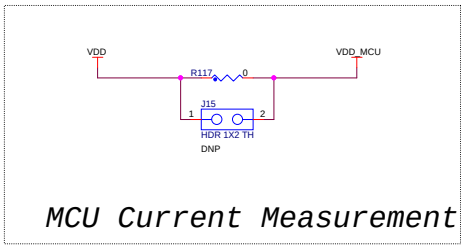

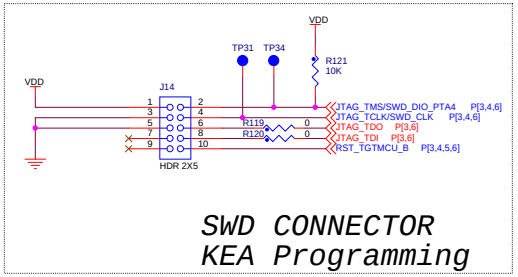

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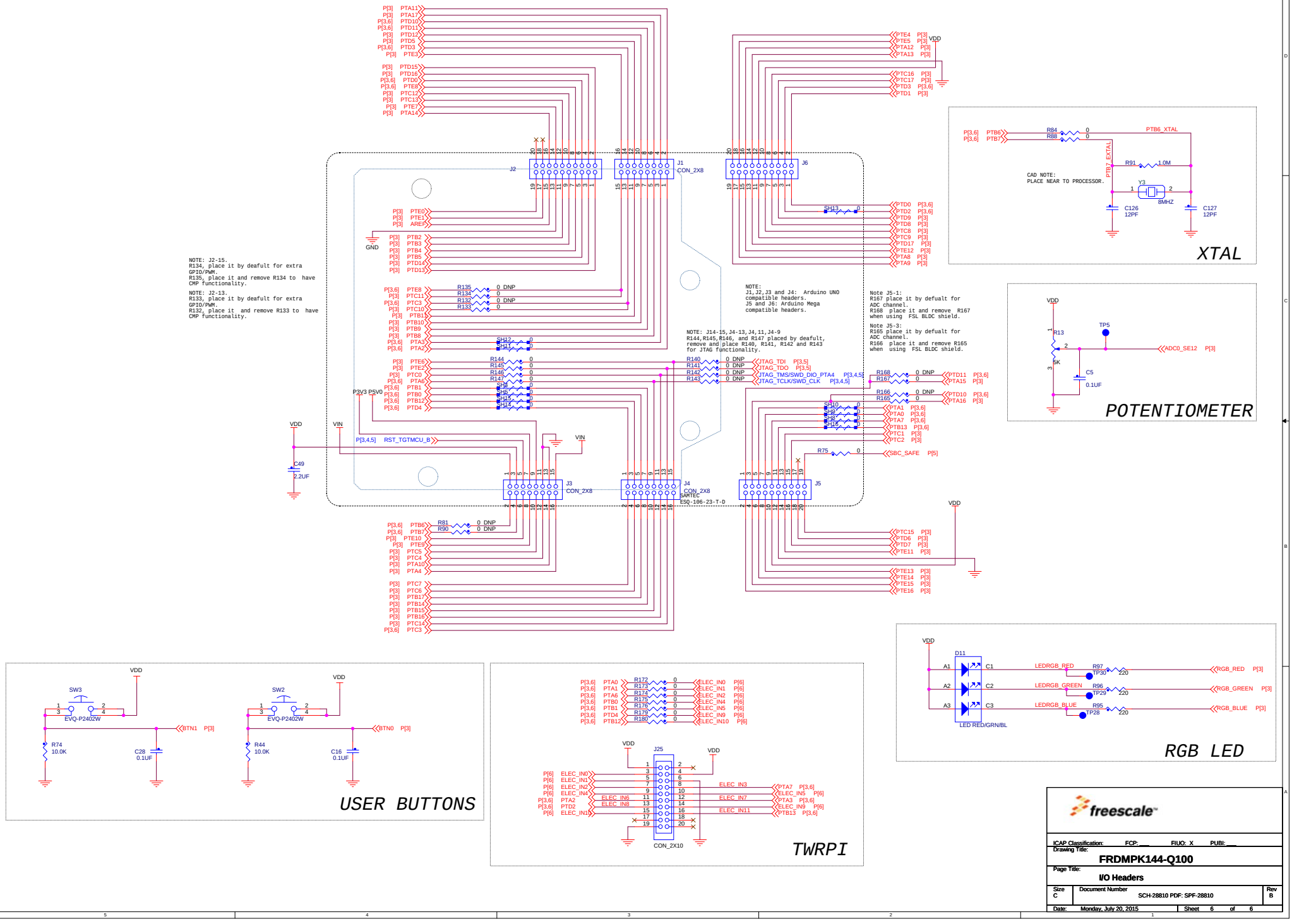

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Page Title: **I/O Headers**

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