ReTest 2 20/21

Tuesday, 19 December 2023 1:30 PM

Copy of RETEST_2...

School of Computing

UTM UNIVERSITI TEKNOLOGI MALAYSIA

RESEARCH UNIVERSITY

RETEST TEST 2 (PART B) SEMESTER I 2020/2021

COURSE CODE	:	**SECR1013 / SCSR1013**
COURSE TITLE	:	**DIGITAL LOGIC**
PROGRAM	:	**SECR/J/B/V/PH / SCSR/J/B/V/P**
DATE	:	**23 JANUARY 2021**

INSTRUCTIONS:

1. You must answer PART B with BLUE or BLACK ink pen/pencil handwritten on a piece of paper.

2. You are strictly prohibited to use any kinds of software to assist you. However, the use of calculator is permitted.

3. Make sure YOUR FULL NAME and YOUR SECTION is on every answer sheet. Use FULL NAME for FILENAME format. The questions are clearly NUMBERED in the answer sheet.

4. Only PDF is permitted to be uploaded to UTM e-learning.

5. You must stop answering at the end of 50 minutes and finish uploading answers during the extra 15 minutes.

6. Please upload your answers to UTM e-Learning before the end of Retest Test 2 time.
RETEST TEST 2: PART B SUBMISSION
Mr Firoz Section 01 06 08
Dr Nur Haliza Section 02 07 13
Ms Marina Section 03 04
Ms Rashidah Section 05 09
Dr Mohd Fo'ad Section 10
Dr Nor Shahida Section 15

Warning!
Students who are caught cheating during the examination will be reported to the disciplinary board for possible suspension of the student for one or two semesters.

This question booklet consists of 2 pages excluding the front page.

QUESTION 1 (9 MARKS)

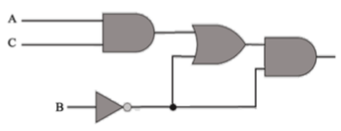
a) Simplify Boolean expression Z using Boolean Algebra simplification. Show all your workings. (5 marks)

$$Z = \overline{A\bar{C} + AB(B + \bar{C})}$$

b) Get simplified POS expression for $Y = \Pi_{ABCD}(1, 5, 8, 15, 10)$ and $d(0, 2, 4, 7, 11, 13, 14)$. Show all your workings. (4 marks)

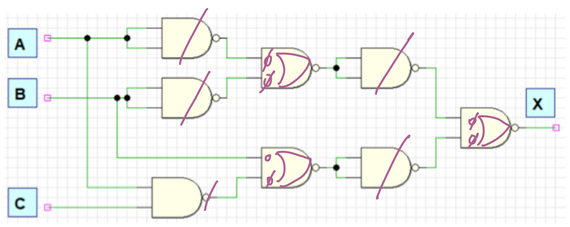
QUESTION 2 (8 MARKS)

a) Convert basic gate combinational logic circuit below by using 2-input Universal NAND gate only. (4 marks)



1 - not
2 - and
3 - or

b) Convert and simplify the following NAND universal circuit to basic gates (AND, OR, NOT) using dual symbol at ODD level. Show all your workings. (4 marks)



(a) $Z = \overline{A\bar{C}}\ \overline{AB(B+\bar{C})}$

$= (\bar{A}+C)(A\bar{B} + (\overline{B+\bar{C}}))$

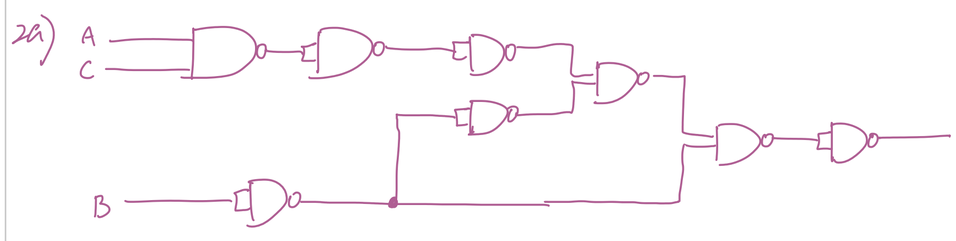
$= (\bar{A}+C)(\bar{A}+\bar{B} + B\bar{C})$

b)

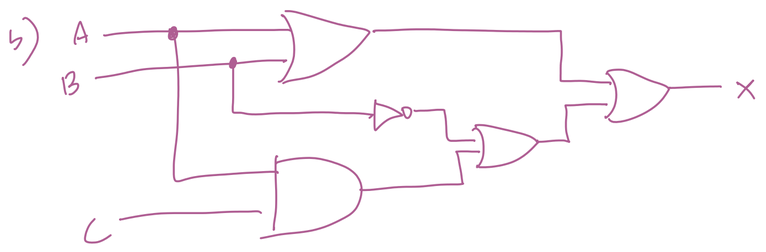
CD \ AB	00	01	11	10
00	X	0	1	X
01	X	0	X	1
11	1	X	0	X
10	0	1	X	0

POS $= (A+C)(B+D)(\bar{A}+\bar{C})$

2a)



b)



QUESTION 3 (13 MARKS)

Design a combinational logic circuit that has three inputs A, B, C and output F, G

Output F condition:
- For input 2, 3, 5, 7 : F will be HIGH only when majority of the inputs are HIGH otherwise F will be LOW
- F will be LOW for other inputs

2 high
3 high = high

Output G condition:
- For input 0, 1, 4, 6 : G will be HIGH only when majority of the inputs are LOW otherwise G will be LOW
- G will be INVALID for other inputs

2 low
3 low = high

a) Create the truth table for the combinational logic circuit.

b) Get simplified SOP expression for F and G using KMAP minimization.

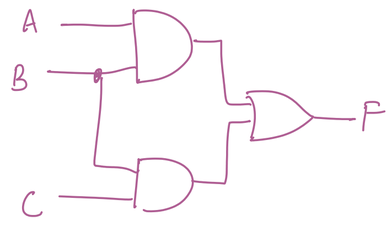
c) Draw output circuit for F and G using 2 input basic gates only (AND, OR, NOT).

	A	B	C	F	G
→ 0	0	0	0	0	1
→ 1	0	0	1	0	1
→ 2	0	1	0	0	X
→ 3	0	1	1	1	X
→ 4	1	0	0	0	1
→ 5	1	0	1	1	X
→ 6	1	1	0	0	0
→ 7	1	1	1	1	X

F:

AB \ C	0	1
00	0	0
01	0	1
11	0	1
10	0	1

SOP: $BC + A\bar{C}$



G:

AB \ C	0	1
00	1	1
01	X	X
11	0	X
10	1	X

SOP: $\bar{B}$