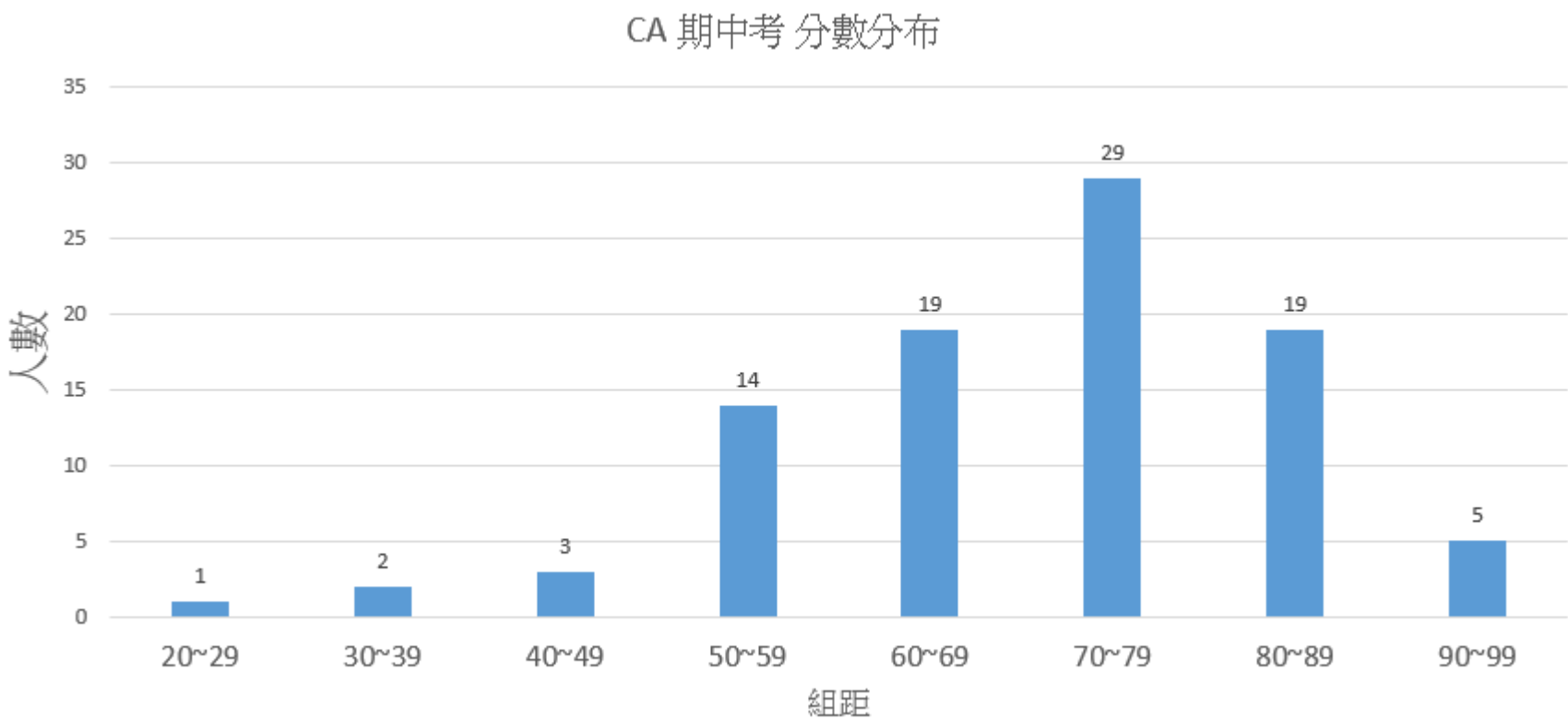
Computer Architecture 2018 Fall Midterm Exam Answer

平均: 70


CA 期中考 分數分布
人數
35
30
25
20
15
10
5
0
1
2
3
14
19
29
19
5
20~29
30~39
40~49
50~59
60~69
70~79
80~89
90~99
組距

1.1 [10 pts]

- Current CPU requires (num arithmetic * 1.2 cycle) + (num load/store * 10 cycles) + (num branch/jump * 3 cycles) = 600*1.2 + 300*10 + 100*3 = 4020 cycles.
- The new CPU requires (.75*num arithmetic * 1.2 cycle) + (num load/store * 10 cycles) + (num branch/jump * 3 cycles) = 450*1.2 + 300*10 + 100*3 = 3840 cycles.
- However, given that each of the new CPU's cycles is 10% longer than the original CPU's cycles, the new CPU's 3840 cycles will take as long as 4224 cycles on the original CPU.

1.2 [5pts]

- If we double the performance of arithmetic instructions by reducing their CPI to 0.6, then the CPU will run the reference program in (600*.6) + (300*10) + 100*3 = 3660 cycles. This represents a speedup of $\frac{4020}{3660} = 1.098$

Q1. 評分標準

- 公式正確就全拿
- 計算錯誤扣1~2分

2. [10pts]

- The UJ instruction format would be most appropriate because:

- Only need one register address
- It would allow the maximum number of bits possible for the “ loop ” parameter, thereby maximizing the utility of the instruction.

Q2. 評分標準

- 寫 U or UJ type 且提到上述原因就全拿 10%

3. [10pts]

```
int i;
for (i = 0; i < 100; i++) {
    result += *MemArray;
    MemArray++;
}
```

Q3. 評分標準

- 因為沒有明確告知 int 幾 bytes, result += *MemArray; 寫成下述也給對
  - result += MemArray[i];
  - result += MemArray[2*i];

- 過程錯誤一個地方 扣三分

4. [5pts]

```
slli   x28, x28, 3       // x28 = i*8
add x12, x10, x28   // x12 = x10 + x28
ld    x28, 0(x12)      // x28 = A[i]
Slli   x29, x29, 3      // x29 = j*8
add x13, x11, x29  // x13 = x11 + x29
ld     x29, 0(x13)     // x29 = B[j]
add x28, x28, x29  // Compute x28 = A[i] + B[j]
sd    x28, 64(x11)   // Store result in B[8]
```

Q4. 評分標準

- 正確 load A[i] & B[j] 拿 3%
- 正確 store 至B[8] 拿 2%
- 過程錯誤扣一分, 包含:
  - Element 8-byte word, 需使用 ld, sd (double word)
  - Assembly code 格式
  - Address offset

5. [5pts]

- The opcode would expand from 7 bits to 9.
- The rs1 , rs2 , and rd fields would increase from 5 bits to 7 bits.

Q5. 評分標準

- rs1 , rs2 , and rd fields 正確拿 3%
- Opcode fields 正確拿 2%

- 因為 instruction set expansion 沒說清楚是否僅R-type, 提及 Opcode or funct3 or funct7 fields expand from 7 bits to 9 也給對

6. [10pts]

sd	IF	ID	EX	MEM	WB								
ld		IF	ID	EX	MEM	WB							
sub			IF	ID	EX	MEM	WB						
beqz				**	**	IF	ID	EX	MEM	WB			
add							IF	ID	EX	MEM	WB		
sub								**	**	IF	ID	EX	MEM	WB

sd	IF	ID	EX	MEM	WB								
ld		IF	ID	EX	MEM	WB							
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add							IF	ID	EX	MEM	WB		
sub								IF	ID	EX	MEM	WB	

Q6. 評分標準

- beqz有stall: 4分
- stall次數正確: 3分

- add, sub的data hazard有處理: 3分

7. [10pts]

- Mem[Reg[rs1]]=Reg[rs2]+immediate

- There needs to be a path from read data 1 directly to Data memory's Address input.
- There needs to be a path from the ALU output to data memory's write data port.
- We need ALU input to be rs2 & imm.
- We need some additional muxes to drive the data paths and support both new and original instructions

Q7. 評分標準

- Mem[Reg[1]] 正確連接至 Mem address 拿5%
- ALU 正確 support Reg[2] + imm 拿5%

- 若直接額外加一個 Adder 來 support Reg[2] + imm 也給對
- 少 mux 元件 support 新舊指令扣2%
- 沒有連接control signal 或敘述 mux 選擇方式扣2%

- 直接用 signal 改動 register 跟 memory block 的 只有一半分數(除非有畫 block內配線修改)

8. [10pts]

- 8.1
- Pipelined: 350; non-pipelined: 1250

- 8.2
- Split the ID stage. This reduces the clock-cycle time to 300ps.

Q8. 評分標準

- 8.1 數字對才有5%
- 8.2 ID stage, 數字對才有5%

9. [15pts]

- 9.1 [5 pts]
- Speedup overall = $\frac{1}{((1-0.25-0.25-X)+\frac{0.25}{30}+\frac{0.25}{20}+\frac{x}{15})} = 10$
- X=45%

9. [15pts]

- 9.2 [5 pts]
- Un-enhanced portion = $(1 - 0.25 - 0.35 - 0.1) = 0.3$
- Enhanced portion = $\frac{0.25}{30} + \frac{0.35}{20} + \frac{0.1}{15} = 0.0325$
- $\%\ time\ of$ Un−enhanced after speedup = $\frac{0.3}{0.3+0.0325} = 90\%$

9. [15pts]

- 9.3 [5 pts]
- Speedup 1 = $\frac{1}{((1-0.15)+\frac{0.15}{30})} = 1.169$
- Speedup 2 = $\frac{1}{((1-0.15)+\frac{0.15}{20})} = 1.166$
- Speedup 3 = $\frac{1}{((1-0.7)+\frac{0.7}{15})} = 2.884$
- If only one enhancement can be implemented, use 3
- If two enhancements can be implemented, use 1 & 3

Q9. 評分標準

- 每題公式對就可以拿5%

10. [5pts]

- A rule stating that the performance enhancement possible with a given improvement is limited by the amount that the improved feature is used.

Amdahl's Law:

$$\text{Execution time after improvement} = \frac{\text{Execution time affected by improvement}}{\text{Amount of improvement}} + \text{Execution time unaffected}$$

Q10. 評分標準

- 寫出 **Amdahl’s Law** 拿 2.5%
- 寫出例子: 如 addi 拿 2.5%

11. [5pts]

- The benchmarks form a workload that the user hopes will predict the performance of the actual workload.
- Benchmarks provide a method of comparing the performance of various subsystems across different chip/system architectures.

Q11. 評分標準

- 提到 comparable, system evaluation 等 拿5%
- 大致正確 4%
- 有明顯瑕疵 2.5%