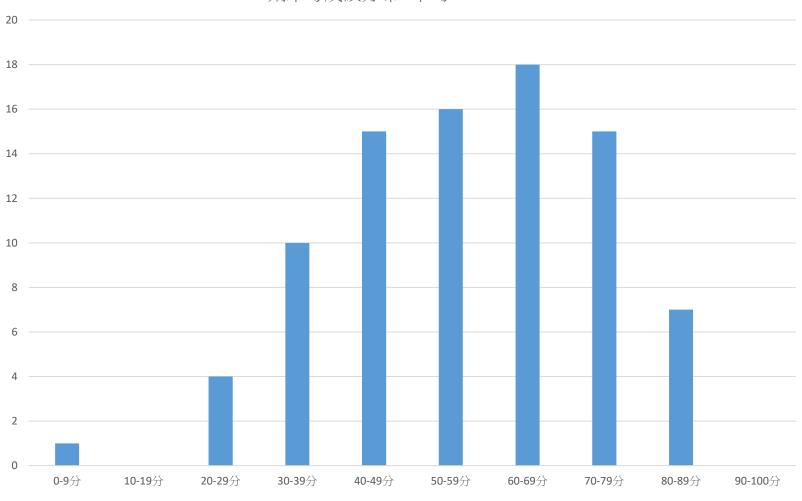
期末考成績分布 平均: 56.4



Q1(a) [10pts]

• 根據題目的限制,該題只有

sd x30, 0(x31)

addi x12, x12, 2

可以issue成一個packet,且

ld x29, 8(x6)

sub x30, x7, x29

之間需一個Stall. 按照上述兩點, 其餘的instructions被issue成一個packet, 或是有其他Stall會扣1~2分

- 需要執行2個iteration, 否則扣5分
- 同樣錯誤出現在兩個iteration不會重複扣分
- 若在這題有 rearrange code, 也會根據題目限制檢查能否被 issue 成一個 packet

Q1(a) [10pts]

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
li v12 0	IF	ID	EX	ME	WB	U	/	0	9	10	11	12	13	14	13	10	1 /	10	19	20	<i>Z</i> 1	ZZ	23	24	23
li x12, 0	IF			1																					
jal ENT		IF	ID	EX	ME	WB																			
bne x12, x13, TOP			IF	ID	EX	ΜE	WB																		
slli x5, x12, 3				IF	ID	EX	ΜE	WB																	
add x6, x10, x5					IF	ID	EX	ΜE	WB																
ld x7, 0(x6)						IF	ID	ΕX	ΜE	WB															
Id x29, 8(x6)							IF	ID	EX	ΜE	WB														
sub x30, x7, x29								**	IF	ID	EX	ΜE	WB												
add x31, x11, x5										IF	ID	EX	ME	WB											
sd x30, 0(x31)											IF	ID	EX	ME	WB										
addi x12 , x12, 2											IF	ID	EX	ΜE	WB										
bne x12, x13, TOP												IF	ID	EX	ΜE	WB									
slli x5 , x12, 3													IF	ID	EX	ΜE	WB								
add x6, x10, x5														IF	ID	EX	ΜE	WB							
ld x7, 0(x6)															IF	ID	EX	ΜE	WB						
ld x29, 8(x6)																IF	ID	ΕX	ΜE	WB					
sub x30, x7, x29																	**	IF	ID	EX	ΜE	WB			
add x31, x11, x5																			IF	ID	EX	ΜE	WB		
sd x30, 0(x31)																				IF	ID	EX	ΜE	WB	
addi x12 , x12, 2																				IF	ID	EX	ΜE	WB	
bne x12, x13, TOP																					IF	ID	EX	ΜE	WB

Q1(b) [10pts]

• 若有提早判斷是否要進入迴圈,或是讓迴圈每次執行的cycle數減少(避免stall, pointer-based approach)都可以拿全部分數,修改後的code每發現一個bug扣1分

```
    Possible Solution:
        bez x13, DONE
        li x12, 0
        jal ENT
    TOP:
        ld x7, 0(x10)
        ld x29, 8(x10)
        addi x12, x12, 2
        sub x30, x7, x29
        sd x30, 0(x11)
        addi x10, x10, 16
        addi x11, x11, 16
    ENT:
        bne x12,x13,TOP
    DONE:
```

Q1(c) [10pts]

• 此題需要將迴圈unroll成一次處理兩組結果, 即 for(i=0;i!=j;i+=4)

```
b[i]=a[i]–a[i+1];
b[i+2]=a[i+2]–a[i+3];
```

- 若沒有unroll則扣5分
- •讓迴圈每次執行的cycle數減少(避免stall, issue packet, pointerbased approach)都可以拿全部分數, 修改後的code每發現一個bug 扣1分

Q1(c) [10pts]

```
• Possible Solution:
      beqz x13, DONE
     li x12, 0
      addi x6, x10, 0
TOP:
      1d x7, 0(x6)
      add x31, x11, x5
      ld x29, 8(x6)
      addi x12, x12, 4
     ld x16, 16(x6)
      slli x5, x12, 3
      ld x15, 24(x6)
      sub x30, x7, x29
      sd x30, 0(x31)
      sub x14, x16, x15
      sd x14, 16(x31)
      add x6, x10, x5
      bne x12,x13,TOP
```

DONE:

Q2 [10pts]

• Predict Result

Total: 25	Always taken	1-bit predictor	2-bit predictor	
Branch 1: T-T-T	T-T-T	T-T-T	T-T-T	
Branch 2: N-N-N-N	T-T-T-T	T-N-N-N	T-T-N-N	
Branch 3: T-N-T-N-T-N	T-T-T-T-T	T-T-N-T-N-T	T-T-T-T-T	
Branch 4: T-T-T-N-T	T-T-T-T	T-T-T-N	T-T-T-T	
Branch 5: T-T-N-T-N-T	T-T-T-T-T-T	T-T-T-N-T-T-N	T-T-T-T-T-T	

Q3 [10pts]

- Each cycle on a 2- Ghz machine takes 0.5 ps. Thus, a main memory access requires 100/0.5 = 200 cycles
- Direct mapped L2 AMAT: $1.5 + .07 \times (12 + 0.035 \times 200) = 2.83$
- 1.5 + 0.07*(50 + x*200) < 2.83
- x 解不合(Miss Rate < 0)
- 故該L2 cache不論多大performance都較差
- 寫出兩方的AMAT算式各3分
- x 的解答4分

Q4 [10pts]

• 該題一共10個Entry (6個Address, 4個TLB) 每個Entry各1分

• 4KB pages → 12bits offset

Address	Bin	Hex	Virtual Page
4522	1000110101010	11AA	1
2044	0011111111100	07FC	0
13225	11001110101001	33A9	3
29890	111010011000010	74C2	7
9094	10001110000110	2386	2
6666	1101000001010	1A0A	1

		TLB and Page	1	TLB			
Address	Virtual page	-	Valid		Dhariadaa		
		Hit/Miss		Tag	Physical page		
4522	1	TLB miss	1 (last access 2)	4	10		
		Page Hit	1 (last access 1)	7	8 7		
			1 (last access 0)	3	 		
		TID and Dane	1 (last access 3)	1	11		
Address	Virtual page	TLB and Page		TLB			
	111 110	Hit/Miss	Valid	Tag	Physical page		
2044	0	TLB miss	1 (last access 2)	4	10		
		Page Miss	1 (last access 1)	7	8		
		· ·	1 (last access 4)	0	14		
			1 (last access 3)	1	11		
Address	Virtual page	TLB and Page	TLB				
Address	Vii tuai page	Hit/Miss	Valid	Tag	Physical page		
13225	3	TLB miss	1 (last access 2)	4	10		
		Page Hit	1 (last access 5)	3	7		
			1 (last access 4)	0	14		
			1 (last access 3)	1	11		
Address	Virtual page	TLB and Page		TLB			
Address	Vii taai page	Hit/Miss	Valid	Tag	Physical page		
29890	7	TLB miss	1 (last access 6)	7	8		
		Page Hit	1 (last access 5)	3	7		
		- 0 -	1 (last access 4)	0	14		
			1 (last access 3)	1	11		
Address	Virtual page	TLB and Page		TLB			
Audress	Vii tuai page	Hit/Miss	Valid	Tag	Physical page		
9094	2	TLB miss	1 (last access 6)	7	8		
303.		Page Hit	1 (last access 5)	3	7		
		1 480 1110	1 (last access 4)	0	14		
			1 (last access 7)	2	3		
Address	Virtual page	TLB and Page		TLB			
Address	Virtual page	Hit/Miss	Valid	Tag	Physical page		
6666	1	TLB miss	1 (last access 6)	7	8		
		Page Hit	1 (last access 5)	3	7		
			1 (last access 8)	1	11		
			1 (last access 7)	2	3		

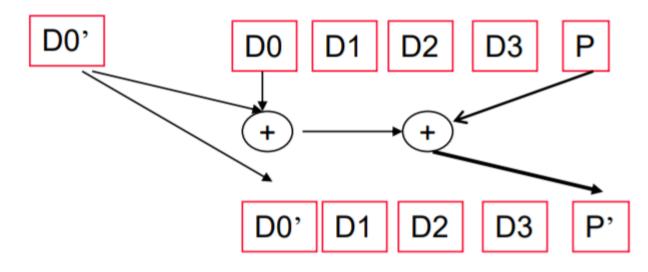
Q5(a) [5pts]

• System A: 20 TB

• System B: 12.5 TB

Q5(b) [5pts]

- 須System A, B都寫對才給分
- System A: The data needs to be written in two locations
 - 60ms
- System B: The system calculates parity and writes that parity, in summary this disk actions that must be done:
 - 1. Read the old data
 - 2. Read the old parity
 - 3. Write the new data
 - 4. Write the new parity
 - 120ms



Q6(a) [5pts]

- 超過3個cycle則沒分
- Possible Solution:

Cycle 1 Cycle 2

Cycle 2 Cycle 3

	Core 1	Core 2			
FU1	FU2	FU1	FU2		
A1		B2	B4		
A3	A2	B1	В3		
	A4				

Q6(b) [5pts]

- 超過7個cycle則沒分
- 題目為 Fine-grained multithreaded processor, 需要Switch threads after each cycle.
- 此外須注意題目沒有說 provides out-of-order issue capabilities
- Possible Solution:

Cycle 1 A1	
Cycle 2 B1	
Cycle 3 A3 A2	
Cycle 4 B2	
Cycle 5 A4	
Cycle 6 B3	
Cycle 7 B4	

Q6(c) [5pts]

- 超過6個cycle則沒分
- 須注意題目沒有說 provides out-of-order issue capabilities
- Possible Solution:

	FU1	FU2
Cycle 1	A1	
Cycle 2	B1	A2
Cycle 3	B2	
Cycle 4	A3	В3
Cycle 5		A4
Cycle 1 Cycle 2 Cycle 3 Cycle 4 Cycle 5 Cycle 6		B4

Q7 [5pts]

- 寫出其中一點給3分, 兩點給5分, 其他答案會斟酌決定要不要給分
- 第一點若拆成兩點來寫也只有3分

Fundamental Architectural Differences between CPU & GPU

- Multi-core CPU
 - Coarse-grain, heavyweight threads
 - Memory latency is resolved though large on-chip caches & out-of-order execution
- Modern GPU
 - Fine-grain, lightweight threads
 - Exploit thread-level parallelism for hiding latency

Q8 [10pts]

• 須說明 Prefetching 會改變 Bandwidth ceilings 的效果,只說明該 Intensity 為 Computation Bound 只有5分

