Biographical Data

Andrew B. Kahng (b. Oct. 1963, San Diego, CA) received the A.B. degree in applied mathematics (physics) from Harvard College, and from June 1983 to June 1986 was affiliated with Burroughs Corporation Micro Components Group in San Diego, where he worked in device physics, circuit simulation, and CAD for VLSI layout. He received the M.S. and Ph.D. degrees in computer science from the University of California at San Diego. He joined the UCLA computer science department as an assistant professor in July 1989, and became associate professor in July 1994 and full professor (at age 34) in July 1998. From April 1996 through September 1997, he was on sabbatical leave and leave of absence from UCLA, as Visiting Scientist at Cadence Design Systems, Inc. He resumed his duties at UCLA in Fall 1997, and from July 1998 to September 2000 served as the computer science department's vice-chair for graduate studies. Effective January 1, 2001 Professor Kahng joined UCSD as Professor in the CSE and ECE Departments. He served as Associate Chair of the UCSD CSE Department from 2003-2004. In October 2004, Professor Kahng co-founded Blaze DFM, Inc., an EDA software company that delivered new cost and yield optimizations at the IC design-manufacturing interface. He served as CTO of the company during a two-year leave of absence, returning to the university full-time in September 2006. The Blaze DFM core technology is responsible for substantial leakage power and total power reductions in such high-volume products as AMD/ATI Radeon graphics processor chips, and starting in ~2008 was embodied in the TSMC Power Trim Service that enables low integrated-circuit power consumption and green products.

Professor Kahng is the author of 3 books and 400+ journal and conference papers. He holds 33 issued U. S. patents. His 26 Ph.D. graduates (Robins, Hagen, Boese, Alpert, Tsao, Muddu, Huang, Masuko, Markov, Liu, Chen, Mantik, Xu, Wang, Reda, Gupta, Sharma, Muddu, Park, Topaloglu, Samadi, Jeong, Kang, Chan, Nath, Li) have gone on to notable successes in both academia and industry. He has received NSF Research Initiation and Young Investigator awards, 18 Best Paper nominations and 6 Best Paper awards (DAC, ISQED (2), ICCD, ASP-DAC/VLSI Design, and BACUS), and is a Fellow of both IEEE and ACM. He was the founding general chair of the 1997 ACM/IEEE International Symposium on Physical Design, founding co-general chair of the ACM Workshop on System-Level Interconnect Prediction, and has served as general chair of the Design Automation Conference, the International Symposium on Quality Electronic Design, and the Electronic Design Processes Workshop. He served on the EDA Council's EDA 200X task force, which produced this report, and has provided analyses of worldwide research funding gaps for the SRC's CADTS and ICSS science areas since 2001. He defined the physical design roadmap as a member of the Design Tools and Test technology working group (TWG) for the 1997-1999 renewals of the International Technology Roadmap for Semiconductors (ITRS), and since 2000 has served as Chair or Co-Chair of the U.S. Design Technology Working Group, and of the Design International Technology Working Group, for the ITRS (with responsibility for the Design Chapter, the System Drivers Chapter, the associated tables, and the models of maximum on-chip frequency, layout density, and defect density in the Overall Roadmap Technology Characteristics). More recently, he chaired the ITRS2.0 System Integration Focus Team (2014-2015), and currently chairs the Systems and Architectures Focus Team in the new International Roadmap for Devices and Systems, which is the successor to the ITRS.

Professor Kahng has served on the editorial boards of *IEEE Transactions on VLSI*, *IEEE Transactions on Circuits and Systems I*, *IEEE Design and Test* (where he contributes the regular column, "The Road Ahead"), and the Research Highlights section of *Communications of the ACM*. He was a member of the executive committee of the MARCO Gigascale Systems Research Center throughout the center's 15-year span (1998-2013). Professor Kahng's research interests include the VLSI design-manufacturing interface, VLSI physical layout design and performance analysis, combinatorial and graph algorithms, and stochastic global optimization.

Selected Honors

- National Science Foundation Young Investigator Award, 1992
- National Science Foundation Research Initiation Award, 1991
- First Place Award, Placement Contest (ACM International Symposium on Physical Design 2005)
- 14 Best Paper Nominations (ACM/IEEE Design Automation Conference 1992, 1994, 2012; European Design Automation Conference 1992, 1994; Asia South-Pacific Design Automation Conference 1999, 1999, 2002; IEEE ISQED 2001, 2007; SPIE BACUS Symposium 2005; IEEE International Conference on Computer Design 2005; IEEE International Conference on Computer-Aided Design 2005,2008)
- Distinguished Paper Award (IEEE International Conference on CAD 1990)
- 6 Best Paper Awards (ACM/IEEE Design Automation Conference 1994, IEEE International Symposium on Quality in Electronic Design 2001, Joint Asia and South Pacific Design Automation Conference and International Conference on VLSI Design 2002, IEEE International Conference on Computer Design 2005, SPIE BACUS Symposium 2005, IEEE International Symposium on Quality in Electronic Design 2007)
- IEEE Fellow, 2010
- ACM Fellow, 2012

Selected Professional Activities

- International Technology Roadmap for Semiconductors. U.S. Design Technology Working Group and International Design Technology Working Group. Chair, 2000-2004. Co-Chair, 2005-present.
- ACM/EDAC/IEEE Design Automation Conference. Technical Program Committee member and session organizer, 1995-2001. Panels Committee member, 1998-2002; 2011. Technical Program Committee Co-Chair, 2004-2005. New Initiatives Chair, 2006. Panels Chair, 2007. Vice Chair and Finance Chair, 2008. General Chair, 2009. Past Chair, 2010.
- ACM/IEEE International Symposium on Physical Design. Founding General Chair, 1997. Steering Committee, 2001.
- IEEE DATC Electronic Design Processes Workshop. Technical Program Chair, 2001. General Chair, 2002.
- ACM International Workshop on System-Level Interconnect Prediction. Founding General Co-Chair, 1999. Technical Program Co-Chair, 2000. Special Sessions Chair, 2001. Steering Committee and other roles, 2001-present.
- Associate Editor, *IEEE Transactions on VLSI Systems*, 2003-2004.

- Associate Editor, *IEEE Transactions on Circuits and Systems I*, 2001-2003.
- Guest Co-Editor, Special Issue on Big Chips, *IEEE MICRO*, July-August 2011.
- Guest Co-Editor, Special Issue on Roadmaps and Visions for Design and Test, *IEEE Design and Test* , November-December 2001.
- Guest Co-Editor, Special Issue on System-Level Interconnect Prediction, *IEEE Trans. on VLSI Systems* , 2000.
- Guest Co-Editor, Special Issue on Physical Design, *IEEE Trans. on CAD*, April 1998.
- Member, Design and Test Working Group (with responsibility for Physical Design), 1997 and 1999 renewals, Semiconductor Industry Association *National Technology Roadmap for Semiconductors*.
- Invited Session Organizer and Chair, INFORMS Annual Meeting, May 1997.
- Technical Program Committee, Asia-Pacific Conference on Circuits and Systems, November 1996.
- Associate Chair, VLSI Track; Panelist, CAD Track; Session Organizer and Chair (Meta-heuristics in VLSI Layout), IEEE International Symposium on Circuits and Systems, May 1996.
- Technical Committee, 3rd Canadian Workshop on Field-Programmable Devices, April 1996.
- Tutorial Organizer/Presenter, ACM/IEEE Design Automation Conference, June 1994, June 1999 and June 2002; IEEE ICCAD November 1999 and November 2000; IEEE ASIC September 1998; IEEE ISQED March 2000 and March 2001.
- Technical Committee, European Design Automation Conf., Paris, February 1994.
- Technical Program Committee, Session Chair and Co-Chair, IEEE Intl. Conf. on Computer-Aided Design, Santa Clara, CA, November 1993, November 1994, November 1995, November 1998, November 2000.
- *Computer Science Fellowship Panel* (one of five members), National Defense Science and Engineering Graduate Fellowship Program, Feb. 1993.
- Technical Program Committee, Session Chair, 4th ACM/SIGDA Physical Design Workshop, Lake Arrowhead, CA April 1993. Technical Program Committee Chair, 5th ACM/SIGDA Physical Design Workshop, Reston, VA April 1996.
- *Expert Panel on Electromagnetic Detection* (organized by U.S. Army Research Office), Research Triangle Park, NC, June 23-26, 1992.
- Technical Program Committee (Sub-Committee Chair), Session Chair and Co-Chair, 5th and 6th IEEE Intl. Conf. on Application-Specific Integrated Circuits, Rochester, NY, September 1992 and September 1993 (also Session Chair and Co-Chair at 4th ASIC Conf. in 1991).
- Board of Editors, {\em J. Graph Algorithms and Applications} and *Intl. J. of High Speed Electronics and Systems*.
- Ph.D. advisor for Gabriel Robins (IBM Fellowship, ACM Outstanding Dissertation Award Nominee, NSF YI Award, Packard Fellowship, Munster Chair, now at Univ. of Virginia CS Dept.); Lars Hagen (IBM Fellowship, now at Cadence Design Systems, Inc.); Kenneth D. Boese (GTE Fellowship, MICRO Fellowship, UCLA Dissertation Year Fellowship, ACM Outstanding Dissertation Award Nominee, now at Cadence Design Systems, Inc.); Charles J. Alpert (DAC Scholarship, UCLA Dissertation Year Fellowship, ACM Outstanding Dissertation Award Nominee, now at IBM Austin Research Laboratory); Sudhakar Muddu (now at Sanera Systems, Inc.); Chung-Wen Albert Tsao (DAC Scholarship, now at Cadence Design Systems, Inc. (via Silicon Perspective Corp.)); Dennis Jen-Hsin Huang (now at Cadence Design Systems, Inc. (via Silicon Perspective, Inc.)); Kei Masuko; Igor L. Markov (now Professor at Univ. of Michigan

EECS Dept.); Bao Liu (now Assistant Professor at Univ. of Texas at San Antonio); Yu Chen (now at Cadence Design Systems, Inc.); Stefanus Mantik (now at Cadence Design Systems, Inc.) Xu Xu (now at Synopsys); Sherief Reda (now Associate Professor at Brown University); Qinke Wang (now at Synopsys); Puneet Gupta (EDAA Outstanding Dissertation Award, now Associate Professor at UCLA EE Department); Chul-Hong Park (now at Samsung Electronics Corp.); Puneet Sharma (now at Synopsys), Rasit Topaloglu (now at IBM Corp.); Swamy Muddu (now at Qualcomm); Kambiz Samadi (now at Qualcomm); Kwangok Jeong (EDAA Outstanding Dissertation Award, now at Samsung Electronics Corp.); Tuck-Boon Chan (now at Qualcomm).

- Reviewer for NSF, ARO, UC MICRO, numerous journals/conferences/symposia.

Miscellaneous Old Talks (beyond those under the TALKS link)

- "Roadmaps Toward a Science of VLSI Design", **invited plenary talk**, May 13, 1996, VLSI CAD Track, IEEE Intl. Symposium on Circuits and Systems, Atlanta, May 1996.
- "Futures and Core Algorithm Technologies for Physical Design", **Distinguished Lecture Series**, June 19, 1997, Cadence Design Systems, Inc, San Jose CA.
- Futures for DSM Physical Implementation: Where is the Value, and Who Will Pay?", **keynote address** , July 12, 2000, 12th Japan DA Show, Tokyo.
- Design Technology Productivity in the DSM Era, **invited talk** , February 2, 2001, Asia South-Pacific Design Automation Conference, Yokohama.