Integrated Transceiver Modules for WLAN 802.11 b/g/n, Bluetooth.

FEATURES

- IEEE 802.11 b,g,n,d,e,i, compliant.
- Typical WLAN Transmit Power:
  - 20.0 dBm, 11 Mbps, CCK (b).
  - 14.5 dBm, 54 Mbps, OFDM (g).
  - 12.5 dBm, 65 Mbps, OFDM (n).
- Bluetooth 2.1+EDR, Power Class 1.5.
- Typical WLAN Sensitivity:
  - - 89 dBm, 8% PER,11 Mbps.
  - -76 dBm, 10% PER, 54 Mbps.
  - - 73 dBm, 10% PER, 65 Mbps.
- Miniature footprint: 18 mm x 13 mm
- Low height profile: 1.9 mm.
- U.FL connector for external antenna.
- Terminal for PCB/Chip antenna feeds.
- Integrated band-pass filter
- Worldwide acceptance: FCC (USA), IC (Canada), and ETSI (Europe)
- Compact design based on Texas Instruments WL1271WSP Transceiver.
- Seamless integration with TI OMAP™ application processor.
- SDIO Host data path interfaces.
- Bluetooth Advanced Audio Interfaces
- Low power operation mode.
- RoHS compliant
- Streamlined development with LSR design services.

APPLICATIONS

- Security
- HVAC Control , Smart Energy
- Sensor Networks
- Medical

DESCRIPTION

The TiWi-R2 module is a high performance 2.4 GHz IEEE 802.11 b/g/n Bluetooth 2.1+EDR radio in a cost effective, pre-certified footprint.

The module realizes the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.

The module also provides a Bluetooth platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port.

Need to get to market quickly? Not an expert in 802.11. or Bluetooth? Need a custom antenna? Would you like to own the design? Would you like a custom design? Not quite what you need? Do you need help with your host board? LS Research Design Services will be happy to develop custom hardware or software, integrate the design, or license the design so you can manufacture yourself. Contact us at sales@lsr.com or call us at 262-375-4400.

ORDERING INFORMATION

Order Number	Description
450-0037	TiWi-R2 Module with U.FL connector for external antenna

Table 1: Orderable TiWi-R2 Model Numbers

MODULE ACCESSORIES

	Order Number	Description
	**001-0001**	2.4 GHz Dipole Antenna with Reverse Polarity SMA Connector
	**080-0001**	u.fl to Reverse Polarity SMA Bulkhead Cable 105mm

BLOCK DIAGRAM

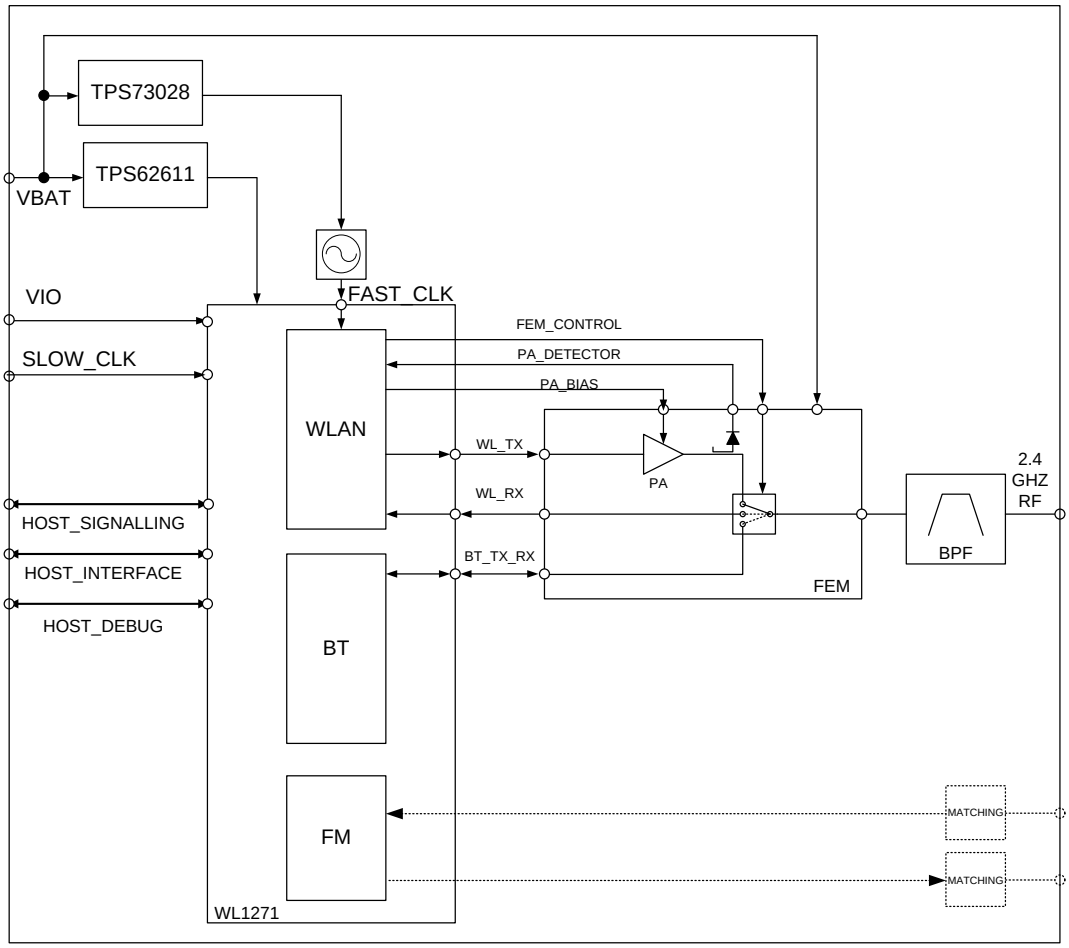


Figure 1: TiWi-R2 Module Block Diagram – Top-Level

TABLE OF CONTENTS

TIWI-R2 MODULE FOOTPRINT AND PIN DEFINITIONS

To apply the TiWi-R2 module, it is important to use the module pins in your application as they are designated in below and in the corresponding pin definition table found on pages 7 and 8. Not all the pins on the TiWi-R2 module may be used, as some are reserved for future functionality.

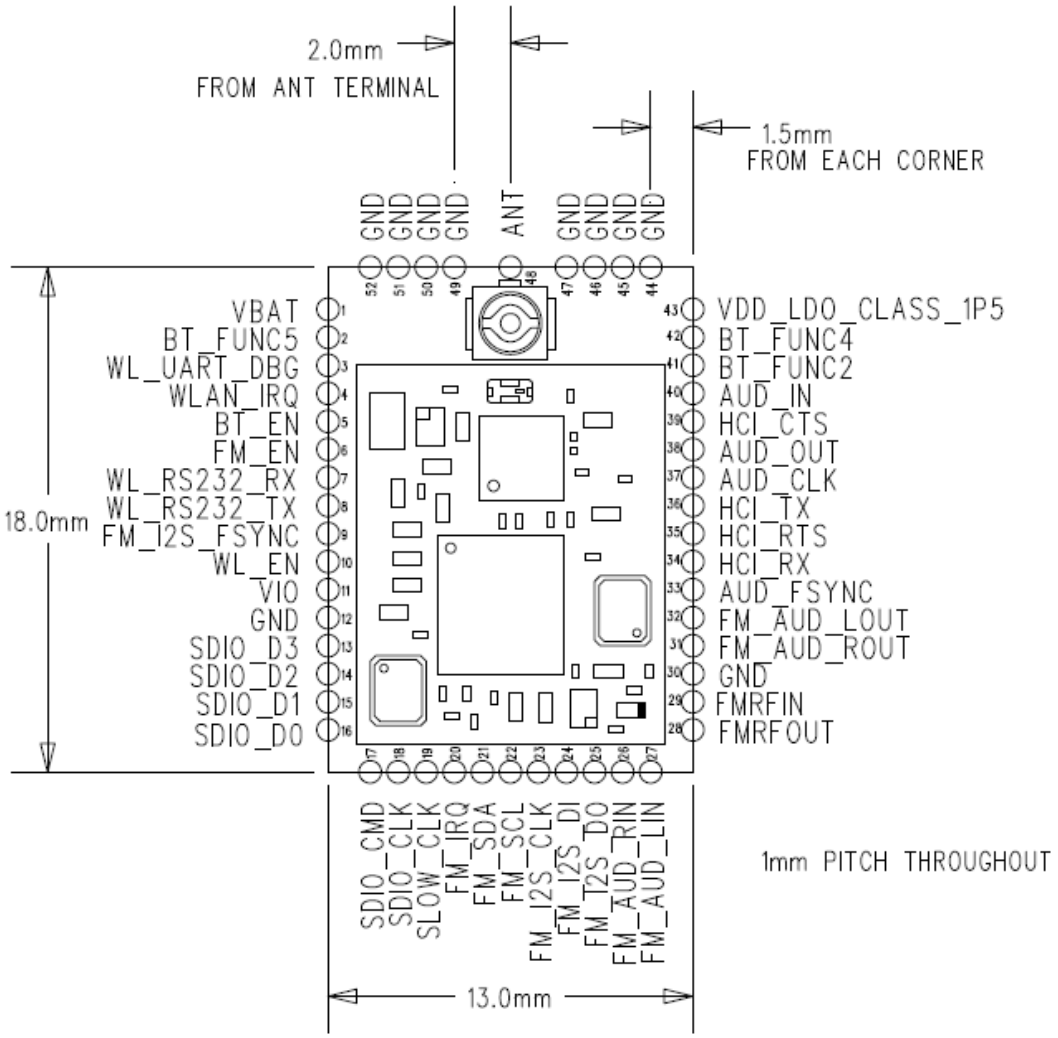


Figure 2: TiWi-R2 Pinout

PIN DESCRIPTIONS

Module Pin	Name	I/O Type	Buffer Type	Description [termination if FM not used]
1	VBAT	PI	-	Battery Voltage 3.6 VDC Nominal (3.0-4.8 VDC)
2	BT_FUNC5	DO	4 mA	HOST_WU (*)
3	WL_UART_DBG	DIO	4 mA	WL_UART_DBG
4	WLAN_IRQ	DO	4 mA	WLAN Interrupt Request
5	BT_EN	DI	-	BT_RST
6	FM_EN	DI	-	FM_RST [GND]
7	WL_RS232_RX	DI	-	WLAN TEST UART RX (*)
8	WL_RW_232_TX	DO	4 mA	WLAN TEST UART TX (*)
9	FM_I2S_FSYNC	DO	4 mA	FM_I2S_IF [NC, OPEN] (*)
10	WL_EN	DI	-	WL_RST
11	VIO	PI	-	POWER SUPPLY FOR 1.8 VDC DIGITAL DOMAIN
12	GND	GND	-	Ground
13	SDIO_D3	DIO	8 mA	SDIO INTERFACE, HOST PULL UP
14	SDIO_D2	DIO	8 mA	SDIO INTERFACE, HOST PULL UP
15	SDIO_D1	DIO	8 mA	SDIO INTERFACE, HOST PULL UP
16	SDIO_D0	DIO	8 mA	SDIO INTERFACE, HOST PULL UP
17	SDIO_CMD	DIO	8 mA	HOST PULL UP
18	SDIO_CLK	DI	-	HOST PULL UP
19	SLOW_CLK	DI	-	SLEEP CLOCK (32 kHz), 1.8 VDC DIGITAL DOMAIN
20	FM_IRQ	DO	4 mA	FM_I2C_IF [NC, OPEN] (*)
21	FM_SDA	DO	4 mA	FM_I2C_IF [NC, OPEN] (*)
22	FM_SCL	DO	4 mA	FM_I2C_IF [NC, OPEN] (*)
23	FM_I2S_CLK	DO	4 mA	FM_I2C_IF [NC, OPEN] (*)
24	FM_I2S_DI	DI	4 mA	FM_I2C_IF [GND]
25	FM_I2S_DO	DO	4 mA	FM_I2C_IF [NC, OPEN] (*)
26	FM_AUD_RIN	AI	-	FM_AUD_RIN [GND]
27	FM_AUD_LIN	AI	-	FM_AUD_LIN[GND]
28	FMRFOUT	AO	-	FMRFOUT [NC, OPEN]
29	FMRFIN	AI	-	FMRFIN [GND]
30	GND	GND	-	Ground
31	FM_AUD_ROUT	AO	-	FM_AUD_ROUT [NC, OPEN]

Module Pin	Name	I/O Type	Buffer Type	Description [termination if FM not used]
32	FM_AUD_LOUT	AO	-	FM_AUD_LOUT [NC,OPEN]
33	AUD_FSYNC	DIO	4 mA	PCM I/F or FM_I2S_FSYNC
34	HCI_RX	DI	8 mA	BT UART (*)
35	HCI_RTS	DO	4 mA	BT UART (*)
36	HCI_TX	DIO	8 mA	BT UART
37	AUD_CLK	DO	4 mA	PCM I/F or FM_I2S_CLK (*)
38	AUD_OUT	DO	4 mA	PCM I/F or FM_I2S_DO (*)
39	HCI_CTS	DI	4 mA	BT UART (*)
40	AUD_IN	DI	4 mA	PCM I/F or FM_I2S_DI (*)
41	BT_FUNC2	DI	4 mA	BT WU/ DC2DC mode (*)
42	BT_FUNC4	DO	4 mA	BT_UARTD (DEBUG) (*)
43	VDD_LDO_CLASS_1P5	NC	-	VBAT VOLTAGE PRESENT, NO CONNECT
44	GND	GND	-	Ground
45	GND	GND	-	Ground
46	GND	GND	-	Ground
47	GND	GND	-	Ground
48	ANT	RF		Antenna terminal for WLAN and Bluetooth (note [1])
49	GND	GND	-	Ground
50	GND	GND	-	Ground
51	GND	GND	-	Ground
52	GND	GND	-	Ground

PI = Power Input
PO = Power Output
DI = Digital Input
DO = Digital Output
AI = Analog Input
AO=Analog Output
AIO = Bi-directional Analog Port
RF = Bi-directional RF Port
GND=Ground
Note[1]: Antenna terminal presents d.c. short circuit to ground.

(*) indicates that pin is capable of bidirectional operation, but is used as the type shown.

Table 2: TiWi-R2 Module Pin Descriptions

ELECTRICAL SPECIFICATIONS

The majority of these characteristics are based on controlling and conditioning the tests using the evaluation kit and TiWi-R2 control software application. Other control conditions may require these values to be re-characterized by the customer.

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power supply voltage (VBAT)	-0.5	+5.5	V
Digital supply voltage (VIO)	-0.5	2.1	V
Voltage on any GPIO	-0.5	VIO + 0.5	V
Voltage on any Analog Pins	-0.5	2.1	V
RF input power, antenna port		+10	dBm
Operating temperature	-40	+85	ºC
Storage temperature	-	+105	ºC

Table 3: Absolute Maximum Ratings[1]

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
V_{BAT}	3.0	3.6	4.8	V
VIO	1.62	1.8	1.92	V
V_{IH}	0.65 X VIO	-	VIO	V
V_{IL}	0	-	0.35 X VIO	V
V_{OH} @ 4, 8 mA	VIO-0.45	-	VIO	V
V_{OL} @ 4, 8 mA	0	-	0.45	V
Ambient temperature range	-40	25	85	ºC

Table 4: Recommended Operating Conditions

[1] Under no circumstances should exceeding the ratings specified in the Absolute Maximum Ratings section be allowed. Stressing the module beyond these limits may result permanent damage to the module that is not covered by the warranty.

General Characteristics

Parameter	Min	Typ	Max	Unit
WLAN RF frequency range	2412		2472	MHz
WLAN RF data rate	1	802.11 b/g/n rates supported	65	Mbps
BT RF frequency Range	2402		2480	MHz

Table 5 General Characteristics

Power Consumption - WLAN

Parameter	Test Conditions	Min	Typ	Max	Unit
CCK (b) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=20 dBm, 11 Mbps CCK L=1200 bytes, t_{delay} (idle)=4 µS.	-	280	-	mA
OFDM (g) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=14.5 dBm, 54 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 µS.	-	185	-	mA
OFDM (n) TX Current	2437 MHz, V_{BAT} =3.6V, T_{amb}=+25°C Po=12.5 dBm, 65 Mbps OFDM L=1200 bytes, t_{delay} (idle)=4 µS.	-	165	-	mA
CCK (b) RX Current		-	100	-	mA
OFDM (g) RX Current		-	100	-	mA
OFDM (n) RX Current		-	100	-	mA
Dynamic Mode [1]		-	<1.2	-	mA

Table 6: WLAN Power Consumption

[1] Total Current from V_{BAT} for reception of Beacons with DTIM=1 TBTT=100 mS, Beacon duration 1.6ms, 1 Mbps beacon reception in Listen Mode.

Power Consumption - Bluetooth

Parameter	Test Conditions	Min	Typ	Max	Unit
GFSK TX Current	Constant Transmit, DH5, PRBS9	-	45	-	mA
EDR TX Current	Constant Transmit, 2DH5,3DH5, PRBS9	-	43	-	mA
GFSK RX Current	Constant Receive, DH1	-	35	-	mA
EDR RX Current	Constant Receive, 2DH5, 3DH5	-	41	-	mA
Deep Sleep Current	Deep Sleep Mode	-	70	-	μA

Table 7: Bluetooth Power Consumption

DC Characteristics – General Purpose I/O

Parameter	Test Conditions	Min	Typ	Max	Unit
Logic input low, V_{IL}		0	-	0.35 X VIO	V
Logic input high, V_{IH}		0.65 X VIO	-	VIO	V
Logic output low, V_{OL} (Full Drive)	Iout = 8 mA	0	-	0.45	V
	Iout = 4 mA	0	-	0.45	V
Logic output low, V_{OL} (Reduced Drive)	Iout = 1 mA	0	-	0.112	V
	Iout = 0.09 mA	0	-	0.01	V
Logic output high, V_{OH} (Full Drive)	Iout = -8 mA	VIO-0.45	-	VCC	V
	Iout = -4 mA	VIO-0.45	-	VCC	V
Logic output high, V_{OH} (Reduced Drive)	Iout = -1 mA	VIO-0.112	-	VCC	V
	Iout = -0.3 mA	VIO-0.033	-	VCC	V

Table 8: DC Characteristics General Purpose I/O

WLAN RF Characteristics

WLAN Transmitter Characteristics
(TA =25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	Unit
11 Mbps CCK (b) TX Output Power	11 Mbps CCK , 802.11(b) Mask Compliance, 35% EVM RMS power over TX packet	-	20	-	dBm
9 Mbps OFDM (g) TX Output Power	9 Mbps OFDM , 802.11(g) Mask Compliance, -8 dB EVM RMS power over TX packet	-	19	-	dBm
54 Mbps OFDM (g) TX Output Power	54 Mbps OFDM, 802.11(g) Mask Compliance, -25 dB EVM RMS power over TX packet	-	14.5	-	dBm
6.5 Mbps OFDM (n) TX Output Power	6.5 Mbps OFDM, 802.11(n) Mask Compliance, -5 dB EVM RMS power over TX packet	-	19	-	dBm
65 Mbps OFDM (n) TX Output Power	65 Mbps OFDM, 802.11(n) Mask Compliance, -28 dB EVM RMS power over TX packet	-	12.5	-	dBm

Table 9: WLAN Transmitter RF Characteristics

WLAN Receiver Characteristics
(TA =25°C, VBAT=3.6 V) [1]

Parameter	Test Conditions	Min	Typ	Max	Unit
1 Mbps CCK (b) RX Sensitivity	8% PER	-	-97	-	dBm
11 Mbps CCK (b) RX Sensitivity	8% PER	-	-89	-	dBm
9 Mbps OFDM (g) RX Sensitivity	10% PER	-	-90	-	dBm
54 Mbps OFDM (g) RX Sensitivity	10% PER	-	-76	-	dBm
6.5 Mbps OFDM (n) RX Sensitivity	10% PER	-	-91	-	dBm
65 Mbps OFDM (n) RX Sensitivity	10% PER	-	-73	--	dBm
11 Mbps CCK (b) RX Overload Level.	8% PER	-10	-	-	dBm
6 Mbps OFDM(g) RX Overload Level.	10% PER	-20	-	-	dBm
54 Mbps OFDM(g) RX Overload Level.	10% PER	-20	-	-	dBm
65 Mbps OFDM(n) RX Overload Level.	10% PER	-20	-	-	dBm

[1] Up to 2 dB degradation at Channel 13 for 11g/n modes and up to 2 dB degradation at Channel 14 for 11b/g/n modes.

Table 10: WLAN Receiver RF Characteristics

BLUETOOTH RF Characteristics

Bluetooth Transmitter GFSK and EDR Characteristics, Class 1.5 (TA =25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	BT Spec	Unit
GFSK RF Output Power		-	9.5	-	-	dBm
EDR RF Output Power		-	7	-		
Power Control Step Size		2	4	8	2-8	dB
EDR Relative Power		-2		1	-4/+1	dB

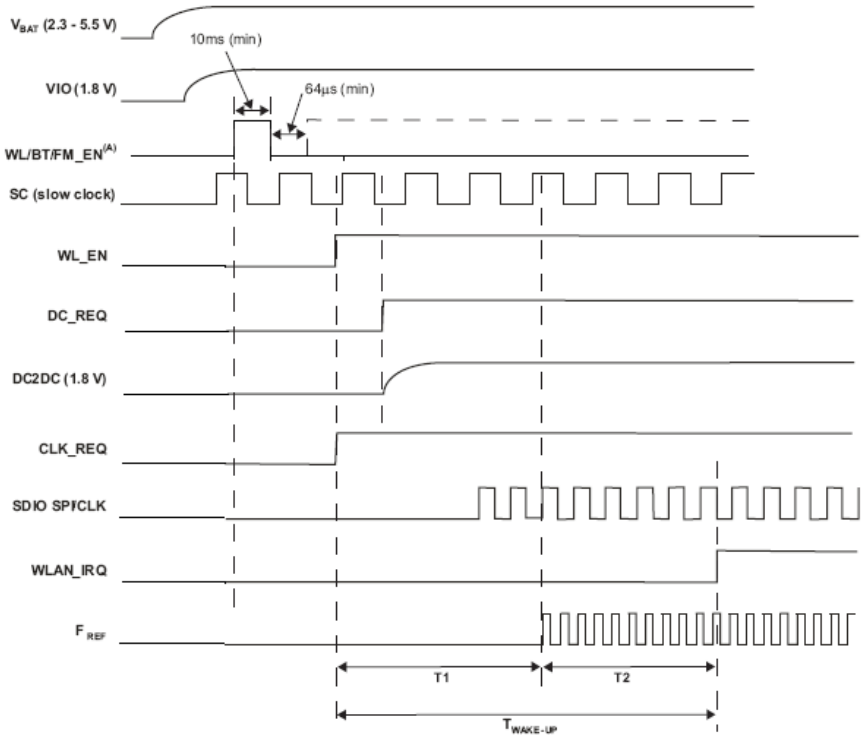
Table 11: Bluetooth Transmitter RF Characteristics

Bluetooth Receiver Characteristics (TA =25°C, VBAT=3.6 V)

Parameter	Test Conditions	Min	Typ	Max	BT Spec	Unit
GFSK Sensitivity	BER=0.1%	-	-92	-	-70	dBm
EDR 2 Mbps Sensitivity	BER=0.01%	-	-91	-	-70	dBm
EDR 3 Mbps Sensitivity	BER=0.01%	-	-82	-	-70	dBm
GFSK Maximum Input Level	BER=0.1%	-	-5	-	-20	dBm
EDR 2 Maximum Input Level	BER=0.1%	-	-10	-	-	dBm
EDR 3 Maximum Input Level	BER=0.1%	-	-10	-	-	-

Table 12: Bluetooth Receiver RF Characteristics

WLAN POWER-UP SEQUENCE



A. After this sequence is completed, the device is in the low VIO-leakage state while in shutdown.

Figure 4-1: TiWi-R2 Power-up Sequence Requirements

The following sequence describes device power-up from shutdown. Only the WLAN Core is enabled; the BT and FM cores are disabled.

1. No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'fail safe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC".

2. VBAT,VIO and SLOWCLK must be available before WL_EN.

3. T_{wakeup} = T1 + T2

The duration of T1 is defined as the time from WL_EN=high until Fref is valid for the SoC, T1 ~55ms

The duration of T2 depends on:
– Operating system
– Host enumeration for the SDIO/WSPI
– PLL configuration
– Firmware download
– Releasing the core from reset
– Firmware initialization

WLAN POWER-DOWN SEQUENCE

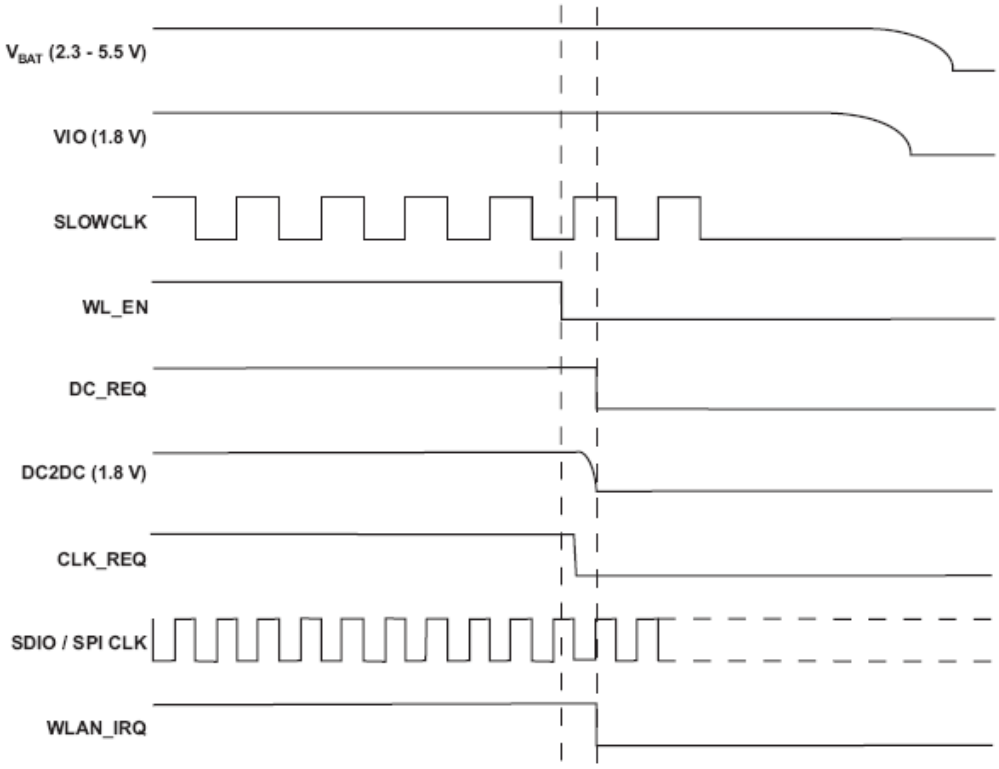


Figure 4-2: TiWi-R2 Module Power-down Sequence Requirements

1. DC_REQ will go low only if WLAN is the only core working. Otherwise if another core is working (e.g BT) it will stay high.

2. CLK_REQ will go low only if WLAN is the only core working. Otherwise if another core is working and using the Fref (e.g BT) it will stay high.

3. If WLAN is the only core that is operating, WL_EN must remain de-asserted for at least 64μsec before it is re-asserted.

BLUETOOTH POWER-UP SEQUENCE

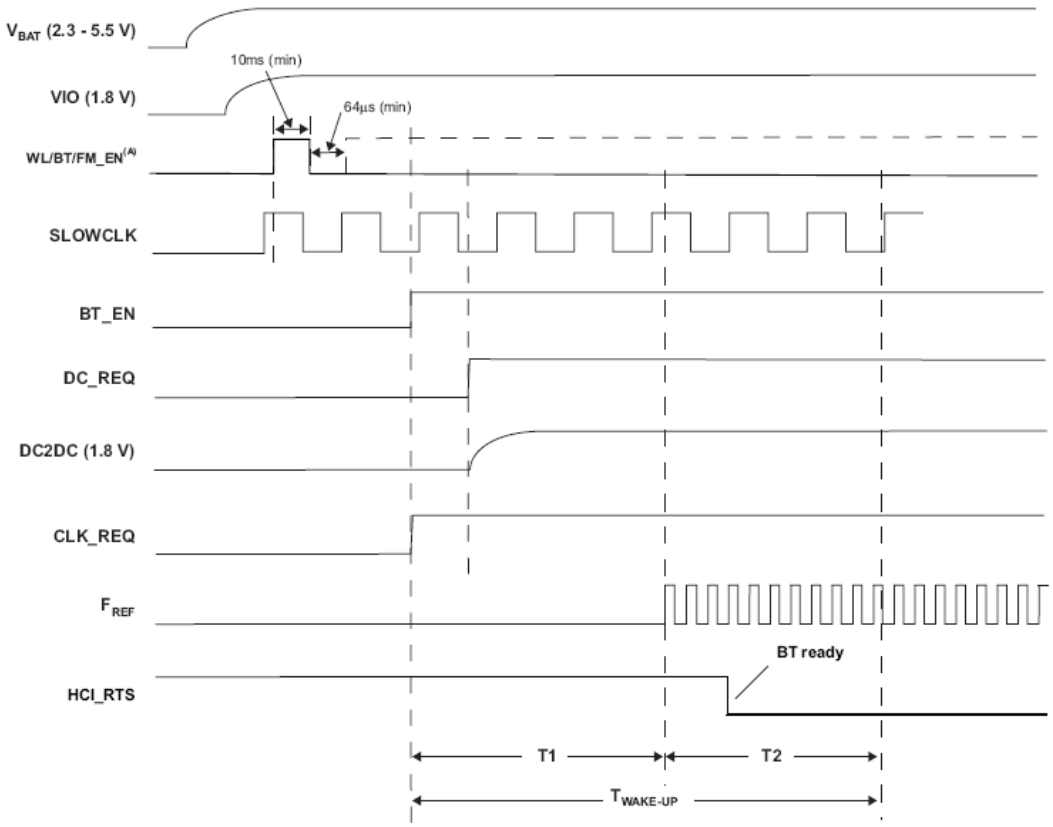
The following sequence describes device power up from shutdown. Only the BT core is enabled; the WLAN core is disabled.

Power up requirements:

1. No signals are allowed on the IO pins if no IO power supplied, because the IOs are not 'failsafe'. Exceptions are CLK_REQ_OUT, SLOWCLK, XTALP and AUD_xxx, which are failsafe and can tolerate external voltages with no VDDS and DC2DC.

2. VDDS and SLOWCLK must be stable before releasing BT_EN.

3. Fast clock must be stable maximum 55 ms after BT_EN goes HIGH.



A. After this sequence is completed, the device is in the low VIO-leakage state while in shutdown.

Figure 4-3. BT Power-up Sequence

BLUETOOTH POWER-DOWN SEQUENCE

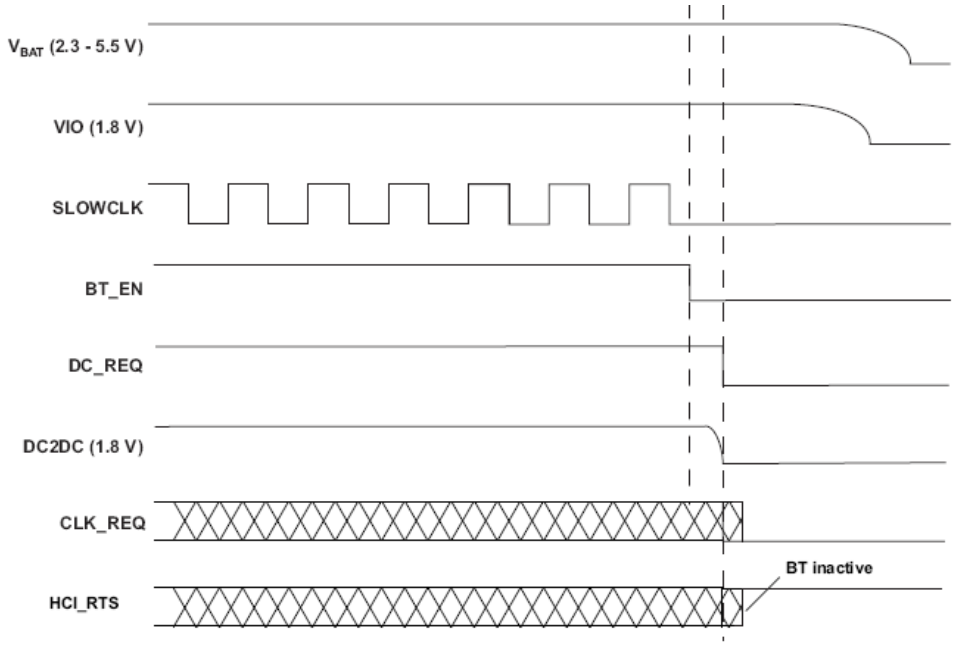


Figure 4-4. BT Power-down Sequence

The TiWi-R2 module indicates completion of BT power up sequence by asserting RTS low. This occurs up to 100 ms after BT_EN goes high.

ENABLE SCHEME

The module has 3 enable pins, one for each core: WL_EN, and BT_EN and FM_EN. Presently, there are 2 modes of active operation now supported: WLAN and BT. It is recommended that the FM_EN pin be grounded to disable the FM section. It is also recommended that the FM section be disabled by Bluetooth HCI commands.

1. Each core is operated independently by asserting each EN to Logic '1'. in this mode it is possible to control each core asynchronously and independently.

2. BT mode operation. WLAN will be operated through WL_EN asynchronously independently of BT

IRQ OPERATION

1. The default state of the WLAN_IRQ prior to firmware initialization is 0.
2. During firmware initialization, the WLAN_IRQ is configured by the SDIO module; a WLAN_IRQ changes its state to 1.
3. A WLAN firmware interrupt is handled as follows:
    a. The WLAN firmware creates an Interrupt-to-Host, indicated by a 1-to-0 transition on the WLAN_IRQ line (host must be configured as active-low or falling-edge detect).
    b. After the host is available, depending on the interrupt priority and other host tasks, it masks the firmware interrupt. The WLAN_IRQ line returns to 1 (0-to-1 transition on the WLAN_IRQ line).
    c. The host reads the internal register status to determine the interrupt sources - the register is cleared after the read.
    d. The host processes in sequence all the interrupts read from this register
    e. The host unmasks the firmware interrupts.
4. The host is ready to receive another interrupt from the WLAN device.

SLOW (32 KHZ) CLOCK SOURCE REQUIREMENTS

Characteristics (1)	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy	WLAN, BT				±150	ppm
Input transition time Tr/Tf -10% to 90%		Tr/Tf			100	ns
Frequency input duty cycle			30	50	70	%
Input voltage limits	Square wave, DC-coupled	VIH	0.65 X VDDS		VDDS	Vpeak
VIL	0		0.35X VDDS			
Input impedence			1			MW
Input capacitance					5	pF
Rise and fall time					100	ns
Phase noise	1 kHz			–125		dBc/Hz
1) Slow clock is a fail safe input						

BT HCI UART

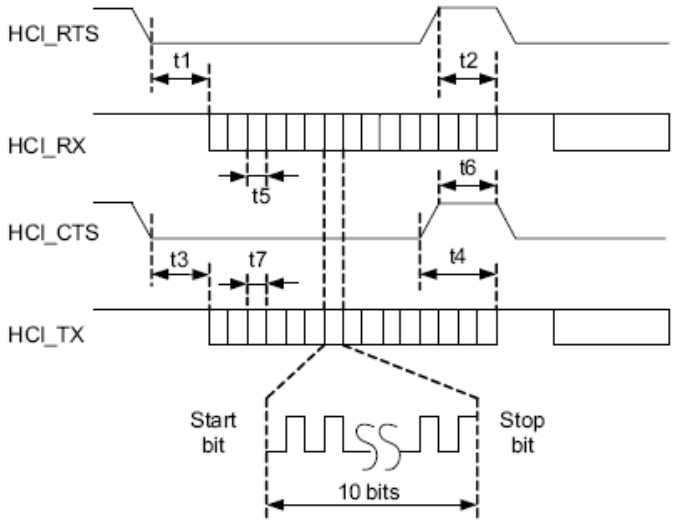


Figure 7-1. UART TIming

Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate	Most rates(1)	37.5		4000	kbps
t5, t7	Baud rate accuracy	Receive/Transmit			–2.5 to 1.5	%
t3	CTS low to TX_DATA on		0	2		µs
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS-high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		µs
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte
tb	Bit width (Jitter)		See application note(1)			% relative to ideal bit width

(1) Some exceptions: e.g. for 19.2-MHz max baud rate = 3.84 kbps.

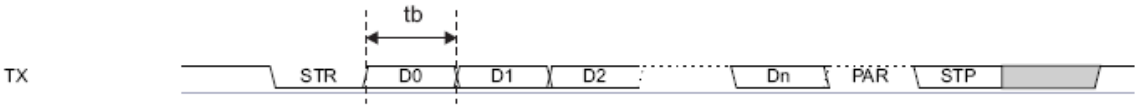


Figure 7-2. Data Frame

Symbol	Description
STR	Start bit
D0...Dn	Data bits (LSB first)
PAR	Parity bit (optional)
STP	Stop bit

SDIO INTERFACE TIMING

Table 7-9. SDIO-Interface Read (see Figure 7-3)

PARAMETER			MIN	MAX	UNIT
t_{CR}	Delay time, assign relative address or data transfer mode	Read-command CMD valid to card-response CMD valid	2	64	Clock cycles
t_{CC}	Delay time, CMD command valid to CMD command valid		58		Clock cycles
t_{RC}	Delay time, CMD response valid to CMD command valid		8		Clock cycles
t_{AC}	Access time, CMD command valid to SD3–SD0 read data valid		2		Clock cycles

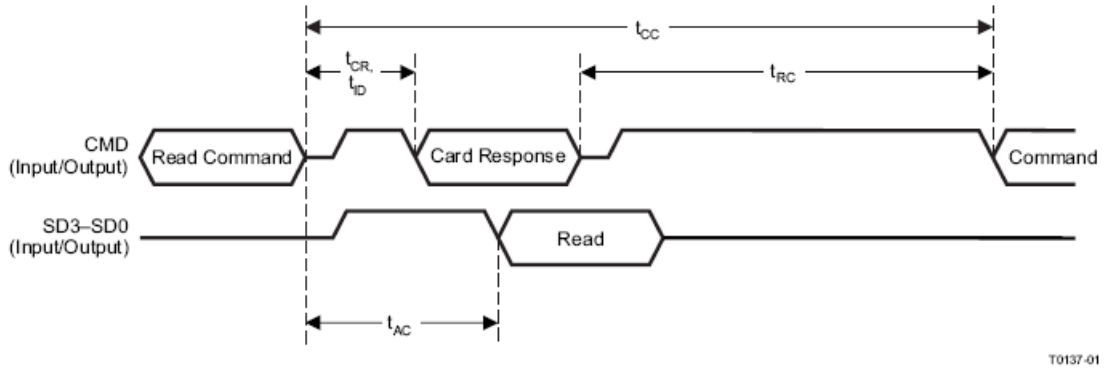
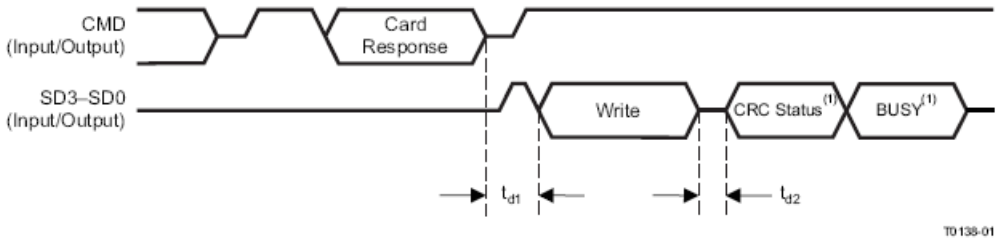


Figure 7-3. SDIO Single Block Read

Table 7-10. SDIO SD Interface Write (see Figure 7-4)

PARAMETER		MIN	MAX	UNIT
t_{d1}	Delay time, CMD card response invalid to SD3–SD0 write data valid	2		Clock cycles
t_{d2}	Delay time, SD3–SD0 write data invalid end to CRC status valid	2	2	Clock cycles



NOTE: CRC status and busy waveforms are only for data line 0. Data lines 1–3 are N/A. The busy waveform is optional, and may not be present.

Figure 7-4. SDIO Single Block Write

SDIO CLOCK TIMING

Over Recommended Operating Conditions

Note: all timing parameters are indicated for the maximum Host-interface clock frequency.

PARAMETER			MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	$C_L \leq 30$ pF	0	26	MHz
DC	Low/high duty cycle	$C_L \leq 30$ pF	40	60	%
t_{TLH}	Rise time, CLK	$C_L \leq 30$ pF		4.3	ns
t_{THL}	Fall time, CLK	$C_L \leq 30$ pF		3.5	ns
t_{ISU}	Setup time, input valid before CLK ↑	$C_L \leq 30$ pF	4		ns
t_{IH}	Hold time, input valid after CLK ↑	$C_L \leq 30$ pF	5		ns
t_{ODLY}	Delay time, CLK↓ to output valid	$C_L \leq 30$ pF	2	12	ns

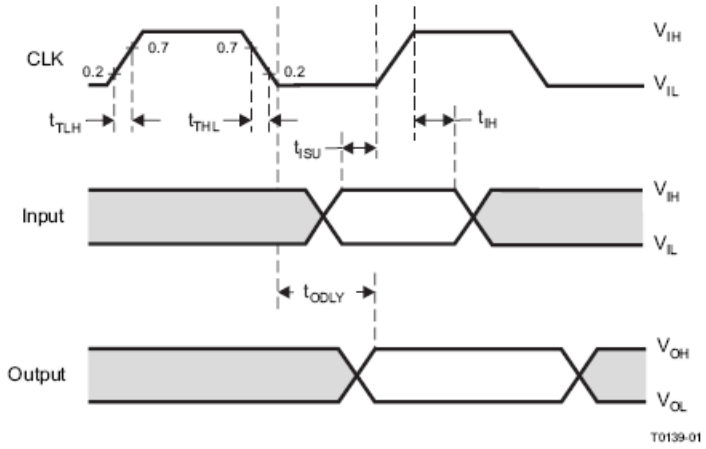
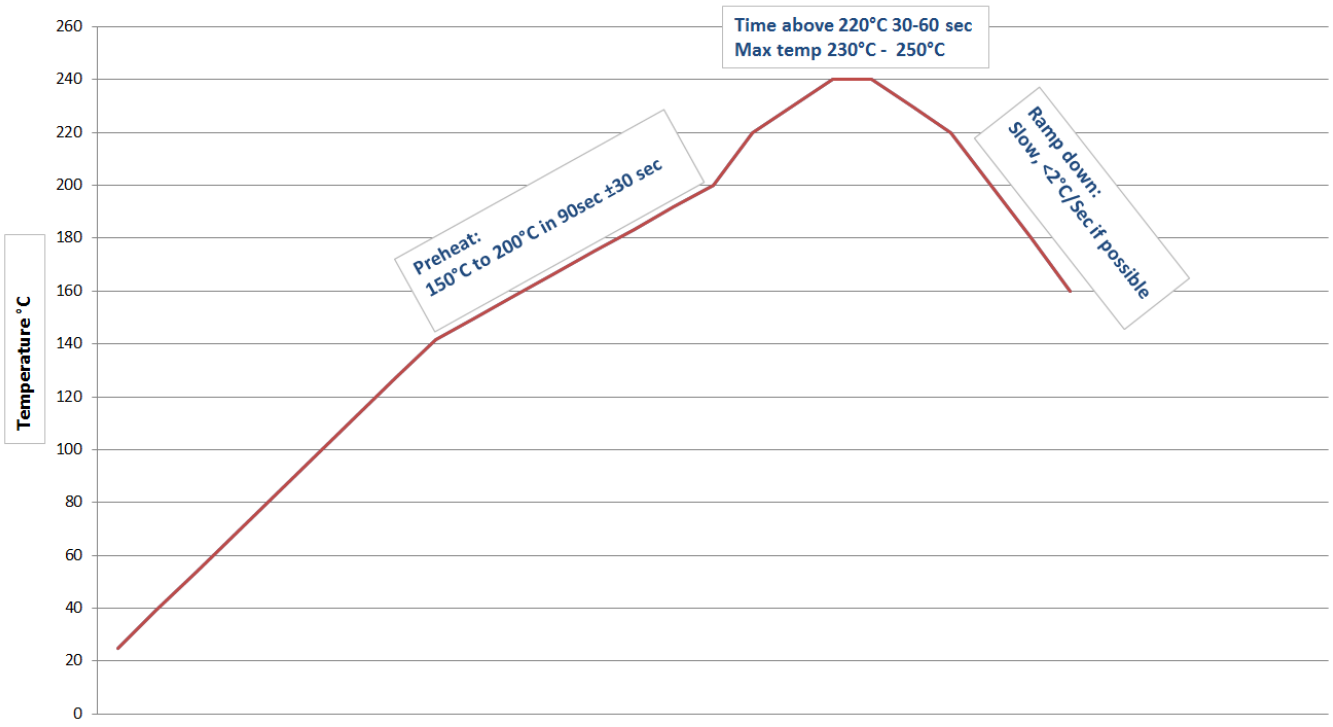


Figure 7-5. SDIO Timing

SOLDERING RECOMMENDATIONS

Recommended Reflow Profile for Lead Free Solder



Note: The quality of solder joints on the castellations ('half vias') where they contact the host board should meet the appropriate IPC Specification. See IPC-A-610-D Acceptability of Electronic Assemblies, section 8.2.4 Castellated Terminations."

CLEANING

In general, cleaning the populated modules is strongly discouraged. Residuals under the module cannot be easily removed with any cleaning process.

- Cleaning with water can lead to capillary effects where water is absorbed into the gap between the host board and the module. The combination of soldering flux residuals and encapsulated water could lead to short circuits between neighboring pads. Water could also damage any stickers or labels.
- Cleaning with alcohol or a similar organic solvent will likely flood soldering flux residuals into the RF shield, which is not accessible for post-washing inspection. The solvent could also damage any stickers or labels.
- Ultrasonic cleaning could damage the module permanently.

OPTICAL INSPECTION

After soldering the Module to the host board, consider optical inspection to check the following:

- Proper alignment and centering of the module over the pads.
- Proper solder joints on all pads.
- Excessive solder or contacts to neighboring pads, or vias.

REWORK

The TiWi-R2 module can be unsoldered from the host board. Use of a hot air rework tool and hot plate for pre-heating from underneath is recommended. Avoid overheating.

Never attempt a rework on the module itself, e.g. replacing individual components. Such actions will terminate warranty coverage.

SHIPPING, HANDLING, AND STORAGE

Shipping

Bulk orders of the TiWi-R2 modules are delivered in trays of 100.

Handling

The TiWi-R2 modules contain a highly sensitive electronic circuitry. Handling without proper ESD protection may destroy or damage the module permanently. ESD protection may destroy or damage the module permanently.

Moisture Sensitivity Level (MSL)

MSL 4, per J-STD-020

Devices not stored in a sealed bag with desiccant pack should be baked.

After opening devices that will be subjected to reflow must be mounted within 72 hours of factory conditions (<30°C and 60% RH) or stored at <10% RH.

Bake devices for 8 hours at 125°C.

Storage

Storage/shelf life in sealed bags is 12 months at <40°C and <90% relative humidity.

Repeating Reflow Soldering

Only a single reflow soldering process is encouraged for host boards.

AGENCY CERTIFICATIONS

FCC ID: TFB-TIWI1-01, 15.247.

IC ID: 5969A-TIWI101, RSS 210

ETSI: The European Telecommunications Standards Institute. It produces the radio and communication standards for Europe. Our testing is to the ETSI standards EN 300 328 and EN 301 489, which are the portions of the relevant directives needed for a radio to obtain a CE mark.

MECHANICAL DATA

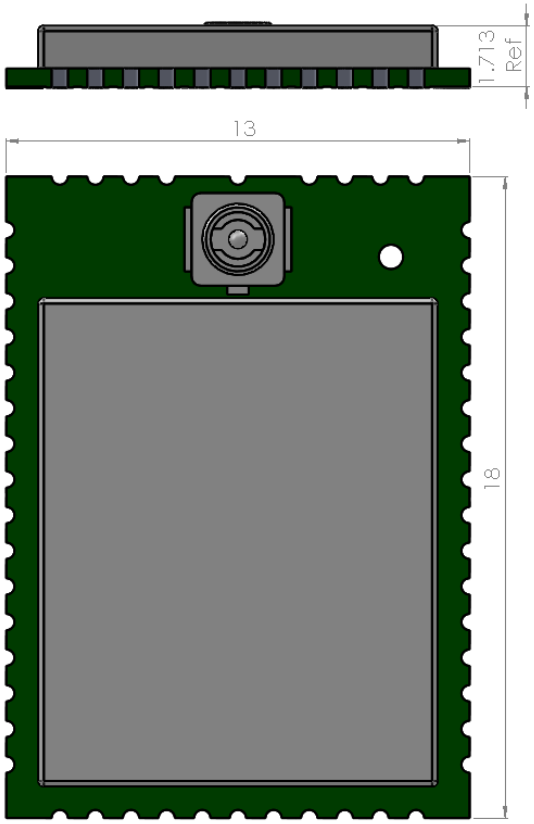
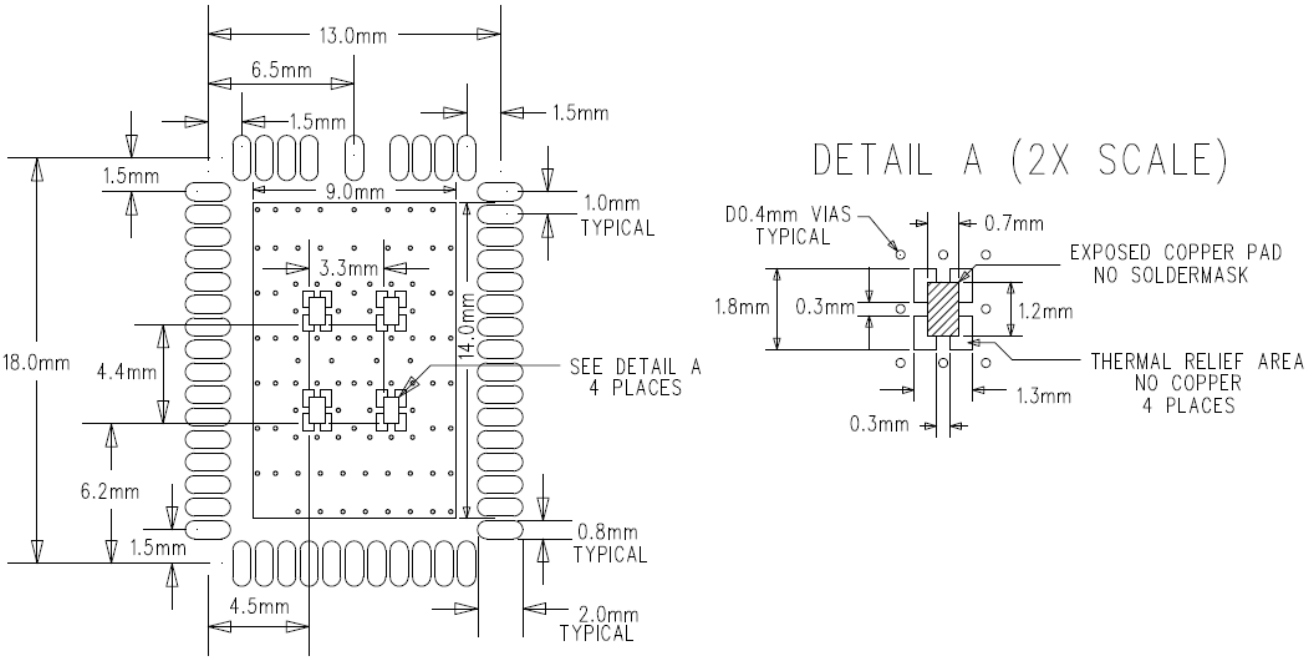


Figure 4: Module Mechanical Dimensions (Maximum Module Height = 1.9 mm)



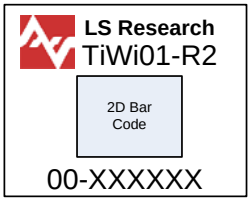
LAYOUT NOTES:
1 – MINIMUM 4-LAYER PCB WITH SECOND LAYER GROUND PLANE
2 – FOUR GROUND PADS BENEATH MODULE TO BE THERMALLY TIED TO
TOP LAYER GROUND POUR (SEE DETAIL A).
CONNECT TOP SIDE POUR TO LAYER 2 GROUND PLANE USING AMPLE VIAS.
3 – AVOID LONG ROUTES ON TOP LAYER BENEATH MODULE. VIA FANOUT BENEATH MODULE IS ACCEPTABLE,

Figure 5: TiWi-R2 Footprint.

DEVICE MARKINGS

Rev 0 Devices

WL1271 Silicon Rev	Front End
WL1271A1YFVR PG2.1	TQM679002A

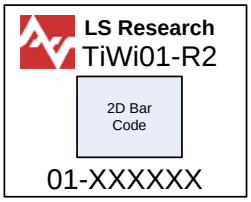


Where 00 = revision

XXXXXX = incremental serial number

Rev 1 Devices

WL1271 Silicon Rev	Front End
WL1271BYFVR PG3.1	TQM679002A



Where 01 = revision

XXXXXX = incremental serial number

CONTACTING LS RESEARCH

Headquarters	LS Research, LLC W66 N220 Commerce Court Cedarburg, WI 53012-2636 USA Tel: (262) 375-4400 Fax: (262) 375-4248
Website	http://www.lsr.com
Technical Support	http://forum.lsr.com
Wiki	http://wiki.lsr.com/TiWi.ashx
Sales Contact	sales@lsr.com

Mouser Electronics

Related Product Links

741-450-0037 - LS Research 450-0037