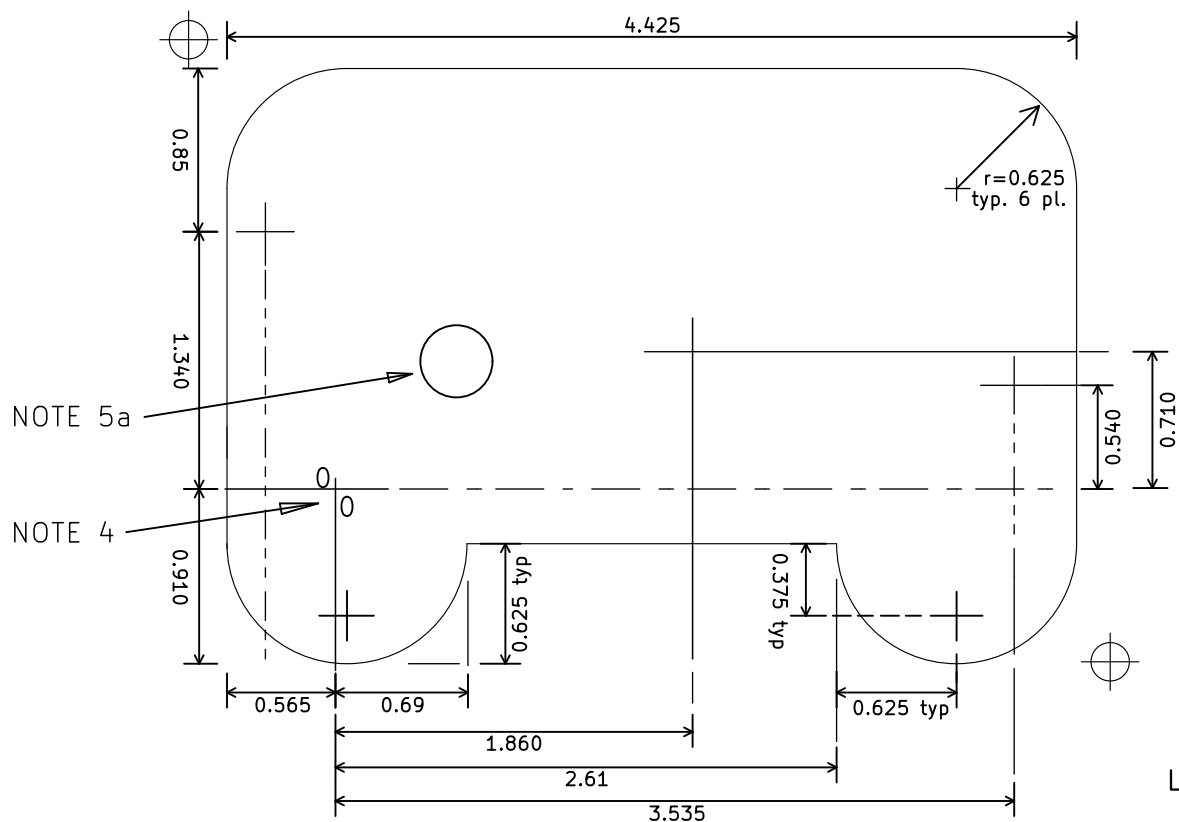


Be sure this is the latest version!

DATE	BY	REVISIONS	ISS.
2/26/14	PR	Initial release	T1
3/29/14	PR	C19: Fix reference text. S1-S7: Fix pin map. U4: Move pin 1 to 3V rail. C18: Place next to U4. D51: Fix 24 & 26 reversed. D4/D5: Fix interference. R16: Chg. 120 was 10K. ADD: Logo, radius corners. U4: Fix footprint. ADD: Batt. light [D52], & layer stack up drawing. MISC: Fix drill hole sizes.	P1



NOTES:

1: DESCRIPTION:

.062" (nominal) Etched Circuit board, 2 side 1 oz (finished) Cu, for hybrid SMT/through lead. Minimum 8/8 SMT design rules. Not for lead free assembly.

2: MATERIAL & FINISH:

Refer to 00-PCB-README file for solder mask & silkscreen colors and quantities.

3: Dimensions:

Finish dimensions per drawing. $\pm .005$ " on decimals, $\pm .003$ " on holes, 1/64" on fractions, unless noted. Undimensioned holes to be positioned per artwork.

4: Co-ordinate System:

Drill file and SMT centroid 0, 0 origin (reference point) located per drawing.

5: ASSEMBLY:

- DS2: LED mounts "face down" on SMD side. Verify presence and size of lens hole prior to assembly.
- Manufacturer & RoHS labels on LC display DS1 must be removed prior to assembly.
- Orient battery holders per legend. Refer to 00-ASM-README file.

LAYER STACK UP DETAIL SMD COMPONENT Side

TOP SILK [thotcon_0x5-F_Silks.gto]	
TOP SOLDER MASK [thotcon_0x5-F_Mask.gts]	
TOP COPPER [thotcon_0x5-F_copper.gtl]	
CORE/DIELECTRIC	
BOTTOM COPPER [thotcon_0x5-B_copper.gbl]	
BOTTOM SOLDER MASK [thotcon_0x5-B_mask.gbs]	
BOTTOM SILK [thotcon_0x5-B_Silks.gbo]	

0.062 +/- 10%

THROUGH-HOLE COMPONENT Side

SEE ALSO thotcon_0x5-F_Paste.gtp (top paste), thotcon_0x5-B_Paste.gbp (bottom paste)

LICENSE: CC-BY-SA-3.0

Project Mgr: R. Ristich

Designed: Paul Reich

Drawn: Paul Reich

Workshop 88

File: thotcon_0x5.brd

Sheet:

Title: BOARD, PC, THOTCON 0X5

Size: A Date: 31 mar 2014

KiCad E.D.A.

Rev: P1

Id: 1/1

BOARD, PC, THOTCON 0x5