Design Assignment 2B

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Primary Github address: https://github.com/WorkuT1226/CPE301.git
Directory:

 Submit the following for all Labs:

- In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.

- Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.

- If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.

- The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

- **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

List of Components used
Block diagram with pins used in the Atmega328P

- **INITIAL/MODIFIED/DEVELOPED CODE OF TASK 1/A**

```
; AssemblerApplication1.asm
; Created: 10/5/2019 6:21:20 PM
; Author : Worku Tafara
;
.org 0
jmp START
.org 0x02
jmp TARGET
START:
```

```
ldi R20, HIGH(RAMEND)
out SPH, R20
ldi R20, LOW(RAMEND)
out SPL, R20
ldi R20, 2
sts EICRA, R20
sbi DDRB, 3
sbi PORTB, 3
sbi PORTD, 2
cbi DDRC, 3
sbi PORTC, 3
ldi R20, 1<<INT0
out EIMSK, R20
sei
here:
jmp here
TARGET:
in R21, PORTB
ldi R22, (1<<3)
eor R21, R22
out PORTB, R21
; Delay 6 000 000 cycles
; 375ms at 16.0 MHz
        ldi  R18, 31
        ldi  R19, 113
        ldi  R20, 31
L1:
 dec  R20
        brne L1
        dec  R19
        brne L1
        dec  R18
        brne L1
        nop
```

- **DEVELOPED MODIFIED CODE OF TASK 2/A from TASK 1/A**

C code
```c
#include <avr/io.h>
#include <avr/interrupt.h>
#include <util/delay.h>
#define F_CPU 16000000UL
int main(void){
```

```c
DDRB |= (1<<3);
PORTB |= (1<<3);
DDRC &= (0<<3);
PORTC |= (1<<3);
EIMSK = (1<<INT0);
EICRA = (1<<ISC01);
sei ();

while (1) {}
}
ISR (INT0_vect) {
  PORTB ^= (1<<3);
  _delay_ms(1333);
}
```

- ### SCREENSHOTS OF EACH TASK OUTPUT (ATMEL STUDIO OUTPUT)

```asm
; AssemblerApplication1.asm
; Created: 10/5/2019 6:21:20 PM
; Author : Worku Tafara
;

.org 0
jmp START
.org 0x02
jmp TARGET

START:
ldi R20, HIGH(RAMEND)
out SPH, R20
ldi R20, LOW(RAMEND)
out SPL, R20
ldi R20, 2
sts EICRA, R20
sbi DDRB, 3
sbi PORTB, 3
sbi PORTD, 2
cbi DDRC, 3
sbi PORTC, 3
ldi R20, 1<<INT0
out EIMSK, R20
sei

here:
jmp here
```

```asm
main.asm   ☒ ASF Wizard
    here:
    jmp here

    TARGET:
    in  R21, PORTB
    ldi R22, (1<<3)
    eor R21, R22
    out PORTB, R21

    ; Delay 6 000 000 cycles
    ; 375ms at 16.0 MHz

        ldi  R18, 31
        ldi  R19, 113
        ldi  R20, 31

    L1:
        dec  R20
        brne L1
        dec  R19
        brne L1
        dec  R18
        brne L1
        nop
```

```
//; AssemblerApplication1.asm
//; Created: 10/5/2019 6:21:20 PM
//; Author : Worku Tafara

#include <avr/io.h>
#include <avr/interrupt.h>
#include <util/delay.h>
#define F_CPU 16000000UL

int main(void){
    DDRB |= (1<<3);
    PORTB |= (1<<3);
    DDRC &= (0<<3);
    PORTC |= (1<<3);
    EIMSK = (1<<INT0);
    EICRA = (1<<ISC01);
    sei ();

    while (1) {}
}

ISR (INT0_vect) {
    PORTB ^= (1<<3);
    _delay_ms(1333);
}
```

- **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

- **VIDEO LINKS OF EACH DEMO**

https://youtu.be/ZWJ7K3NarFc

- **GITHUB LINK OF THIS DA**

"This assignment submission is my own, original work".

Worku Tafara