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Homework #2

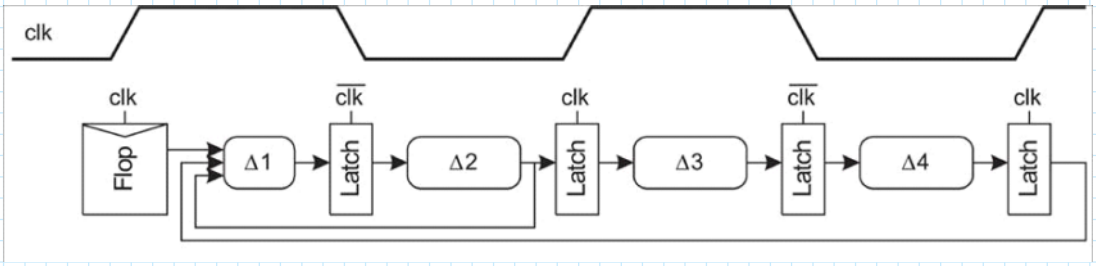
Monday, July 18, 2016 6:35 PM

1. Determine the minimum clock period at which the circuit below will operate correctly for each of the following logic delays. Assume there is zero clock skew and the latch delays are accounted for in the propagation delay Δ's.
   a) Δ1=300ps; Δ2=400ps; Δ3=200ps; Δ4=350ps
   b) Δ1=300ps; Δ2=400ps; Δ3=400ps; Δ4=550ps
   c) Δ1=300ps; Δ2=900ps; Δ3=200ps; Δ4=350ps

   Use the following table:

   Setup Time / clk-to-Q Delay / D to Q Delay / Hold Time

FFs	65ps	50ps	n/a	30ps	= 145ps
Latches	25ps	50ps	40ps	30ps	= 145ps

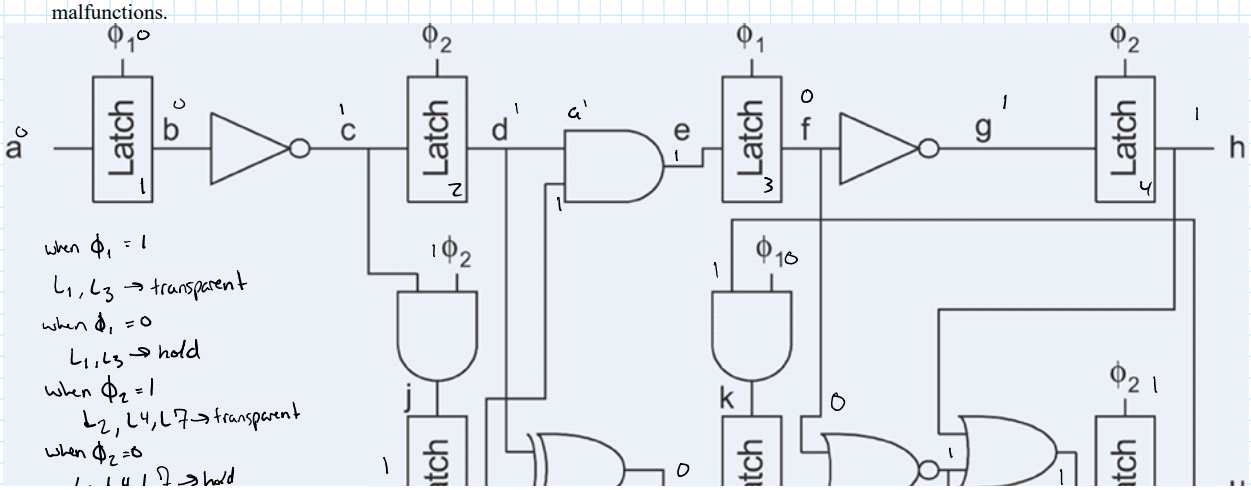


a) greatest delay → Δ1Δ2 = 700ps

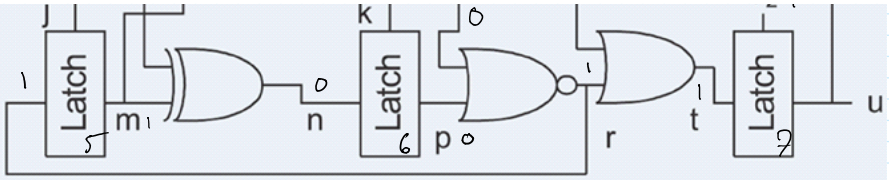
b) greatest delay → Δ3Δ4 = 950ps

c) greatest delay → Δ1Δ2 = 1200ps

2. Annotate each of the signals in Figure below with its timing type. If the circuit contains any illegal connections, identify the problems and explain why the connections could cause malfunctions.



when $\phi_2 = 1$
$L_2, L_4, L_7 \rightarrow$ transparent
when $\phi_2 = 0$
$L_2, L_4, L_7 \rightarrow$ hold



		L_1	L_2	L_3	L_4	L_5	L_6	L_7
ϕ_1	0	H		H				
	1	T		T				
ϕ_2	0		H		H			H
	1		T		T			T

depends on a

depends on u

b	c	d	e	f	g	h	i	j	k	m	n	p	r	t	u
a	b'		e	f'											
	c				g		a'		r						

j & k are the illegal connections
because they make the circuit asynchronous
– it no longer takes the clock as a direct enable and distorts the signal