Homework 1

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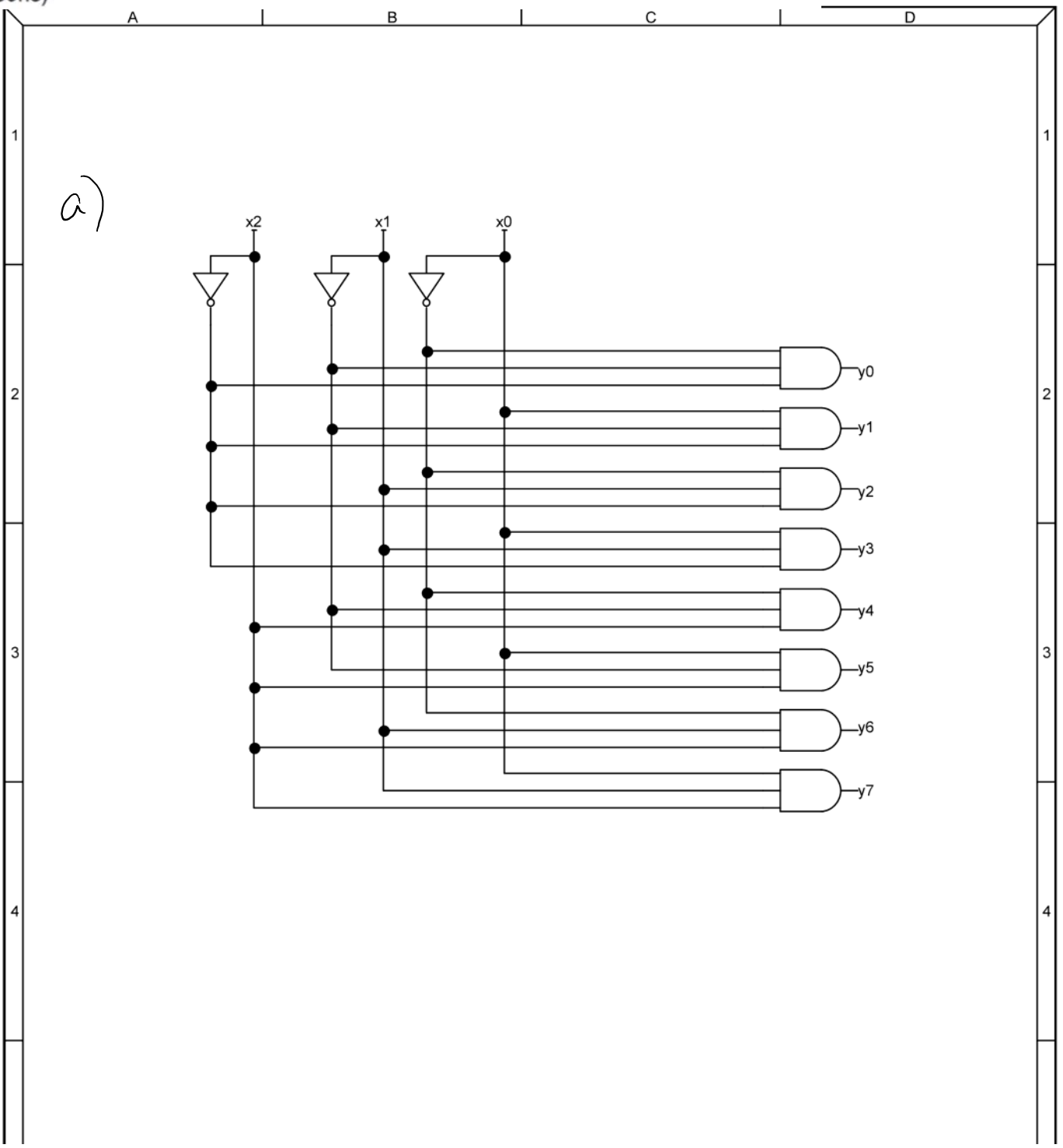
1. Sketch a gate-level design of 3:8 decoder (use labels throughout for clarity, include inverters for complementary signals)

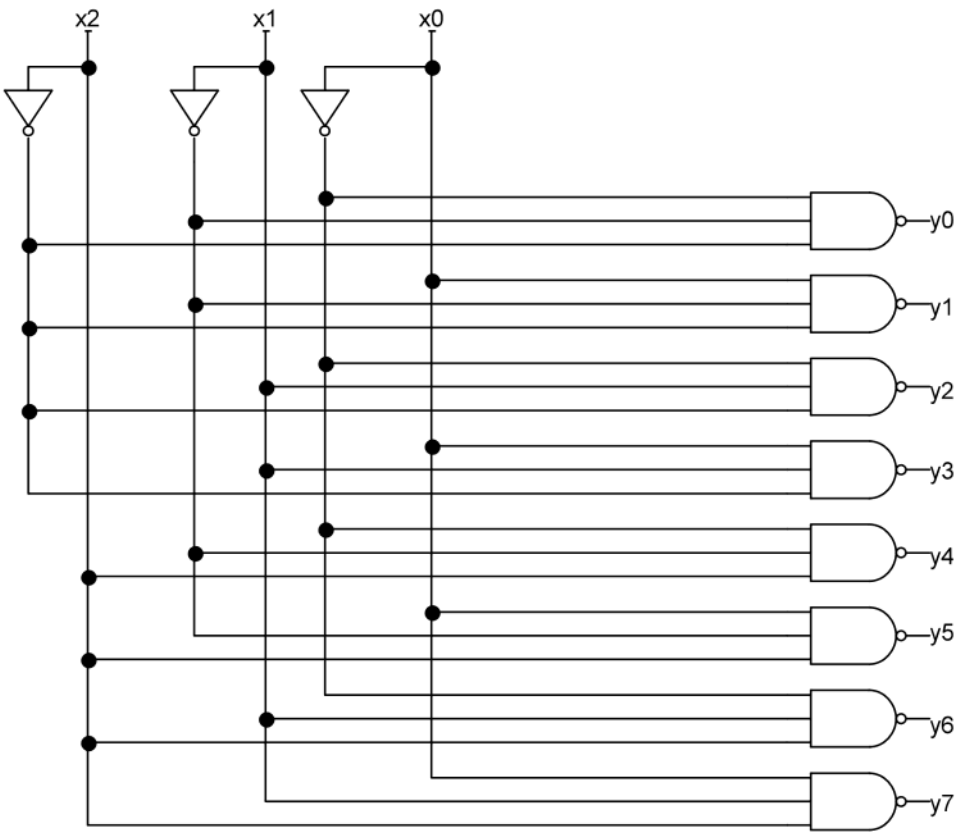
a. Using AND gates
b. Using NAND gates only
c. Using NOR gates only
d. Comment on advantages or disadvantages of one design over others (min. two reasons)

a)

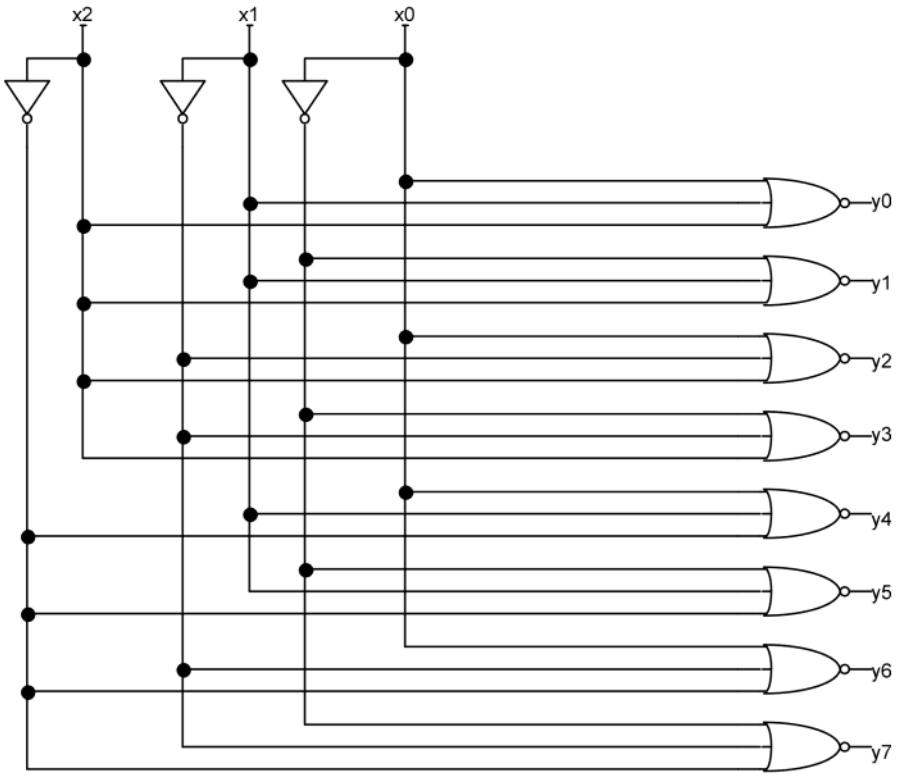



5
5
A
B
C
D

b)

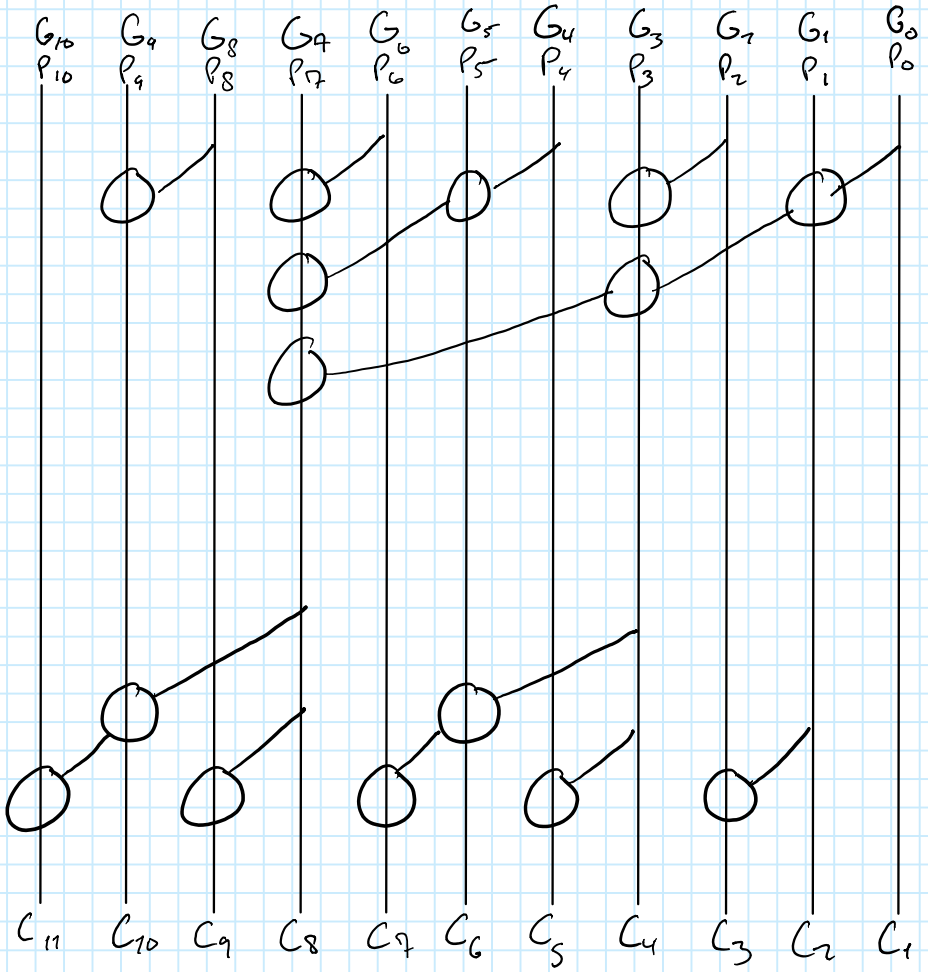


c)



d) A is the worst of these due to the fact that AND gates are more complex than NAND/NOR. This makes it slower, larger, and possibly out of synch with itself

2. Sketch a design of 11-bit Brent-Kung Adder. Make sure that the connections are clear and visible. (Use the example of 8-bit design from the class to help you figure out the 11-bit solution)



3. Perform a multiplication of the following floating point numbers in normalized IEEE single precision format:
a. 6.25 * -23.125
b. –17.875 * -42.5

a) 6.25×-23.125

$6.25 \rightarrow 110.01 = 1.1001 \times 2^2$

$-23.125 \rightarrow 10111.001 = 1.0111001 \times 2^4$

$0.25 \times 2 = 0.5$
$0.5 \times 2 = 1$

$0.125 \times 2 = 0.25$
$0.25 \times 2 = 0.5$
$0.5 \times 2 = 1$

6.25 → 110.01 = 1.1001 x 2^2   0.5 x 2 = 1

-23.125 → 10111.001 = 1.0111001 x 2^4

| 0 | 1000 0001 | 10010000.... |

x

| 1 | 1000 0011 | 0111001000.... |

```
              1.1001
x       1.0111001
        1.0111001
     1.0111001
   1.0111001
  1001000001001
```

1.00100000 1 0001 x 2^6

→ | 1 | 1000 0110 | 0010000010001000... |

b) -17.875 x -42.5

17 = 10001
.875 = → 111

0.875 x 2 = 1.75
0.75 x 2 = 1.5
0.5 x 2 = 1

42 = 10 1010
.5 = 1

17.875 → 1 0001.111 → 1.0001111 x 2^4
42.5 → 101010.1   1.010101 x 2^5   → 9 + 127 = 136 = 10001000

```
          1.010101
x    1.00011111
     1000 1111
   10001111
  10001111
 10001111
10111110111011
```

→ | 0 | 1000 1000 | 01111011111011 00.... |