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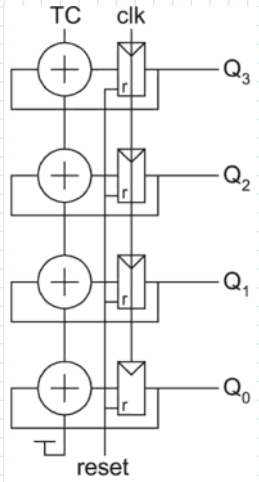
Homework #3

Sunday, July 31, 2016 2:33 PM

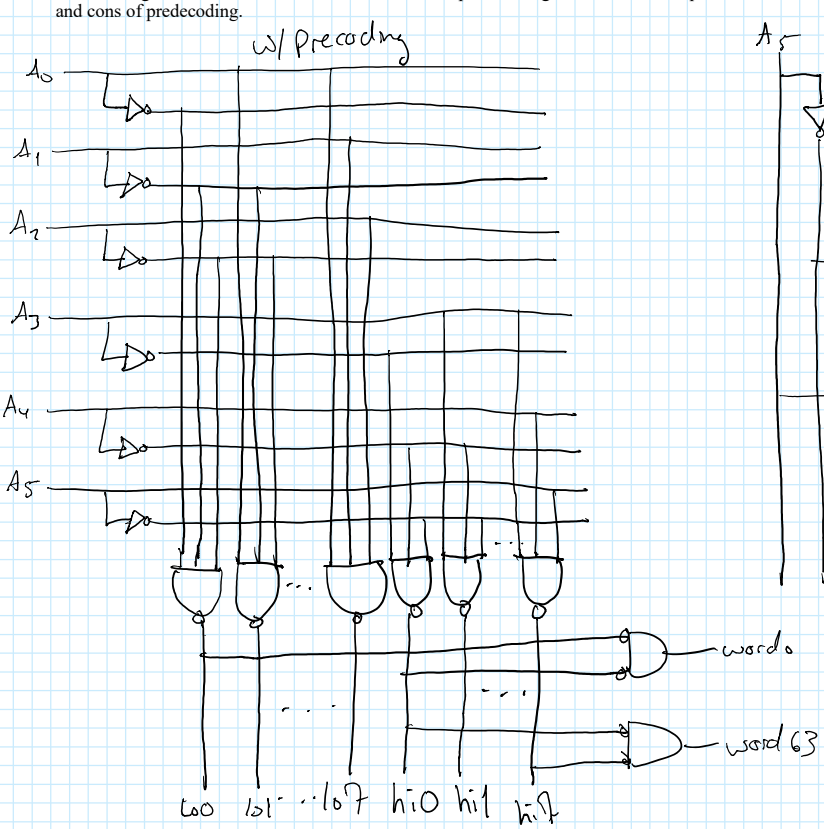
1. Identify the circuit below and determine what values it cycles through after asynchronous reset.

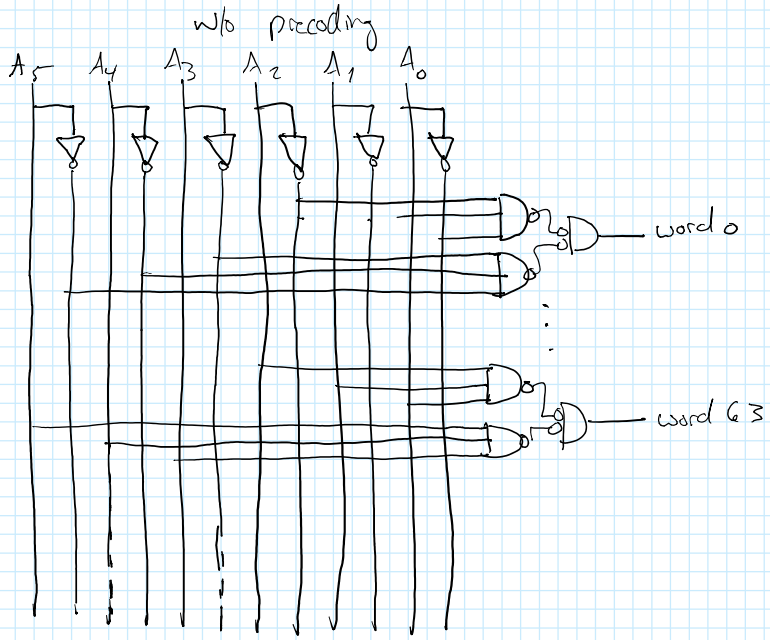
cycle	Q0	Q1	Q2	Q3	TC
0	0	0	0	0	0
1	1	0	0	0	0
2	0	1	0	0	0
3	1	1	0	0	0
4	0	0	1	0	0
5	1	0	1	0	0
6	0	1	1	0	0
7	1	1	1	0	0
8	0	0	0	1	0
9	1	0	0	1	0
10	0	1	0	1	0
11	1	1	0	1	0
12	0	0	1	1	0
13	1	0	1	1	0
14	0	1	1	1	0
15	1	1	1	1	0
16	0	0	0	0	1



4 chained half adders
→ 4 bit counter tied to clock cycles

2. Sketch designs for 6:64 decoder with and without the predecoding. Comment on the pros and cons of predecoding.





Precoding uses 16 3-input NAND gates vs non-precoding's 128
→ both designs have same path effort
→ precoding is more efficient

. The figure below shows a logical unit that is a part of ALU used in a microprocessor. The logical unit is designed with 2-1 multiplexers. Determine which combination of encoding inputs P_0-P_3 sets the logical unit to perform the following operations XNOR(A,B), XOR(A,B) and NOT(A).

Operation	P0	P1	P2	P3
XOR*(A,B)*	0	1	1	0
XNOR*(A,B)*	1	0	0	1
NOT*(A)*	1	1	0	0

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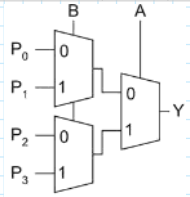
XOR*(A,B)*	0	1	1	0
XNOR*(A,B)*	1	0	0	1
NOT*(A)*	1	1	0	0



A	B	Y
0	0	P_0
0	1	P_1
1	0	P_2
1	1	P_3

XOR(A,B)	Y	XNOR(A,B)
0	P_0	1
1	P_1	0
1	P_2	0
0	P_3	1

Y	NOT(A)
P_0	1
P_1	1
P_2	0
P_3	0