Tech Mahindra Cerium Pvt Ltd
No 527, 22nd Main Road,
Sector 1 Sector 1, HSR Layout
Bangalore, Karnataka 560102, India

November 06, 2023

To Whomsoever it may concern

This is to certify that Mr. **Bhuvanesh Sathish Kayarabettu** (Employee ID – **719873**), who is a skilled and dedicated engineer, has been an integral part of our team at Tech Mahindra Cerium from December 1st, 2020, till date.

In his first project assigned to him by Tech Mahindra Cerium at Intel, Bangalore, Bhuvanesh contributed to the hardware verification of Intel's proprietary IP, which is a high-speed DAC and ADC IPs used on Intel/Altera FPGAs.

Bhuvanesh is contained in Intel, Bangalore as a Client FPGA IP Design Engineer. During his 2nd Intel project, Bhuvanesh worked on two significant projects, each lasting a year. His most recent project involved the implementation of the subIP for two communication protocol FPGA IPs. In this role, he was responsible for RTL Design, RTL Lint & CDC analysis, Code-Coverage analysis, and Timing analysis.

Currently, Bhuvanesh is working as a Client RTL Design Engineer at Qualcomm, Bangalore. He is working on the Neural Signal Processing IP used in Qualcomm SoCs. His responsibilities at Qualcomm encompass various levels, including RTL Design, Lint, CDC, UNR, and timing analysis.

Throughout his tenure here, Bhuvanesh has displayed a strong commitment to meeting project goals and deadlines. He excels as a team player, collaborating effectively with colleagues and stakeholders to drive project success.

For Tech Mahindra Cerium Pvt Ltd.

Suvidha Vashisth

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Manager - HR