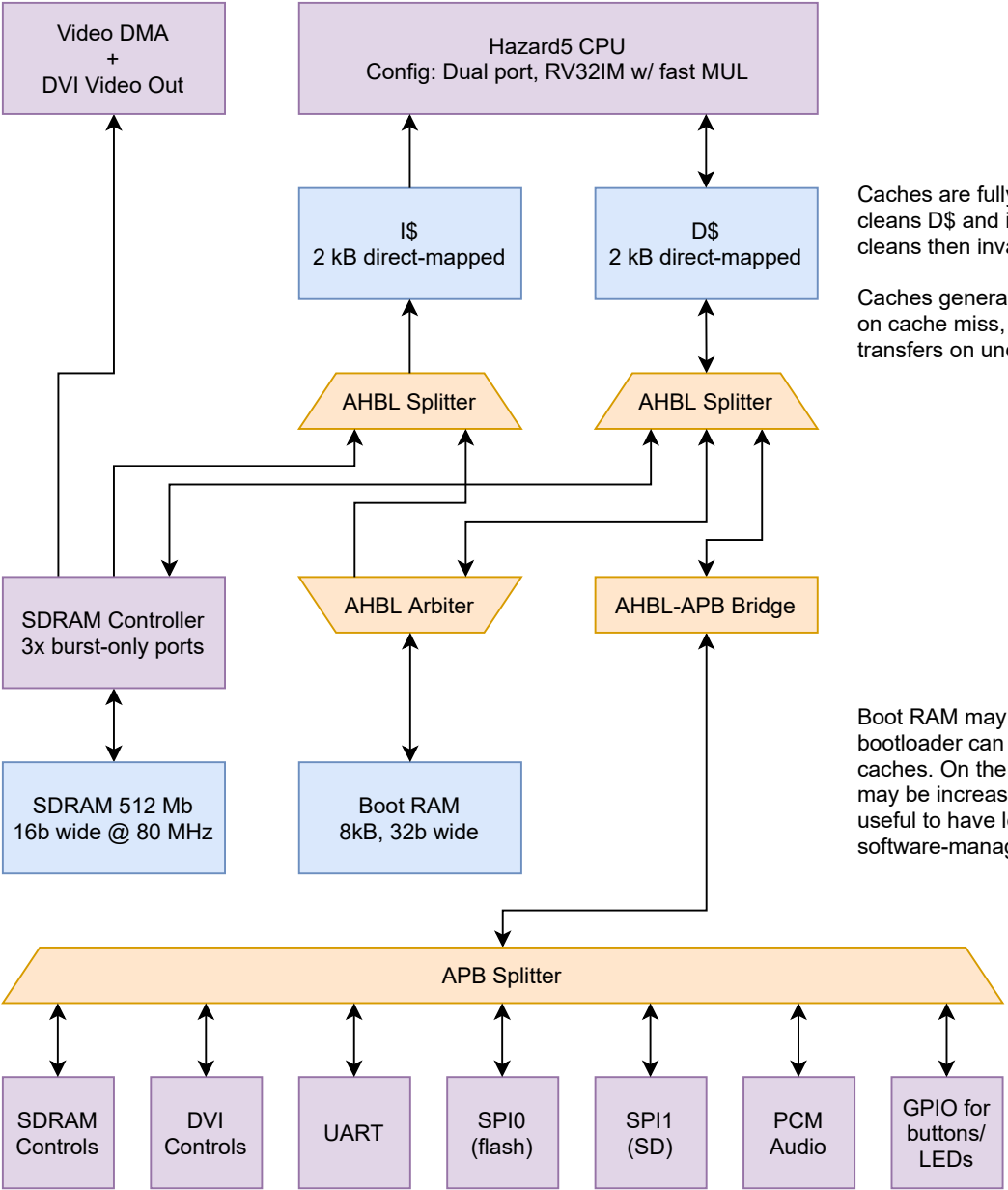

Caches are fully incoherent. FENCE.I cleans D$ and invalidates I$; FENCE cleans then invalidates D$.

Caches generate 4x32b aligned bursts on cache miss, and single 8b/16b/32b transfers on uncached transfers.

Boot RAM may be deleted if the bootloader can be preloaded into the caches. On the other hand its size may be increased if it turns out to be useful to have local RAM as a software-managed L2.