CEA Standard

A DTV Profile for Uncompressed High Speed Digital Interfaces

CEA-861-D

www.CE.org

July 2006

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(Formulated under the cognizance of the CEA R4.8 DTV Interface Subcommittee.)

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FOREWORD

This standard was developed under the auspices of the Consumer Electronics Association (CEA) R4.8 DTV Interface Subcommittee.

CEA-861-D supersedes CEA-861-C.

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A DTV Profile for Uncompressed High Speed Digital Interfaces

1 Scope

CEA-861-D establishes protocols, requirements, and recommendations for the utilization of uncompressed digital interfaces by consumer electronics devices such as digital televisions (DTVs), digital cable, satellite or terrestrial set-top boxes (STBs), and related peripheral devices including, but not limited to DVD players/recorders, and other related source or sink devices.

CEA-861-D is applicable to a variety of standard DTV-related high-speed digital physical interfaces - such as Digital Visual Interface (DVI) 1.0 [3], Open LVDS Display Interface (LDI) [7], and High-Definition Multimedia Interface (HDMI) [29] specifications. Protocols, requirements, and recommendations that are defined include video formats and waveforms; colorimetry and quantization; transport of compressed and uncompressed, as well as Linear Pulse Code Modulation (LPCM), audio; carriage of auxiliary data; and implementations of the Video Electronics Standards Association (VESA*) Enhanced Extended Display Identification Data Standard* (E-EDID) [9], which is used by sink devices to declare display capabilities and characteristics.

CEA-861-D adopters are strongly encouraged to implement High-bandwidth Digital Content Protection (HDCP) [2] content protection defined by the Digital Content Protection (DCP), LLC) method, in order to be compatible with digital cable STBs as authorized by 47 C.F.R. § 76.602 [27] and 47 C.F.R. §76.640 [28]. HDCP [29] permits viewing of high-value content that may be available from other video sources in a home network.

2 General

2.1 References

CEA-861-D includes mechanisms that allow a digital video source (such as a cable, satellite or terrestrial STB, digital VCR, or DVD player) to supply displayable, baseband, digital video to High Definition Television (HDTV) monitors and Enhanced Definition Television (EDTV) monitors (DTV Monitors), as defined in *CEA Expands Definitions for Digital Television Products* [16].

2.1.1 Normative References

The following standards contain provisions that, through reference in this text, constitute normative provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed in Sec. 2.1.1.1. If the referenced standard is dated, the reader is advised to use the version specified.

2.1.1.1 Normative Reference List[1]

1. ANSI/SMPTE 170M-2004, *Composite Analog Video Signal—NTSC for Studio Applications*
2. DCP, L.L.C., *HDCP Specification*, Revision 1.1, June 9, 2003
3. DDWG, *Digital Visual Interface*, Revision 1.0, April 2, 1999
4. IEC 61966-2-4: *Multimedia systems and equipment - Colour measurement and management - Part 2-4: Colour management - Extended-gamut YCC colour space for video applications*, January 2006
5. ITU-R BT.601-5, *Studio Encoding parameters of digital television for standard 4:3 and wide-screen 16:9 aspect ratios*, 1995
6. ITU-R BT.709-5, *Parameter Values for the HDTV standards for production and International Programme Exchange*, 2002
7. *Open LVDS Display Interface (Open LDI) Specification*, Version 0.95, May 13, 1999
8. VESA E-DDC™ Standard, *VESA Enhanced Display Data Channel Standard*, Version 1.1, March 24, 2004

[1] In some instances, only specified sections of a standard may be normative. References listed below shall take precedence over references within these listed references.

9. VESA E-EDID™ Standard, *VESA Enhanced Extended Display Identification Data Standard*, Release A, Revision 1, February 9, 2000
10. VESA Monitor Timing Specifications, *VESA and Industry Standards and Guidelines for Computer Display Monitor Timing* (DMT), Version 1.0, Revision 10, Adoption Date: October 29, 2004

2.1.1.2 Normative Reference Acquisition

ANSI/CEA Standards

- Global Engineering Documents, World Headquarters, 15 Inverness Way East, Englewood, CO USA 80112-5776; Phone 800-854-7179; Fax 303-397-2740
  URL global.ihs.com; Email global@ihs.com

ANSI/SMPTE Standards

- Society of Motion Picture and Television Engineers, 595 W. Hartsdale Avenue, White Plains, NY 10607-1824, Phone 914-761-1100, Fax 914-761-3115 URL http://www.smpte.org

DDWG

- Contact Digital Display Working Group (DDWG); Attn: DDWG Administrator; M/S JF3-361; 2111 NE 25th Avenue, Hillsboro, OR 97124-5961, USA; Fax: (503)264-5959; Email: ddwg.if@intel.com; URL: http://www.ddwg.org

HDCP

- Contact Digital Content Protection, L.L.C., c/o Intel Corporation, Stephen Balogh, JF2-55; 2111 NE 25th Ave; Hillsboro, OR 97124; Email: info@digital-cp.com ; URL: http://www.digital-cp.com/home; EMail: info@digital-cp.com; URL: www.digital-cp.com

ITU Standards

- International Telecommunications Union, Place des Nations, CH-1211 Geneva 20, Switzerland; Phone +41 22 730 5111; Fax +41 22 733 7256
  URL http:// www.itu.int/publications/default.aspx ; Email itumail@itu.int

OpenLDI

- Contact National Semiconductor: WWW.National.com/appinfo/fpd

VESA Standards

- Contact Video Electronics Standards Association, 860 Hillview Court, Suite 150, Milpitas, CA 95035, USA; telephone: (408) 957-9270 ; URL http://www.vesa.org

2.1.2 Informative References

The following documents contain information that is useful in understanding this standard. At the time of publication, the editions indicated were valid. All documents are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the documents listed in Section 2.1.2.1. Some of these documents are drafts of standards that may become normative references in a future release of this standard.

2.1.2.1 Informative Document List

11. ANSI/SMPTE Standard 253M (1998), *Standard for Television—Three-Channel RGB Analog Video Interface*
12. ANSI/SMPTE Standard 274M (2005), *SMPTE Standard for Television—1920x1080 Image Sample Structure, Digital Representation and Digital Timing Reference Sequences for Multiple-Picture Rates*
13. ANSI/SMPTE Standard 293M (2003), *SMPTE Standard for Television—720x483 Active Line at 59.94 Hz Progressive Scan Production—Digital Representation*
14. ANSI/SMPTE 296M (2001), *Standard for Television—1280x720 Scanning, Analog and Digital Representation and Analog Interface*
15. ATSC Standard A/52B, *Digital Audio Compression (AC-3) Standard*, June 14, 2005
16. CEA Press Release; *CEA Expands Definitions for Digital Television Products*; August 31, 2000
17. CEA-608-C, *Line 21 Data Service*, August 2005
18. CEA-708-C, *Digital Television (DTV) Closed Captioning,* July, 2006

19. CEA-770.2-C, *Standard Definition TV Analog Component Video Interface*, August 2001
20. CEA-770.3-C, *High Definition TV Analog Component Video Interface*, August 2001
21. CEA-849-A, *Application profiles for EIA-775-A compliant DTVs*, December 2001
22. CEA-CEB16, *Automatic Format Description (AFD) and Bar Data*, July, 2006
23. *DTS-HD Product Certification Manual*, Version 1.0, DTS, Inc., 2006
24. DVD Forum, *DVD Specifications for Read-Only Disc, Part3, Video Specifications*, Version 1.0, August 1996
25. DVD Forum, *DVD Specifications for Read-Only Disc, Part 4, Audio Specifications*, Version 1.0
26. ETSI TS 101 154 v1.7.1, *Digital Video Broadcasting (DVB); Implementation guidelines for the use of Video and Audio Coding in Broadcasting Applications based on the MPEG-2 Transport Stream (Annex B)*, June 14, 2005
27. FCC Regulations, Part 76, *Cable Television Service*, 47 C.F.R. §76.602
28. FCC Regulations, Part 76, *Cable Television Service*, 47 C.F.R. §76.640
29. *High-Definition Multimedia Interface Specification*, Version 1.2a, December 14, 2005
30. IEC 60958-1 *Digital Audio Interface - Part 1: General*, First Edition, 1999
31. IEC 60958-3 *Digital Audio Interface - Part 3: Consumer Applications*, First Edition, 1999
32. IEC 61937 *Digital Audio - Interface for non-linear PCM encoded audio bitstreams applying IEC 60958*, First Edition, 2000
33. IEC 61966-2-1 (1999-10) *Multimedia systems and equipment - Colour measurement and management - Part 2-1: Colour management - Default RGB colour space – sRGB*
34. ISO/IEC 11172-3:1993, *Information Technology - Coding of moving pictures and associated audio for digital storage media at up to about 1.5 Mbit/sec*, Part 3: Audio, 1993
35. ISO/IEC 13818-3, *Information Technology - Generic coding of moving pictures and associated audio information, Part 3: Audio*, Second Edition, 1998-04-15
36. ISO/IEC 14496-3, *Information Technology - Coding of audio-visual objects - Part 3: Audio, Amendment 1: Audio Extensions*, 2000-09-15
37. ISO/IEC 14496-3:2001, *Information Technology – Coding of audio-visual objects – Part 3: Audio, Amendment 6: Lossless Coding of Oversampled Audio*
38. ITU-R BT.470–6, *Conventional Television Systems*, 1998
39. ITU-R BT.656–4, *Interfaces for Digital Component Video Signals in 525-line and 625-line Television Systems Operating at the 4:2:2 Level of Recommendation*, 1998
40. ITU-R BT.711–1, *Synchronizing Reference Signals for the Component Digital Studio*, 1992
41. ITU-R BT.1358, *Studio Parameters of 625 and 525 Line Progressive Scan Television Systems*, 1998
42. Royal Philips Electronics and Sony Corporation, *Super Audio CD System Description,* Version 2.0
43. VESA *Coordinated Video Timings (CVT)*, Version 1.1, September 10, 2003
44. VESA DDC/CI Standard, *VESA Display Data Channel Command Interface (DDC/CI) Standard*, Version 1.1, October 29, 2004
45. VESA DI-EXT, *Display Information Extension Block (DI-EXT™) for E-EDID,* Release A, August 21, 2001
46. VESA E-EDID™ Implementation Guide, *VESA Enhanced Extended Display Identification Data—Implementation Guide*, Version 1.0, June 4, 2001
47. VESA GTF Standard, *VESA Generalized Timing Formula Standard*, Version 1.1, September 2, 1999.
48. *WMA Pro*, May 2006

2.1.2.2 Informative Document Acquisition

CEA Standards

- Global Engineering Documents, World Headquarters, 15 Inverness Way East, Englewood, CO USA 80112-5776; Phone 800-854-7179; Fax 303-397-2740
  URL global.ihs.com; Email global@ihs.com

ETSI
- European Telecommunications Standards Institute, 650, route des Lucioles, 06921 Sophia-Antipolis Cedex, France; Phone +33 (0)4 92 94 42 00; Fax +33 (0)4 93 65 47 16; URL http://www.etsi.org/#

FCC
- FCC Regulations, U.S. Government Printing Office, Washington, D.C. 20401; Internet http://www.access.gpo.gov/cgi-bin/cfrassemble.cgi?title=199847

HDMI
- HDMI Licensing, LLC, 1060 E. Arques Avenue, Suite 100, Sunnyvale, CA 94085; URL http://www.hdmi.org

ITU Standards
- International Telecommunications Union, Place des Nations, CH-1211 Geneva 20, Switzerland; Phone +41 22 730 5111; Fax +41 22 733 7256
  URL http:// www.itu.int/publications/default.aspx; Email itumail@itu.int

Royal Philips Electronics and Sony Corporation, Super Audio CD Description Version 2
- Philips Intellectual Property & Standards; Building WAH, P.O. Box 220, 5600 AE Eindhoven, The Netherlands; Fax +31-40-2732113; URL www.licensing.philips.com

SMPTE Standards
- Society of Motion Picture & Television Engineers (SMPTE), 595 West Hartsdale Avenue, White Plains, NY 10607; Phone 914-761-1100; Fax 914-761-3115
  URL www.smpte.org; Email smpte@smpte.org

VESA Standards
- Contact Video Electronics Standards Association, 860 Hillview Court, Suite 150, Milpitas, CA 95035, USA, telephone (408) 957-9270, http://www.vesa.org

WMA Pro
- See http://www.microsoft.com/windows/windowsmedia/howto/articles/WMAPro_in_CEA861.aspx

2.2 Definitions
For the purposes of CEA-861-D, the following definitions apply.

Active Format Description (AFD)—A data structure that describes what portion of the picture actually contains useful information (i.e., letterbox and sidebars [bars] are not considered useful information). It is standardized in DVB, and is partially adopted in CEA-861-D. Note that the use of the term “active” in this definition is not consistent with the use of this term in other portions of CEA-861-D and most of the other documents referenced by CEA-861-D.

Auxiliary Video Information (AVI)—Additional information (defined in CEA-861-D) related to the video being sent from a source device to a DTV Monitor.

A/V—Audio and Video.

Bars—Region of the display screen that is being driven or scanned at either zero luminance or at a uniform luminance; or regions of a picture that are intended to be driven (e.g., matrix addressed) or scanned (e.g., cathode ray tube (CRT)) at either zero luminance or at a uniform luminance. In other words, it is the portion of the picture that does not contain useful information.

Basic Audio—Uncompressed, two channel, digital audio. Exact parameters are determined by the interface specification used with CEA-861-D (e.g., 2 channel IEC 60958 LPCM, 32, 44.1, and 48 kHz sampling rates, 16 bits/sample).

Byte—8 bits of data.

CE Video Format—Any video format listed in Table 2 except 640x480p.

CEA Extension—The E-EDID Standard [9] defines a VESA-assigned tag (02_{16}) that allows for an extension to be added with additional timing formats.

Compressed Audio—All audio formats other than LPCM and One Bit Audio.

Digital Television (DTV)—A device that receives, decodes, and presents audio and video material that has been transmitted in a compressed form. The device can be a single unit or it can be constructed from a number of individual components (e.g. a digital terrestrial STB and an analog television).

Direct Stream Digital (DSD)—see One Bit Audio.

Direct Stream Transport (DST)—lossless compressed DSD.

DTV Monitor—Defined in CEA-861-D to be an EDTV, HDTV, or SDTV Monitor. A DTV Monitor can also be any combination of these terms. A DTV with an uncompressed video input is also considered a DTV Monitor.

Dual Aspect Ratio DTV Monitor—A DTV Monitor that simultaneously supports both picture aspect ratios of a video format timing (e.g., 720x480p). Simultaneous support is signified by listing both formats in the EDID data structure at the same time.

Dual Aspect Ratio Timing—A video format timing (e.g., 720x480p) that is available in both picture aspect ratios (16:9 and 4:3) with no difference in the timing for the two formats.

EDTV Monitor—A video monitor capable of displaying 720x480p in 16:9 or 4:3 aspect ratios.

Full Quantization Range—RGB quantization range having an R, G and B black level at 0 and white level at 255.

HDTV Monitor—A video monitor capable of displaying 1920x1080i or 1280x720p video in its format on a 16:9 screen. An HDTV Monitor also has EDTV Monitor capabilities.

InfoFrame—A data transfer structure for sending miscellaneous information from a source device to a DTV monitor over a CEA-861-D interface. Various InfoFrames are described in Section 6.

IT Video Format—Any video format that is not a CE video format. Specifically, any format not listed in Table 2 plus 640x480p.

Limited Quantization Range—RGB quantization range having an R, G and B black level at 16 and white level at 235.

Multi-channel Audio—Digital audio with more than two channels, for example, LPCM or AC-3.

Native Display Device Aspect Ratio—Ratio of maximum width to height dimension of the addressable portion of a physical display device screen, which is indicated in the EDID 1.3 block's "Max Horizontal Image Size" and "Max Vertical Image Size" fields.

Native Format—a video format with native pixel layout and scanning method that the display device accepts and displays without any internal scaling, de-interlacing, interlacing or frame rate conversion.

Native Pixel Layout—the exact number of horizontal pixels and vertical lines (or pixel mapping) that matches the physical structure of the display device.

One Bit Audio—1-bit Sigma-Delta (Delta-Sigma) modulated signal stream such as that used by Super Audio CD by the name of DSD (Direct Stream Digital).

Picture—That portion of an uncompressed video signal, a compressed video stream, or a sequence on a display that constitutes a single displayable image (i.e., the addressable picture elements). For the purposes of CEA-861-D, picture refers to the data transferred during a single video frame in the uncompressed video signal.

Picture Aspect Ratio—Ratio of width to height dimension of the picture as delivered across the uncompressed digital interface, including any top, bottom, or side bars. Only two Picture Aspect Ratios are specified for this interface, 16:9 and 4:3.

Preferred Picture Aspect Ratio—In a Dual Aspect Ratio DTV Monitor, the preferred aspect ratio of a given Video Format Timing (e.g., 720x480p) is the aspect ratio of the first such timing listed in the EDID data structure (see Section 4.1). This would be the picture aspect ratio that would be displayed if a DTV Monitor were to receive a Video Format Timing with no accompanying picture aspect ratio information (i.e., no AVI sent from source).

Preferred Video Format—the video format that a display manufacturer determines provides optimum image.

NOTE—Source implementers are encouraged to review Section 7.2.3 for related guidance.

RGB—A general representation of an analog or digital component video signal, where R represents the red color, G represents green, and B represents blue; and each component is sampled at a uniform rate (4,4,4). For the purpose of CEA-861-D, the signal is digital.

Sink—a device which receives an uncompressed A/V signal.

Source—a device which generates an uncompressed A/V signal.

Source Pass-through Mode—A mode supported by some media-based sources, wherein decompressed video passes directly (in its original format) to a sink device without deinterlacing, scaling, or frame rate conversion.

Standard Definition Television (SDTV) Monitor—A video monitor capable of displaying 720x480i video in at least one of two aspect ratios, 16:9 or 4:3.

Uncompressed Audio—Linear Pulse Code Modulated (LPCM) and One Bit Audio.

Video Field—The period between two vertical syncs (VSYNCs) or the timing pattern associated with that period.

Video Format—A video format is sufficiently defined such that when it is received at the DTV Monitor, the DTV Monitor has enough information to properly display the video to the user. The definition of each format includes a Video Format Timing, the Picture Aspect Ratio, Colorimetry Space, and Quantization levels.

Video Format Timing—The waveform associated with a video format. Note that a specific Video Format Timing may be associated with more than one Video Format (e.g., 720x480p@4:3 and 720x480p@16:9).

Video Frame—The period (beginning where the active edges of horizontal and vertical sync align) for vertical total lines of timing. Interlaced timings have two video fields per video frame, while progressive timings have only one. Therefore, in the case of progressive timings, the terms video field and video frame are synonymous.

YC_BC_R—A general representation of a digital component video signal, where Y represents luminance, C_B represents the color blue, and C_R represents red; The color component may be sub-sampled at half the rate as luminance (4:2:2) or may be sampled at a uniform rate (4:4:4). For the purposes of CEA-861-D, it may be considered a digital representation of YP_BP_R.

2.3 Symbols and Abbreviations

AAC	Advanced Audio Coding
AFD	Active Format Description
ANSI	American National Standards Institute
ATRAC	Adaptive Transform Acoustic Coding
A/V	Audio/Video
AR	Aspect Ratio
AV/C	Audio/Video Control
AVI	Auxiliary Video Information
BD	Blu-Ray Disc
CD	Compact Disk
CEA	Consumer Electronics Association
CRT	Cathode Ray Tube
DAC	Digital to Analog Converter
DBS	Direct Broadcast Satellite
DDWG	Digital Display Working Group
DMT	Display Monitor Timing specification [10])
DSC	Digital Still Camera
DSD	Direct Stream Digital
DST	Direct Stream Transport
DTD	Detailed Timing Descriptor
DTS	Digital Theater System
DTV	Digital Television
DVC	Digital Video Camera
DVD	Digital Versatile Disk
D-VHS	Digital VHS
DVI	Digital Visual Interface [3]
E-DDC	Enhanced Display Data Channel
E-EDID	Enhanced Extended Display Identification Data Standard
EDTV	Enhanced Definition Television
EUI	Extended Unique Identifier
HDCP	High-bandwidth Digital Content Protection [2]
HDD	Hard Disk Drive
HDMI	High-Definition Multimedia Interface
HDTV	High Definition Television
HPD	Hot Plug Detect
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IRE	Percent of white with respect to black
ISO	International Organization for Standardization
ITU	International Telecommunications Union
LCD	Liquid Crystal Display
LDI	LVDS Display Interface
LPCM	Linear Pulse Code Modulation
lsb	least significant bit
MAT	MLP Audio Transport
MLP	Meridian Lossless Packing
LVDS	Low Voltage Differential Signaling
MPEG	Moving Picture Experts Group
msb	most significant bit

OpenLDI	Open LVDS Display Interface [7]
OUI	Organizationally Unique Identifier
SACD	Super Audio CD
SADB	Speaker Allocation Data Block
SDTV	Standard Definition Television
SMPTE	Society of Motion Picture & Television Engineers
STB	Set-Top Box
SVD	Short Video Descriptor
VCR	Video Cassette Recorder
VESA	Video Electronics Standards Association
VSDB	Vendor Specific Data Block
WMA Pro	Windows Media Audio Professional

2.4 Compliance Notation

As used in this document, *"shall"* denotes mandatory provisions of the standard. *"Should"* denotes a provision that is recommended but not mandatory. *"May"* denotes a feature whose presence does not preclude compliance and implementation of which is optional. *"Optional"* denotes items that may or may not be present in a compliant device.

3 Overview

CEA-861-D describes requirements for video sources and DTV Monitors that include an uncompressed, baseband, digital video interface. These requirements apply to any baseband digital video interface that makes use of VESA E-EDID (structures for discovery of supported video formats) [9] and supports 24-bit RGB. The 60 Hz/59.94 Hz video timings are based on analog formats already standardized in CEA-770.2-C [19] and CEA-770.3-C [20]. A preferred physical/link interface is not specified in CEA-861-D. See the annexes on how to apply CEA-861-D to the individual interfaces available at the time of this writing. Digital Visual Interface (DVI 1.0) [3] and OpenLDI 0.95 [7] can be used to enable minimal digital interface functionality. To take advantage of these enhancements, the physical interface also needs a way to transport CEA InfoFrames, digital audio, and YC_BC_R pixels from the source device to the DTV Monitor. The High-Definition Multimedia Interface (HDMI) [29] is now available to take advantage of these enhancements.

Enhanced Extended Display Identification Data (E-EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which would be stored in the DTV Monitor, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The source device (e.g., STB) is responsible for the format conversions necessary to supply video in an understandable form to the DTV Monitor.

CEA-861-D includes the sink device's ability to describe other capabilities in the E-EDID, in addition to supported video formats (e.g., digital audio). In those cases, the same basic mechanism applies (i.e., the source device reads EDID data in the DTV Monitor to determine its capabilities and then the source device only sends what the DTV Monitor can understand).

The physical/link standards in Annex B, Annex C and Annex D do not support transport of closed captioning (CEA-608-C and CEA-708-C); therefore, the source device processes these elements. Specifically, if closed captioning is to be displayed, it is decoded by the source device, inserted into the video and displayed as open captions. Similarly, if system Information, program information, events, service descriptors, etc. are displayed, related graphical information is inserted into the video by the source device. Control of closed captioning settings, programs, events, etc. is a feature of the source device, not supported by this interface and beyond the scope of CEA-861-D.

Furthermore, content advisory user menus, settings and blocking are accommodated in the source device, and are beyond the scope of CEA-861-D.

3.1 General Video Format Requirements

Any DTV monitor complying with CEA-861-D shall support 640x480p [10]. Additionally, any DTV Monitor complying with CEA-861-D shall also support 720x480p or 720x576p in both of the two picture aspect ratios (4:3 and 16:9) as defined in Section 4.5 or Section 4.9. Additionally, any HDTV Monitor complying with CEA-861-D shall also support either 1920x1080i or 1280x720p (with a 16:9 picture aspect ratio) as defined in Sections 4.3 and 4.4 or Sections 4.7 and 4.8.[2] Formats for 720x480i and 720x576i are also defined in CEA-861-D, and are optional.

Table 1 summarizes display requirements specified by CEA-861-D. Incorporated in the same table are recommendations for source devices. These recommendations are based on the CEA's Definitions for Digital Television Products [16]. In the table, the CEA term *tuner* refers to a device that decodes a digital video signal that has been modulated onto an RF carrier and outputs video. To comply with CEA-861-D, a source device does not have to be a tuner.

[2] This implicitly allows any source device (intended to supply content to such a DTV Monitor) to only support 720x480p (720x576p for 50 Hz systems) or 640x480p. For the source device to be able to supply high definition content to any HDTV Monitor, it must be capable of supporting 1920x1080i and 1280x720p since the HDTV Monitor may support only one of the two formats. It implies that, in some cases, the source device (e.g., STB) would need to convert the video from the format at its input (e.g., 720x480i) to one of the formats supported by the DTV over this interface (e.g., 720x480p). For additional guidance for source devices see Table 1 and Section 7.2.3.

60 Hz Systems

CEA Definition	Video Format	EDTV Monitor (Display)	HDTV Monitor (Display)	EDTV Tuner (Source)	HDTV Tuner (Source)
SDTV	720(1440)x480i @ 60 Hz	O	O	O	O
EDTV	640x480p @ 60 Hz	✗	✗	✔*	✔*
EDTV	720x480p @ 60 Hz	✗	✗		
HDTV	1280x720p @ 60 Hz	O	✗*	O	✔
HDTV	1920x1080i @ 60 Hz	O		O	✔

50 Hz Systems

CEA Definition	Video Format	EDTV Monitor (Display)	HDTV Monitor (Display)	EDTV Tuner (Source)	HDTV Tuner (Source)
SDTV	720(1440)x576i @ 50 Hz	O	O	O	O
EDTV	640x480p @ 60 Hz	✗	✗	✔*	✔*
EDTV	720x576p @ 50 Hz	✗	✗		
HDTV	1280x720p @ 50 Hz	O	✗*	O	✔
HDTV	1920x1080i @ 50 Hz	O		O	✔

Legend

✗	Required by CEA-861-D
✗*	Either one of the two formats is required, the other is optional
✔	Recommended by CEA-861-D and implied by CEA DTV definitions
✔*	Either one of the two formats is recommended, the other is optional
O	Optional

Table 1 Video Format Timings—Support Requirements and Recommendations

4 Video Formats and Waveform Timings

Throughout CEA-861-D, the term “video format timing” (or shorthand “video timing”) does not include aspect ratio, whereas the term “video format” does encompass the aspect ratio.

To support the 720x480i, 720x576i, 720x240p or 720x288p video timings, the pixels are double clocked for each line to meet the minimum speed requirements of the interface. Thus, 720x480i is referred to as (1440)x480i in Table 3, 720x576i is referred to as (1440)x576i, 720x240p is referred to as (1440)x240p,

and 720x288p is referred to as (1440)x288p. Additionally, the “2880” timings ((2880)x480i, (2880)x240p, (2880)x576i, and (2880)x288p) each represent a family of formats in which the pixels are repeated a number of times. The number of times that the pixel is repeated is sent to the DTV Monitor by the source device.

For 60 Hz systems, the DTV Monitor shall be capable of displaying either 59.94 or 60 Hz (frame rate for progressive scan and field rate for interlaced scan) for the formats that it supports. Therefore, the 59.94 Hz and 60 Hz versions of a video format shall be considered the same video format with slightly different pixel clocks.

The additional low-resolution progressive video format timings (1440x240p, 2880x240p, 1440x288p, and 2880x288p) consist of one of several frame formats. These frame formats differ only by one or two scan lines in the vertical blanking interval. For that reason, they are treated as the same video format with a slight variation in the parameters (i.e., handled in a way similar to the 59.94Hz/60Hz formats). For this reason, if a DTV Monitor declares support of one of these video formats of a specific picture aspect ratio (through EDID), then it shall support all variations of that video format of the same picture aspect ratio. The mandatory and optional formats defined in CEA-861-D shall comply with the timing parameters in Table 2.

									(kHz)	(Hz)	(MHz)
	Code	H active	V active	I/P	H total	H blank[5]	V total	V blank[5]	H Freq[5]	V Freq[4]	Pixel Freq[5]
Low Field Rate	32	1920	1080	Prog	2750	830	1125	45	26.973	23.976	74.176
	32	1920	1080	Prog	2750	830	1125	45	27.000	24.000[3]	74.250
	33	1920	1080	Prog	2640	720	1125	45	28.125	25.000	74.250
	34	1920	1080	Prog	2200	280	1125	45	33.716	29.970	74.176
	34	1920	1080	Prog	2200	280	1125	45	33.750	30.000[3]	74.250
50Hz	17,18	720	576	Prog	864	144	625	49	31.250	50.000	27.000
	19	1280	720	Prog	1980	700	750	30	37.500	50.000	74.250
	20	1920	1080	Int	2640	720	1125	22.5[1]	28.125	50.000	74.250
	21,22	1440[2]	576	Int	1728[2]	288	625	24.5[1]	15.625	50.000	27.000
	23,24	1440[2]	288	Prog	1728[2]	288	312	24	15.625	50.080	27.000
	23,24	1440[2]	288	Prog	1728[2]	288	313	25	15.625	49.920	27.000
	23,24	1440[2]	288	Prog	1728[2]	288	314	26	15.625	49.761	27.000
	25,26	2880[2]	576	Int	3456[2]	576	625	24.5[1]	15.625	50.000	54.000
	27,28	2880[2]	288	Prog	3456[2]	576	312	24	15.625	50.080	54.000
	27,28	2880[2]	288	Prog	3456[2]	576	313	25	15.625	49.920	54.000
	27,28	2880[2]	288	Prog	3456[2]	576	314	26	15.625	49.761	54.000
	29,30	1440[2]	576	Prog	1728[2]	288	625	49	31.250	50.000	54.000
	31	1920	1080	Prog	2640	720	1125	45	56.250	50.000	148.500
	37,38	2880[2]	576	Prog	3456[2]	576	625	49	31.250	50.000	108.000
	39	1920	1080	Int	2304	384	1250	85	31.250	50.000	72.000
59.94Hz	1	640	480	Prog	800	160	525	45	31.469	59.940	25.175
	2,3	720	480	Prog	858	138	525	45	31.469	59.940	27.000
	4	1280	720	Prog	1650	370	750	30	44.955	59.940	74.176
	5	1920	1080	Int	2200	280	1125	22.5[1]	33.716	59.940	74.176
	6,7	1440[2]	480	Int	1716 [2]	276	525	22.5[1]	15.734	59.940	27.000
	8,9	1440[2]	240	Prog	1716 [2]	276	262	22	15.734	60.054	27.000
	8,9	1440[2]	240	Prog	1716 [2]	276	263	23	15.734	59.826	27.000
	10,11	2880[2]	480	Int	3432 [2]	552	525	22.5[1]	15.734	59.940	54.000
	12,13	2880[2]	240	Prog	3432 [2]	552	262	22	15.734	60.054	54.000
	12,13	2880[2]	240	Prog	3432 [2]	552	263	23	15.734	59.826	54.000
	14,15	1440	480	Prog	1716	276	525	45	31.469	59.940	54.000
	16	1920	1080	Prog	2200	280	1125	45	67.433	59.940	148.352
	35,36	2880[2]	480	Prog	3432[2]	552	525	45	31.469	59.940	108.000

Table 2 Video Format Timings—Detailed Timing Information

									(kHz)	(Hz)	(MHz)
	Code	H active	V active	I/P	H total	H blank[5]	V total	V blank[5]	H Freq[5]	V Freq[4]	Pixel Freq[5]
60Hz[3]	1	640	480	Prog	800	160	525	45	31.500	60.000	25.200
	2,3	720	480	Prog	858	138	525	45	31.500	60.000	27.027
	4	1280	720	Prog	1650	370	750	30	45.000	60.000	74.250
	5	1920	1080	Int	2200	280	1125	22.5[1]	33.750	60.000	74.250
	6,7	1440[2]	480	Int	1716[2]	276	525	22.5[1]	15.750	60.000	27.027
	8,9	1440[2]	240	Prog	1716[2]	276	262	22	15.750	60.115	27.027
	8,9	1440[2]	240	Prog	1716[2]	276	263	23	15.750	59.886	27.027
	10,11	2880[2]	480	Int	3432[2]	552	525	22.5[1]	15.750	60.000	54.054
	12,13	2880[2]	240	Prog	3432[2]	552	262	22	15.750	60.115	54.054
	12,13	2880[2]	240	Prog	3432[2]	552	263	23	15.750	59.886	54.054
	14,15	1440[2]	480	Prog	1716[2]	276	525	45	31.500	60.000	54.054
	16	1920	1080	Prog	2200	280	1125	45	67.500	60.000	148.500
	35,36	2880	480	Prog	3432	552	525	45	31.500	60.000	108.108
100 Hz	40	1920	1080	Int	2640	720	1125	22.5[1]	56.250	100.00	148.500
	41	1280	720	Prog	1980	700	750	30	75.000	100.00	148.500
	42, 43	720	576	Prog	864	144	625	49	62.500	100.00	54.000
	44, 45	1440[2]	576	Int	1728[2]	288	625	24.5[1]	31.250	100.00	54.000
119.88 Hz	46	1920	1080	Int	2200	280	1125	22.5[1]	67.432	119.88	148.352
	47	1280	720	Prog	1650	370	750	30	89.909	119.88	148.352
	48, 49	720	480	Prog	858	138	525	45	62.937	119.88	54.000
	50, 51	1440[2]	480	Int	1716[2]	276	525	22.5[1]	31.469	119.88	54.000
120 Hz[3]	46	1920	1080	Int	2200	280	1125	22.5[1]	67.500	120.00	148.500
	47	1280	720	Prog	1650	370	750	30	90.000	120.00	148.500
	48, 49	720	480	Prog	858	138	525	45	63.000	120.00	54.054
	50, 51	1440[2]	480	Int	1716[2]	276	525	22.5[1]	31.500	120.00	54.054
200 Hz	52, 53	720	576	Prog	864	144	625	49	125.000	200.00	108.00
	54, 55	1440[2]	576	Int	1728[2]	288	625	24.5[1]	62.500	200.00	108.00
239 Hz	56, 57	720	480	Prog	858	138	525	45	125.874	239.76	108.000
	58, 59	1440[2]	480	Int	1716[2]	276	525	22.5[1]	62.937	239.76	108.000

Table 2 Video Format Timings—Detailed Timing Information (Continued)

									(kHz)	(Hz)	(MHz)
	Code	H active	V active	I/P	H total	H blank[5]	V total	V blank[5]	H Freq[5]	V Freq[4]	Pixel Freq[5]
240 Hz[3]	56,57	720	480	Prog	858	138	525	45	126.000	240.00	108.108
	58,59	1440[2]	480	Int	1716[2]	276	525	22.5[1]	63.000	240.00	108.108

1 V blanking—Fractional values indicate that the number of blanking lines varies (see timing diagram for more details).

2 Note: the pixels for the 720xN 480i, 240p, 576i, and 288p formats (where N is the number of lines) are double clocked for each line to meet minimum speed requirements of the interface, thus H active is shown as 1440, instead of 720. Each pixel of the 1440xN 480p and 576p formats, as well as the 2880xN 480i, 240p, 480p, 576i, 288p, and 576p formats, is repeated a variable number of times. The repeat value is communicated using the AVI InfoFrames (see Section 6.4).

3 Format Note: For 60 Hz formats, displays respond automatically to either 60 Hz or 59.94 Hz (same format with slightly different clocks). The 25.2 MHz pixel frequency value is within the ± 0.5% (allowed in the VESA DMT [10]) of 25.175 MHz. The 480p formats and the 480i formats are typically 59.94 Hz, and the HDTV formats are typically 60 Hz.

4 To avoid fractional frame rate conversions in source and sink devices, source devices should use the exact vertical frequencies of 25.000 Hz, 50.000 Hz, 100.000 Hz, 120.000 Hz, 200.000 Hz, and 240.000 Hz at 25 Hz, 50 Hz, 100 Hz, 120 Hz, 200 Hz, and 240 Hz, respectively. Likewise, source devices should use the exact vertical frequencies of (24 * 1000) / 1001 Hz, (30 * 1000) / 1001 Hz, (60 * 1000) / 1001 Hz, (120 * 1000) / 1001 Hz, and (240 * 1000) / 1001 Hz at 24.98 Hz, 29.97 Hz, 59.94 Hz, 119.88 Hz, 239.76 Hz, respectively."

5 Data in this column is provided for informational purposes only.

Table 2 Video Format Timings—Detailed Timing Information (Continued)

4.1 Aspect Ratio

A DTV Monitor should always indicate its native (physical) aspect ratio in the EDID 1.3 block's "Max Horizontal Image Size" and "Max Vertical Image Size" fields even if the maximum image size is unknown or variable. Typically, the ratio of these two fields is 16:9 or 4:3 though this may not be true for some displays with non-standard aspect ratios. The source should use these fields to determine the native aspect ratio of the display.

The 480p, 480i, 240p, 576p, 576i, and 288p formats are available in two different aspect ratios (4:3 and 16:9). Video formats with the same timing, but different picture aspect ratios are considered different formats that can be independently supported and discovered. These are referred to as dual-aspect ratio timings.

For any dual-aspect ratio video timing, the Preferred Picture Aspect Ratio for that timing is indicated by the first listing of that timing in the EDID. When receiving a signal not accompanied by an aspect ratio indication (because no AVI InfoFrame is transmitted) a DTV Monitor shall assume that the aspect ratio is the Primary Picture Aspect Ratio for the transmitted video timing.

If a Dual Aspect Ratio DTV Monitor is receiving a video format timing for which it has declared support for both picture aspect ratios in EDID and the source device has indicated the picture aspect ratio by including the AVI in the video stream, then the DTV Monitor shall display the picture in the aspect ratio that has been indicated by the source device in the AVI. If the source device does not support transmission of the AVI, then the source device shall provide the video to the DTV monitor in the preferred aspect ratio.

For a display device to simultaneously support both formats, the source device needs a way to let the display device know the picture aspect ratio in which the video should be displayed. A DTV Monitor shall

list only one picture aspect ratio of any dual-aspect ratio timing unless it is capable of receiving and decoding the AVI InfoFrame defined in Section 6.

However, it is possible for a DTV Monitor that has no support for the AVI InfoFrame to still support both aspect ratios of such formats as a user programmable option. In that case, the EDID Detailed Timing Descriptor could be modified during operation to reflect the selected picture aspect ratio and the change could be signaled to the source (e.g. with Hot Plug Detect on DVI or HDMI).

The effects on the EDID data structure are explained in Section 7.2.2. See Table 3 for Video ID Code and Aspect Ratios.

Video ID Code	Formats	Field Rate	Picture Aspect Ratio (H:V)[1]	Pixel Aspect Ratio (H:V)
1	640x480p	59.94Hz/60Hz	4:3	1:1
2	720x480p	59.94Hz/60Hz	4:3	8:9
3	720x480p	59.94Hz/60Hz	16:9	32:27
4	1280x720p	59.94Hz/60Hz	16:9	1:1
5	1920x1080i	59.94Hz/60Hz	16:9	1:1
6	720(1440)x480i	59.94Hz/60Hz	4:3	8:9
7	720(1440)x480i	59.94Hz/60Hz	16:9	32:27
8	720(1440)x240p	59.94Hz/60Hz	4:3	4:9
9	720(1440)x240p	59.94Hz/60Hz	16:9	16:27
10	2880x480i	59.94Hz/60Hz	4:3	2:9 - 20:9[3]
11	2880x480i	59.94Hz/60Hz	16:9	8:27 -80:27
12	2880x240p	59.94Hz/60Hz	4:3	1:9 - 10:9
13	2880x240p	59.94Hz/60Hz	16:9	4:27 - 40:27
14	1440x480p	59.94Hz/60Hz	4:3	4:9
15	1440x480p	59.94Hz/60Hz	16:9	16:27
16	1920x1080p	59.94Hz/60Hz	16:9	1:1
17	720x576p	50Hz	4:3	16:15
18	720x576p	50Hz	16:9	64:45
19	1280x720p	50Hz	16:9	1:1
20	1920x1080i	50Hz	16:9	1:1
21	720(1440)x576i	50Hz	4:3	16:15
22	720(1440)x576i	50Hz	16:9	64:45
23	720(1440)x288p	50Hz	4:3	8:15
24	720(1440)x288p	50Hz	16:9	32:45
25	2880x576i	50Hz	4:3	2:15 - 20:15
26	2880x576i	50Hz	16:9	16:45-160:45
27	2880x288p	50Hz	4:3	1:15 - 10:15
28	2880x288p	50Hz	16:9	8:45 - 80:45
29	1440x576p	50Hz	4:3	8:15
30	1440x576p	50Hz	16:9	32:45
31	1920x1080p	50Hz	16:9	1:1
32	1920x1080p	23.97Hz/24Hz	16:9	1:1
33	1920x1080p	25Hz	16:9	1:1
34	1920x1080p	29.97Hz/30Hz	16:9	1:1
35	2880x480p	59.94Hz/60Hz	4:3	2:9
36	2880x480p	59.94Hz/60Hz	16:9	8:27

[3] Although the pixel repeat field is 4 bits (see Section 6.4), the largest value used for typical formats is 10. Therefore, in this standard the pixel repeat value can vary from 1 to 10. This results in a factor of 10 variations in the Pixel Aspect Ratio.

Video ID Code	Formats	Field Rate	Picture Aspect Ratio (H:V)[1]	Pixel Aspect Ratio (H:V)
37	2880x576p	50Hz	4:3	4:15
38	2880x576p	50Hz	16:9	16:45
39	1920x1080i (1250 total)	50Hz	16:9	1:1

Table 3 Video Formats—Video ID Code and Aspect Ratios

Video ID Code	Formats	Field Rate	Picture Aspect Ratio (H:V)[1]	Pixel Aspect Ratio (H:V)
40	1920x1080i	100Hz	16:9	1:1
41	1280x720p	100Hz	16:9	1:1
42	720x576p	100Hz	4:3	16:15
43	720x576p	100Hz	16:9	64:45
44	720(1440)x576i	100Hz	4:3	16:15
45	720(1440)x576i	100Hz	16:9	64:45
46	1920x1080i	119.88/120Hz	16:9	1:1
47	1280x720p	119.88/120Hz	16:9	1:1
48	720x480p	119.88/120Hz	4:3	8:9
49	720x480p	119.88/120Hz	16:9	32:27
50	720(1440)x480i	119.88/120Hz	4:3	8:9
51	720(1440)x480i	119.88/120Hz	16:9	32:27
52	720x576p	200Hz	4:3	16:15
53	720x576p	200Hz	16:9	64:45
54	720(1440)x576i	200Hz	4:3	16:15
55	720(1440)x576i	200Hz	16:9	64:45
56	720x480p	239.76/240Hz	4:3	8:9
57	720x480p	239.76/240Hz	16:9	32:27
58	720(1440)x480i	239.76/240Hz	4:3	8:9
59	720(1440)x480i	239.76/240Hz	16:9	32:27
60-127	Reserved for the Future			
0	No Video Code Available (Used with AVI InfoFrame only)			

[1]Picture Aspect Ratio—The display shall state what picture aspect ratios it supports for a given format, and the source can choose how to support it. For example, with the 720x480 (16:9) data format and a 4:3 display, the source could (1) use pan and scan information to crop the data to 540 horizontal pixels and then resample up to the required 720 pixels for output to the display or (2) vertically resample to 360 lines and create bars of 60 lines above and below it to send this “letterbox” with the required 480 lines for output. Other picture scaling methods are possible in either source device or DTV Monitor. For example, picture aspect ratio scaling (picture expand, shrink, etc.) can be accomplished in the source device, including, possibly, added black/gray lines in the addressable pixel portion of the video. The exception to this is the 640x480 format, which is always sent as 4x3 data, and it is up to the display to determine how it wants to display it.

Table 3 Video Formats—Video ID Code and Aspect Ratios (Continued)

4.2 640x480p @59.94/60 Hz (Format 1)

This timing is based on the timing in *VESA Monitor Timings Specification*, version 1.0 revision 10 [10] and is available only in a 4:3 aspect ratio]. The only difference is where VESA defines blanking as not including the border while CEA-861-D includes the border within the blanking interval. Unlike the other formats, IT quantization levels (see Section 5.4) are used for this format. See Figure 1.

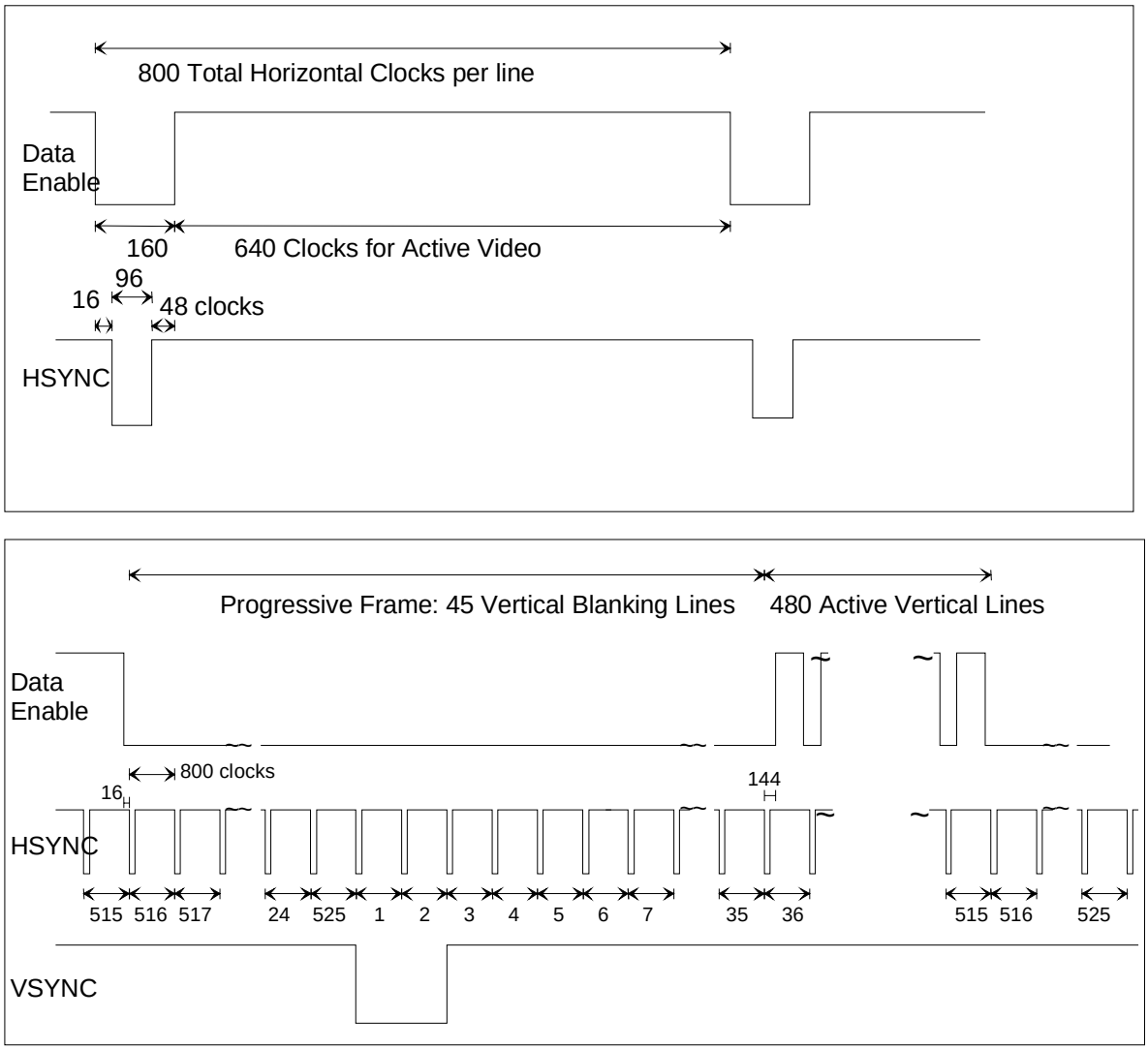

Figure 1 Timing Parameters for 640x480p @ 59.94/60 Hz

4.3 1280x720p @59.94/60 Hz (Format 4)

This format is available only in a 16:9 aspect ratio. This timing is based on CEA-770.3-D [20], but there are two differences. First, CEA-770.3-C uses tri-level sync, while CEA-861-D uses bi-level. Bi-level sync timing is accomplished using the second half of the CEA-770.3-C tri-level sync, defining the actual sync time to be the rising edge of that pulse.

Second, CEA-770.3-C uses a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync. See Figure 2.

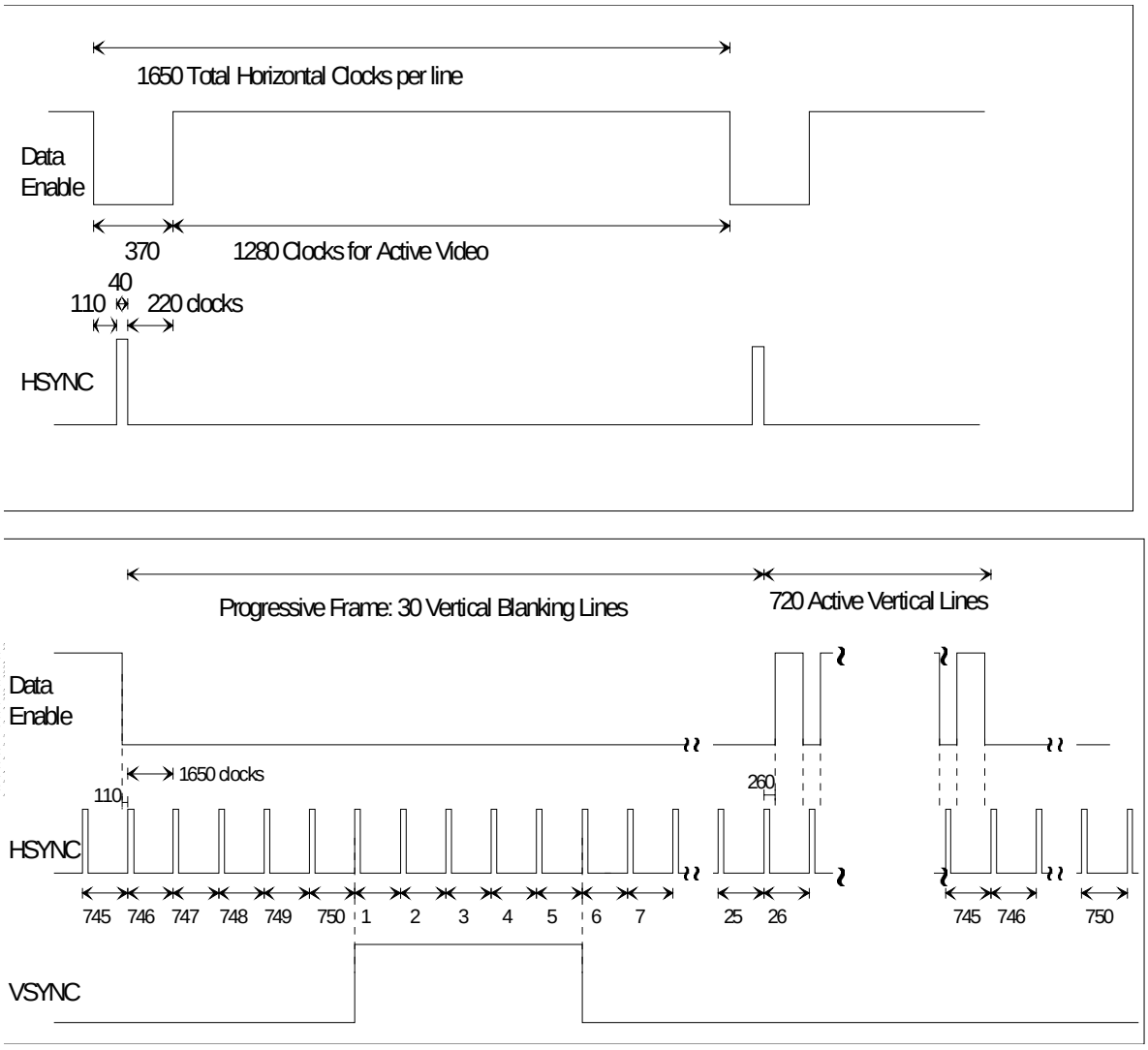

Figure 2 Timing Parameters for 1280x720p @ 59.94/60 Hz

4.4 1920x1080i @59.94/60 Hz (Format 5)

This format is available only in a 16:9 aspect ratio. This timing is based on CEA-770.3-C [20], but there are two differences: First, CEA-770.3-C uses tri-level sync, while CEA-861-D uses bi-level. Bi-level sync timing is accomplished using the second half of the CEA-770.3-C tri-level sync, defining the actual sync time to be the rising edge of that pulse. See Figure 3 .

Second, CEA-770.3-C uses a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync.

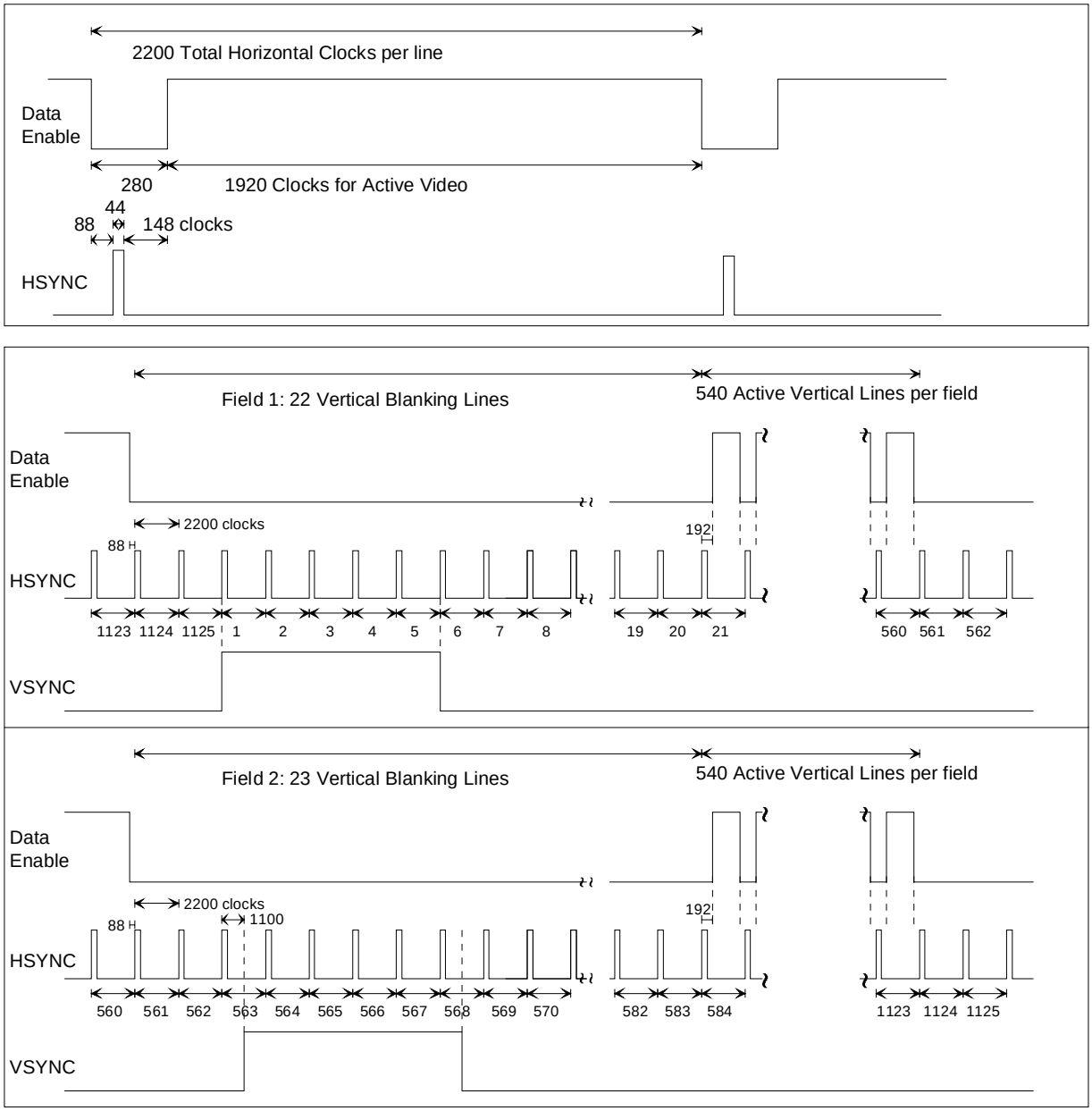

Figure 3 Timing Parameters for 1920x1080i @ 59.94/60

4.5 720x480p @59.94/60 Hz (Formats 2 & 3)

This timing is based on CEA-770.2-C [19], with one difference. CEA-770.2-C has a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync. This format timing can use either 4:3 or 16:9 aspect ratio.

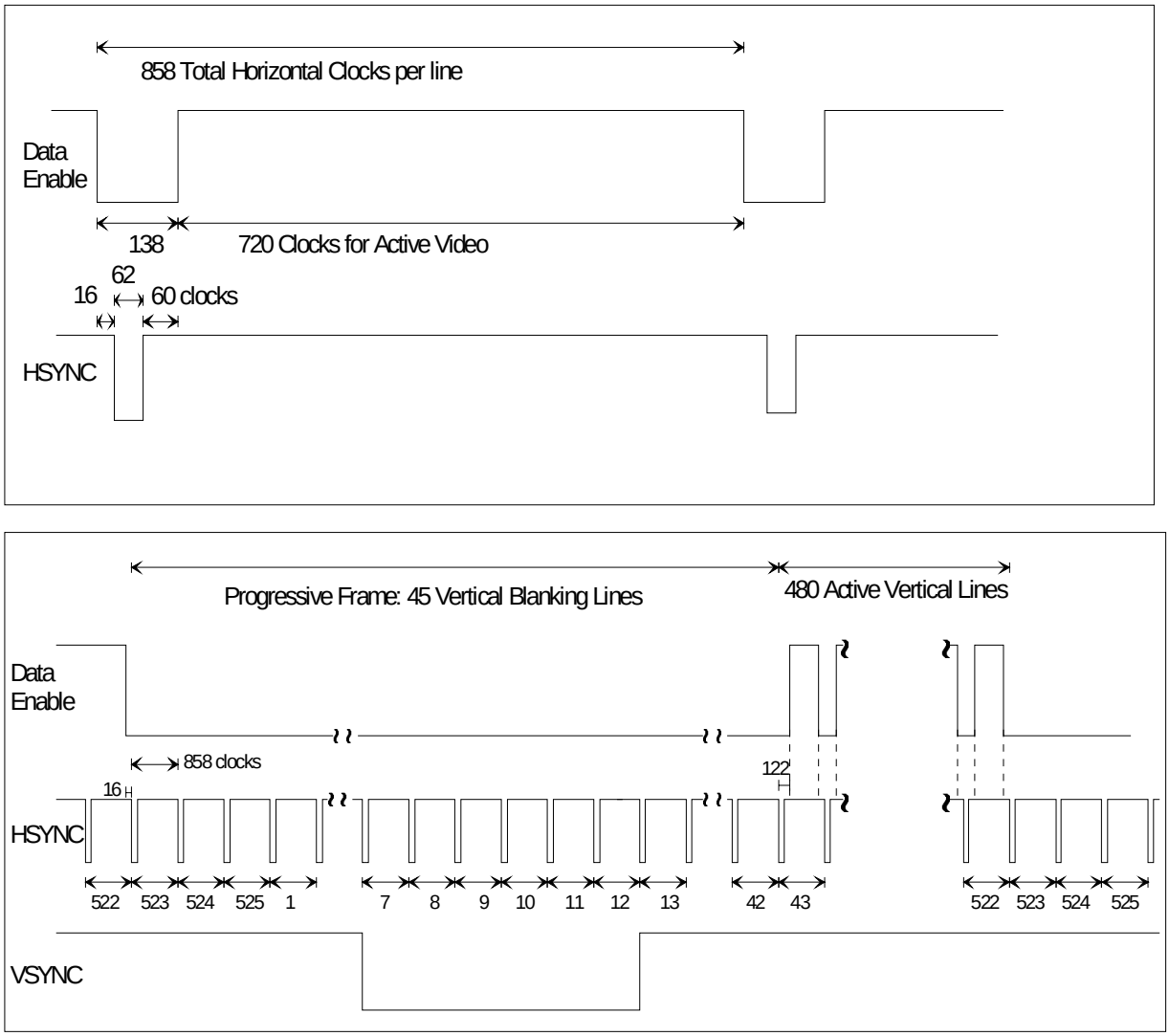

Figure 4 Timing Parameters for 720x480p @ 59.94/60 Hz

4.6 720(1440)x480i @59.94/60 Hz (Formats 6 & 7)

This timing is based on CEA-770.2-C [19], with a few differences. CEA-770.2-C has a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync. This format also assumes the pixels are double clocked to meet minimum clock speed requirements for the interface. This format timing can use either 4:3 or 16:9 aspect ratio.

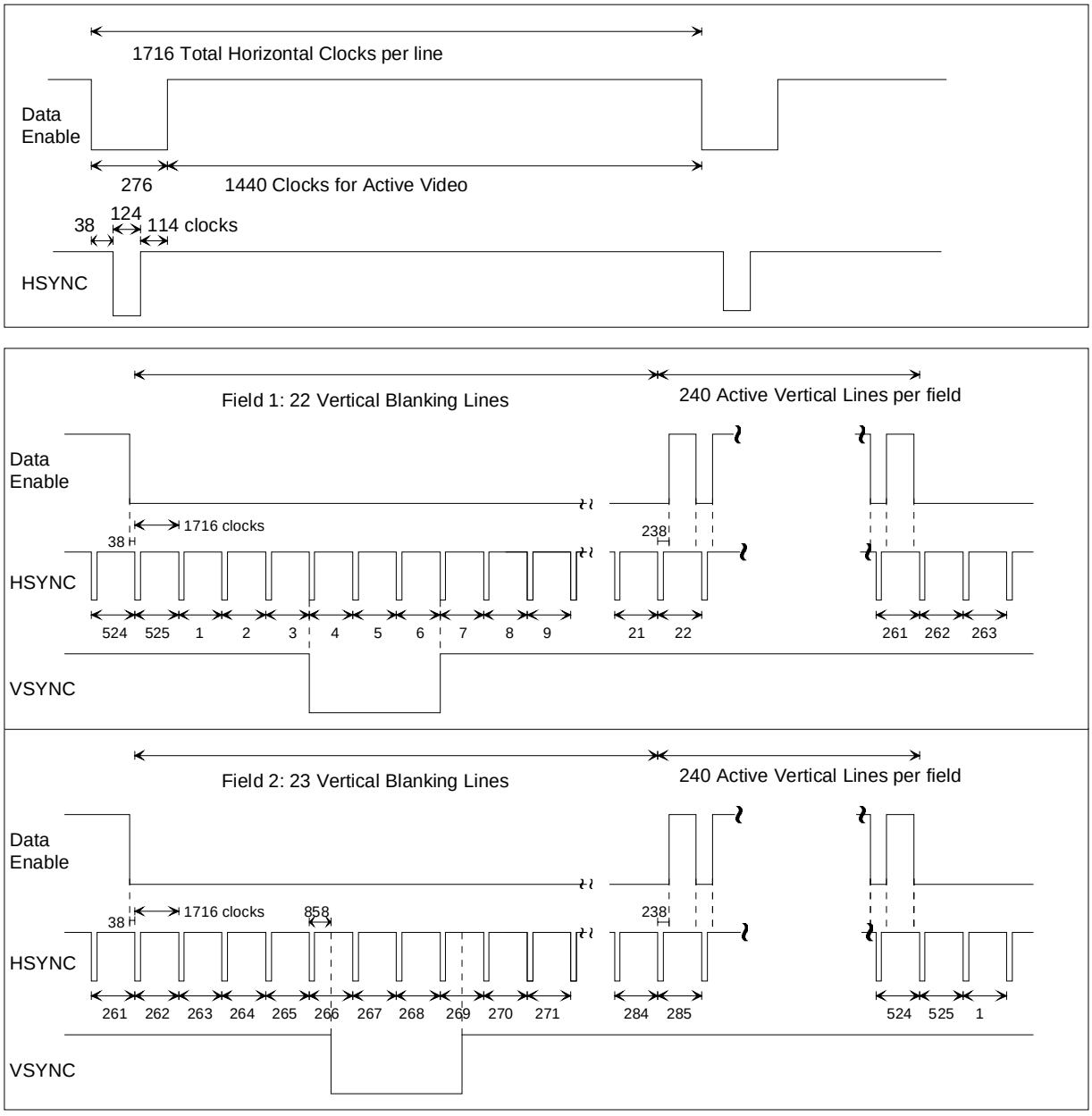

Figure 5 Timing Parameters for 720(1440)x480i @ 59.94/60 Hz

4.7 1280x720p @ 50 Hz (Format 19)

This format is available only in a 16:9 aspect ratio. This timing is based on SMPTE 296M [14], but there are two differences. First, SMPTE 296M uses tri-level sync, while CEA-861-D uses bi-level. Bi-level sync timing is accomplished using the second half of the SMPTE 296M tri-level sync, defining the actual sync time to be the rising edge of that pulse.

Second, SMPTE 296M uses a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync.

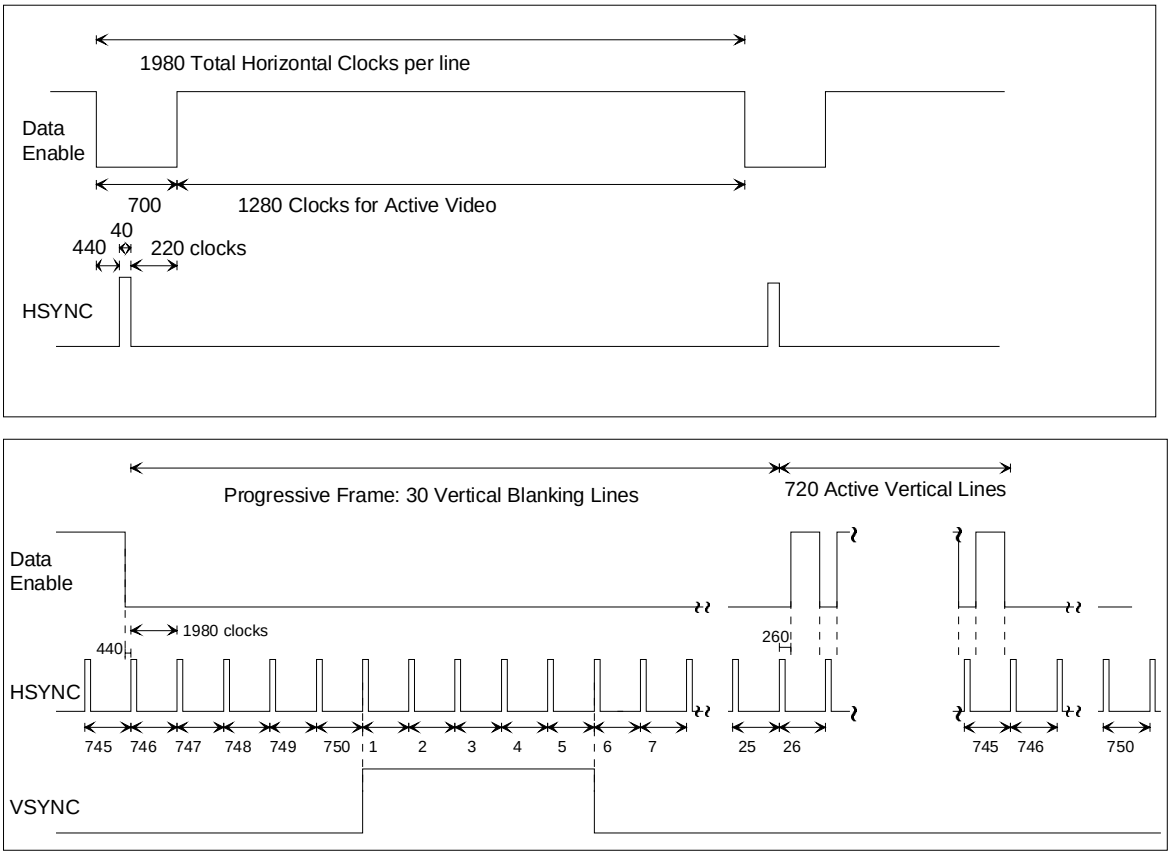

Figure 6 Timing Parameters for 1280x720p @ 50Hz

4.8 1920x1080i @ 50 Hz (Format 20)

This format is available only in a 16:9 aspect ratio. This timing is based on SMPTE 274M [12], but there are two differences: First, SMPTE 274M uses tri-level sync, while CEA-861-D uses bi-level. Bi-level sync timing is accomplished using the second half of the SMPTE 274M tri-level sync, defining the actual sync time to be the rising edge of that pulse.

Second, SMPTE 274M uses a composite sync while CEA-861-D uses separate sync signals, thus eliminating the need for serrations during vertical sync.

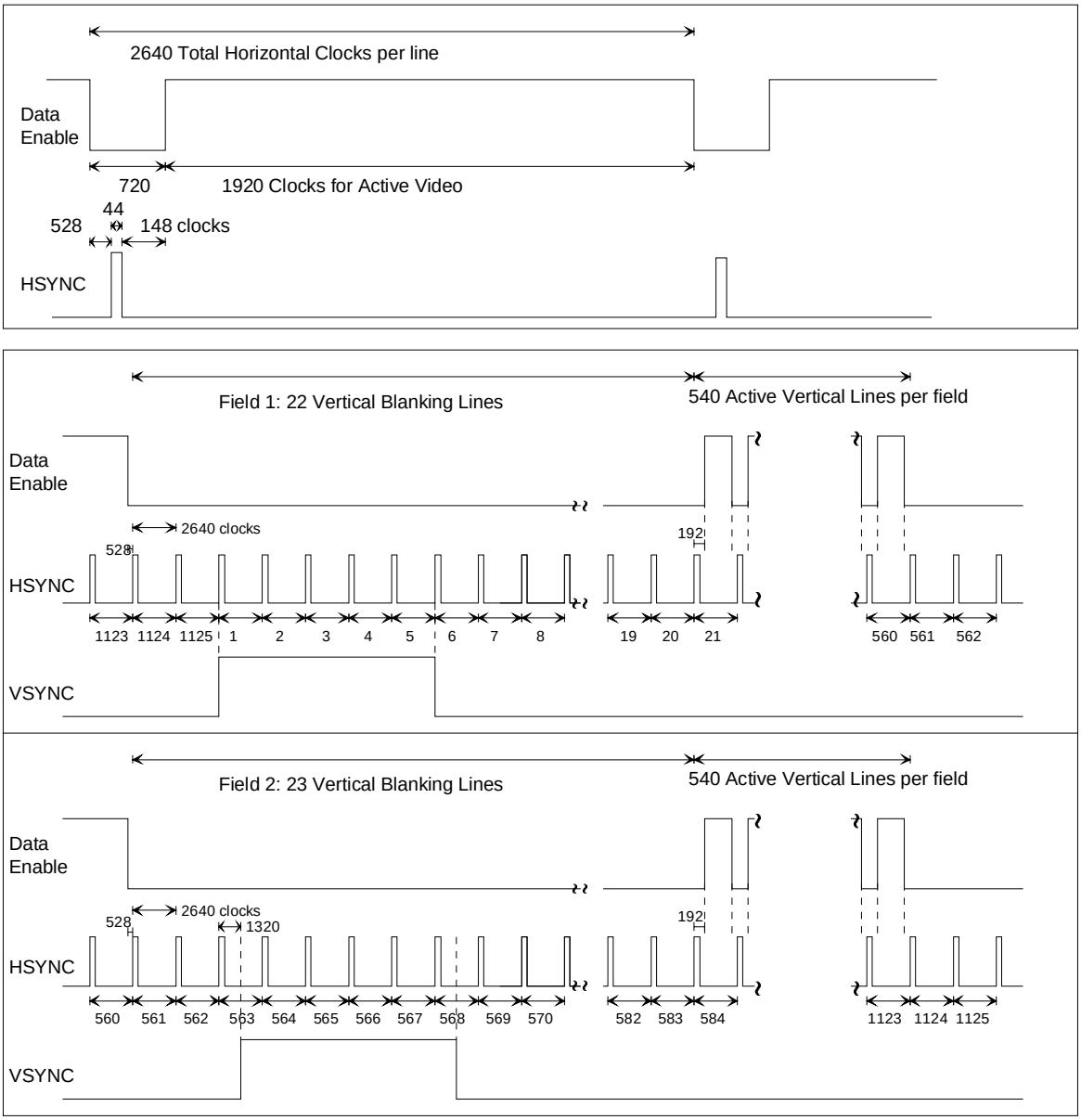

Figure 7 Timing Parameters for 1920x1080i @ 50 Hz

4.9 720x576p @ 50 Hz (Formats 17 & 18)

This timing is based on ITU-R BT.1358 [41]. This format timing can use either 4:3 or 16:9 aspect ratio.

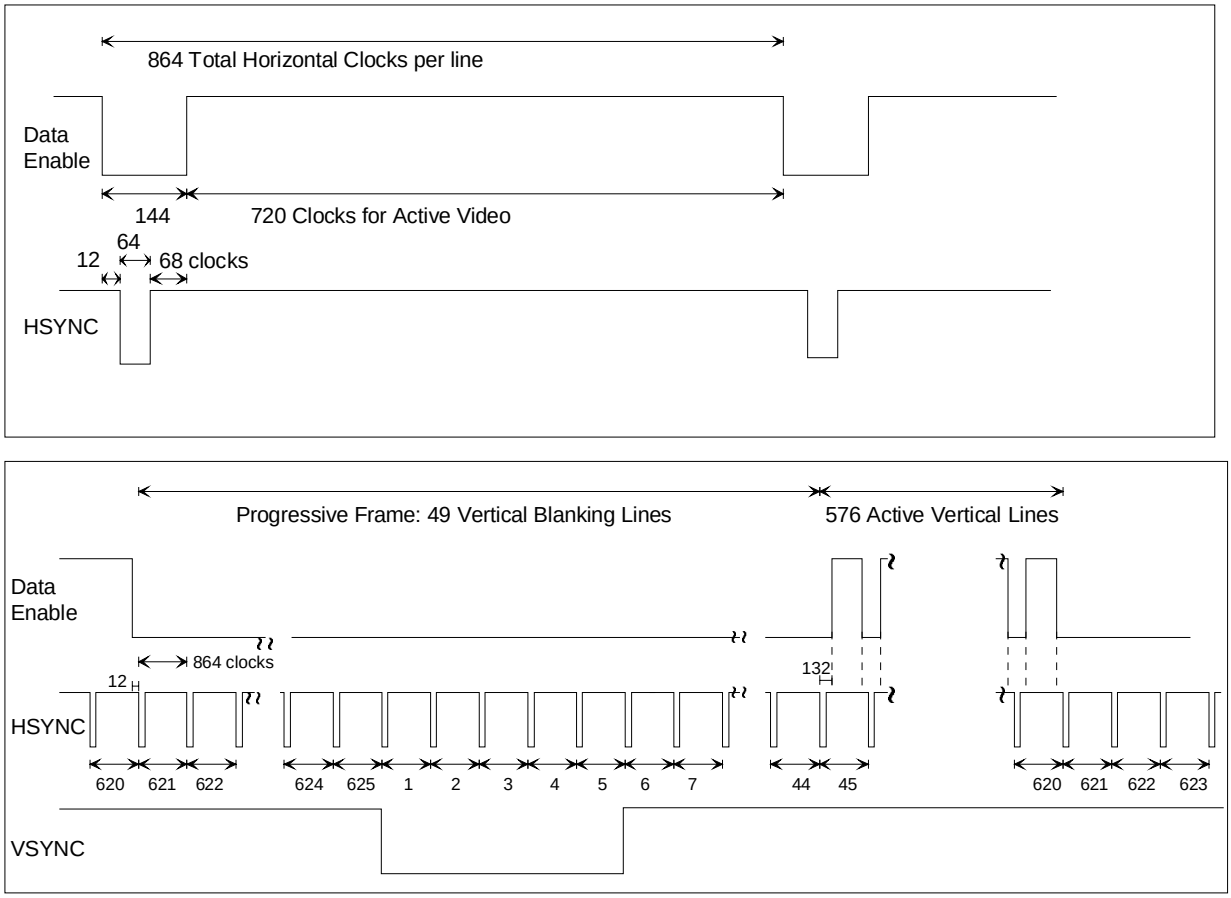

Figure 8 Timing Parameters for 720x576p @ 50 Hz

4.10 720(1440)x576i @ 50 Hz (Formats 21 & 22)

This timing is based on ITU-R BT.656–4 [39] except for horizontal and vertical synchronization pulse durations, which are specified in ITU-R BT.711–1 [40] and ITU-R BT.470–6 [38]. This format assumes the pixels are double clocked to meet minimum clock speed requirements for the interface. Thus, the clock is 27 MHz. This format timing can use either 4:3 or 16:9 aspect ratio.

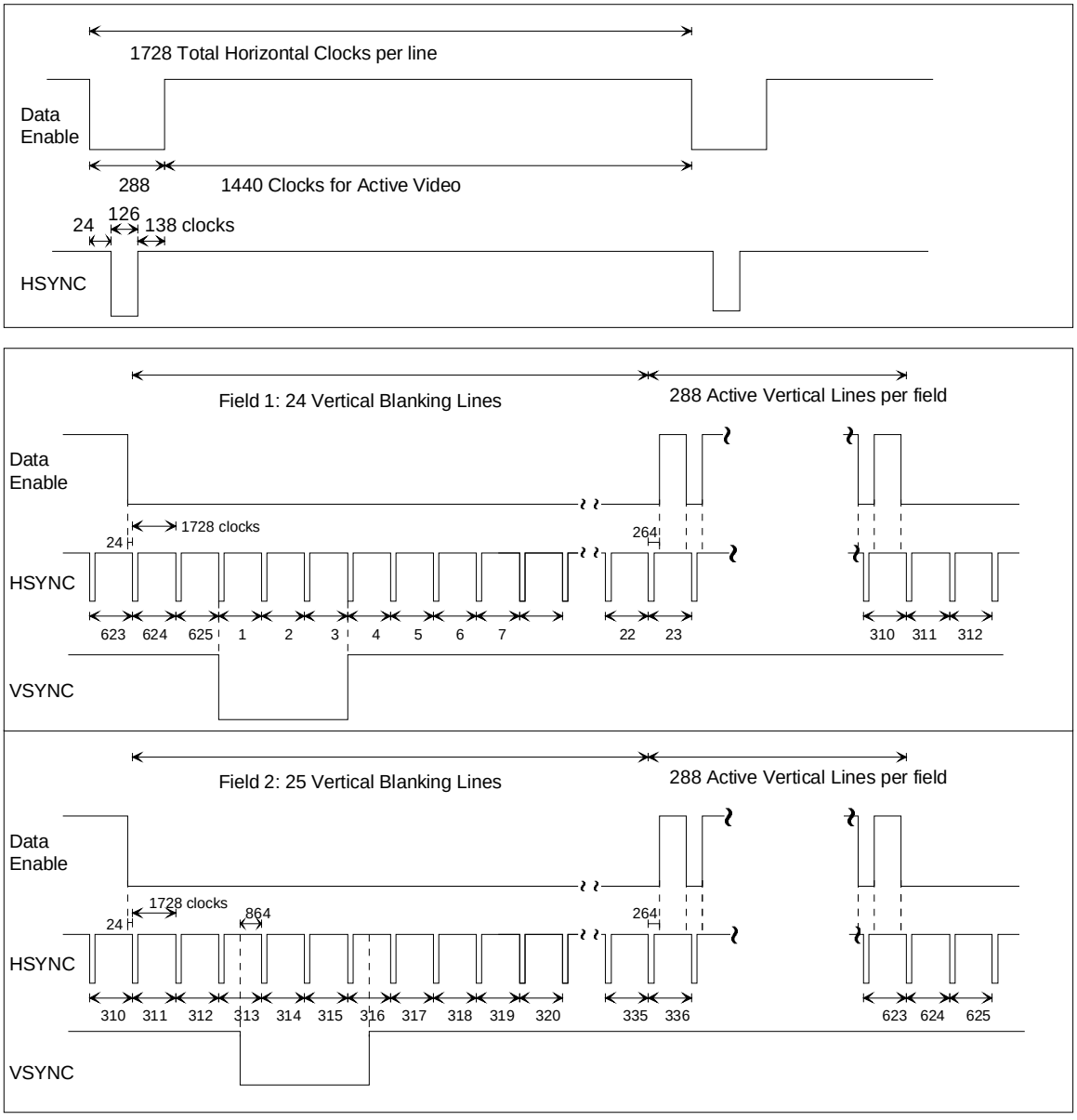

Figure 9 Timing Parameters for 720(1440)x576i @ 50 Hz

4.11 720(1440)x240p @ 59.94/60 Hz (Formats 8 & 9)

This format assumes the pixels are double clocked to meet minimum clock speed requirements for the interface. There are two possible frame formats that differ only in the number of lines in the vertical blanking interval of the frame. Both are considered variations of the same format. This format timing can use either 4:3 or 16:9 aspect ratio.

Designers should be aware that this format was not defined in prior versions of CEA-861-D and it is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

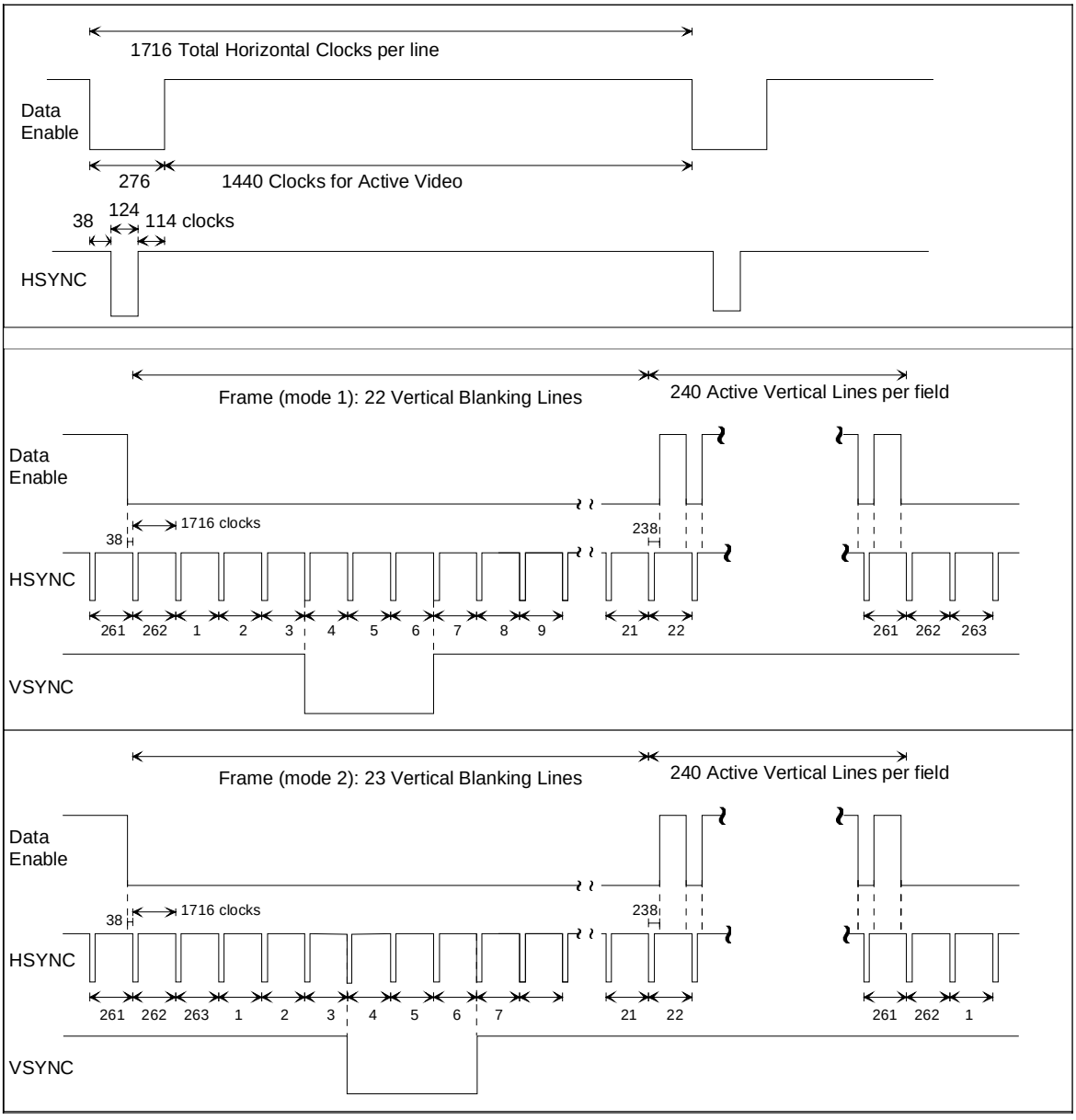

Figure 10 Timing Parameters for 720(1440)x240p @ 59.94/60 Hz

4.12 (2880)x480i @ 59.94/60 Hz (Formats 10 & 11)
This format is a superset of a variety of video formats used in various game consoles. This format is unique in that, depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent any of the following typical formats:

a) 2880/10=288 pixels/line
b) 2880/8=360 pixels/line
c) 2880/7=411 pixels/line
d) 2880/5=576 pixels/line
e) 2880/4=720 pixels/line

The pixel repetition factor is specified in the AVI. The DTV Monitor indicates it can accept any of the formats implied by this format superset through EDID.

This format will also typically have bars on the left and right sides. These bars will be 160/*n* pixels wide where *n* is the repetition factor.

This format timing can use either 4:3 or 16:9 aspect ratio.

Users should be aware that this format, due to the repetition factor, is only supported with HDMI implementations of CEA-861-D. See Figure 11.

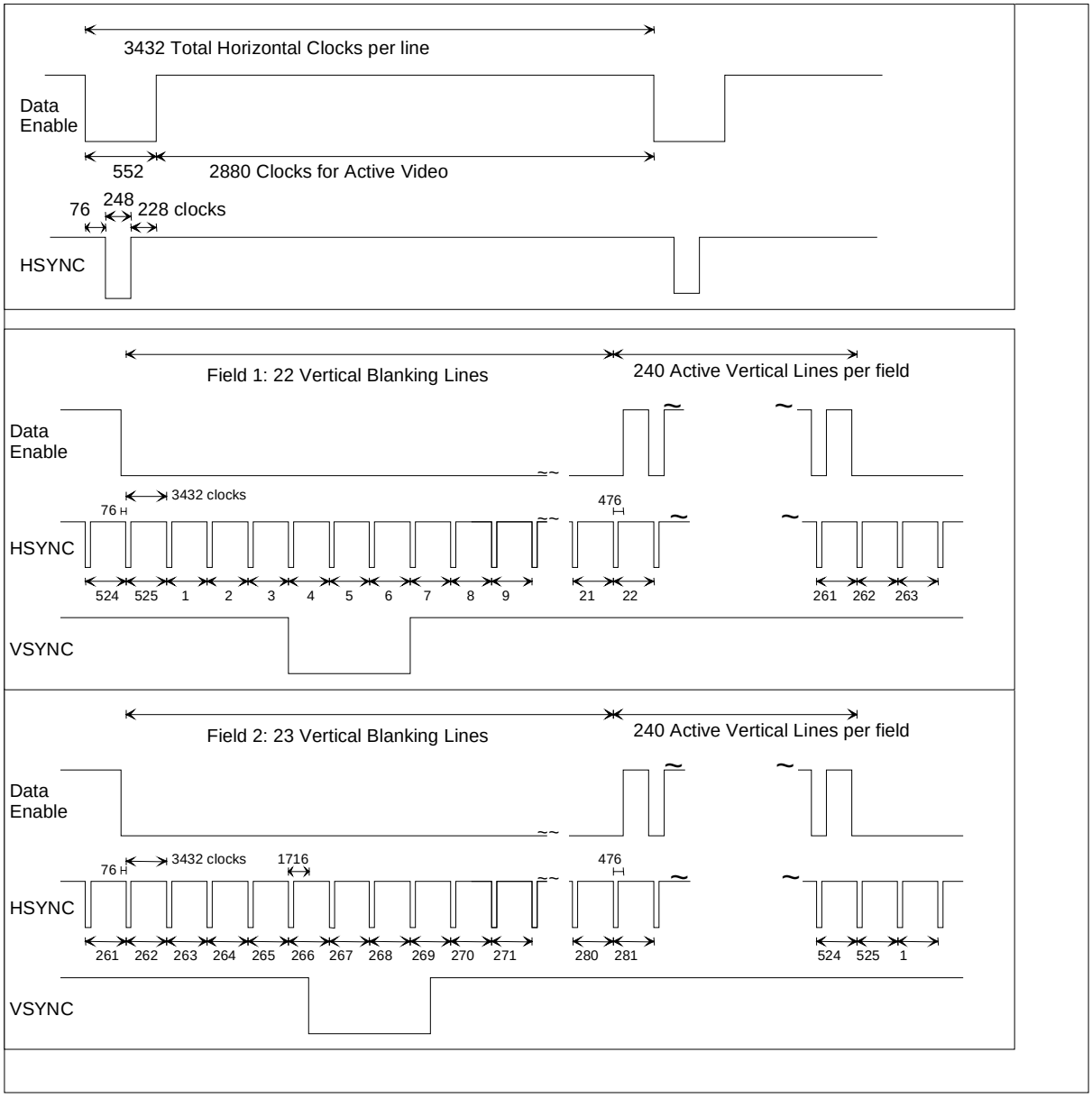

Figure 11 Timing Parameters for (2880)x480i @ 59.94/60 Hz

4.13 (2880)x240p @ 59.94/60 Hz (Formats 12 & 13)
This format is a superset of a variety of video formats used in various game consoles. This format is unique in that, depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent any of the following typical formats:

a) 2880/10=288 pixels/line
b) 2880/8=360 pixels/line
c) 2880/7=411 pixels/line
d) 2880/5=576 pixels/line
e) 2880/4=720 pixels/line

The pixel repetition factor is specified in the AVI. The DTV Monitor indicates it can accept any of the formats implied by this format superset through EDID.

This format will also typically have bars on the left and right sides. These bars will be 160/*n* pixels wide where *n* is the repetition factor.

There are two possible frame formats that differ only in the number of lines in the vertical blanking interval of the frame. Both are considered variations of the same format.

This format timing can use either 4:3 or 16:9 aspect ratio.

Users should be aware that this format, due to the repetition factor, is only supported with HDMI implementations of CEA-861-D. See Figure 12.

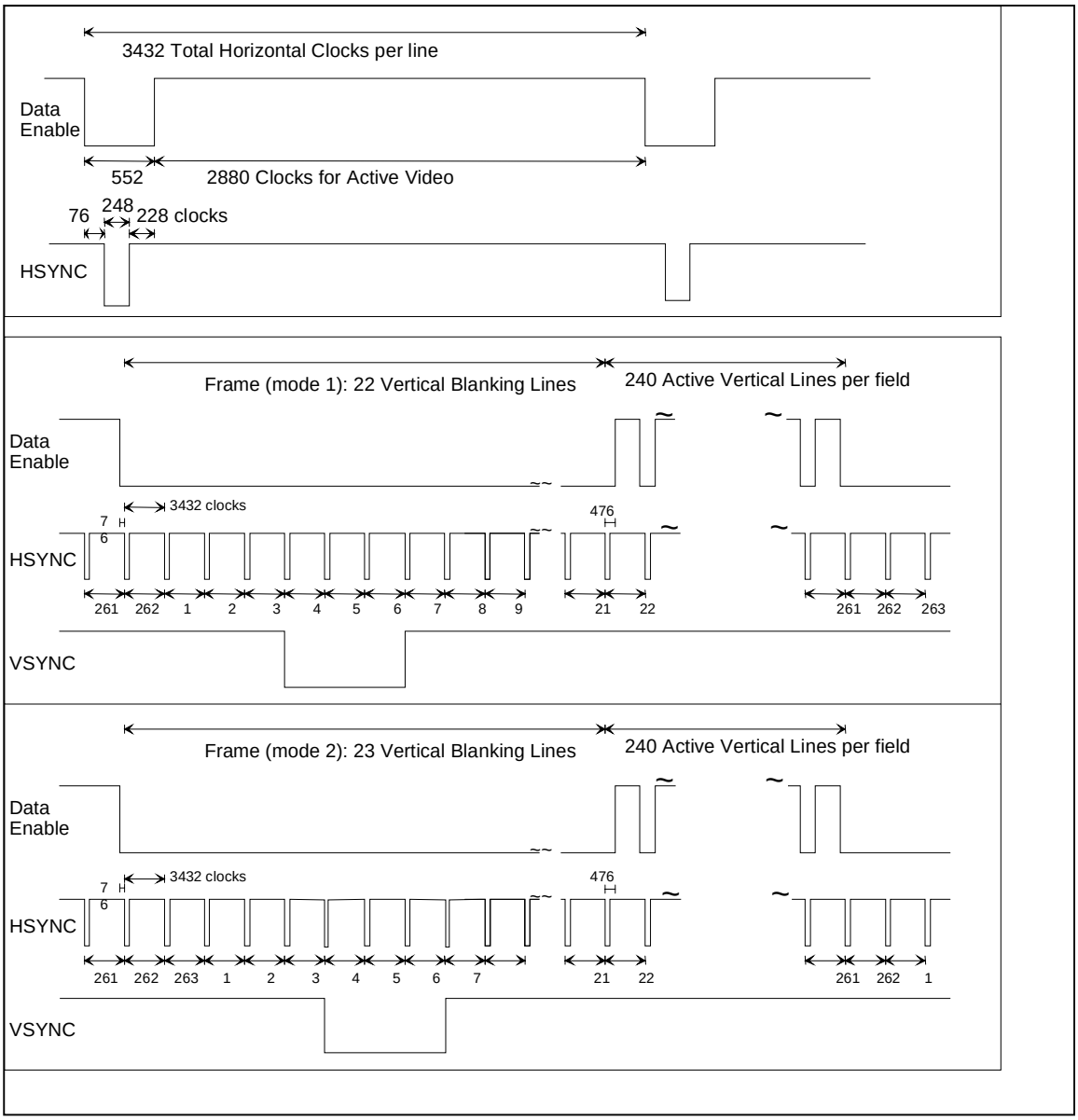

Figure 12 Timing Parameters for (2880)x240p @ 59.94/60 Hz

4.14 1440x480p @ 59.94/60 Hz (Formats 14 & 15)

This format can use either 4:3 or 16:9 aspect ratio. It provides either additional horizontal video resolution or additional bandwidth for carrying audio data.

Depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent either of the following typical formats:

a) 1440/2=720 pixels/line
b) 1440/1=1440 pixels/line

The first format is typically used to increase the available bandwidth for audio transmission on HDMI while transmitting the normal 720 pixels per line. The second format is used to increase the horizontal resolution. If this timing is advertised in the EDID, the DTV Monitor shall be able to accept either of these two pixel repetition factors.

It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

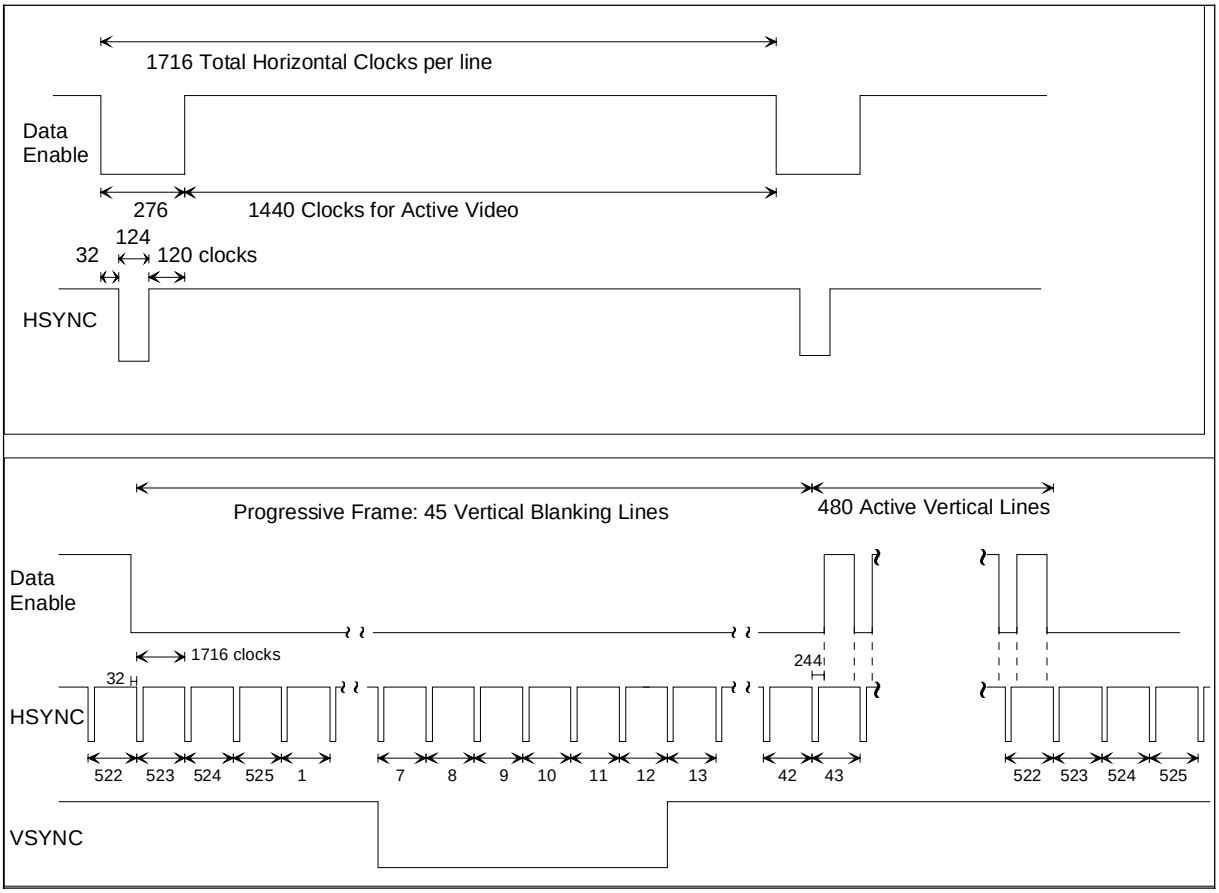

Figure 13 Timing Parameters for 1440x480p @ 59.94/60 Hz

4.15 1920x1080p @ 59.94/60Hz (Format 16)

This format is available only in a 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

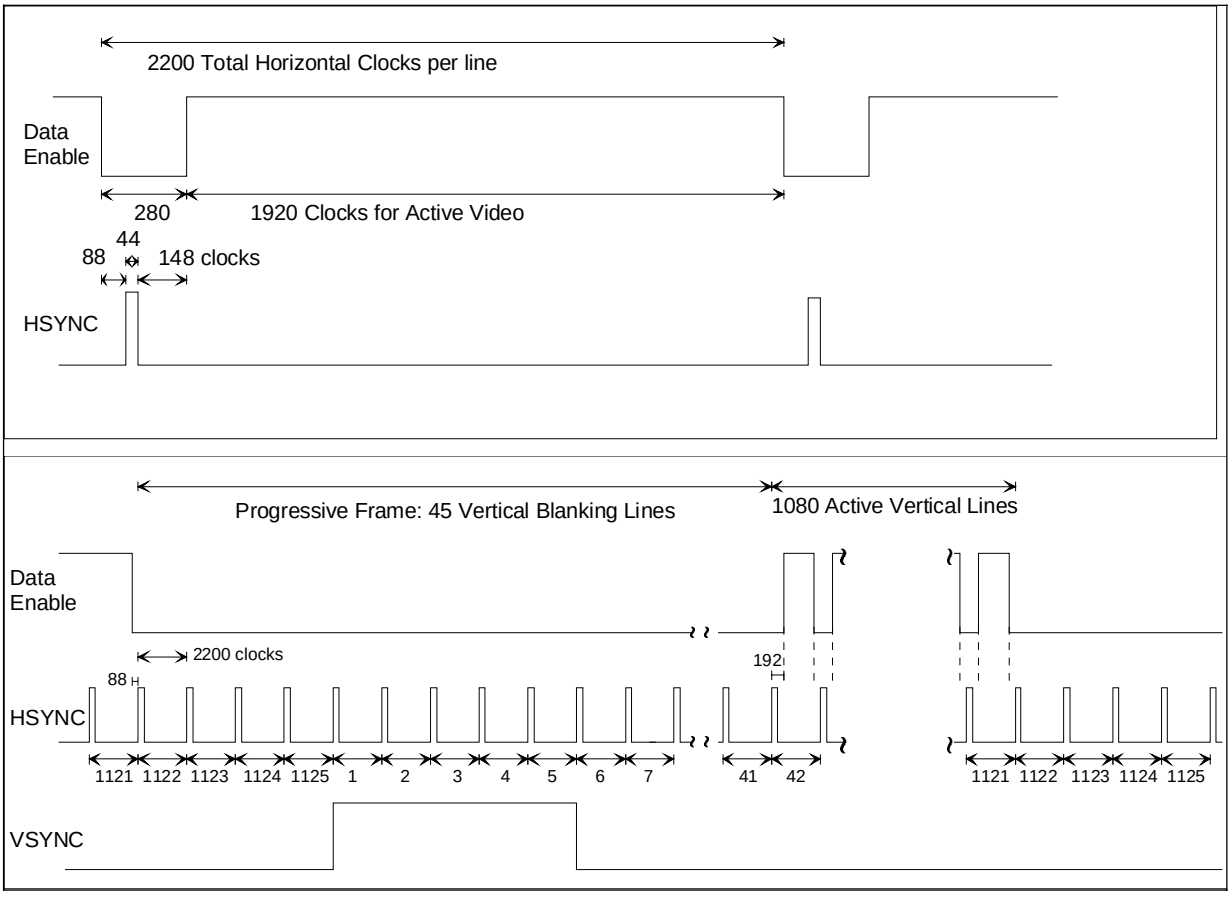

Figure 14 Timing Parameters for 1920x1080p @ 59.94/60 Hz

4.16 720(1440)x288p @ 50 Hz (Formats 23 & 24)

This format assumes the pixels are double clocked to meet minimum clock speed requirements for the interface. There are three possible frame formats that differ only in the number of lines in the vertical blanking interval of the frame. All three are considered variations of the same format.

This format timing can use either 4:3 or 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor. See Figure 15.

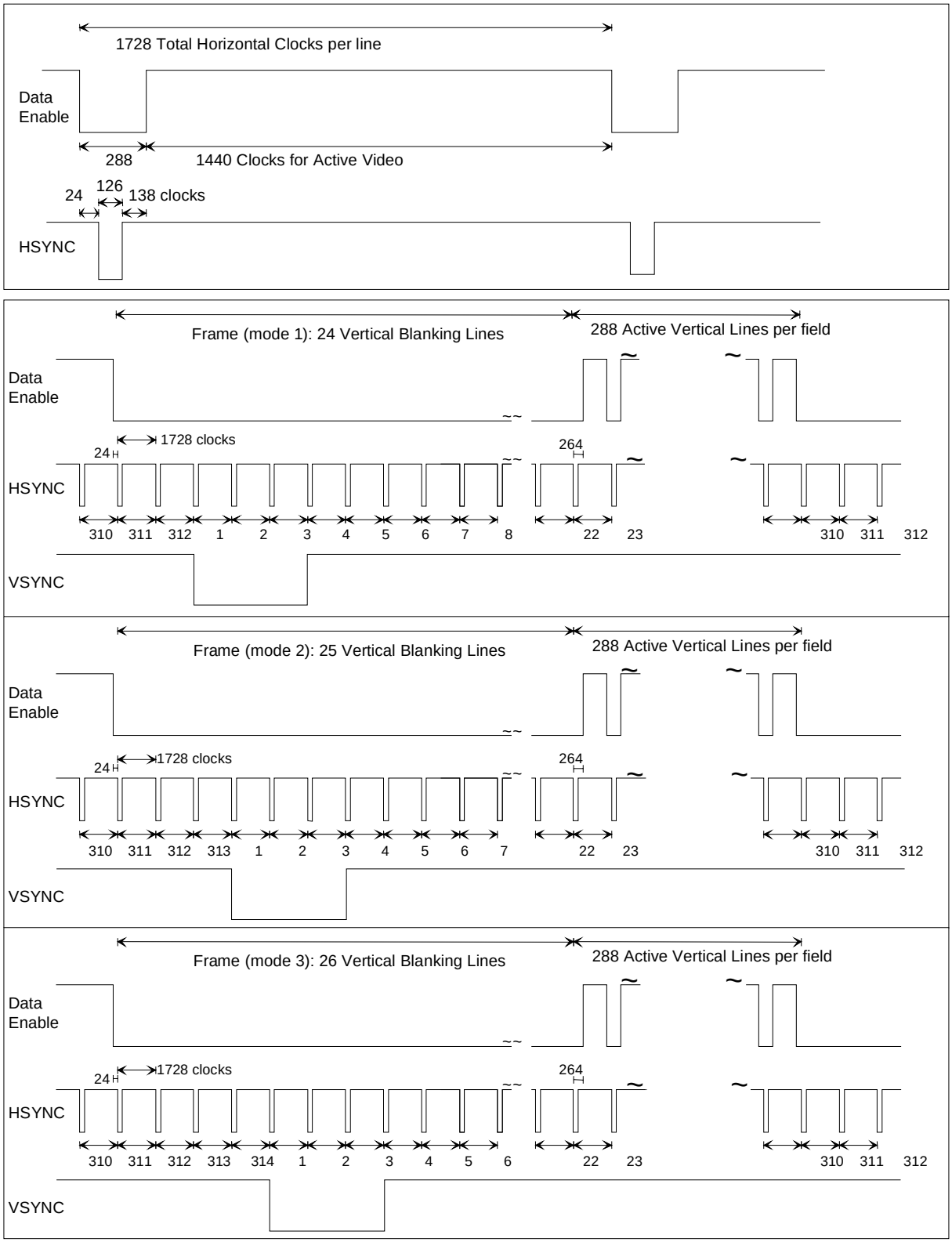

Figure 15 Timing Parameters for 720(1440)x288p @ 50 Hz

4.17 (2880)x576i @ 50Hz (Formats 25 & 26)

This format is a superset of a variety of video formats used in various game consoles. This format is unique in that, depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent any of the following typical formats:

a) 2880/10=288 pixels/line
b) 2880/8=360 pixels/line
c) 2880/7=411 pixels/line
d) 2880/5=576 pixels/line
e) 2880/4=720 pixels/line

The pixel repetition factor is specified in the AVI. The DTV Monitor indicates it can accept any of the formats implied by this format superset through EDID.

This format will also typically have bars on the left and right sides. These bars will be 160/*n* pixels wide where *n* is the repetition factor.

This format timing can use either 4:3 or 16:9 aspect ratio.

It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor. See Figure 16.

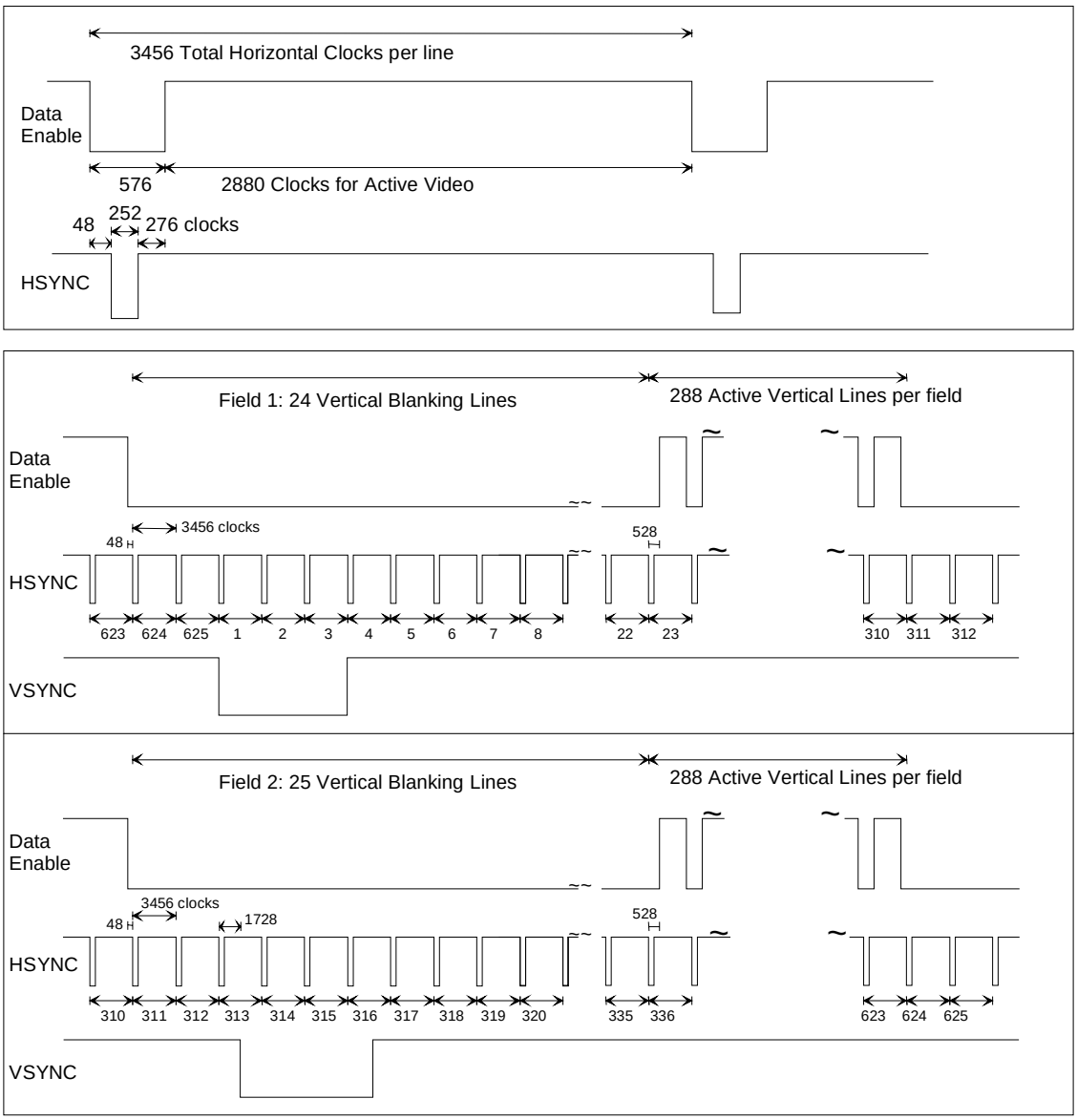

Figure 16 Timing Parameters for (2880)x576i @ 50 Hz

4.18 (2880)x288p @ 50 Hz (Formats 27 & 28)

This format is a superset of a variety of video formats used in various game consoles. This format is unique in that, depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent any of the following typical formats:

a) 2880/10=288 pixels/line
b) 2880/8=360 pixels/line
c) 2880/7=411 pixels/line
d) 2880/5=576 pixels/line
e) 2880/4=720 pixels/line

The pixel repetition factor is specified in the AVI. The DTV Monitor indicates it can accept any of the formats implied by this format superset through EDID.

This format will also typically have bars on the left and right sides. These bars will be 160/*n* pixels wide where *n* is the repetition factor.

There are three possible frame formats that differ only in the number of lines in the vertical blanking interval of the frame. All three are considered variations of the same format.

This format timing can use either 4:3 or 16:9 aspect ratio.

Users should be aware that this format, due to the repetition factor, is only supported by interfaces capable of signaling pixel repetition via AVI Infoframes, such as HDMI. See Figure 17.

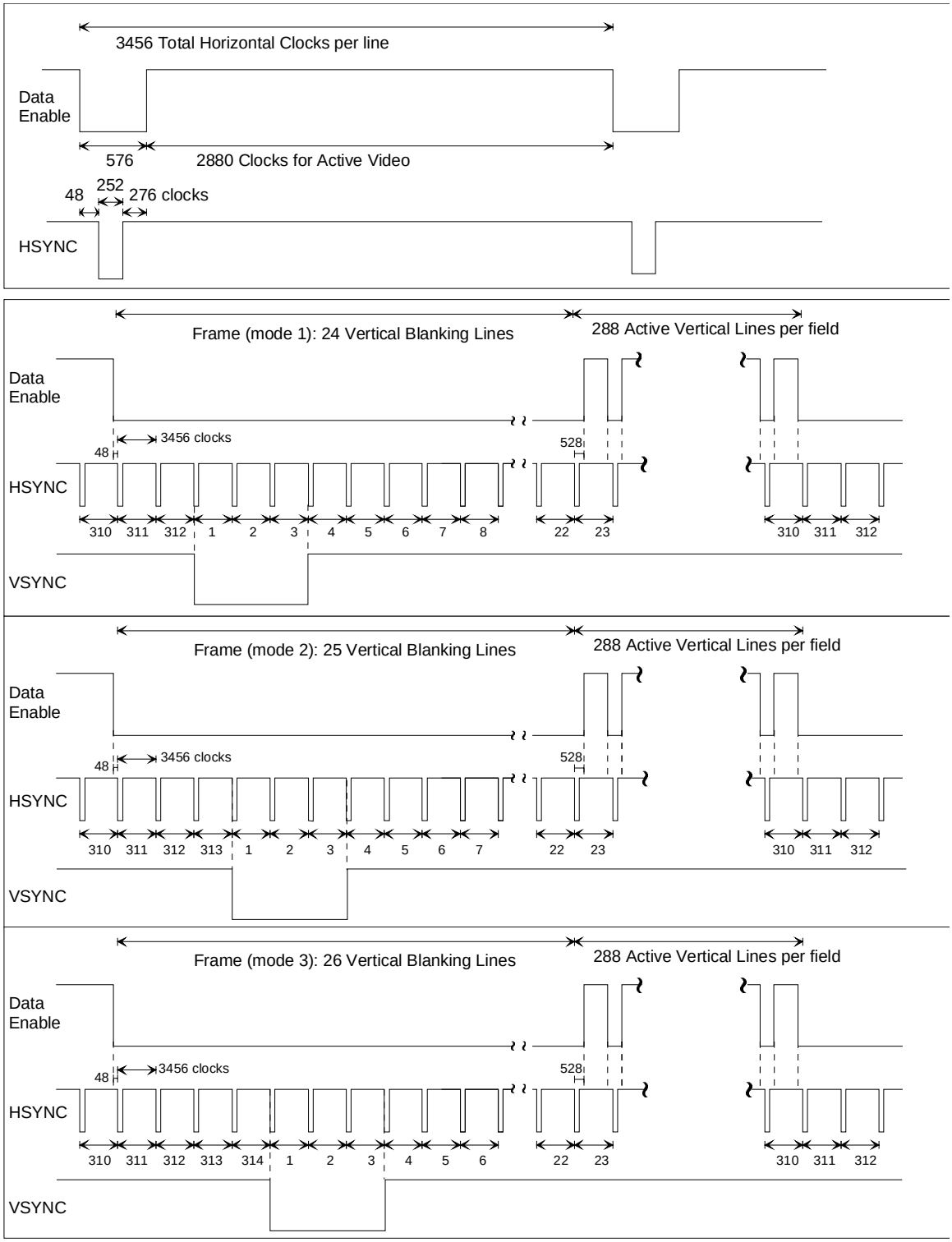

Figure 17 Timing Parameters for (2880)x288p @ 50 Hz

4.19 1440x576p @ 50Hz (Formats 29 & 30)

This format can use either 4:3 or 16:9 aspect ratio. It provides either additional horizontal video resolution or additional bandwidth for carrying audio data.

Depending upon the pixel repetition factor specified in the AVI InfoFrame, this format can represent either of the following typical formats:

a) 1440/2=720 pixels/line
b) 1440/1=1440 pixels/line

The first format is typically used to increase the available bandwidth for audio transmission on HDMI while transmitting the normal 720 pixels per line. The second format is used to increase the horizontal resolution. If this timing is advertised in the EDID, the DTV Monitor shall be able to accept either of these two pixel repetition factors.

It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

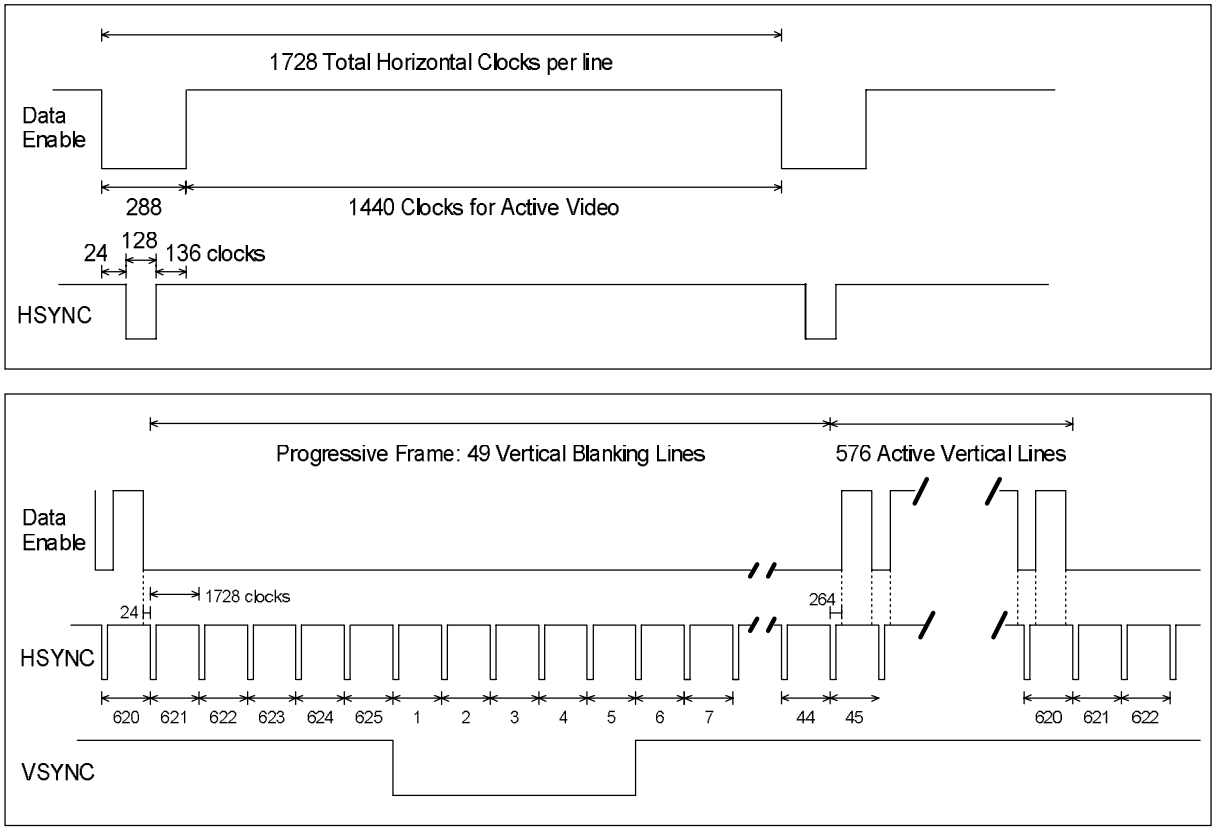

Figure 18 Timing Parameters for 1440x576p @ 50 Hz

4.20 1920x1080p @ 50 Hz (Format 31)

This format is available only in a 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

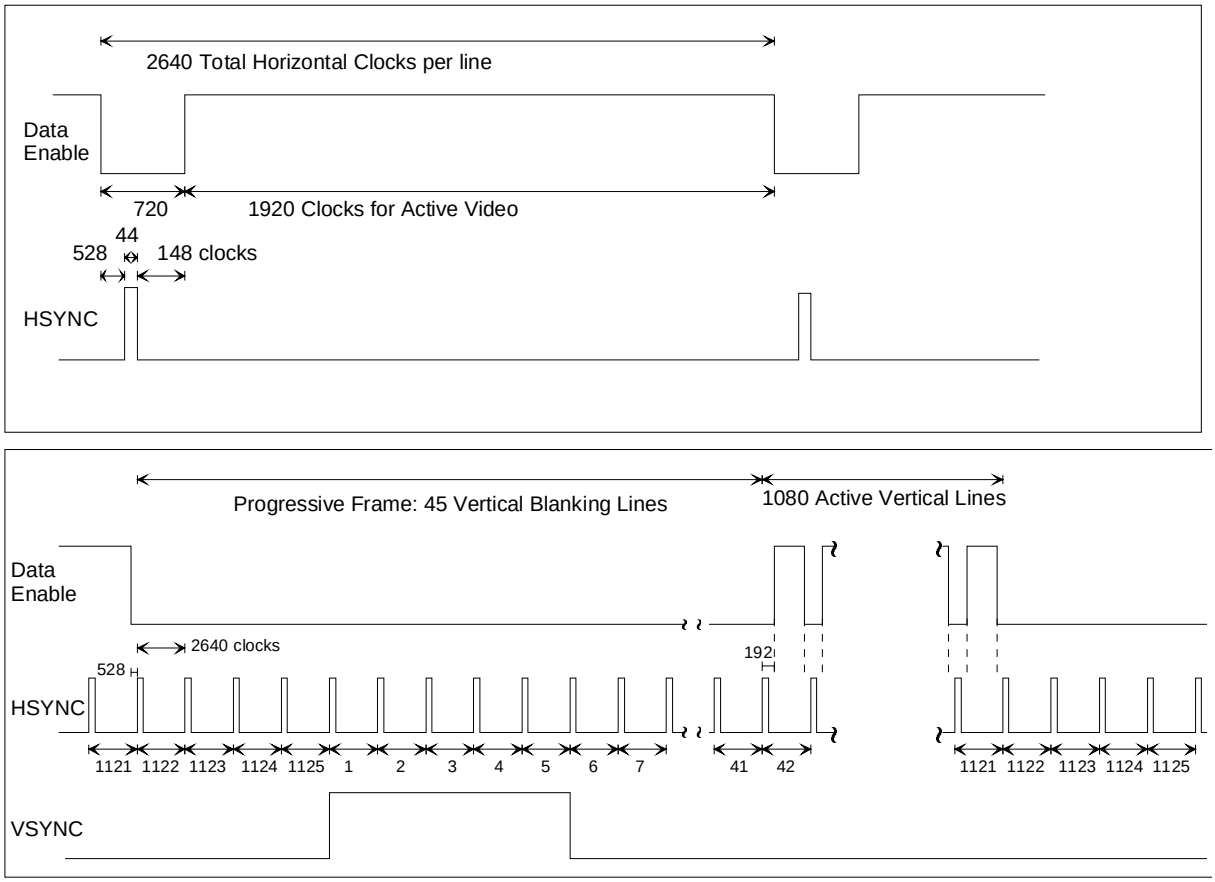

Figure 19 Timing Parameters for 1920x1080p @ 50 Hz

4.21 1920x1080p @ 23.98/24 Hz (Format 32)

This format is available only in a 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

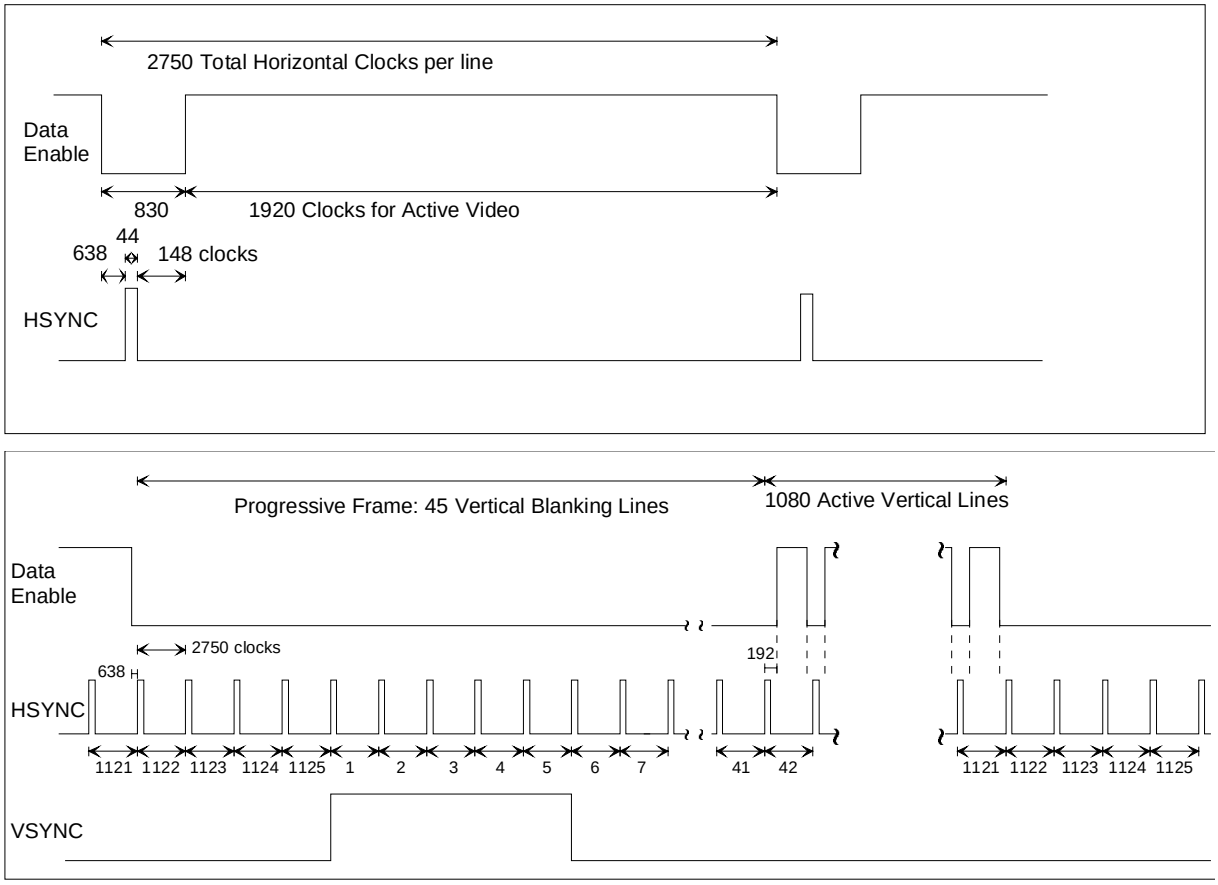

Figure 20 Timing Parameters for 1920x1080p @ 23.98/24 Hz

4.22 1920x1080p @ 25 Hz (Format 33)

This format is available only in a 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

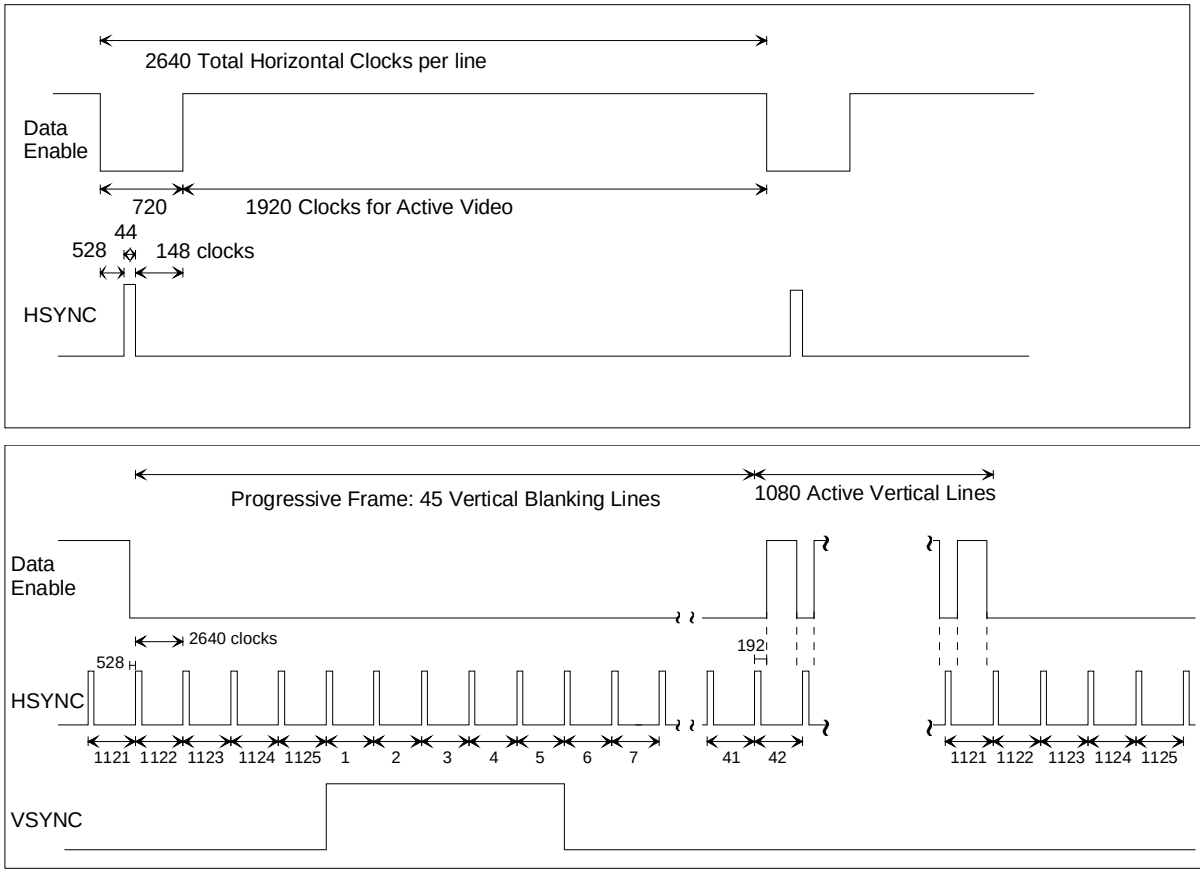

Figure 21 Timing Parameters for 1920x1080p @ 25 Hz

4.23 1920x1080p @ 29.97/30 Hz (Format 34)

This format is available only in a 16:9 aspect ratio. It is likely that non-HDMI source devices may not recognize this format in a Detailed Timing Descriptor.

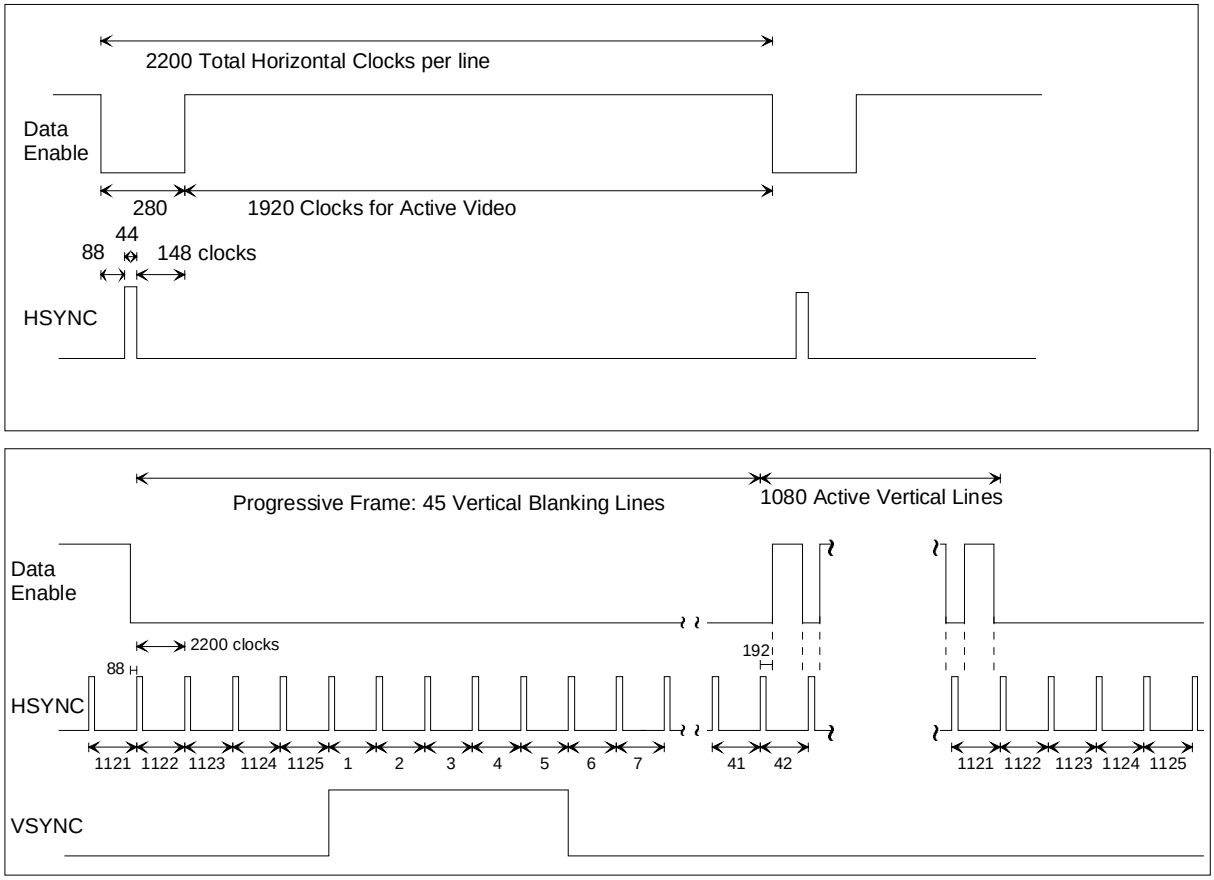

Figure 22 Timing Parameters for 1920x1080p @ 29.97/30 Hz

4.24 2880x480p @ 59.94/60 Hz (Formats 35 and 36)

These formats can use either 4:3 or 16:9 aspect ratio. They provide additional bandwidth for carrying audio data and can also provide additional horizontal video resolution.

Depending upon the pixel repetition factor specified in the AVI InfoFrame, these formats can represent any of the following formats:

a) 2880/4=720 pixels/line
b) 2880/2=1440 pixels/line
b) 2880/1=2880 pixels/line

If this timing is advertised in the EDID, the DTV Monitor shall be able to accept any of these pixel repetition factors.

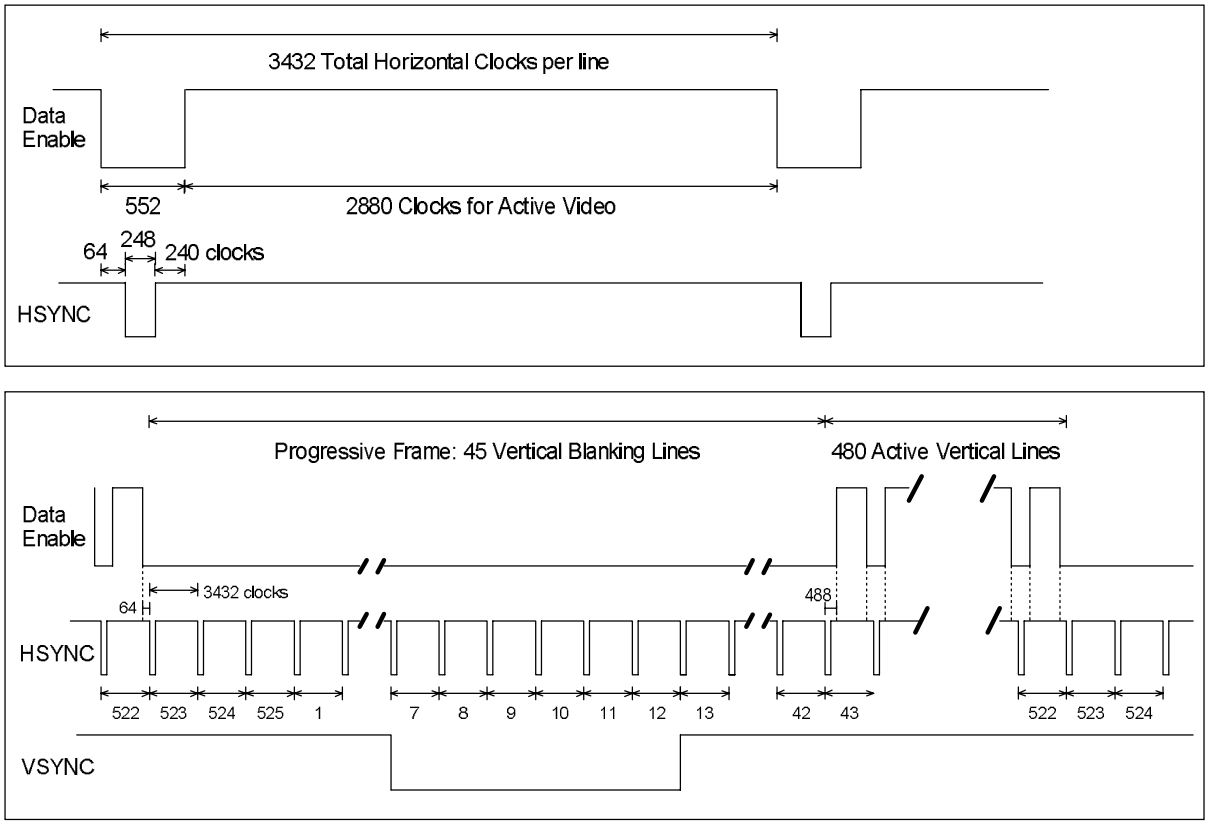

Figure 23 Timing Parameters for 2880x480p @ 59.94/60 Hz

4.25 2880x576p @ 50 Hz (Formats 37 and 38)

These formats can use either 4:3 or 16:9 aspect ratio. They provide additional bandwidth for carrying audio data and can also provide additional horizontal video resolution.

Depending upon the pixel repetition factor specified in the AVI InfoFrame, these formats can represent any of the following formats:

a) 2880/4=720 pixels/line
b) 2880/2=1440 pixels/line
b) 2880/1=2880 pixels/line

If this timing is advertised in the EDID, the DTV Monitor shall be able to accept any of these pixel repetition factors.

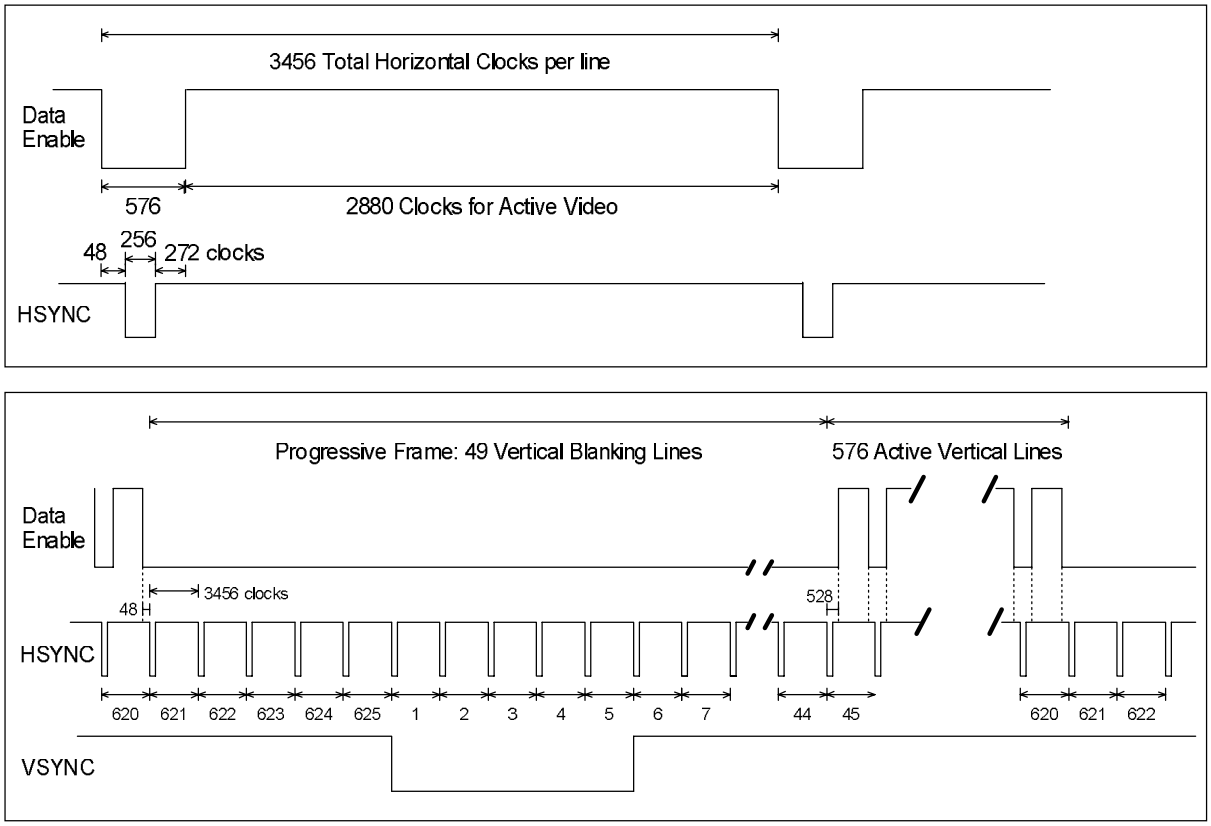

Figure 24 Timing Parameters for 2880x576p @ 50 Hz

4.26 1920x1080i (1250 Total) @ 50 Hz (Format 39)

This format is available only in a 16:9 aspect ratio. The format is specifically designed for use with 31.25 kHz constant horizontal rate cathode-ray tube televisions.

The format has a total of 1250 vertical lines - instead of the normal 1125 found in SMPTE 274 based timings. It has a frame, which is split into two unequal fields of 624.5 and 625.5 lines. The format is specifically designed for use with special 31.25 kHz constant horizontal rate cathode-ray tube televisions and should be used with caution. Timing is similar to the 1250/50/2:1 system that described in Australian AS 4933.1-2005 standard. See Figure 25 for details.

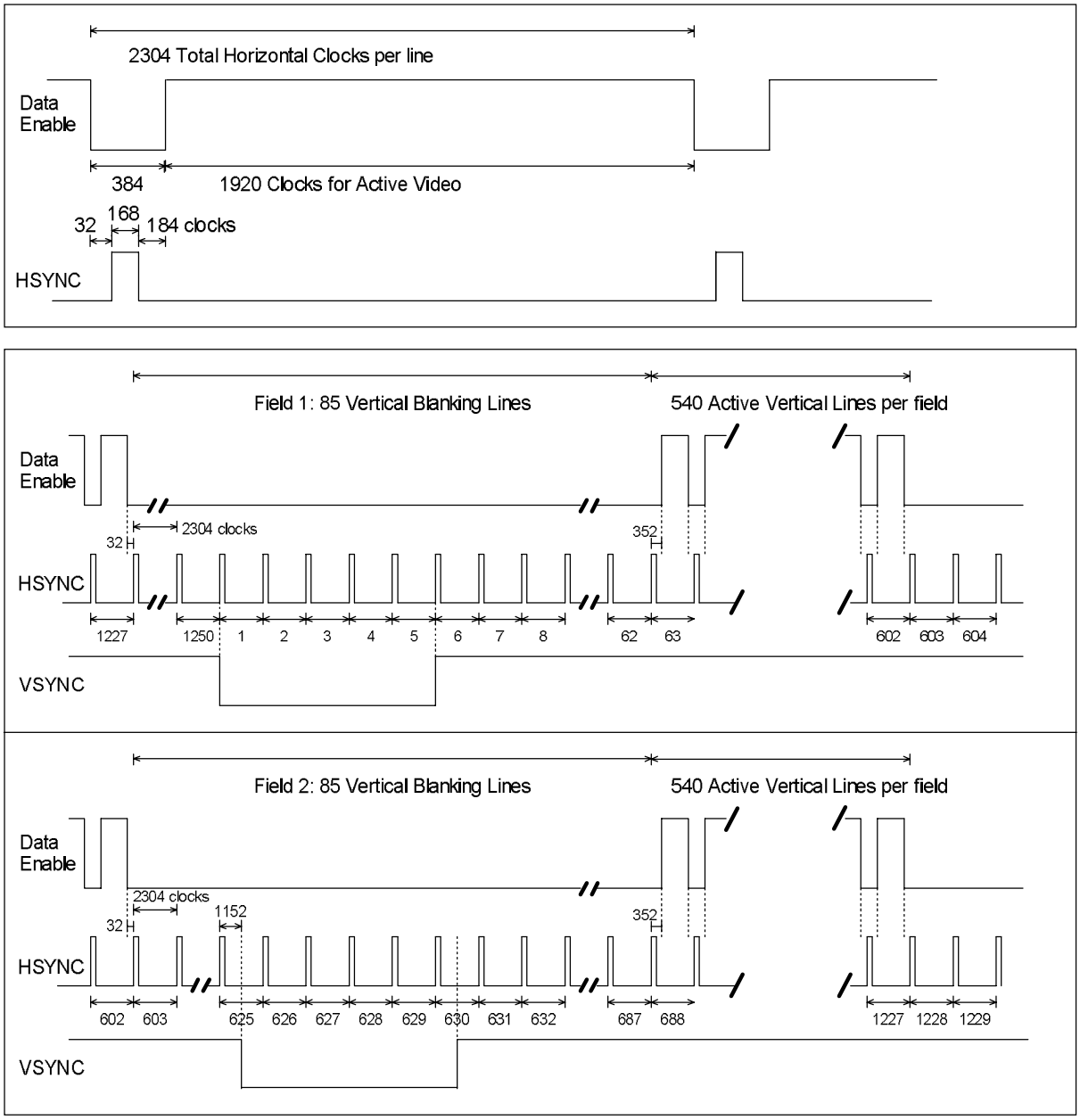

Figure 25 Timing Parameters for 1920x1080i (1250 Total) @ 50 Hz

4.27 1920x1080i @ 100 Hz (Format 40)

This is a high frame rate version of the video format described in Section 4.8. This format is available only in a 16:9 aspect ratio. See Figure 26.

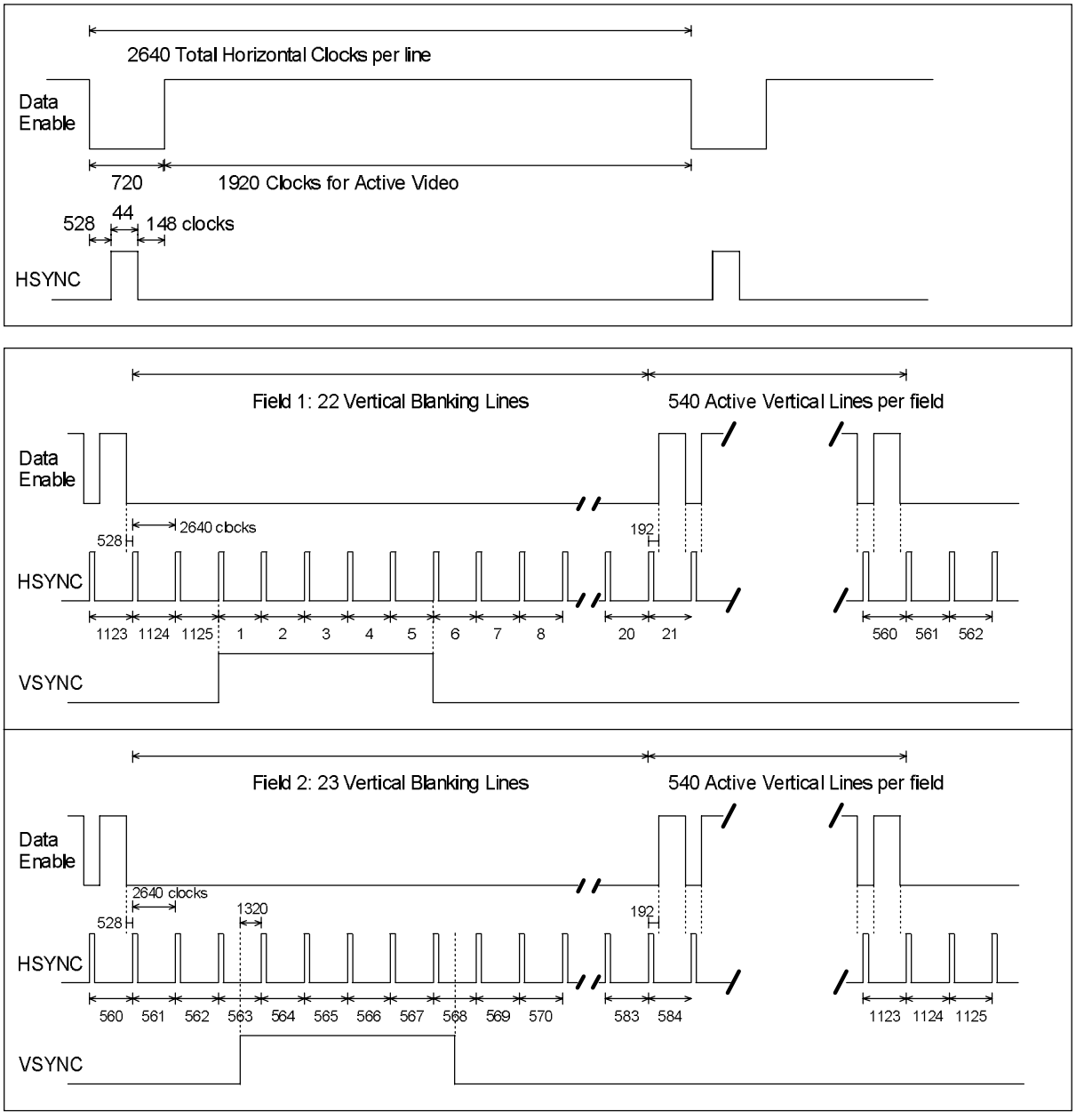

Figure 26 Timing Parameters for 1920x1080i @100 Hz

4.28 1280x720p @ 100 Hz (Format 41)

This is a high frame rate version of the video format described in Section 4.7. This format is available only in a 16:9 aspect ratio. See Figure 27.

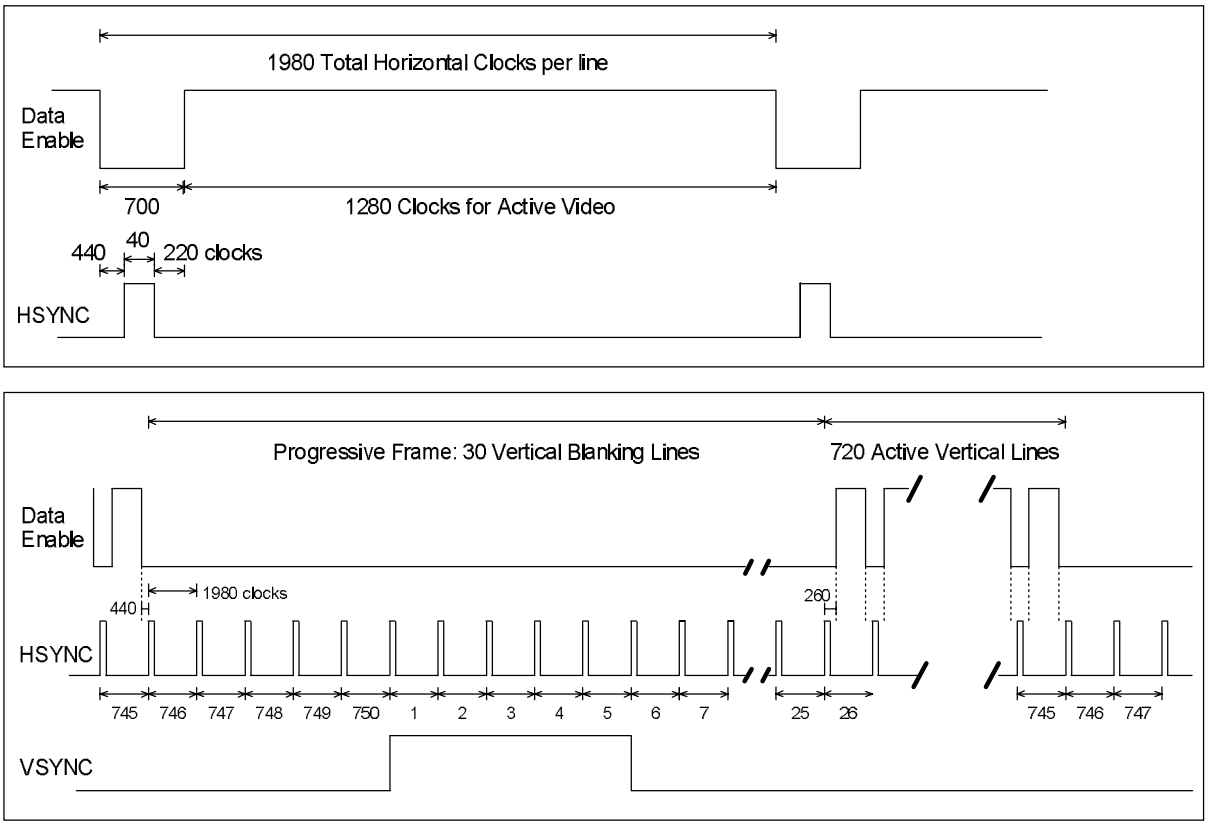

Figure 27 Timing Parameters for 1280x720p @ 100 Hz

4.29 720x576p @ 100 Hz (Formats 42 and 43)

This is a high frame rate version of the video format described in Section 4.9. This format timing can use either 4:3 or 16:9 aspect ratio. See Figure 28.

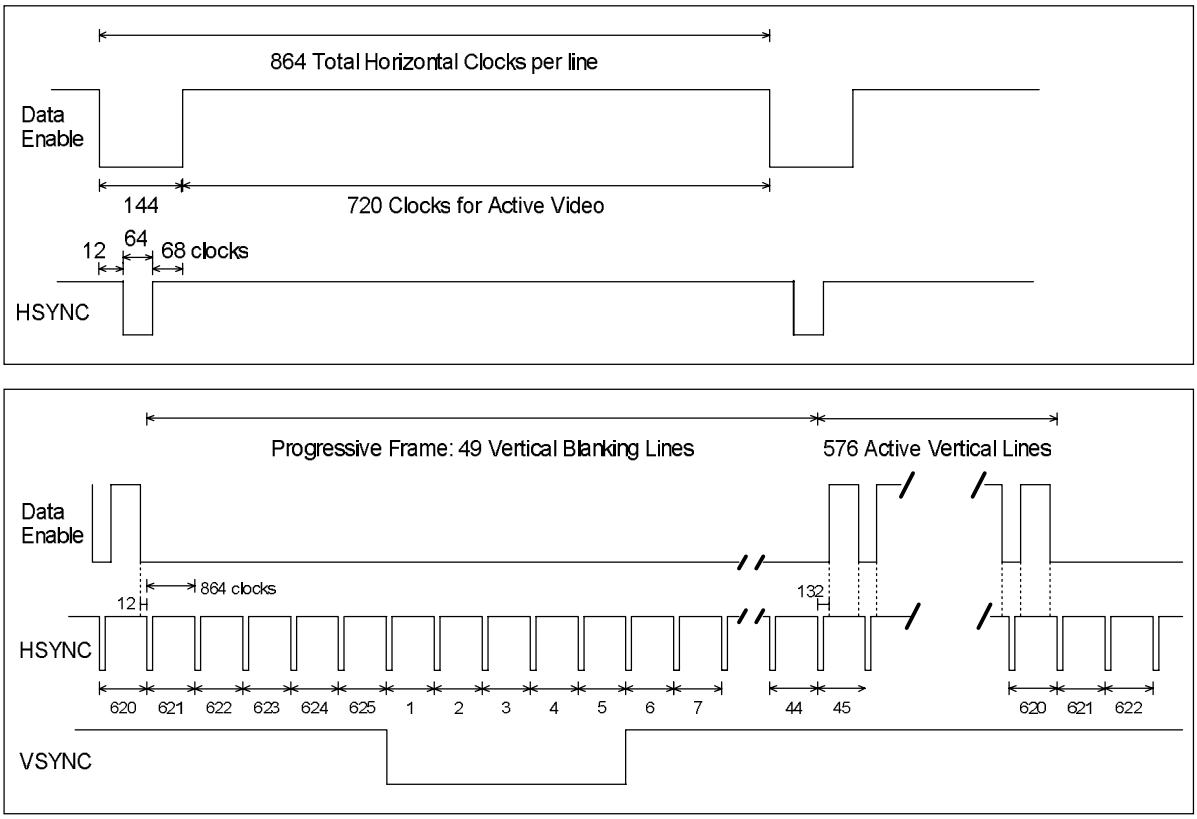

Figure 28 Timing Parameters for 720x576p @ 100 Hz

4.30 720(1440)x576i @ 100 Hz (Formats 44 and 45)

This is a high frame rate version of the video format described in Section 4.10. This format assumes the pixels are double clocked. This format timing can use 4:3 or 16:9 aspect ratio. See Figure 29.

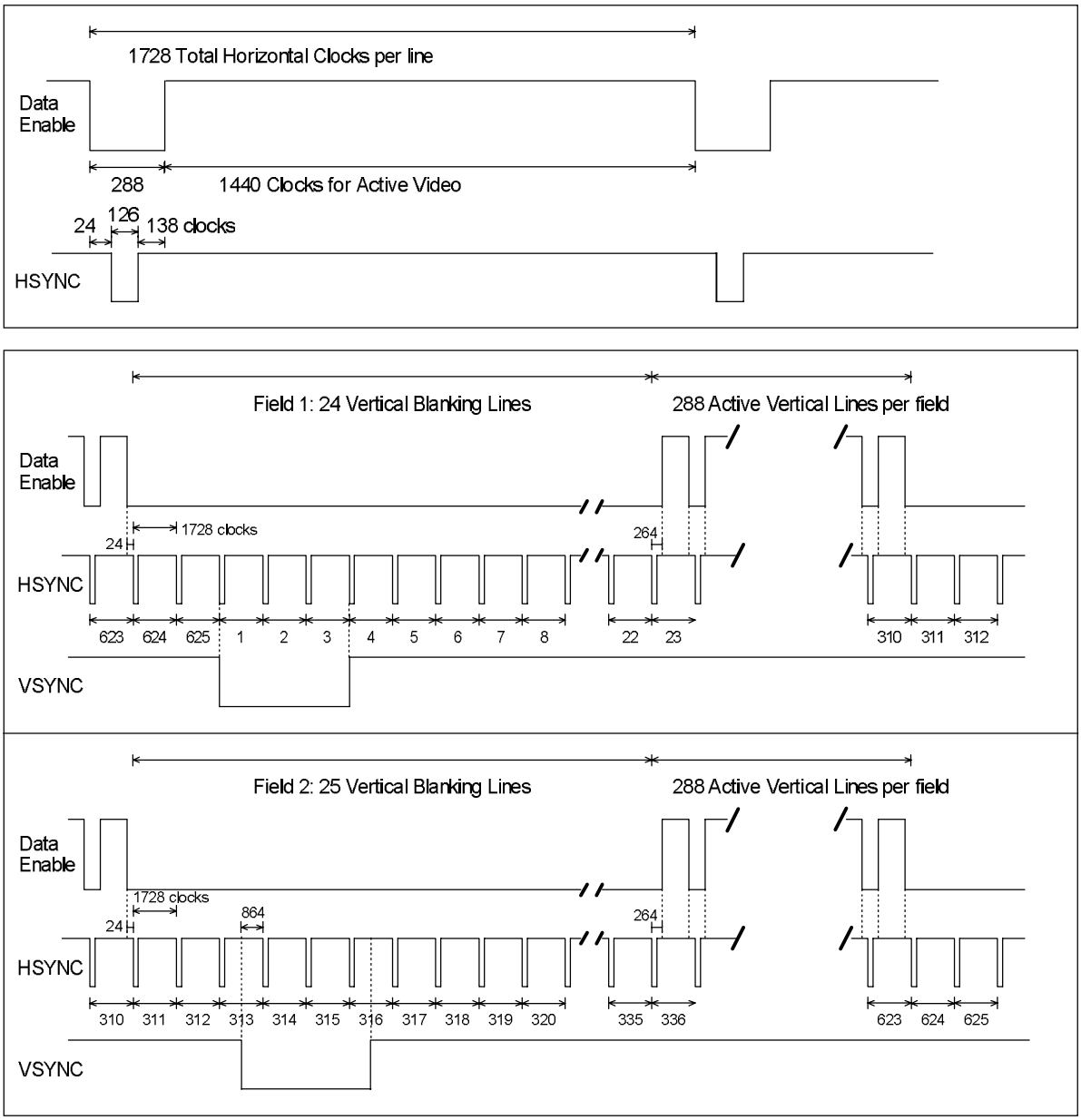

Figure 29 Timing Parameters for 720(1440)x576 @ 100 Hz

4.31 1920x1080i @ 119.88/120 Hz (Format 46)

This is a high frame rate version of the video format described in Section 4.4. This format is available only in a 16:9 aspect ratio. See Figure 30.

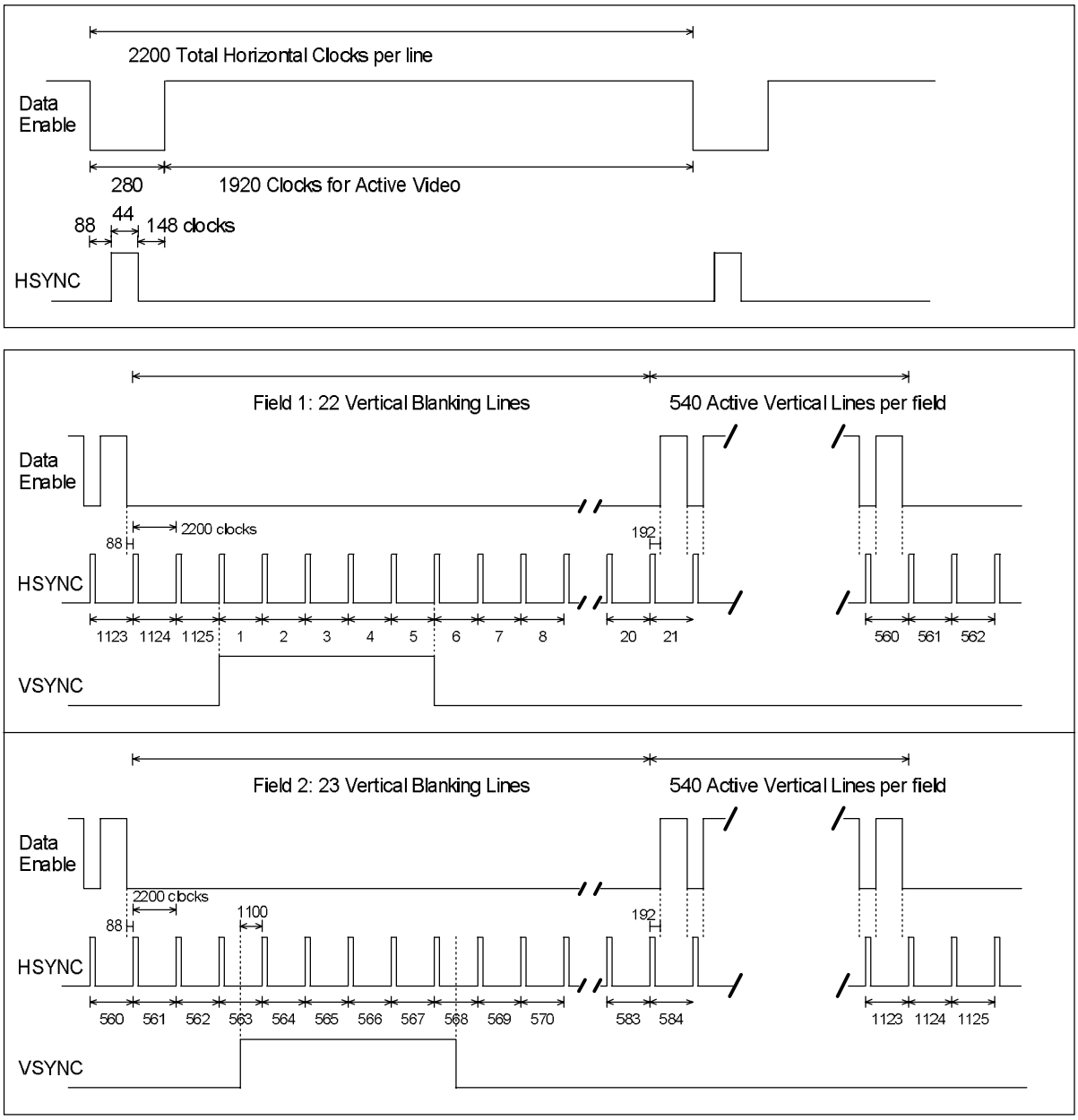

Figure 30 Timing Parameters for 1920x1080i @119.88/120 Hz

4.32 1280x720p @ 119.88/120 Hz (Format 47)

This is a high frame rate version of the video format described in Section 4.3. This format is available only in a 16:9 aspect ratio. See Figure 31.

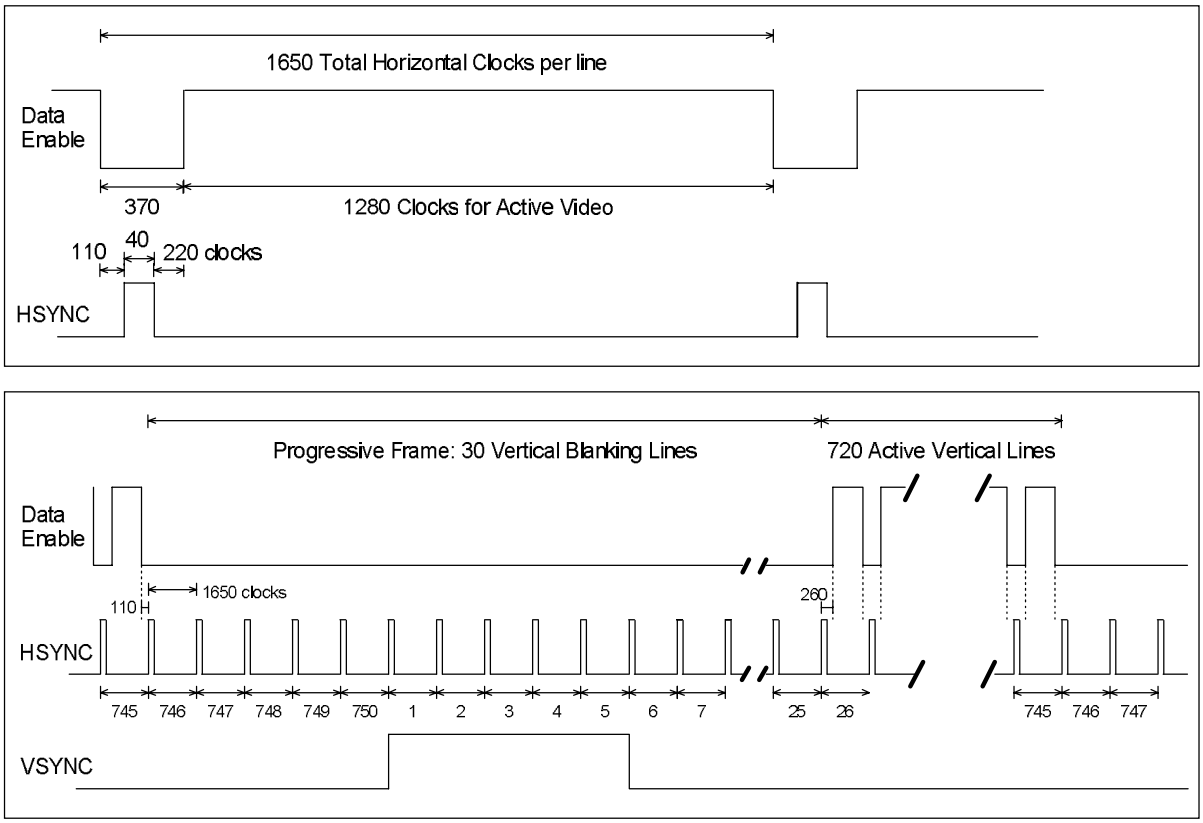

Figure 31 Timing Parameters for 1280x720p @ 119.88/120 Hz

4.33 720x480p @ 119.88/120 Hz (Formats 48 and 49)

This is a high frame rate version of the video format described in Section 4.5. This format timing can use either 4:3 or 16:9 aspect ratio. See Figure 32.

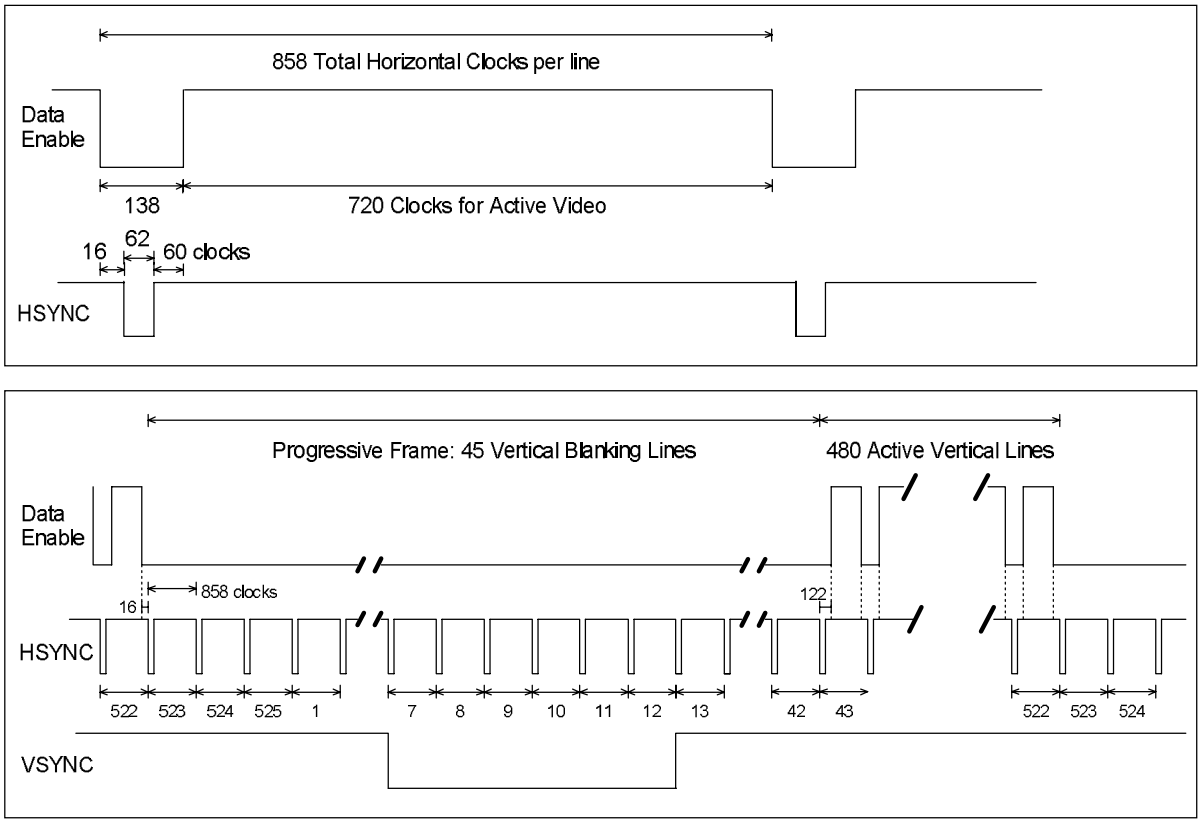

Figure 32 Timing Parameters for 720x480p @ 119.88/120 Hz

4.34 720(1440)x480i @ 119.88/120 Hz (Formats 50 and 51)

This is a high frame rate version of the video format described in Section 4.6. This format assumes the pixels are double clocked. This format timing can use 4:3 or 16:9 aspect ratio. See Figure 33.

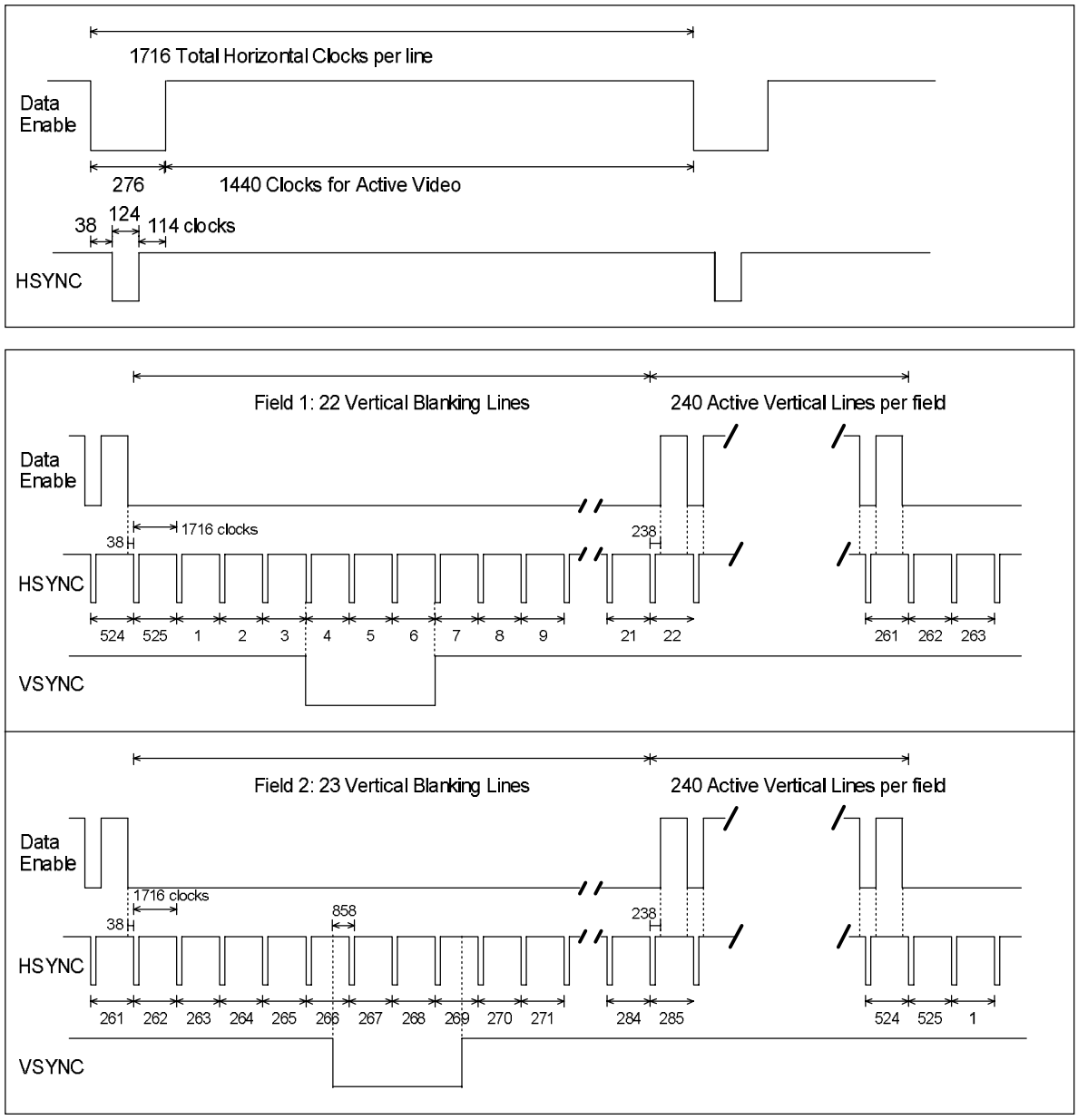

Figure 33 Timing Parameters for 720(1440)x480i @ 119.88/120 Hz

4.35 720x576p @ 200 Hz (Formats 52 and 53)

This is a high frame rate version of the video format described in Section 4.9. This format timing can use either 4:3 or 16:9 aspect ratio. See Figure 34.

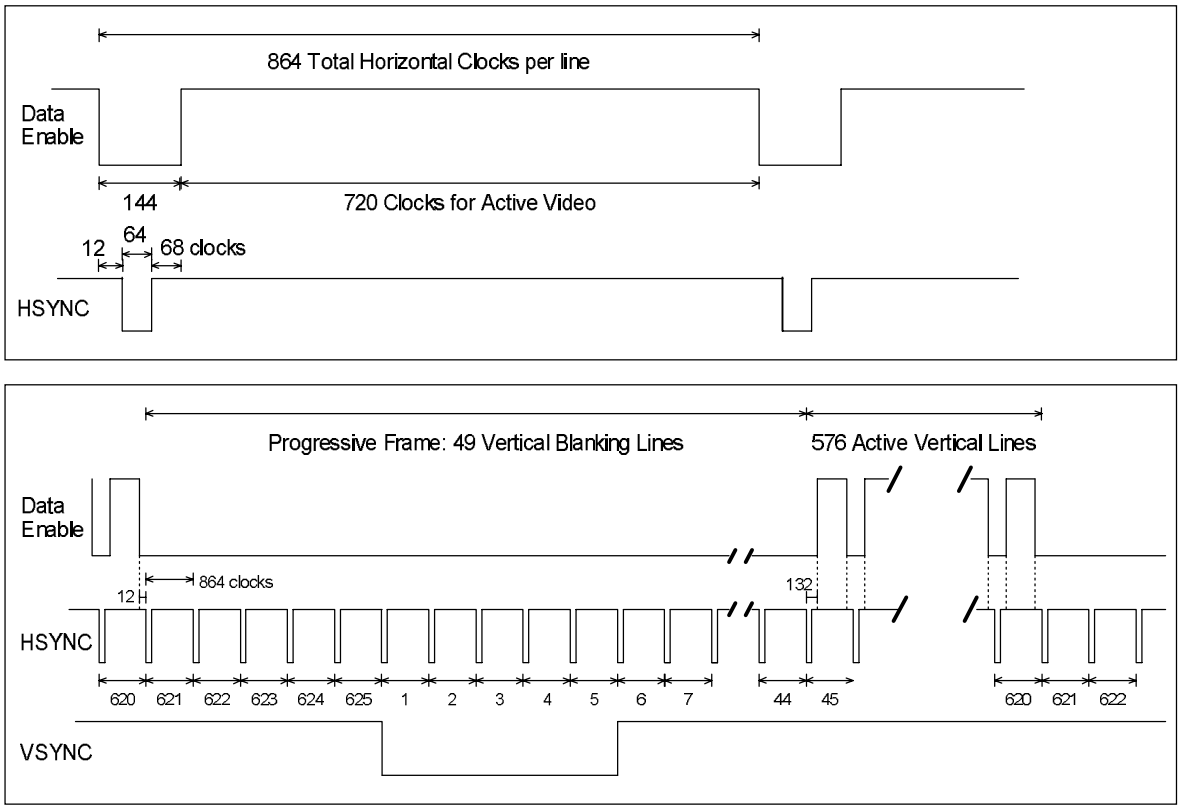

Figure 34 Timing Parameters for 720x576p @ 200 Hz

4.36 720(1440)x576i @ 200 Hz (Formats 54 and 55)

This is a high frame rate version of the video format described in Section 4.10. This format assumes the pixels are double clocked. This format timing can use 4:3 or 16:9 aspect ratio.

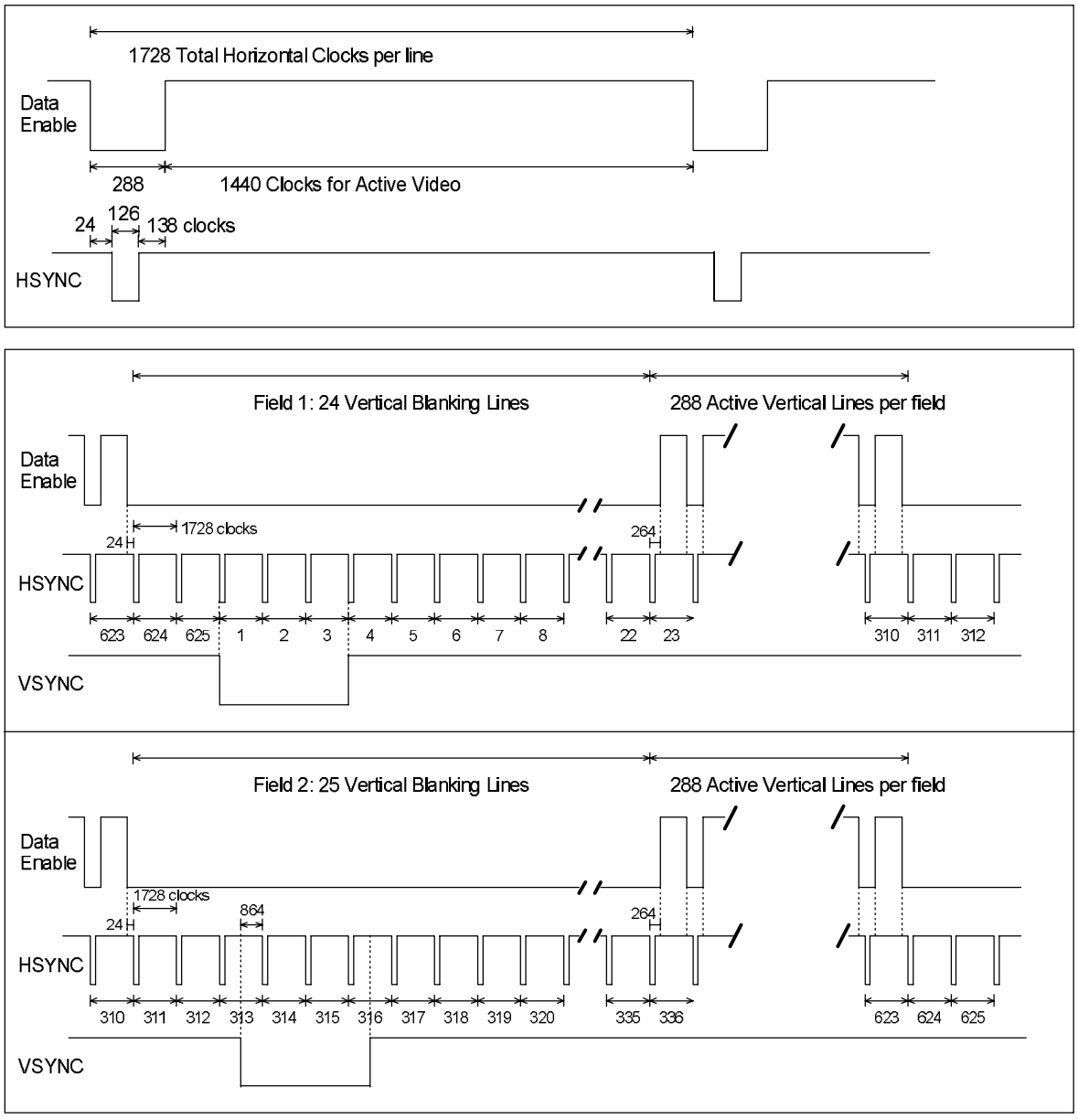

Figure 35 Timing Parameters for 720(1440)x576i @ 200 Hz

4.37 720x480p @ 239.76/240 Hz (Formats 56 and 57)

This is a high frame rate version of the video format described in Section 4.5. This format timing can use either 4:3 or 16:9 aspect ratio. See Figure 36.

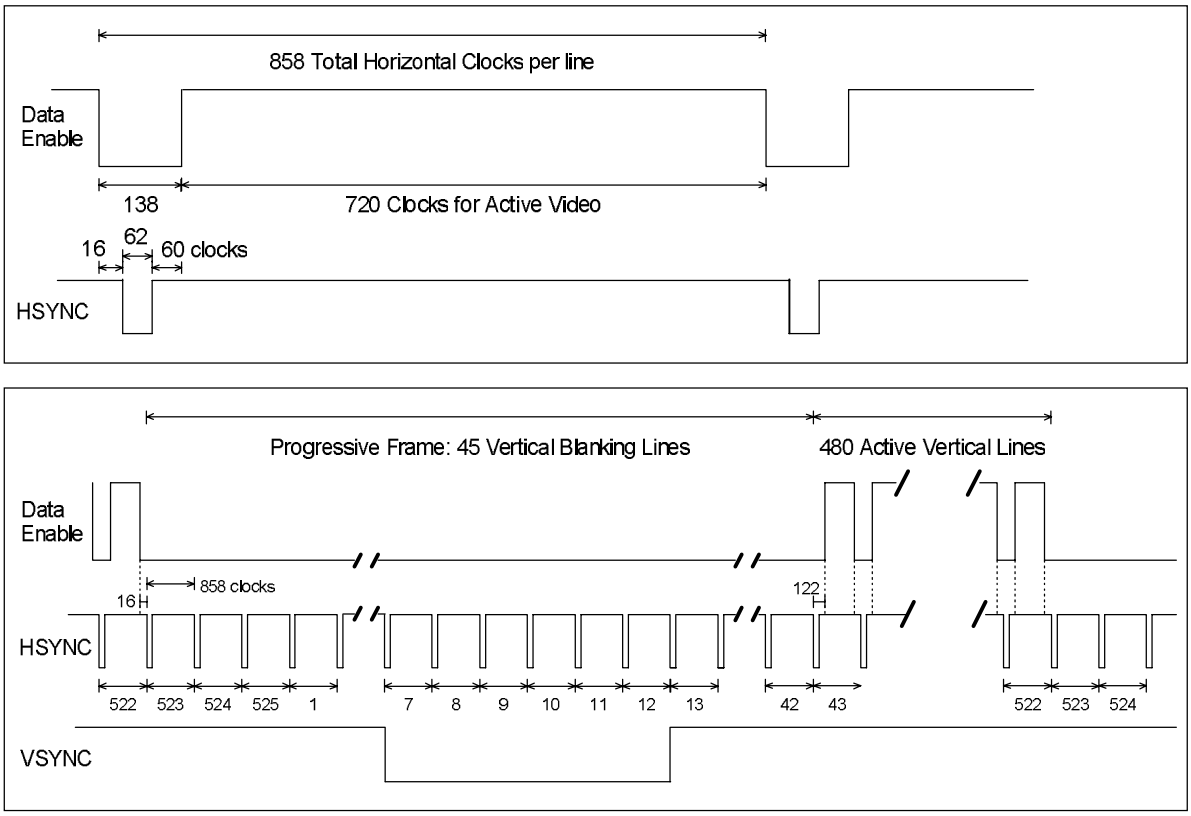

Figure 36 Timing Parameters for 720x480p @ 239.76/240 Hz

4.38 720(1440)x480i @ 239.76/240 Hz (Formats 58 and 59)

This is a high frame rate version of the video format described in Section 4.6. This format assumes the pixels are double clocked. This format timing can use 4:3 or 16:9 aspect ratio.

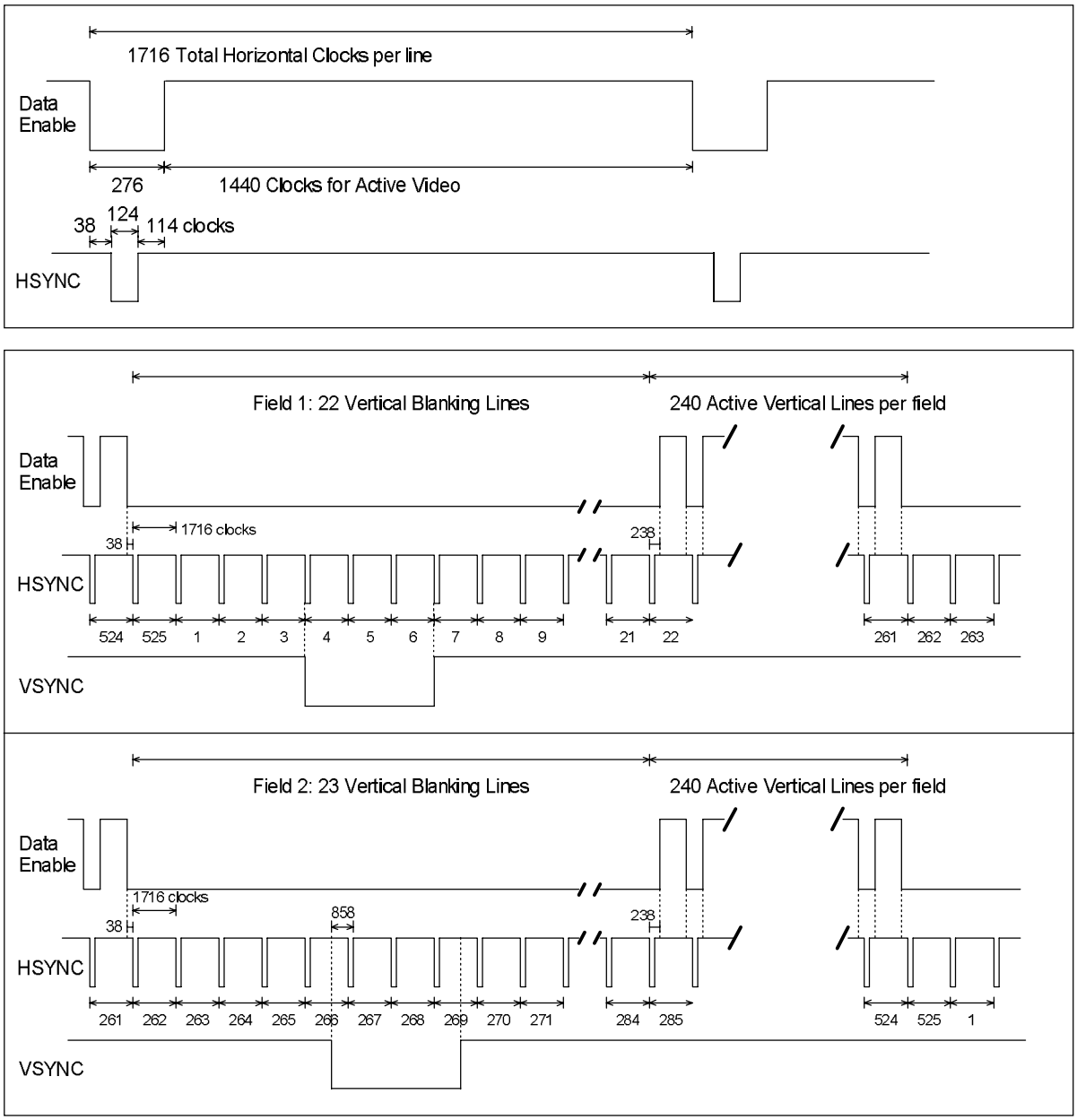

Figure 37 Timing Parameters for 720(1440)x480i @ 239.76/240 Hz

5 Colorimetry and Quantization

This interface shall be capable of supporting RGB (red, green, and blue), with encoding parameters based on the format. The interface may optionally support YC_BC_R.

5.1 480p, 480i, 576p, 576i, 240p, and 288p

The default color space used by the 480-line, 576-line, 240-line, and 288-line formats is that specified in SMPTE 170M [1].[4]

ITU-R BT.601-5 Section 3.5 [5] (or CEA-770.2-C Section 3.3 [19]) shall be used for any color space conversion needed in the course of processing unless a different colorimetry is specified in the Auxiliary Video Information InfoFrame.

The encoding parameter values shall be as defined in Table 3 of ITU-R BT.601-5 [5] and are summarized below:

The coding shall be 8-bit coding (scale of 0 to 255). R, G, B, and Y signals shall have 220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally move beyond level 235. C_BC_R signals shall have 225 quantization levels with a zero level corresponding to digital level 128 and the full range corresponding with 16 to 240. For R, G, B, Y, C_B, C_R signals, 0 and 255 are reserved and should not be considered video. See Section 5.4 for 640x480p and other IT video formats.

5.2 1080i, 1080p, and 720p

The default color space used by the high definition formats is that specified in ITU-R BT.709-5 [6].

ITU-R BT.709-5 Part 1, Section 4 [6] (or CEA-770.3-C Sections 5.4-5.7 [20]) shall be used for any color space conversion needed in the course of processing unless a different colorimetry is specified in the AVI.

The digital representation shall be as defined in Part 1, Section 6.10 of ITU-R BT.709-5 and is summarized below:

The coding shall be 8-bit coding (scale of 0 to 255). R, G, B, and Y signals shall have 220 quantization levels with the black level corresponding to level 16 and the peak white level corresponding to level 235. The signal level may occasionally move beyond level 235. C_BC_R signals shall have 225 quantization levels with a zero level corresponding to digital level 128 and full range corresponding with 16 to 240. For R, G, B, Y, C_B, C_R signals, 0 and 255 are reserved and should not be considered video. See section 5.4 for 640x480p and other IT video formats.

5.3 Recommendations on Conversions to/from Analog Signals

If the digital video signal is converted to an analog signal in the sink device, it is recommended that for RGB or Y, the black level (i.e., sync level and blanking level) should be aligned with the video portion of the signal at digital levels 16 and the white level at digital level 235, such that the full range of the digital to analog converted signal is the same as the actual video.[5] This means that zero analog level (0.0 IRE) should be associated with digital level 16. Digital levels 1 - 15 (undershoot region) and level 235 - 254 (overshoot region) are recommended to be passed through the digital to analog converter; however, full range of the analog signal should be aligned with 16-235 since it is expected that essential video is in the 16-235 range. For the 640x480p format, it is recommended that the full 0-255 range be displayed for this format.

If the digital video signal is converted to an analog signal, it is recommended that for the C_BC_R portion of the YC_BC_R digital signal (P_B, P_R for analog signal), the clamping level (sync level and blanking level) should be aligned with digital level 128 and the full range of the analog signal should be aligned with

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[4] The service provider (e.g., cable, DBS, terrestrial, etc.) is expected to signal to the source device (receiver, video card, etc.) via its digital Transport Stream, which color space is being transmitted and associated with the video content.

[5] RGB signals have the same notation in the digital and analog domains. Typically, Y, C_B, C_R notation is used for digital domains; and Y, P_B, P_R is used for analog domains.

digital level 16 to 240. However, the digital to analog converter may pass the full 1-254 range or may pass levels 16-254. See section 5.4 for 640x480p and other IT video formats.

5.4 IT formats

The color space used by IT formats is out of the scope of this specification but will commonly be sRGB, specified in IEC 61966-2-1 [33].

When transmitting IT formats using an RGB color space, the coding shall be 8-bit coding with a default R, G, and B signal quantization of 256 levels with the black level corresponding to level 0 and the white level corresponding to level 255. When transmitting using a YC_BC_R color space, the coding and quantization ranges for YC_BC_R shall correspond to those described in Section 5.1 and Section 5.2.

6 Auxiliary Information Carried from Source to DTV Monitor

Various types of auxiliary data can be carried from the Source to the DTV Monitor using InfoFrames. This section describes the InfoFrames that have been defined so far.

The actual mechanism for carrying these InfoFrames may vary depending on the digital interface being used[6].

> NOTE—Previous versions of CEA-861-D relied on a Revision number in the included CEA Extension to indicate whether the DTV Monitor could accept InfoFrames. Due to a significant number of DVI (not InfoFrame-capable) sink devices having the Revision Number set to 3, indicating support of InfoFrames, and not being capable of doing so, it is necessary to deprecate this requirement and thus, source and sink devices shall not rely on the Revision Number. Sink devices shall now declare InfoFrame capability by including an interface related (e.g. HDMI) VSDB in their EDID via CEA Extension. Source devices shall only assume InfoFrame capability, when an appropriate (e.g. HDMI) VSDB is found.

DVI does not support the transmission of any InfoFrames, independent of CEA Extension version number. CEA-861-D sink devices accept any of the InfoFrames defined here.

Five types of InfoFrames are defined in CEA-861-D (Auxiliary Video Information InfoFrame, Vendor Specific InfoFrame, Source Product Description InfoFrame, Audio InfoFrame, and MPEG Source InfoFrame). The assigned type codes for these InfoFrames are shown in Table 4. The first byte of the InfoFrame designates the type of InfoFrame while the second byte indicates the version of that particular InfoFrame. All future versions of a specific InfoFrame shall be backward compatible with previous versions. They may contain additional information, but old and new devices should be able to access and interpret the information previously present. All of the InfoFrames defined in CEA-861-D are version 1 except for the AVI InfoFrame which has a version 1 (now obsolete) and version 2. The InfoFrame Length Field is contained in the third byte of each InfoFrame. This length field is the total number of bytes in the InfoFrame Payload. It does not include the Type, Version, or Length fields. In the case of the Vendor Specific InfoFrame, the length includes the 24-bit IEEE Registration ID, as well as any additional bytes defined by the vendor to be in the InfoFrame (see Table 5).

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[6] Neither DVI 1.0 [3] nor OpenLDI 0.95 [7] contain a mechanism for transporting InfoFrames. These physical interfaces can be used to implement this standard with reduced functionality. HDMI, which is backward compatible with DVI 1.0 and contains mechanisms for transferring InfoFrames, digital audio, and YC_BC_R pixel data, is available and can be used to implement the full capabilities of CEA-861-D.

Info Frame Type Code	Type of InfoFrame
00_{16}	Reserved
01_{16}	Vendor Specific (defined in Section 6.1)
02_{16}	Auxiliary Video Information (defined in Section 6.2)
03_{16}	Source Product Description (defined in Section 6.5)
04_{16}	Audio (defined in Section 6.6 of this document)
05_{16}	MPEG Source (defined in Section 6.7 of this document)
06_{16}-FF_{16}	Reserved for future use

Table 4 List of InfoFrame Type Codes

When creating new versions of an InfoFrame, the version number shall be incremented from what it was in the previous version. New versions of any specific InfoFrame shall contain all of the fields in the previous version for the purpose of backward compatibility. The length field shall always be set correctly so that DTV Monitors that don't fully understand the format of a given InfoFrame may skip to the end.

The contents of the Auxiliary Video Information InfoFrame are described in Section 6.2. The contents of the Product Description InfoFrame is described in Section 6.5. The contents of the Audio InfoFrame are described in Section 6.6. The contents of the MPEG Source InfoFrame are described in Section 6.7.

6.1 Vendor Specific InfoFrames

The content of the Vendor Specific InfoFrame is defined in Table 5. This InfoFrame can be used by product manufacturers or organizations who have an assigned 24-bit IEEE Registration Identifier to transport information not defined elsewhere. The Vendor Specific Payload would be defined by the organization to which the 24-bit IEEE number refers. The 24-bit IEEE number, also called "company_id" or OUI, is sent least significant byte first. It is recommended that the Vendor Specific Payload contain a "length field" to facilitate extensibility, but this is not required.

Byte #	Field Name	Contents
n	Vendor Specific InfoFrame Type Code	01_{16}
n+1	Vendor Specific InfoFrame Version	01_{16}
n+2	L_V InfoFrame Length	Total number of bytes in InfoFrame Payload including IEEE Registration ID
n+3	24 bit IEEE Registration Identifier	24 bit IEEE Registration ID[7] (Least Significant Byte first)
....		
n+5		
...	Vendor Specific Payload	Vendor Specific Payload
n+L_V-1		

Table 5 Vendor Specific InfoFrame

6.2 Auxiliary Video Information (AVI) InfoFrame

The AVI is carried in the AV-stream from the source device to the DTV Monitor as an InfoFrame.

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[7] The IEEE Registration Authority maintains a database of 24-bit numbers uniquely assigned to organizations and vendors. Any organization or vendor that wishes to define a vendor specific InfoFrame shall obtain a registration ID (also known as vendor ID, organizationally unique ID, or company ID) from:

Institute of Electrical and Electronic Engineers, Inc.
IEEE Registration Authority
c/o IEEE Standards Association
445 Hoes Lane
Piscataway, NJ 08855-1331

NOTE—Previous versions of CEA-861-D defined the Version 1 AVI InfoFrame. Support for version 1 is not included in CEA-861-D.

Sources shall not use AVI InfoFrame version 1.

If the source device supports the transmission of the Auxiliary Video Information (AVI) and if it determines that the DTV Monitor is capable of receiving that information, it shall send the AVI to the DTV Monitor once per VSYNC period. The data applies to the next full frame of video data.

For DTV Monitors that support any video format with video identification code greater than 7, or that simultaneously support two different aspect ratios for the same video format timing (e.g., dual-aspect ratio timings such as 720x480p), the DTV Monitor shall be able to receive and decode the AVI InfoFrame described in this Section. Simultaneous support of timings available in two different aspect ratios shall be indicated by listing both formats in the EDID data structure at the same time.

If, for some reason, an indication is received that conflicts with the video format being received (e.g., the source device indicates 4:3 but sends the 1920x1080i format), then the DTV Monitor shall ignore the conflicting information in the AVI.

If a DTV Monitor supports YC_BC_R (in addition to RGB), then it shall include the version 3 CEA Extension with at least one of the YC_BC_R bits set and shall be capable of receiving the AVI. If no AVI is being sent from the source device, then the DTV Monitor shall assume the video data is RGB.

The information on “Active Format Aspect Ratio,” bar widths, overscan/underscan, non-uniform picture scaling, and colorimetry is information that can be used by the DTV Monitor to improve the picture. Use of this information by the DTV Monitor is optional. If this information is present at the source device and valid,[8] and if the DTV Monitor is capable of receiving the AVI, it is required that this information be sent.

For DTV Monitors not capable of receiving AVI, the DTV Monitor shall not declare in its EDID data structure more than one format that is the same except for picture aspect ratio at the same time.

6.3 Format of Version 1 AVI InfoFrame

The Version 1 AVI InfoFrame was originally defined in a predecessor of CEA-861-D but not used. For historical purposes, the Version 1 AVI InfoFrame is shown in Table 6.

[8] The data may not be valid if, for example, the stream was converted from an analog signal with no reliable aspect ratio or format information.

Gst}vklx$Gsrwyq ivGtpigpuxsrngw$Ewwsgmexmsr$
Tvszmihs$[}9MLW$yrhiv$pqmirwi${md$GIES$
Rs$vitvshygpuxsr$sv$rix{svoork$tivqmxihs${mdsyx$pqmirwi$jusq9MLW
Wsph3es+HMKMXEP^SRI$JS2D$PXH2D$[4868846
RsxjsvViwepi0544;3;36$9><974$QX

InfoFrame Type Code	InfoFrame Type = 02_{16}							
InfoFrame Version Number	Version = 01_{16}							
Length of AVI InfoFrame	Length of AVI InfoFrame (13)							
Data Byte 1	F17=0	Y1	Y0	A0	B1	B0	S1	S0
Data Byte 2	C1	C0	M1	M0	R3	R2	R1	R0
Data Byte 3	F37=0	F36=0	F35=0	F34=0	F33=0	F32=0	SC1	SC0
Data Byte 4	F47=0	F46=0	F45=0	F44=0	F43=0	F42=0	F41=0	F40=0
Data Byte 5	F57=0	F56=0	F55=0	F54=0	F53=0	F52=0	F51=0	F50=0
Data Byte 6	Line Number of End of Top Bar (lower 8 bits)							
Data Byte 7	Line Number of End of Top Bar (upper 8 bits)							
Data Byte 8	Line Number of Start of Bottom Bar (lower 8 bits)							
Data Byte 9	Line Number of Start of Bottom Bar (upper 8 bits)							
Data Byte 10	Pixel Number of End of Left Bar (lower 8 bits)							
Data Byte 11	Pixel Number of End of Left Bar (upper 8 bits)							
Data Byte 12	Pixel Number of Start of Right Bar (lower 8 bits)							
Data Byte 13	Pixel Number of Start of Right Bar (upper 8 bits)							

Table 6 Auxiliary Video Information InfoFrame format (Version 1)

6.4 Format of Version 2 AVI InfoFrame

The format of the Version 2 AVI InfoFrame is backward compatible with Version 1. All of the fields that were contained in the Version 1 AVI InfoFrame are also contained in the Version 2 AVI InfoFrame. Their purpose and use remain unchanged. All fields of the Version 2 AVI are described here. The Version 2 AVI InfoFrame is shown in Table 7.

InfoFrame Type Code	InfoFrame Type = 02_{16}							
InfoFrame Version Number	Version = 02_{16}							
Length of AVI InfoFrame	Length of AVI InfoFrame (13)							
Data Byte 1	F17=0	Y1	Y0	A0	B1	B0	S1	S0
Data Byte 2	C1	C0	M1	M0	R3	R2	R1	R0
Data Byte 3	ITC	EC2	EC1	EC0	Q1	Q0	SC1	SC0
Data Byte 4	F47=0	VIC6	VIC5	VIC4	VIC3	VIC2	VIC1	VIC0
Data Byte 5	F57=0	F56=0	F55=0	F54=0	PR3	PR2	PR1	PR0
Data Byte 6	Line Number of End of Top Bar (lower 8 bits)							
Data Byte 7	Line Number of End of Top Bar (upper 8 bits)							
Data Byte 8	Line Number of Start of Bottom Bar (lower 8 bits)							
Data Byte 9	Line Number of Start of Bottom Bar (upper 8 bits)							
Data Byte 10	Pixel Number of End of Left Bar (lower 8 bits)							
Data Byte 11	Pixel Number of End of Left Bar (upper 8 bits)							
Data Byte 12	Pixel Number of Start of Right Bar (lower 8 bits)							
Data Byte 13	Pixel Number of Start of Right Bar (upper 8 bits)							

Table 7 Auxiliary Video Information (AVI) InfoFrame Format (Version 2)

Data Byte 1 (Table 8) contains bits that describe overscan/underscan (e.g., computer graphics or video), two bits to indicate whether optional YC_BC_R is being used, and bits that indicate the presence of valid active format and/or bar information. If the bar information and the active format information do not agree, then the bar information shall take precedence.

A source shall set S=1 (S1=0, S0=1) or S=2 (S1=1, S0=0) if it is confident of the accuracy of those values. Otherwise, it shall set S=0 (no data). The source shall follow these rules for setting S even in the absence of an indication that the sink responds to S.

A sink should adjust its scan based on S. Such a device would overscan if it received S=1, and underscan if it received S=2. If it receives S=0, then it should overscan for a CE format and underscan for an IT format. A sink should indicate its overscan/underscan behavior using a Video Capabilities Data Block (see Section 7.5.6).

F7	Future Use, all Zeros
0	

Y1	Y0	RGB or YCbCr
0	0	RGB (default)
0	1	YCbCr 4:2:2
1	0	YCbCr 4:4:4
1	1	Future

A0	Active Format Information Present
0	No Data
1	Active Format (R0…R3) Information valid

B1	B0	Bar Info
0	0	Bar Data not valid
0	1	Vert. Bar Info valid
1	0	Horiz. Bar Info Valid
1	1	Vert. and Horiz. Bar Info valid

S1	S0	Scan Information
0	0	No Data
0	1	Composed for an overscanned display, where some active pixels and lines at the edges are not displayed.
1	0	Composed for an underscanned display, where all active pixels & lines are displayed, with or without a border.
1	1	Future

Table 8 AVI InfoFrame Data Byte 1

Data Byte 2 (Table 9) contains bits that describe colorimetry, picture aspect ratio, and whether the active format information is valid. Data Byte 2, C0 and C1 are used in conjunction with Data Byte 3, EC0 through EC3 to indicate source material colorimetry. If bits C0 and C1 are zero, the colorimetry shall correspond to the default colorimetry described in Sections 5.1, Section 5.2 and Section 5.4.

C1	C0	Colorimetry
0	0	No Data
0	1	SMPTE 170M [1] ITU601 [5]
1	0	ITU709 [6]
1	1	Extended Colorimetry Information Valid (colorimetry indicated in bits EC0, EC1, EC2. See Table 11)

M1	M0	Picture Aspect Ratio
0	0	No Data
0	1	4:3
1	0	16:9
1	1	Future

R3	R2	R1	R0	Active Format Aspect Ratio
1	0	0	0	Same as picture aspect ratio
1	0	0	1	4:3 (Center)
1	0	1	0	16:9 (Center)
1	0	1	1	14:9 (Center)
other values				Per DVB AFD active_format field in ETSI [26].

Table 9 AVI InfoFrame Data Byte 2

Table 10 illustrates the terminology and examples of common aspect ratio information that can be communicated from a source device to a display device using CEA-861-D. It illustrates some of the possibilities for the two standard picture aspect ratios (4:3 and 16:9) with the active format over the picture. The “active format” codes shall be shall be transmitted when received with content. Originating devices creating such codes may create codes in accordance with the Active Format Description[9] (AFD) in the DVB specification [26].[10] All of the active format codes defined in [26] are reproduced in informative Annex H.

[9] Note that the use of the term “active” in the “Active Format Description” differs from how it is used in other places of this standard and documents referenced by this standard. Active usually refers to any and all addressable pixels. In this case, Active Format refers to the useful information within this active area.

[10] DVB [26] supports 10 active formats. Other active formats can be supported by the bar information contained in bytes 6-13 of the AVI InfoFrame.

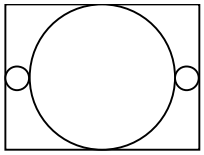
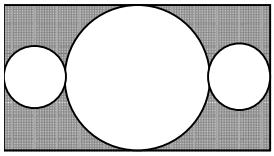
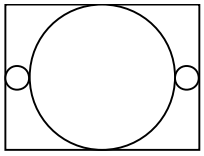
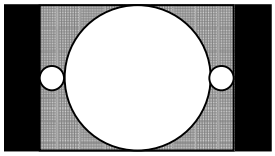
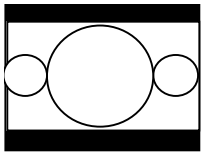
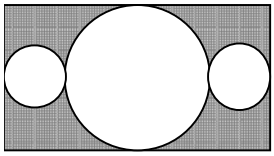
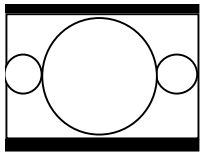
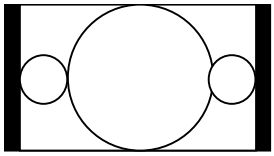
Active Format		Illustration of Described Format	
Value	**Description**	**4:3 Picture AR**	**16:9 Picture AR**
1000	Same as Picture		
1001	4:3 (center)		
1010	16:9 (center)		
1011	14:9 (center)		

Table 10 Common Active Formats

See CEA-CEB16 [22] for more information about AFD processing.

Data Byte 3 is divided into four sections as shown in Table 11.

Bits SC1 and SC0 provide information on whether the picture has been scaled in a non-uniform way (i.e., unequal along horizontal and vertical dimensions) prior to transmission to the DTV Monitor. The Nonuniform Picture Scaling bits shall be set if the source device scales the picture or has determined that scaling has been performed in a specific direction. If the picture has been stretched or shrunk in a uniform way (i.e., equally along both dimensions), then the bits should not be set. These bits are present to help avoid situations such as the one illustrated in Annex I.

Displays conforming to CEA-861-D accept both a limited quantization range of 220 levels (16 to 235) and a full range of 256 levels (0 to 255) when receiving video with RGB color space (see Sections 5.1, Section 5.2, Section 5.3 and Section 5.4). By default, RGB pixel data values should be assumed to have the limited range when receiving a CE video format, and the full range when receiving an IT format. The quantization bits allow the source to override this default and to explicitly indicate the current RGB quantization range. The value 0 (Q1=0, Q2=0) indicates that the current quantization range corresponds to the default range for the transmitted video format. A source shall not send a non-zero Q value that does not correspond to the default range for the transmitted video format unless the sink indicates support for the Q bit in a Video Capabilities Data Block (see Section 7.5.6).

The extended colorimetry bits, EC2, EC1, and EC0, describe optional colorimetry encoding that may be applicable to some implementations and are always present, whether their information is valid or not (see Section 7.5.5).

In IT applications (e.g. involving bit mapped text), each pixel in the source's frame buffer is most clearly displayed if it is directly mapped to a light-emitting pixel on the display device - such that adjacent pixels are completely independent and do not interact. The IT content bit indicates when picture content is composed according to common IT practice (i.e. without regard to Nyquist criterion) and is unsuitable for analog reconstruction or filtering. When the IT content bit is set to 1, downstream processors should pass pixel data unfiltered and without analog reconstruction.

ITC	IT content
0	No data
1	IT content

EC2	EC1	EC0	Extended Colorimetry
0	0	0	$xvYCC_{601}$
0	0	1	$xvYCC_{709}$
-	-	-	All other values reserved

Q1	Q0	RGB Quantization Range
0	0	Default (depends on video format)
0	1	Limited Range
1	0	Full Range
1	1	Reserved

SC1	SC0	Non-Uniform Picture Scaling
0	0	No Known non-uniform Scaling
0	1	Picture has been scaled horizontally
1	0	Picture has been scaled vertically
1	1	Picture has been scaled horizontally and vertically

Table 11 AVI InfoFrame Data Byte 3

Data Byte 4 contains a Video Identification Code. In most cases, the video format can be uniquely determined from the video format timing itself. However, if the source box is sending one of the video formats defined in this document, then it shall set this field to the proper code. If a video format not listed in CEA-861-D is sent, then the Video Identification Code shall be set to 0. If this field is used and if it is inconsistent with the video format being received, then it shall be ignored by the DTV Monitor. If the picture aspect ratio implied by this field does not agree with the picture aspect ratio communicated in Data Byte 2, then Data Byte 2 shall take precedence. The codes associated with each video format are shown in Table 3. These same codes are used in the Short Video Descriptors used in the Version 3 CEA Extension, which is described in Section 7.5. If the source device needs to convey "no information" regarding the video format (perhaps it is sending a proprietary format that was defined using the EDID Detailed Timing Descriptor in the DTV Monitor), then this field shall be set to 0.

Data Byte 5 contains the pixel repetition factor, which indicates to the DTV Monitor how many repetitions of each unique pixel are transmitted for the optional (2880)x480i/240p or (2880)x576i/288p or 1440x480p or 1440x576p formats. These are the only formats that allow for a range of values. In those cases, the AVI shall be sent to the DTV Monitor with this field set correctly and the DTV Monitor shall properly interpret it. As with all video formats, the source box shall read the EDID to determine if the specific format is supported before it sends it.

If the AVI InfoFrame is sent, then the Pixel Repeat field shall be set correctly no matter what video format is being transmitted. In non-repeated formats, this value is 0. For pixel-repeated formats, this value indicates the number of pixels that shall be decimated by the receiver or repeated depending on the signal process. In all cases, the first transmitted pixel data of a line of video is unique. If pixel repetition is used, subsequent pixels shall be repetition(s) of the previous pixel. The values for Pixel Repeat are shown in Table 12.

PR3	PR2	PR1	PR0	Pixel Repetition Factor
0	0	0	0	No Repetition (i.e., pixel sent once)
0	0	0	1	pixel sent 2 times (i.e., repeated once)
0	0	1	0	pixel sent 3 times
0	0	1	1	pixel sent 4 times
0	1	0	0	pixel sent 5 times
0	1	0	1	pixel sent 6 times
0	1	1	0	pixel sent 7 times
0	1	1	1	pixel sent 8 times
1	0	0	0	pixel sent 9 times
1	0	0	1	pixel sent 10 times
0Ah-0Fh				Reserved

Table 12 AVI InfoFrame Pixel Repetition Field, Data Byte 5

A list of allowable Pixel Repeat values for each CE video format is shown in Table 13. Note that this characteristic is independent of Picture Aspect Ratio.

Video Codes	Video Description	Valid Pixel Repeat Values
1	640x480p @ 59.94/60Hz	No Repetition
2, 3	720x480p @ 59.94/60Hz	No Repetition
4	1280x720p @ 59.94/60Hz	No Repetition
5	1920x1080i @ 59.94/60Hz	No Repetition
6, 7	720(1440)x480i @ 59.94/60Hz	pixel sent 2 times
8, 9	720(1440)x240p @ 59.94/60Hz	pixel sent 2 times
10, 11	2880x480i @ 59.94/60Hz	pixel sent 1 to 10 times
12, 13	2880x240p @ 59.94/60Hz	pixel sent 1 to 10 times
14, 15	1440x480p @ 59.94/60Hz	pixel sent 1 to 2 times
16	1920x1080p @ 59.94/60Hz	No Repetition
17, 18	720x576p @ 50Hz	No Repetition
19	1280x720p @ 50Hz	No Repetition
20	1920x1080i @ 50Hz	No Repetition
21, 22	720(1440)x576i @ 50Hz	pixel sent 2 times
23, 24	720(1440)x288p @ 50Hz	pixel sent 2 times
25, 26	2880x576i @ 50Hz	pixel sent 1 to 10 times
27, 28	2880x288p @ 50Hz	pixel sent 1 to 10 times
29, 30	1440x576p @ 50Hz	pixel sent 1 to 2 times
31	1920x1080p @ 50Hz	No Repetition
32	1920x1080p @ 23.98/24Hz	No Repetition
33	1920x1080p @ 25Hz	No Repetition
34	1920x1080p @ 29.98/30Hz	No Repetition
35, 36	2880x480p @ 59.94/60Hz	pixel sent 1, 2 or 4 times
37, 38	2880x576p @ 50Hz	pixel sent 1, 2 or 4 times
39	1920x1080i (1250) @ 50Hz	No Repetition
40	1920x1080i @ 100Hz	No Repetition
41	1280x720p @ 100Hz	No Repetition
42	720x576p @ 100Hz	No Repetition
43	720x576p @ 100Hz	No Repetition
44	720(1440)x576i @ 100Hz	pixel sent 2 times
45	720(1440)x576i @ 100Hz	pixel sent 2 times
46	1920x1080i @ 119.88/120Hz	No Repetition
47	1280x720p @ 119.88/120Hz	No Repetition
48	720x480p @ 119.88/120Hz	No Repetition
49	720x480p @ 119.88/120Hz	No Repetition
50	720(1440)x480i @ 119.88/120Hz	pixel sent 2 times
51	720(1440)x480i @ 119.88/120Hz	pixel sent 2 times
52	720x576p @ 200Hz	No Repetition
53	720x576p @ 200Hz	No Repetition
54	720(1440)x576i @ 200Hz	pixel sent 2 times
55	720(1440)x576i @ 200Hz	pixel sent 2 times
56	720x480p @ 239.76/240Hz	No Repetition
57	720x480p @ 239.76/240Hz	No Repetition
58	720(1440)x480i @ 239.76/240Hz	pixel sent 2 times
59	720(1440)x480i @ 239.76/240Hz	pixel sent 2 times

Table 13 Valid Pixel Repeat Values for Each Video Format Timing

Data Bytes 6 through 13 contain the size of bars as shown in Table 14. The 8 bytes of bar data are present in the AVI whether their information is valid or not. The packets and bits are defined below.

For the purposes of the Line Number and the Pixel Number, the pixel in the upper left hand corner is considered to be in row 1, column 1. Lines and pixels are numbered consecutively as they would appear on a display.[11] All of the values are unsigned integers.

a) **Line Number of End of Top Bar—**An unsigned integer value representing the last line of a horizontal letterbox bar area at the top of the picture. Zero means no horizontal bar is present at the top of the picture.
b) **Line Number of Start of Bottom Bar—**An unsigned integer value representing the first line of a horizontal letterbox bar area at the bottom of the picture. If greater than the Maximum Vertical Active Lines of the known format, no horizontal bar is present at the bottom of the picture.
c) **Pixel Number of End of Left Bar—**An unsigned integer value representing the last horizontal pixel of a vertical pillar-bar area at the left side of the picture. Zero means no vertical bar is present on the left of the picture.
d) **Pixel Number of Start of Right Bar—**An unsigned integer value representing the first horizontal pixel of a vertical pillar-bar area at the right side of the picture. If greater than the Maximum Horizontal Pixels of the known format, no vertical bar is present on the right side of the picture.

6.5 Source Product Description (SPD) InfoFrame

The Source Product Description (SPD) InfoFrame communicates the name and product type of the source device. This allows the user to see which device is being selected when changing inputs on the DTV Monitor.

Support of the SPD InfoFrame in the DTV Monitor is indicated by including an appropriate VSDB in the DTV Monitor's EDID data structure. The transmission of this InfoFrame is optional for the source device. The use of the information by the DTV Monitor is also optional. It shall not be sent more than once per video frame. If used, it is recommended that it be sent once every second.

The format of the Source Product Description InfoFrame is shown in Table 14.

[11] In this context, line numbers are not the same as the line numbers used in timing diagrams.

InfoFrame Type Code	InfoFrame Type = **03** $_{16}$	
InfoFrame Version Number	Version = 01 $_{16}$	
Length of Source Product Description InfoFrame	Length of Source Product Description InfoFrame = 25	
Data Byte 1	0	Vendor Name Character 1 VN1 (7bit ASCII code)
Data Byte 2	0	Vendor Name Character 2 VN2
Data Byte 3	0	Vendor Name Character 3 VN3
Data Byte 4	0	Vendor Name Character 4 VN4
Data Byte 5	0	Vendor Name Character 5 VN5
Data Byte 6	0	Vendor Name Character 6 VN6
Data Byte 7	0	Vendor Name Character 7 VN7
Data Byte 8	0	Vendor Name Character 8 VN8
Data Byte 9	0	Product Description Character 1 PD1 (7-bit ASCII code)
Data Byte 10	0	Product Description Character 2 PD2
Data Byte 11	0	Product Description Character 3 PD3
Data Byte 12	0	Product Description Character 4 PD4
Data Byte 13	0	Product Description Character 5 PD5
Data Byte 14	0	Product Description Character 6 PD6
Data Byte 15	0	Product Description Character 7 PD7
Data Byte 16	0	Product Description Character 8 PD8
Data Byte17	0	Product Description Character 9 PD9
Data Byte 18	0	Product Description Character 10 PD10
Data Byte 19	0	Product Description Character 11 PD11
Data Byte20	0	Product Description Character 12 PD12
Data Byte 21	0	Product Description Character 13 PD13
Data Byte 22	0	Product Description Character 14 PD14
Data Byte 23	0	Product Description Character 15 PD15
Data Byte 24	0	Product Description Character 16 PD16
Data Byte 25	**Source Device Information**	

Table 14 Source Product Description InfoFrame Format

The Vendor Name consists of eight 7-bit ASCII characters. The name should be left justified (i.e., first character in Data Byte 1) and all unused characters should be Null (i.e., 00_{16}). The Vendor Name is intended to be the name of the company whose name appears on the product. The Product Description (contained in Data Bytes 9-24) consists of sixteen 7-bit ASCII characters. This code is meant to be the model number of the product and may contain a short description also (e.g., RC5240 DVD Player). Data Byte 25 consists of a code that classifies the source device. Codes for the most common types of source devices are shown in Table 15.

Code	Source Device Information
00h	unknown
01h	Digital STB
02h	DVD player
03h	D-VHS
04h	HDD Videorecorder
05h	DVC
06h	DSC
07h	Video CD
08h	Game
09h	PC general
0Ah	Blu-Ray Disc (BD)
0Bh	Super Audio CD
0Ch ... FFh -	Reserved

Table 15 Source Product Description InfoFrame Data Byte 25

6.6 Audio InfoFrame

The Audio InfoFrame contains information that allows for the format of the digital audio streams to be identified more quickly via out-of-band information and, for multi-channel uncompressed audio (which does not otherwise give such information), provides channel allocation information for the sink device's speakers.

If the sink device supports any digital audio, it shall be capable of receiving the Audio InfoFrame and also capable of interpreting the audio identification information in Data Bytes 1-3. Support for digital audio other than basic audio is indicated in the Version 3 (or higher) CEA Extension (see Section 7.5).
If the sink device supports multi-channel (i.e., more than 2 channels) digital audio and has included speaker placement information in EDID (see Section 7.5), it shall be able to interpret the speaker channel assignment information and down-mix information in Data Bytes 4 & 5.

If the source device supports the transmission of the Audio InfoFrame and if it determines that the DTV Monitor is capable of receiving the Audio InfoFrame (i.e., the DTV Monitor has included CEA Extension Version 3 in EDID) and digital audio, then the Audio InfoFrame, with Data Bytes 1 through 3 set correctly, shall be sent once per VSYNC period while digital audio is being sent across the interface. The data applies to the audio associated with the next full frame of video data.

If the source device is sending multi-channel uncompressed audio, then it shall also send valid speaker channel allocation information and down-mix information in Data Bytes 4 & 5 of this InfoFrame.

The format of the Audio InfoFrame is shown in Table 16.

InfoFrame Type Code	InfoFrame Type = **04** $_{16}$							
InfoFrame Version Number	Version = 01 $_{16}$							
Length of Audio InfoFrame	Length of Audio InfoFrame (10)							
Data Byte 1	CT3	CT2	CT1	CT0	F13=0	CC2	CC1	CC0
Data Byte 2	F27=0	F26=0	F25=0	SF2	SF1	SF0	SS1	SS0
Data Byte 3	F37=0	F36=0	F35=0	F34=0	F33=0	F32=0	F31=0	F30=0
Data Byte 4	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Data Byte 5	DM_INH	LSV3	LSV2	LSV1	LSV0	F52=0	F51=0	F50=0
Data Byte 6	F67=0	F66=0	F65=0	F64=0	F63=0	F62=0	F61=0	F60=0
Data Byte 7	F77=0	F76=0	F75=0	F74=0	F73=0	F72=0	F71=0	F70=0
Data Byte 8	F87=0	F86=0	F85=0	F84=0	F83=0	F82=0	F81=0	F80=0
Data Byte 9	F97=0	F96=0	F95=0	F94=0	F93=0	F92=0	F91=0	F90=0
Data Byte 10	F107=0	F106=0	F105=0	F104=0	F103=0	F102=0	F101=0	F100=0

Table 16 Audio InfoFrame Format

6.6.1 Audio Identification Information

The information in Data Bytes 1-3 may be useful in identifying audio. If the DTV and the source device support more than “basic audio,” as defined by the physical/link specification, then this information shall be sent and shall accurately identify the stream while digital audio is being sent. If the source device only supports basic audio, it is not required to send this information, but it is recommended. In most cases, it is possible to identify the audio by parsing the actual audio stream (e.g., as specified in IEC 61937 [32]). In cases where the audio information in the Audio InfoFrame does not agree with the actual audio stream being received, the conflicting information in the Audio InfoFrame shall be ignored.

NOTE—HDMI requires the CT, SS and SF fields to be set to 0 ("Refer to Stream Header") as these items are carried in the audio stream.

Data Byte 3 is reserved and shall be zero.

CT3	CT2	CT1	CT0	Audio Coding Type
0	0	0	0	Refer to Stream Header
0	0	0	1	IEC 60958 PCM [30, 31]
0	0	1	0	AC-3
0	0	1	1	MPEG1 (Layers 1 & 2)
0	1	0	0	MP3 (MPEG1 Layer 3)
0	1	0	1	MPEG2 (multichannel)
0	1	1	0	AAC
0	1	1	1	DTS
1	0	0	0	ATRAC
1	0	0	1	One Bit Audio
1	0	1	0	Dolby Digital +
1	0	1	1	DTS-HD
1	1	0	0	MAT (MLP)
1	1	0	1	DST
1	1	1	0	WMA Pro
1	1	1	1	Reserved

CC2	CC1	CC0	Audio Channel Count
0	0	0	Refer to Stream Header
0	0	1	2ch
0	1	0	3ch
0	1	1	4ch
1	0	0	5ch
1	0	1	6ch
1	1	0	7ch
1	1	1	8ch

Table 17 Audio InfoFrame Data Byte 1

SF2	SF1	SF0	Sampling Frequency
0	0	0	Refer to Stream Header
0	0	1	32 kHz
0	1	0	44.1 kHz (CD)
0	1	1	48 kHz
1	0	0	88.2 kHz
1	0	1	96 kHz
1	1	0	176.4 kHz
1	1	1	192 kHz

SS1	SS0	Sample Size
0	0	Refer to Stream header
0	1	16 bit
1	0	20 bit
1	1	24 bit

Table 18 Audio InfoFrame Data Byte 2

6.6.2 Speaker Mapping and Down-mix Information

Data Bytes 4 and 5 apply only to multi-channel (i.e., more than two channels) uncompressed audio.

CEA-861-D contains the capability to transmit Multi-Channel Linear Pulse Code Modulation (LPCM) Audio by using up to four IEC 60958 compliant transport streams. This is because the Audio InfoFrame and the CEA Extension are capable of supporting up to eight channels of LPCM. However, additional information is required to support carriage of Multi-Channel LPCM streams. This information is provided by the speaker channel allocation information in Data Byte 4.

Data Byte 4 contains information that describes how various speaker locations are allocated to transmission channels. Data Byte 5 contains information that tells the DTV Monitor how much the source device attenuated the audio during a down-mixing operation. The down-mix inhibit flag (**DM_INH**) describes whether audio output is permitted to be down-mixed or not. This flag is used in DVD Audio applications.

The labels and placements of speakers used in CEA-861-D are defined in Figure 38 and Table 19.

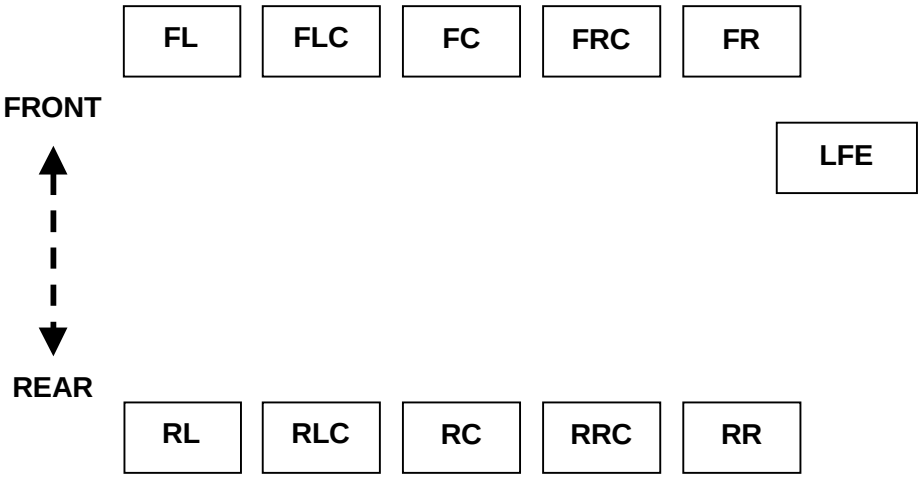


Figure 38 Speaker Placement

Label	Location
FL	Front Left
FC	Front Center
FR	Front Right
FLC	Front Left Center
FRC	Front Right Center
RL	Rear Left
RC	Rear Center
RR	Rear Right
RLC	Rear Left Center
RRC	Rear Right Center
LFE	Low Frequency Effect

Table 19 Speaker Placement

Data Byte 4 contains information that describes how various speaker locations are allocated to transmission channels. The channel allocation is shown in Table 20.

CA (binary)								CA (hex)	Channel Number							
7	6	5	4	3	2	1	0		8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	00	-	-	-	-	-	-	FR	FL
0	0	0	0	0	0	0	1	01	-	-	-	-	-	LFE	FR	FL
0	0	0	0	0	0	1	0	02	-	-	-	-	FC	-	FR	FL
0	0	0	0	0	0	1	1	03	-	-	-	-	FC	LFE	FR	FL
0	0	0	0	0	1	0	0	04	-	-	-	RC	-	-	FR	FL
0	0	0	0	0	1	0	1	05	-	-	-	RC	-	LFE	FR	FL
0	0	0	0	0	1	1	0	06	-	-	-	RC	FC	-	FR	FL
0	0	0	0	0	1	1	1	07	-	-	-	RC	FC	LFE	FR	FL
0	0	0	0	1	0	0	0	08	-	-	RR	RL	-	-	FR	FL
0	0	0	0	1	0	0	1	09	-	-	RR	RL	-	LFE	FR	FL
0	0	0	0	1	0	1	0	0A	-	-	RR	RL	FC	-	FR	FL
0	0	0	0	1	0	1	1	0B	-	-	RR	RL	FC	LFE	FR	FL
0	0	0	0	1	1	0	0	0C	-	RC	RR	RL	-	-	FR	FL
0	0	0	0	1	1	0	1	0D	-	RC	RR	RL	-	LFE	FR	FL
0	0	0	0	1	1	1	0	0E	-	RC	RR	RL	FC	-	FR	FL
0	0	0	0	1	1	1	1	0F	-	RC	RR	RL	FC	LFE	FR	FL
0	0	0	1	0	0	0	0	10	RRC	RLC	RR	RL	-	-	FR	FL
0	0	0	1	0	0	0	1	11	RRC	RLC	RR	RL	-	LFE	FR	FL
0	0	0	1	0	0	1	0	12	RRC	RLC	RR	RL	FC	-	FR	FL
0	0	0	1	0	0	1	1	13	RRC	RLC	RR	RL	FC	LFE	FR	FL
0	0	0	1	0	1	0	0	14	FRC	FLC	-	-	-	-	FR	FL
0	0	0	1	0	1	0	1	15	FRC	FLC	-	-	-	LFE	FR	FL
0	0	0	1	0	1	1	0	16	FRC	FLC	-	-	FC	-	FR	FL
0	0	0	1	0	1	1	1	17	FRC	FLC	-	-	FC	LFE	FR	FL
0	0	0	1	1	0	0	0	18	FRC	FLC	-	RC	-	-	FR	FL
0	0	0	1	1	0	0	1	19	FRC	FLC	-	RC	-	LFE	FR	FL
0	0	0	1	1	0	1	0	1A	FRC	FLC	-	RC	FC	-	FR	FL
0	0	0	1	1	0	1	1	1B	FRC	FLC	-	RC	FC	LFE	FR	FL
0	0	0	1	1	1	0	0	1C	FRC	FLC	RR	RL	-	-	FR	FL
0	0	0	1	1	1	0	1	1D	FRC	FLC	RR	RL	-	LFE	FR	FL
0	0	0	1	1	1	1	0	1E	FRC	FLC	RR	RL	FC	-	FR	FL
0	0	0	1	1	1	1	1	1F	FRC	FLC	RR	RL	FC	LFE	FR	FL
0	0	1	0	0	0	0	0	20	Reserved							
…																
1	1	1	1	1	1	1	1	FF								

Table 20 Audio InfoFrame Data Byte 4

The sink device's speaker allocation is not always the same as that contained within the source audio. In this case, the source device should down mix the audio in order to properly meet the sink device's speaker configuration. In actual implementations, all down-mix coefficients are equally attenuated to prevent calculation overflows. The total sound level becomes lower after down-mixing. For this reason, the Level Shift Value should also be transmitted to the sink device to insure the proper sound level is achieved.

Data Byte 5 contains Level Shift Information and a Down-mix Inhibit Flag.

The values of attenuation associated with the Level Shift Values (LSV0-LSV3) are shown in Table 21.

LSV3	LSV2	LSV1	LSV0	Level Shift Value
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
0	0	1	1	3dB
0	1	0	0	4dB
0	1	0	1	5dB
0	1	1	0	6dB
0	1	1	1	7dB
1	0	0	0	8dB
1	0	0	1	9dB
1	0	1	0	10dB
1	0	1	1	11dB
1	1	0	0	12dB
1	1	0	1	13dB
1	1	1	0	14dB
1	1	1	1	15dB

Table 21 Audio InfoFrame Data Byte 5, Level Shift Value

The Down-mix Inhibit Flag is shown in Table 22.

DM_INH	Describes whether the down mixed stereo output is permitted or not.
0	Permitted or no information about any assertion of this
1	Prohibited

Table 22 Audio InfoFrame Data Byte 5, Down-mix Inhibit Flag

6.7 MPEG Source InfoFrame

The MPEG Source InfoFrame describes aspects of the compressed video stream that were used to produce the uncompressed video. In many cases, the compressed source is MPEG2, although this InfoFrame can be applied to any similar compressed format. Some DTV Monitors use this information to improve the displayed picture.

> NOTE—Problems with the MPEG Source Infoframe have been identified that were not able to be fixed in time for CEA-861-D. Implementation is strongly discouraged until a future revision fixes the problems.

Transmission of this information by the source device is optional. Use of this information by the DTV Monitor is also optional. However, if the DTV Monitor has included Version 3 (or higher) of the CEA Extension in its EDID data structure, it shall be able to receive Version 1 of this InfoFrame.

If the source device supports the transmission of the MPEG Source InfoFrame and if it determines that the DTV Monitor is capable of receiving the MS InfoFrame (i.e., the DTV Monitor has included CEA Extension Version 3 in EDID), then this information should be sent once per video frame when applicable. The data applies to the next full frame of video data.

The format of the MPEG Source InfoFrame is shown in Table 23.

11dd00ddddd00ddd00d00d01d1d00d00d00d00d111
Gst}vklx$Fsrwyq ivxFipgvxsrngw$Ewwsgmexsr$
Tvszmihx$F}$WLW$yrhivxmgirwi${ mdGIE
Rs$vitvshygvxsr$sv$rix{ svoork$tivq mxihx${ mdsyxmgirwi$jvsq$WLW
Wsph$s=HMKMXEP^S R I$JS 2G$PXH 2G$[4868846
RsxjsvViwepi0544;3;36$9><$74$QX

InfoFrame Type Code	InfoFrame Type = **05** $_{16}$							
InfoFrame Version Number	Version = 01 $_{16}$							
Length of MPEG Source InfoFrame	Length of MPEG Source InfoFrame (10)							
Data Byte 1	MB#0 (MPEG Bit Rate: Hz Lower → Upper)							
Data Byte 2	MB#1							
Data Byte 3	MB#2							
Data Byte 4	MB#3 (Upper Byte)							
Data Byte 5	F57=0	F56=0	F55=0	FR0	F53=0	F52=0	MF1	MF0
Data Byte 6	F67=0	F66=0	F65=0	F64=0	F63=0	F62=0	F61=0	F60=0
Data Byte 7	F77=0	F76=0	F75=0	F74=0	F73=0	F72=0	F71=0	F70=0
Data Byte 8	F87=0	F86=0	F85=0	F84=0	F83=0	F82=0	F81=0	F80=0
Data Byte 9	F97=0	F96=0	F95=0	F94=0	F93=0	F92=0	F91=0	F90=0
Data Byte 10	F107=0	F106=0	F105=0	F104=0	F103=0	F102=0	F101=0	F100=0

Table 23 MPEG Source InfoFrame format

Data Bytes 1-4 give the MPEG bit rate. The MPEG Bit Rate is stored as a 32-bit number and is expressed in Hertz. MB#0 contains the least significant byte while MB#3 contains the most significant byte. If the MPEG Bit Rate is unknown or this field doesn't apply, then all of the bits in Data Bytes 1-4 shall be set to 0.

Example:
10 Mbps → 10,000,000 Hz (dec.) → 0x 00 98 96 80 (hex.) Upper … Lower Byte

Byte 1 MB#0 0x80 Lower Byte

Byte 2 MB#1 0x96

Byte 3 MB#2 0x98

Byte 4 MB#3 0x00 Upper

MF1 and MF0 in Data Byte 5 (see Table 24) designate whether the current field/frame was generated from an I, B, or P picture from the source MPEG stream. If this is unknown or doesn't apply, then the field shall be set to "unknown."

In some cases, the source device creates 60 field/second video from 24 frames/second source material. 3:2 pulldown is commonly used. FR0 can be used to designate whether a field is a repeated field or not. The DTV Monitor can use this information to improve the picture. If 3:2 pulldown does not apply to the current video decoding, then all of the fields/frames should be marked as "New field."

FR0	Field Repeat (for 3:2 pull-down)
0	New field (picture)
1	Repeated Field

MF1	MF0	MPEG Frame
0	0	Unknown (No Data)
0	1	I Picture
1	0	B Picture
1	1	P Picture

Table 24 MPEG Source InfoFrame Data Byte 5

7 EDID Data Structure

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into

account the format of the original video stream and the formats supported by the DTV Monitor. The source device (e.g., STB) is responsible for the format conversions necessary to supply video in an understandable form to the DTV Monitor.

The EDID content shall comply with EDID data structure version 1, revision 3 [9] or newer. This is known as Enhanced EDID (i.e., E-EDID). The DTV Monitor shall support E-DDC [8] as the method of transporting EDID information. A source device shall be capable of using Enhanced DDC to read the entire EDID since critical information may not otherwise be readable if the monitor contains a large EDID.[12] Upcoming VESA revisions are expected to change the EDID 1.3 block's version number, as well as the version number of the CEA Extension. Because the data structure of these blocks will remain backwards compatible, the source shall ignore these version numbers during the parsing of the EDID.

The DTV Monitor shall protect its EDID from accidental corruption resulting from I2C errors by write-protecting its contents.

See Annex A and Annex D for an example EDID.

7.1 Use of CEA Extensions

Two of the four 18-byte descriptor slots contained in EDID Block 0 are designated for a Monitor Range Limits Descriptor and a Monitor Name Descriptor. Users of CEA-861-D should note that future alternate usage of these descriptors is possible, including replacing them with additional Detailed Timing Descriptors, and, therefore, dependency upon data in these descriptors should be avoided. Consequently, the E-EDID standard provides a method for including only two Detailed Timing Descriptors. To accommodate additional Detailed Timing Descriptors, the CEA Extension has been defined. The tag (02_{16}) for this extension was previously reserved within VESA, but has now been assigned to CEA for the purposes of CEA-861-D. Therefore, further changes to this structure are under the control of CEA. It is referred to in CEA-861-D as the CEA Extension.

Three versions of the CEA Extension exist. If more than one CEA Extension is included in EDID, they shall all be the same version.

To maintain backward compatibility, newer versions of the CEA Extension include all of the fields that were present in the previous versions. Additionally, length fields are provided on internal data structures to let the source device know how big a block is so that it can skip over it if it doesn't understand it. Future versions of the CEA Extension are expected to have the version number incremented and be backward compatible with previous versions. A current generation source is capable of parsing these future EDIDs exactly as it does existing EDIDs, if it ignores version number. Sources shall ignore the version number during the parsing of the EDID structure.

CEA Extension Version 1 only provides a way to supply extra Detailed Timing Descriptors. It is still permitted to be used for some DTV Monitors (e.g. limited format DVI displays) but Version 3 is more applicable for most devices.

CEA Extension Version 2 is no longer supported and shall not be included in DTV Monitors.

CEA Extension Version 3 includes all of the fields and capabilities of Versions 1 & 2, but also includes the ability to specify any of the CEA video formats using "CEA Short Video Descriptors." It provides the ability for the DTV Monitor to specify what types of advanced audio it supports using "CEA Short Audio Descriptors." It also provides a way for the sink device to specify its speaker configuration. This information is complementary to the speaker channel allocation information that is sent in the Audio InfoFrame.

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[12] VESA has recently published a display information extension (DI-EXT) for EDID [45]. To be able to accommodate this extension and other extensions (such as the extension containing additional detailed timing descriptors), a DTV Monitor may need to use E-DDC to be able to include more than one extension. It is recommended that the source device be able to read any extension that may be included per the guidelines contained in Enhanced EDID [9].

If a DTV Monitor supports any video format with a format code greater than 7, YC_BC_R color space, InfoFrames, or digital audio (e.g., is an HDMI monitor), then it shall include the version 3 (or higher) CEA Extension in its EDID data structure.

7.2 Describing Video Formats in EDID

Two methods of describing video formats are used in CEA-861-D: Detailed Timing Descriptors and CEA Short Video Descriptors.

The DTV Monitor shall declare support for all of the DTV formats that it supports in EDID block 0 or in the CEA Extension(s). The 640x480@60Hz flag, in the Established Timings area, shall always be set, since the 640x480p format is a mandatory default timing.

When using CEA Extension Version 1, all of the CEA video formats listed in E-EDID are described using Detailed Timing Descriptors. No matter which CEA Extension is used, there is also room for two Detailed Timing Descriptors in EDID Block 0. CEA Extension Version 3 can include a combination of Detailed Timing Descriptors and Short Video Descriptors.

If a Version 3 CEA Extension has been included in EDID, all CEA video formats shall be advertised using Short Video Descriptors, even if they are also advertised using the Detailed Timing Descriptors (see 7.2.1).

Even though Short Video Descriptors are now available in the Version 3 CEA Extension, there is still a need to use Detailed Timing Descriptors if full backward compatibility with legacy sources is desired. Formats with video ID codes of 2 to 5 and 17 to 20 should be advertised using the Detailed Timing Descriptors for any video formats that the DTV designer wishes to guarantee are available to sources that do not understand the Short Video Descriptors and that require Detailed Timing Descriptors for proper operation. If sufficient room is not available in the first two blocks of the EDID for all of the supported video formats, the DTV designer may choose to declare support for some of the less important formats in Short Video Descriptors only.

7.2.1 Use of EDID Detailed Timing Descriptors

For the purposes of CEA-861-D, a DTV Monitor intended for 60 Hz countries shall support both the 60 Hz and 59.94 Hz version of any format it supports. The 60 Hz version shall be described in the EDID structure for HDTV formats, the 59.94Hz version shall be described for all 480-line formats.

All DTDs and SVDs shall be listed in order of priority; meaning that the first is the one that the display manufacturer has identified as optimal.

Note that the EDID Detailed Timing Descriptor allows for the designation of an interlaced format. However, there are no provisions to specify separate vertical blanking/sync for Field 1 and Field 2. Therefore, for the purposes of CEA-861-D, the following rules apply for interlaced formats:

a) The Field 1 Vertical Blanking Interval shall equal the Vertical Blanking Lines in the Detailed Timing Descriptor.
b) The Field 2 Vertical Blanking Interval shall equal the Vertical Blanking Lines in the Detailed Timing Descriptor + 1.
c) The Field 1 Vertical Sync Offset shall equal the Vertical Sync Offset in the Detailed Timing Descriptor.
d) The Field 2 Vertical Sync Offset shall equal the Vertical Sync Offset in the Detailed Timing Descriptor + 1/2.

Different Detailed Timing Descriptors are required for video formats with different picture aspect ratios. The vertical and horizontal image size parameters shall contain numbers that describe the aspect ratio of the displayed video (actual dimensions are preferred, but not required). Two cases are anticipated: either 4:3 or 16:9.

Examples of Detailed Timing Descriptors for the video formats are contained in Annex A.

7.2.2 Order of Dual-Aspect Ratio Detailed Timing Descriptors

Source devices that do not support the AVI InfoFrame (e.g., DVI sources) shall consider the first EDID descriptor of any dual-aspect ratio timing to be the display-assumed aspect ratio for that timing. DTV Monitors that support any dual-aspect ratio timing shall list the preferred aspect ratio before the other and shall assume that any signal matching that timing should be displayed at the preferred aspect ratio unless receiving an alternate indication in an AVI InfoFrame.

Source devices shall also handle transmission of a dual-aspect ratio timing to a DTV Monitor that does not support the reception of aspect ratio information (e.g., a DVI monitor). In that case, the DTV Monitor only supports one of these two formats. The supported format would be advertised in the EDID data structure.

7.2.3 Source Device Guidance

It is strongly recommended that a source device provide an option of operating in "pass-through" mode. When operating in "pass-through" mode, the source transmits the video to the DTV monitor without performing any deinterlacing or scaling on the transmitted content. A source operating in "pass through" mode determines the supported video formats of the DTV Monitor and utilizes this information to ensure that it passes through only video formats supported by the DTV Monitor. If no corresponding video format is supported by the DTV Monitor, then some conversion is necessary; it is recommended that the conversion be to the video format specified as the DTV Monitor's preferred timing mode. Examples of different conversions are illustrated in Annex F. Typically, PCs and game machines locally determine the resolution of the content rather than processing pre-recorded or broadcast content at a preset resolution. In these cases, it is recommended that the source generate the content at the DTV Monitor's preferred timing.

7.3 CEA Extension Version 1

The first version was created for CEA-861 and only provides a way to supply extra EDID Detailed Timing Descriptors.

The CEA Extension in Table 25 follows the format described in Section 2.2.1.3 of [9]. The EDID Extension Tag for this extension shall be 02h. VESA has given control of the definition of this extension to CEA for the purposes of CEA-861-D. The first detailed timing (DTD) listed in the base EDID data structure is preferred. The first short video descriptor (SVD), listed in the CEA extension, is also preferred.

Byte #	Value	Description	Format
0	02h	Tag (02h)	
1	01h	Revision Number	
2		Byte number offset ***d*** where 18-byte descriptors begin (typically Detailed Timing Descriptors)	***d*** = offset for the byte following the reserved data block. If no data is provided in the reserved data block, then ***d***=4. If no DTDs are provided, then ***d***=0.
3		Reserved	Set to 00h
4		Start reserved data block	This section was previously reserved for 8 byte timing descriptors but is currently a reserved data block.
d-1		End of reserved data block.	
d		Start of 18-byte descriptors	See Section 3.10.2 of [9]
d+(18*n)-1		End of 18-byte descriptors where ***n*** is the number of descriptors included	
d+(18*n)	00h	Beginning of Padding	
126	00h	End of Padding	
127		Checksum	xxh = This byte should be programmed such that a one-byte checksum (add all bytes together) of the entire 128 byte block equals “00h”.

Table 25 CEA Extension Version 1

7.4 CEA Extension Version 2

CEA Extension Version 2 is deprecated and shall not be included in DTV monitors. See Table 26.

Byte #	Value	Description	Format
0	02h	Tag (02h)	
1	02h	Revision Number	
2		Byte number offset ***d*** where 18-byte descriptors begin (typically Detailed Timing Descriptors)	***d*** = offset for the byte following the reserved data block. If no data is provided in the reserved data block, then ***d***=4. If ***d***=0, then no detailed timing descriptors are provided and no data is provided in the reserved data block.
3		Total number of native Detailed Timing Descriptors in entire E-EDID structure. Also, indication of underscan support, audio support, and support of YC_BC_R is included	bit 7 (underscan) = 1 if DTV Monitor underscans IT formats by default. bit 6 (audio) = 1 if DTV Monitor supports basic audio bit 5 (YC_BC_R 4:4:4) = 1 if DTV Monitor supports YC_BC_R 4:4:4 in addition to RGB bit 4 (YC_BC_R 4:2:2) = 1 if DTV Monitor supports YC_BC_R 4:2:2 in addition to RGB lower 4 bits = total number of native DTDs (see Section 2.2 for definition of "Native Format").
4		Start reserved data block	This section was previously reserved for 8 byte timing descriptors[13] but is currently a reserved data block.
d-1		End of reserved data block.	
d		Start of 18-byte descriptors	See Section 3.10.2 of [9]
d+(18****n***)-1		End of 18-byte descriptors where ***n*** is the number of descriptors included	
d+(18****n***)	00h	Beginning of Padding	
126	00h	End of Padding	
127		Checksum	xxh = This byte should be programmed such that a one-byte checksum (add all bytes together) of the entire 128 byte block equals “00h”.

Table 26 CEA Extension Version 2

7.5 CEA Extension Version 3

Version 3 includes all of the capabilities of Versions 1 & 2, but also includes the ability to specify any of the CEA formats using “CEA Short Video Descriptors.” It provides the ability for the DTV Monitor to specify what types of advanced audio it supports using “CEA Short Audio Descriptors.” It also provides a way for the sink device to specify its speaker configuration. This information is complementary to the speaker channel allocation information that is sent in the Audio InfoFrame.

If more than one CEA extension is needed, then the value of byte 3 shall be the same in all extensions.

CEA Extension Version 3 is shown in Table 27.

[13] The 8-byte descriptors do not support the DTV formats defined in this standard since they are not compliant with VESA GTF [47].

Byte #	Value	Description	Format
0	02h	Tag (02h)	
1	03h	Revision Number	
2		Byte number offset ***d*** where 18-byte descriptors begin (typically Detailed Timing Descriptors)	***d*** = offset for the byte following the reserved data block. If no data is provided in the reserved data block, then ***d***=4. If ***d***=0, then no detailed timing descriptors are provided and no data is provided in the reserved data block.
3		Total number of Detailed Timing Descriptors describing native formats in entire E-EDID structure. Also, indication of underscan support, audio support, and support of YC_BC_R is included	**bit 7** (underscan) = 1 if DTV monitor underscans IT video formats by default. **bit 6** (audio) = 1 if sink device supports basic audio **bit 5** (YC_BC_R 4:4:4) = 1 if sink device supports YC_BC_R 4:4:4 in addition to RGB **bit 4** (YC_BC_R 4:2:2) = 1 if sink device supports YC_BC_R 4:2:2 in addition to RGB **lower 4 bits** = total number of native DTDs (see Section 2.2 for definition of "Native Format")
4		Start of data block collection	This section was previously reserved for 8 byte timing descriptors[14] but is currently used for CEA Data Block Collection (see Table 28).
d-1		End of data block collection.	
d		Start of 18-byte detailed timing descriptors	See Section 3.10.2 of [9]
d+(18*__n__)-1		End of 18-byte detailed timing descriptors where ***n*** is the number of descriptors included	
d+(18*__n__)	00h	Beginning of Padding	
126	00h	End of Padding	
127		Checksum	xxh = This byte should be programmed such that a one-byte checksum (add all bytes together) of the entire 128 byte block equals “00h”.

Table 27 CEA Extension Version 3

The lower 4 bits of byte 3 indicates the total number of DTDs defining native formats in the whole EDID (see Section 2.2 for definition of "Native Format").The placement of native DTDs shall be contiguous, starting with the first DTD in the DTD list (which starts in the base EDID block). Value zero means that this information is not provided (for backward compatibility with prior implementations), or that the display does not support reception of native format.

In most cases, the native format count equals one, but a CRT-based display may indicate support for two: a native progressive and a native interlaced timing.

In order to ensure YC_BC_R interoperability between any two YC_BC_R-capable devices, a DTV monitor that supports either type of YC_BC_R pixel data (4:2:2 or 4:4:4) should support both types and therefore would set both bits 4 and 5 of byte 3.

[14] The 8-byte descriptors do not support the DTV formats defined in this standard since they are not compliant with VESA GTF [47].

NOTE—The HDMI specification requires this behavior.

A DTV monitor that does not support YC_BC_R pixel data shall have both bits 4 and 5 clear.

If the DTV Monitor supports any type of digital audio on this interface, then it shall also support Basic Audio and shall indicate this by setting the Basic Audio bit (bit 6).

Bit 7 of byte 3 shall be set if the DTV Monitor underscans IT formats by default.

The format of the “CEA Data Block Collection” shall conform to that shown in Table 28. The order of the Data Blocks is not constrained. It is also possible to have more than one of a specific type of data block if necessary to include all of the descriptors needed to describe the DTV Monitor’s capabilities.

The header of a Data Block consists of one byte (Table 29), with 3 bits used for the tag code to label the type of data and 5 bits used to indicate the length of the block. The list of tag codes is shown in Table 30. The length does not include the tag. The General Tag format is shown in Table 29. The first three bits are a Tag Code. This tag code designates the format of the bytes that follow. The last five bits are a length field that designates the number of bytes in the data block associated with the tag. The number of bytes does not include the tag. In the case of a video data block or an audio data block, the data block consists of a number of short descriptors. For other data blocks, the format may be different (e.g., Speaker Allocation Data Block). However, the length is always the number of bytes following the tag.

	Byte#	Bits 5-7	Bits 0-4
Video Data Block	1	Video Tag Code	length=total number of video bytes following this byte (L_1)
	2	CEA Short Video Descriptor 1	
	3	CEA Short Video Descriptor 2	
	...	...	
	$1+L_1$	CEA Short Video Descriptor L_1	
Audio Data Block	$2+L_1$	Audio Tag Code	length=total number of audio bytes following this byte (L_2)
	$3+L_1$	CEA Short Audio Descriptor 1	
	$4+L_1$		
	$5+L_1$		
	... ...		
	L_1+L_2	CEA Short Audio Descriptor L_2/3	
	$1+L_1+L_2$		
	$2+L_1+L_2$		
Speaker Allocation Data Block	$3+L_1+L_2$	Speaker Allocation Tag Code	length=total number of speaker allocation bytes following this byte (L_3=3)
	$4+L_1+L_2$	Speaker Allocation Data Block Payload (3 bytes)	
	$5+L_1+L_2$		
	$6+L_1+L_2$		
Vendor Specific Data Block	$7+L_1+L_2$	Vendor Specific Tag Code	length=total number of vendor specific bytes following this byte (L_4)
	$8+L_1+L_2$	24-bit IEEE Registration Identifier (least significant byte first)	
	$9+L_1+L_2$		
	$10+L_1+L_2$		
	....	Vendor Specific Data Block Payload (L_4-3 bytes)	

Table 28 General Format of "CEA Data Block Collection"

These data structures may grow in the future and so the source shall continue to parse the known (currently specified) fields in a data block even if the length is longer than currently specified.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	Tag Code			Length of following data block payload (in bytes)				

Table 29 Data Block Header Byte

Codes	Type of Data Block
0	Reserved
1	Audio Data Block (includes one or more Short Audio Descriptors)
2	Video Data Block (includes one or more Short Video Descriptors)
3	Vendor Specific Data Block
4	Speaker Allocation Data Block
5	VESA DTC Data Block
6	Reserved
7	Use Extended Tag

Table 30 CEA Data Block Tag Codes

If the Tag Code is 7 (Use Extended Tag) then the second byte of the data block contains the Extended Tag Code, which indicates the actual type of the data block. For backwards compatibility, the Length field in the first byte does include the second byte, which contains the Extended Tag Code. Note that data blocks with Tag Codes of 1 through 6 are limited to containing 31 useful bytes whereas those with Extended Tag Codes are limited to 30 useful bytes.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
2	Extended Tag Code							

Table 31 Extended Tag Format (2nd Byte of Data Block)

Extended Tag Codes	Type of Data Block
0	Video Capability Data Block
1	Vendor-Specific Video Data Block
2	Reserved for VESA Video Display Device Information Data Block
3	Reserved for VESA Video Data Block
4	Reserved for HDMI Video Data Block
5	Colorimetry Data Block
6…15	Reserved for video-related blocks
16	CEA Miscellaneous Audio Fields
17	Vendor-Specific Audio Data Block
18	Reserved for HDMI Audio Data Block
19…31	Reserved for audio-related blocks
32…255	Reserved for general

Table 32 CEA Data Block Tag Codes

Any data block with an Extended Tag in the 0 to 15 range indicates strictly video-related characteristics of the display. Any repeater device that re-transmits a video stream from a source to a DTV monitor without any modification of the video timing or video data or video-related InfoFrame(s) shall also pass every such data block upstream, that is, the repeater shall copy the contents of the data block(s) from the downstream DTV Monitor's EDID to the repeater's own upstream EDID.

Any data block with an Extended Tag in the 16 to 31 range indicates strictly audio-related characteristics of the display. Any repeater device that re-transmits an audio stream from a source to a DTV monitor without any modification of the audio timing or audio data or audio-related InfoFrame(s) shall also pass every such data block upstream, that is, the repeater shall copy the contents of the data block(s) from the downstream DTV Monitor's EDID to the repeater's own upstream EDID.

Repeaters shall not copy the contents of any other data block from a downstream EDID to their own upstream EDID unless the characteristics of the DTV Monitor indicated by that data block are known to be also true for the repeater device or the combination of the repeater and downstream device. This also applies to the original Vendor-Specific Data Block (Data Block Tag = 3); if the repeater does not recognize the vendor ID or does not understand the entire contents of that block, it shall not be copied into the repeater's EDID.

7.5.1 Video Data Block

When a Version 3 CEA Extension is provided in the DTV Monitor's EDID data structure, a short video descriptor shall be provided for each CEA video format supported by the DTV Monitor. The format of the short video descriptor shall conform to that shown in Table 33. The lower 7-bits are an index associated with the video format supported. These indexes are the same as those used in the AVI InfoFrame and are shown in Table 3. All DTDs and SVDs shall be listed in order of priority; meaning that the first is the one that the display manufacturer has identified as optimal. The most significant bit declares whether the format is a native format of the display (native =1, not native = 0). Typically, there is a single SVD, with its native bit set. Sources should not necessarily convert video formats to a native format, but should follow recommendations for using pass-through and preferred timing (see Section 7.2.3).

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	Native	Video Identification Code						

Table 33 Short Video Descriptor

7.5.2 Audio Data Block

If audio is supported in the DTV Monitor, as indicated by the basic audio support bit in the Version 3 CEA EDID Descriptor, then CEA short audio descriptors shall be used to declare which (if any) audio formats are supported in addition to basic audio. If only basic audio is supported, no Short Audio Descriptors are necessary.

The Short Audio Descriptor shall conform to the formats given in Table 34, Table 35 and Table 36. Several types of audio may be supported, but each one shall be listed in its own short audio descriptor with its designated code and the associated information. The list of audio coding types is given in Table 37.

Each Short Audio Descriptor is 3-bytes long. There can be up to 31 bytes following any tag, therefore there may be up to 10 Short Audio Descriptors in the Audio Data Block.

The format of the third byte is determined by the audio format code contained in the first byte as shown in Table 34, Table 35 and Table 36. One format code is used for uncompressed audio (i.e., Linear PCM), the others are used for compressed audio (e.g., AC-3, MPEG2, DTS, etc.). For some compressed formats, byte 3 is further defined in other format-specific documents. For an Audio Format Code of 11 (DTS-HD), refer to the DTS-HD Product Certification Manual for additional support requirements and for rules regarding use of all fields in the DTS-HD Short Audio Descriptor. The CEA Short Audio Descriptors are shown in Table 34, Table 35, and Table 36.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	F17=0	Audio Format Code = 0001				Max Number of channels - 1		
2	F27=0	192 kHz	176.4 kHz	96 kHz	88.2 kHz	48 kHz	44.1 kHz	32 kHz
3	F37=0	F36=0	F35=0	F34=0	F33=0	24 bit	20 bit	16 bit

Table 34 CEA Short Audio Descriptor for Audio Code = 1 (LPCM)

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	F17=0	Audio Format Code				Max Number of channels - 1		
2	F27=0	192 kHz	176.4 kHz	96 kHz	88.2 kHz	48 kHz	44.1 kHz	32 kHz
3	Maximum bit rate divided by 8 kHz							

Table 35 CEA Short Audio Descriptor for Audio Codes 2 to 8

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	F17=0	Audio Format Code				Max Number of channels - 1		
2	F27=0	192 kHz	176.4 kHz	96 kHz	88.2 kHz	48 kHz	44.1 kHz	32 kHz
3	[Default = 0, unless Defined by Audio Codec Vendor]							

Table 36 CEA Short Audio Descriptor for Audio Codes 9 to 15

The Audio Format Codes used in each Short Audio Descriptor are shown in Table 37. These values are the same as the values used in the Audio InfoFrame, which are shown in Table 17.

Codes	Audio Format Description
0	Reserved
1	Linear PCM (e.g., IEC 60958)
2	AC-3
3	MPEG1 (Layers 1 & 2)
4	MP3 (MPEG1 Layer 3)
5	MPEG2 (multichannel)
6	AAC
7	DTS
8	ATRAC
9	One Bit Audio
10	Dolby Digital +
11	DTS-HD
12	MAT (MLP)
13	DST
14	WMA Pro
15	Reserved for audio format 15

Table 37 Audio Format Codes

Some information on typical audio applications is contained in Annex J (Informative).

7.5.3 Speaker Allocation Data Block

If the DTV Monitor supports multi-channel uncompressed digital audio as indicated in the Audio Data Block, then the Speaker Allocation Data Block shall be included in the CEA Extension. It is recommended that the DTV Monitor include a valid Speaker Allocation Data Block if it supports any type of digital audio (including Basic Audio), but this is not required.

The payload of the Speaker Allocation Data Block is shown in Table 38. This payload is preceded by a Tag Code Byte that includes a tag equal to 4 and a length of 3 (see Table 28 and Table 30). The first byte of the Data block payload consists of seven bits and one reserved bit. The DTV Monitor signifies that a speaker, or pair of speakers, is present by setting the bit associated with that speaker or pair of speakers to one. The speaker designations are the same as is used in the Audio InfoFrame (see Figure 38 and Table 19). The Front Left and Front Right channels are not independent and are shown as FL/FR in the table. The Front Left Center and Front Right Center (FLC/FRC) Rear Left and Rear Right (RL/RR), and Rear Left Center and Rear Right Center (RLC/RRC) channels are also not independent.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	F17=0	RLC/RRC	FLC/FRC	RC	RL/RR	FC	LFE	FL/FR
2	F27=0	F26=0	F25=0	F24=0	F23=0	F22=0	F21=0	F20=0
3	F37=0	F36=0	F35=0	F34=0	F33=0	F32=0	F31=0	F30=0

Table 38 Speaker Allocation Data Block Payload

7.5.4 Vendor Specific Data Block

The content of the Vendor Specific Data Block is defined in Table 28.

A DTV Monitor may contain one or more Vendor-Specific Data Blocks (VSDB) to indicate proprietary information that may be of interest to the vendor's own source devices.

The VSDB shall contain the 3 bytes of the IEEE OUI as well as any additional payload bytes needed.

> NOTE—HDMI sinks use one version of the VSDB to indicate HDMI-specific characteristics of the DTV Monitor. Additional VSDBs, such as those with the vendor's own IEEE OUI, may also be included in the E-EDID.

7.5.5 Colorimetry Data Block

The Colorimetry Data Block indicates support of specific extended colorimetry standards and gamut-related as yet, undefined metadata. Details regarding the contents of the Colorimetry Data Block are provided in Table 39, Table 40 and Table 41.

Byte 3 is allocated for Colorimetry data and the flags for bit0 and bit1 are defined for colorimetry based upon IEC 61966-2-4. xvYCC601 indicates support for IEC 61966-2-4 with standard definition primaries and xvYCC709 indicates support for IEC 61966-2-4 with high definition primaries. Byte 4, bits 0 through 2 are designated for future gamut-related metadata. As yet undefined, this metadata is carried in an interface-specific way.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	Tag Code (07h)			Length of following data block (in bytes) (03h)				
2	Extended Tag Code (05h)							
3	F37=0	F36=0	F35=0	F34=0	F33=0	F32=0	$xvYCC_{709}$	$xvYCC_{601}$
4	F47=0	F46=0	F45=0	F44=0	F43=0	MD2	MD1	MD0

Table 39 Colorimetry Data Block

Flag	Colorimetry
$xvYCC_{601}$	Standard Definition Colorimetry based on IEC 61966-2-4
$xvYCC_{709}$	High Definition Colorimetry based on IEC 61966-2-4

Table 40 Data Byte 3 Colorimetry Support Flags

Flag	Metadata
MD0	Future metadata profile
MD1	Future metadata profile
MD2	Future metadata profile

Table 41 Data Byte 4 Colorimetry Metadata Support Flags

7.5.6 Video Capability Data Block

The Video Capability Data Block (VCDB) allows a display to declare its overscan/underscan behavior and support for source override of the default quantization level (see Table 42). Separate overscan/underscan options may be declared for Preferred, IT, and CE video format categories.

NOTE—The VCDB payload currently only contains a single byte in addition to the Extended Tag Code, while future versions may contain additional bytes. The source should ignore such additional bytes (when present) and continue to parse the single byte as defined in Table 42 and Table 43.

	bits							
Byte#	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	Tag Code (07h)			Length of following data block (in bytes) (02h)				
2	Extended Tag Code (00h)							
3	F37=0	**QS**	**S_PT1**	**S_PT0**	**S_IT1**	**S_IT0**	S_CE1	S_CE0

Table 42 Video Capability Data Block (VCDB)

F37	Future Use, all Zeros	QS	Quantization Range Selectable (Applies to RGB only)	S_PT1	S_PT0	PT Overscan/ underscan behavior (Applies to the preferred video format)	S_IT1	S_IT0	IT Overscan/ underscan behavior (Applies to IT video formats)	S_CE1	S_CE0	CE Overscan/ underscan behavior (Applies to CE video formats)
0		0	No Data	0	0	No Data (refer to **S_CE** or **S_IT** fields)	0	0	IT video formats not supported	0	0	CE video formats not supported
		1	Selectable (via AVI Q)	0	1	Always Overscanned	0	1	Always Overscanned	0	1	Always Overscanned
				1	0	Always Underscanned	1	0	Always Underscanned	1	0	Always Underscanned
				1	1	Supports both over- and underscan	1	1	Supports both over- and underscan	1	1	Supports both over- and underscan

Table 43 Video Capability Descriptor Data Byte 3

Displays do not always present the entire incoming picture to the viewer. Sometimes displays overscan the incoming video format such that pixels along the periphery of the picture are masked (occluded). For example, a display may purposely mask a portion of the picture to hide distracting content (received from a source) or the unsightly edges of a raster. In either case, what the viewer sees is either an underscanned or overscanned picture, which may either include (in the case of underscanning) the whole incoming picture or (in the case of overscanning) a somewhat occluded picture.

CE application specific displays (e.g. DTVs) typically overscan all video formats, while IT application specific displays (e.g. computer displays) typically underscan all video formats. Multipurpose displays

typically adapt to the incoming signal by either overscanning or underscanning depending on the type of video format received. The **S_CE**, **S_IT** and **S_PT** values allow a display to formally declare its overscan/underscan options by CE, IT, and Preferred video format category (see Table 43).

Each of the three **S_xx** fields indicate whether the display will, for all video formats in that category, always overscan those formats, always underscan those formats or support both overscanning and underscanning of those formats. Indications shall be accurate for all video format categories – so long as a VCDB is present in the EDID. If the display does not support the reception of one of the two main video format categories (CE and IT), then the indication for the unsupported category shall be set to 00.

The display's Preferred Timing Format may be either a CE or an IT format but may have different overscan/underscan behavior than the rest of the CE or IT formats supported by the display. If the display declares a non-zero value for the **S_PT** (preferred timing overscan/underscan behavior) field, and the source outputs that video format, then the **S_PT** declaration shall take precedence over both **S_CE** and **S_IT** declarations. If the **S_PT** field is 0 then the overscan/underscan behavior of this format is indicated by either the **S_CE** or **S_IT** fields, depending on whether the Preferred Timing Format is a CE or IT format.

If the display declares that it can support both overscan and underscan for a video format category and the source outputs that type, then the display shall either automatically overscan or underscan (in response to the AVI InfoFrame S field) or provide user options of selecting an overscan or an underscan mode. If operating in an automatic mode, the display shall overscan the incoming picture if it receives AVI S=1 and it shall underscan if it receives AVI S=2. The source shall always set the AVI S field correctly if that information is known by the source. If the display receives no AVI or AVI S=0, then the display should overscan CE video formats and underscan IT video formats by default but may provide a user-selectable alternative behavior.

If the display does not provide a VCDB then the source should assume that CE formats are overscanned by the display and that IT format behavior is indicated by CEA Extension byte 3 bit 7 (underscan). If underscan=1 then the source should assume that IT video formats are underscanned and if underscan=0, that IT video formats are overscanned.

If the source outputs a video format that can be underscanned by the display, then the source may safely place essential content at the very edge of the signaled picture and the display shall ensure that the entire signaled picture is visible.

When outputting a video format that is always overscanned by the display, IT sources (which normally render interactive menus and window controls along the periphery of the transmitted picture) should confine essential content to a smaller area of the signaled picture - to ensure the viewer operability. Media-centric sources, on the other hand, which fill the signaled picture with (decompressed) broadcast or prerecorded content - precomposed for an overscanned display, should simply pass-through such content without further processing.

The exact dimensions of the overscanned picture may vary and are not specified in CEA-861-D.

CEA-861-D supports both limited (16 to 235) and full (0 to 255) quantization ranges when receiving video with RGB color space. By default, RGB pixel data values should be assumed to have a limited range when receiving a CE video format (see Sections 5.1 and 5.2), and a full range when receiving an IT format (see Section 5.4). The QS (Q support) bit of byte 3 allows a display to declare that it supports the reception of either type of quantization range for any video format, under the direction of AVI InfoFrame Q data (see Section 6.4 for information concerning bits Q1 and Q0). This allows a source to override the default quantization range for any video format.

If the sink declares Quantization Range is "Selectable" (QS=1), then it shall expect limited range pixel values if it receives AVI Q=1 and it shall expect full range pixel values if it receives AVI Q=2 (see section

6.4). For other values of Q, the sink shall expect pixel values with the default range for the transmitted video format.

Annex A Example EDID and Detailed Timing Descriptors

Annex A addresses issues related to the VESA Extended Display Identification Data (EDID) tables utilized within CEA-861-D. In Annex A, the letter 'h' after numbers or A through F designates the preceding values are in hexidecimal notation.

Annex A provides examples and guidance to manufacturers that utilize CEA-861-D; however included in this Annex are several normative requirements identified by the "shall" verb. Specifically, this guidance is for the implementation of EDID tables. Primarily, the motivation is to help insure interoperability between various source and sink devices. Annex A should in no way prohibit consumer device manufacturers from including additional features, and Annex A should not be interpreted as stipulating any form of upper limit to EDID features.

A.1 Background

CEA-861-D follows requirements in the VESA Enhanced Extended Display Identification Data Standard (E-EDID). EDID tables exist within the sink device and are used to declare its capabilities to source devices. The source device uses these declared capabilities to determine the appropriate signal parameters to send across the interface for consumption by the sink device.

Possibly, there are varied and inconsistent ways to create EDID tables and therefore, a common methodology is desirable to help insure interoperability between various sink and source devices. The purpose of Annex A is to provide a consistent and understandable guideline for creating EDID tables that reside within consumer electronics products. Consequently, Annex A does not address implementations that utilize repeaters.

A.2 EDID Tables

CEA-861-D requires use of the VESA EDID version 1.3 data structure, or newer. Previous versions of EDID are not supported and such use is deprecated. EDID 1.3 requires use of certain features for Computer Displays. Despite these requirements, some features are not applicable to certain display technologies and applications. For example, the Monitor Range Limits descriptor and support of the Generalized Timing Formula apply to CRT based multi-scan systems and not flat panel or most consumer electronics equipment. For consumer electronics devices (CE devices) the application is limited to a simple declaration of the sink device’s capabilities and attributes. This section provides an outline describing the various blocks that reside with the EDID structure.

A.2.1 EDID Table Construction

The table construction is divided into blocks dedicated to specifying various attributes. Each block is 128 bytes in length. Block 0 is mandatory and the following blocks are called “extensions”. The extensions are limited to 254 blocks.

It is possible to use the first extension as a data block or as an index (EDID Block Map Extension) that lists more than one extension. When only one extension is required, it is called Block 1 and is used for data. In cases where more than one extension is required, the first extension or Block 1 is used as an index map that lists extension locations. Additional extensions are referred to as Blocks, such as Block 2, Block 3, and so on.

Each extension contains a Block Tag that declares the contents of each extension. Source devices should read Block 0 (at address 7Eh), check for multiple extensions, identify each block or extension and be able to appropriately interpret the data contained therein. Users should be knowledgeable of defined Tags contained within section 2.2.1.4 of the VESA E-EDID standard.

Source devices should read all extensions and Block Tags. CEA Extension Version 1 or Version 3 specifies additional video formats as necessary. There are three possible versions of the CEA Extension and source devices should read the contents of the extension even if they cannot recognize the version number. This is to insure that the Detailed Timing Descriptors are read.

For CE devices, the number of extensions or blocks is dependent upon the amount of supported video formats and features. Annex A shows one extension containing four Detailed Timing Descriptors (see Section A.3).

A.2.2 Detailed Explanation of EDID Block Zero

For this discussion, block zero and subsequent extension blocks are divided into smaller sections, each receiving an explanation of terminology and use. The contents in each section are a possible example of a typical CE device application.

A data format protocol is required to properly utilize the various blocks. Data within the various blocks is placed in fields with varying bit lengths. These lengths range from one bit to two bytes. The data length convention is defined and shown in Table 44 .

Bit range	Convention
1 ~ 7 bits	Binary, consecutive sequence
8 bits (byte)	Binary, according to location
9 ~ 15 bits	Binary, sequence according to field
16 bits (two bytes)	Binary, LSB first
Greater than two bytes: (Character string)	ASCII code, consecutive string order, ex: HDTV = 0x48, 0x44, 0x54, 0x56

Table 44 Standard Data Lengths

A.2.3 Block Zero Header Section

The header is comprised of eight addresses, 00h through 07h, containing a simple binary data pattern that is used to identify the EDID table. There is one byte per address for a total of eight bytes. Address locations 00h and 07h contain data values 00h and locations 01h through 06h contain FFh as data values. CEA-861-D requires this data. This header is used to determine the beginning of an EDID structure in a sink device. See Table 45.

Address Hex	Example Data Hex	Dec	Format	Remarks
00	00	0	Binary	These fixed values are **REQUIRED** to properly identify start of EDID table data
01	FF	255		
02	FF	255		
03	FF	255		
04	FF	255		
05	FF	255		
06	FF	255		
07	00	0		

Table 45 Block Zero Header

Although future versions of EDID may not contain an 8-byte header at the beginning of Block 0, compliant devices are expected to use this header. However, presence of the header is not an indication that the following EDID data is valid. A checksum byte is provided for the purpose of verifying that a device's EDID structure has been correctly read. See Section A.2.11 for more detail.

A.2.4 Vendor / Product Identification

This section's example starts and ends with address locations 08h and 11h. Byte allocation for each location is as follows:

08h ~ 09h are a two byte EISA ID for Manufacturer Name and should contain a valid identification number. Data for these bytes is based upon compressed ASCII, for example: "CEA" is created by using five-bit codes, where "C" = 00011. "E" = 00101, and "A" = 00001. Table 3 illustrates the address location and sample data for Manufacturer's Name, which is "CEA".

For information on how to obtain an EISA ID, contact:

Microsoft
URL: http://www.microsoft.com/whdc/system/pnppwr/pnp/pnpid.mspx
E-mail: pnpid@microsoft.com

0Ah ~ 0Bh are two bytes available for Product code; the manufacturer determines this code.

0Ch ~ 0Fh are four bytes to be used for product Serial Number, which is defined as a 32-bit serial number. There is no specific requirement defined for the data or format of the serial number. This field should be zero if the serial number is contained in an ASCII serial number descriptor (see Section A.2.17). CEA-861-D implementations should use 00h as padding for the Block 0 serial number if no serial number is provided in Block 0.

For the source box, if an ASCII Serial Number Descriptor is included in the sink device, then the source box should ignore the Serial Number field in Block 0. If no ASCII Serial Number Descriptor is present, then the field may have meaning. Ignore this block if all bytes are 00h.

10h is one byte for Week of Manufacture. The designated values for this field range from 1 to 53. Values greater than 53 are not recognized. Zero may be used when no week is designated. The manufacturer determines the week numbering system. Manufacturers should use a system in which the week number's integer value increases as the year progresses. If a manufacturer chooses to declare Model Year only (in the field "Year of Manufacture"), then FFh shall be placed in Address 10 (Week of Manufacture).

11h is one byte representing Year of Manufacture. This value is determined by the actual year of production minus 1990. For example: 2002 – 1990 = 12 or 0Ch. See Table 46.

Address	**Example Data**		**Description**	**Remarks**
Hex	**Hex**	**Dec**		
08	0C	12	Manufacturer Name using EISA ID	Example = CEA
09	A1	161		
0A	00	0	Product Code	Used to differentiate between different models from the same manufacturer.
0B	00	0		
0C	00	0	Serial Number	Optional. The serial number can also be stored in a separate descriptor block (see Section A.2.17).
0D	00	0		
0E	00	0		
0F	00	0		
10	00	0	Week of Manufacture	If this field is unused, the value should be set to 0. If the next field is used for Model Year, then FFH should be set.
11	0C	12	Year of Manufacture/Model Year	Example = 2002

Table 46 Vendor / Product Identification

A.2.5 EDID Version

The version of EDID is declared in addresses 12h and 13h. Each address contains one byte of data. The first address contains the version number and the second, the revision number. In the case of EDID version 1.3, the value one (01h) is placed in the first location (i.e., 12h) and three (03h) placed in the

second area (13h). No other numbers are allowed for this space. If other numbers are placed in this area, the source device may disregard the whole EDID table. See Table 47.

Address Hex	Example Data Hex	Dec	Format	Remarks
12	01	1	Binary	Version #
13	03	3		Revision #

Table 47 Vendor / Product Identification

A.2.6 Basic Display Parameters and Features

Basic Display Parameters and Features are defined as Video Input Definition, Maximum Horizontal Image Size, Maximum Vertical Image Size, Display Transfer Characteristic (Gamma), and Feature Support. In the following example, each item is allocated one byte and the address range is from 14h to 18h.

14h: Video Input Definition is located at 14h and used to identify the output configuration required by the sink device. For digital displays, including CE devices, the recommended setting is 80h. This value is used to declare that the device supports a digital interface.

15h ~16h: The Maximum Horizontal Image Size and Vertical Image Size fields (bytes 15h, 16h) are used to indicate the sink device's screen size and aspect ratio. When known, the maximum physical dimensions of the effective display area should be provided (in these fields, in cm). An important use of these fields is to indicate the aspect ratio of the actual screen. If the aspect ratio of the maximum image size is known, the ratio of the Maximum Size fields should equal that aspect ratio, even if the maximum image size is unknown or variable across different device configurations (such as in a projection system).

The following rules should be used in filling out the Maximum Image Size fields:

a) If the aspect ratio is known and the display size is known, then the actual size should be indicated, to the nearest cm.
b) If the aspect ratio is known but the size is unknown, any values corresponding to a typical or expected configuration of the display can be used, but the ratio of the Max Horizontal and Vertical fields shall be equal to the aspect ratio.
c) If the aspect ratio is unknown, or it is desired that it not be discoverable, then values of 0, 0 should be used.

If the fields are set to zero, the source should not make any assumptions regarding screen size or aspect ratio.

In typical configurations, the image sizes described in each DTD (in bytes at offsets 0Ch, 0Dh, 0Eh, in mm) should correlate to the values in the Maximum Size fields. For instance, a 160 cm by 90 cm display would indicate 1600 mm x 900 mm for all 16:9 video formats and 1200 mm x 900 mm for all 4:3 formats.

For example, data entry into the 15h, 16h EDID bytes may be as summarized in Table 48.

Category of Display	EDID Physical Horizontal Screen Size (cm)	EDID Physical Vertical Screen Size (cm)	Physical AR to be calculated by the source (unitless)
Direct View	Enter dimension in cm	Enter dimension in cm	Source Divides H by V
Rear Projector	Enter dimension in cm	Enter dimension in cm	Source Divides H by V
Front Projector (enter either data row at option of implementer)	Typical dimension in cm	Typical dimension in cm	Source Divides H by V
	Enter 00h	Enter 00h	AR is undefined

Table 48 Example 15h, 16h EDID Screen Size Data and Certain Display Categories

17h: Display Transfer Characteristics (Gamma) could be used by the source device to tailor the video output according the display device's gamma. The concept of declaring gamma has to do with personal computer CRT displays that accept non-gamma corrected signals. Digital and analog television video signals are gamma corrected according to established industry practices and thus the need to declare CRT gamma is not always necessary. However, this is needed for Personal Computer CRT applications. Although the source device possibly may not need to use the display's gamma value, the correct gamma value of the display device should be present. Since some television CRTs commonly have similar gamma, the value 2.2 is used in this example. The gamma value, itself, is not inserted into the table. Instead, a value equal to (gamma x 100) – 100 is inserted.

18h: Feature Support consists of 8 bits that identify various display or sink device parameters. These include power savings modes based upon VESA Display Power Management Signaling Standard (DPMS), Display Type, Standard Default Color Space, Preferred Timing Mode, and Default Generalized Timing Formula (GTF). In most cases, none of this information is relevant to CE devices and personal computer displays, since GTF is not commonly used. In Table 49, the function of each bit is indicated.

Bits	Feature	Description
7	Standby	1 = Standby supported, 0 = not supported
6	Suspend	1 = Suspend supported, 0 = not supported
5	Active Off	1 = Active Off supported, 0 = not supported
4 ~ 3	Display Type (4:3)	Bit 4 Bit 3 1 1 Undefined 1 0 Non-RGB Display 0 1 RGB Display 0 0 Monochrome Display
2	Color Space	1 = sRGB supported, 0 = not supported
1	Preferred Timing	1 = preferred timing is indicated in first detailed timing block (required), 0 = not indicated (not allowed)
0	Default GTF	1 = GTF supported, 0 = not supported

Table 49 Feature Support Detail

The minimum that a CE device should declare is Display Type and Preferred Timing. In this example, 0Ah is used to designate a RGB display type and a preferred timing descriptor. The preferred timing descriptor bit shall be set to one and address locations 36h through 47h shall contain the Preferred Format. No other data is allowed in those locations. All DTDs and SVDs shall be listed in order of priority; meaning

that the first is the one that the display manufacturer has identified as optimal; however, in the context of total system optimization, source implementers are advised to follow guidance provided in Section 7.2.3.

Address Hex	Example Data Hex	Dec	Description	Remarks
14	80	128	Video Input Definition	Example indicates: Digital; VESA DFP1X: not compatible
15	50	80	Max. Horizontal Image Size in cm	CRT devices should list parameters. However, due to projector and auto sizing devices, the system should not make any assumption regarding display size if data not supplied. This example indicates a 16:9 aspect ratio device.
16	2D	45	Max. Vertical Image Size in cm	Optional; See above; This example indicates a 16:9 aspect ratio device.
17	78	120	Gamma: (gamma x 100)-100 = value	Example is: (for gamma = 2.2) (2.2 x 100)-100 = 120
18	0A	10	Feature Support	Example indicates: RGB color Display type; Preferred timing: first detailed timing block; GTF timing: not supported; Standby mode: not supported; Suspend mode: not supported; Active off: not supported

Table 50 Basic Display Parameters and Features Block

A.2.7 Color Characteristics

Color Characteristics provides information about the display device's chromaticity and color temperature parameters (white temperature in degrees Kelvin).

Table 52 shows EDID addresses 19h through 22h, which contain data used to describe various chromaticity characteristics; this example uses 9300° K as the white color temperature. These characteristics are represented by 10-bit binary fractions. Bits nine through two of a particular characteristic are stored as a single byte in addresses 1Bh ~ 22h. Bits one to zero of that corresponding characteristic are paired with the lower order bits of other color characteristics to form bytes and are stored in addresses 19h ~ 1Ah. Table 52 shows the arrangement of these fractional binary values by EDID address. In the E-EDID standard, a decimal fraction such as 0.625 is represented by a 10-bit binary value. Each of the bit positions from left to right in the binary value represent powers of 2 from 2^{-1} ~ 2^{-10}. Table 51 illustrates an example decimal to binary conversion used for these color characteristics. Further explanation can be found in VESA E-EDID [9] Section 3.7.

Value	10-bit Binary	Conversion
0.625	1010000000	0.625
0.340	0101011100	0.33984375
0.155	0010011111	0.1552734375

Table 51 Binary to Decimal Conversion Example

How the table is filled is dependent upon the setting of address 18h in the Feature Support section. If sRGB is selected, then all values should be set in accordance to sRGB definition. For displays not supporting the sRGB definition, the example in Table 52 is applicable.

Address Hex	Example Data Hex	Dec	Description	Remarks
19	0D	13	Red/Green Low Bits	Bits 1~0 of RxRyGxGy = 00001101
1A	C9	201	Blue/White Low Bits	Bits 1~0 of BxByWxWy = 11001001
1B	A0	160	Red-x	Bits 9~2 of 10-bit value 0.625 = 10100000
1C	57	87	Red-y	Bits 9~2 of 10-bit value 0.340 = 01010111
1D	47	71	Green-x	Bits 9~2 of 10-bit value 0.280 = 01000111
1E	98	152	Green-y	Bits 9~2 of 10-bit value 0.595 = 10011000
1F	27	39	Blue-x	Bits 9~2 of 10-bit value 0.155 = 00100111
20	12	18	Blue-y	Bits 9~2 of 10-bit value 0.070 = 00010010
21	48	72	White-x	Bits 9~2 of 10-bit value 0.283 = 01001000
22	4C	76	White-y	Bits 9~2 of 10-bit value 0.298 = 01001100
Note—This data based on a CRT Display with a white point of ~9300^{o} K (X = 0.283; Y = 0.298)				

Table 52 Color Characteristics Block

Multiple white points can be specified using the Color Point Monitor Descriptor. However, there is no way to correlate to the individual video formats. Therefore chromaticity specified in Block 0 should be associated with the display device's characteristics; however the White Point data does not. The source device should not rely on the colorimetry information contained in this part of the EDID data structure for CEA-861-D formats. This recommended practice suggests the source device use the colorimetry that has been associated with the format in CEA-861-D when possible. Note that this may not be possible because the source device probably just passes on the video stream.

A.2.8 Established Timings

In the example in Table 53, addresses 23h through 25h are used to declare Established Timings. Established Timings are computer display timings recognized by VESA. This table is also used to indicate that the established timings were adjusted and verified at the factory, which means these timings are supported and correctly rendered on the display.

In the example, Table 53, address 23h contains the default 640x480p timing and the remaining addresses are not used to list any other timings. Personal Computers, DVI-1.0, Open LDI, CEA-861-D require 640x480p as a default timing format. This is to insure that all source and sink devices commonly support one format. Other supported or preferred timings may be described in the Standard Timing (see A.2.9) or Detailed Timing Descriptors (see A.2.10). Use of other timings is permissible. See VESA E-EDID Standard section 3.8.1 for a list of possible formats.

Address Hex	Example Data Hex	Dec	Description	Remarks
23	20	32	Established Timing 1	640x480 @ 60Hz
24	00	0	Established Timing 2	None
25	00	0	Manufacturer's Timing	None

Table 53 Established Timings Block

A.2.9 Standard Timing ID #1 – 8

Standard timings are those either recognized by VESA through the VESA Discrete Monitor Timing or Generalized Timing Formula standards. The display device should list timings supported. The address range for this portion of the example EDID table is 26h through 35h and the data length is two bytes.

Since CE devices possibly may not support, other than the required 640x480p format, any of the VESA timings or GTF, the example in Table 54 does not contain any timing information. When no timings are declared, it is necessary to fill each unused byte, of the byte pairs, with 01h as padding. Other padding values are not recognized.

Address Hex	Example Data Hex	Dec	Description	Remarks
26	01	1	Standard Timing ID #1	PC Application
27	01	1		
28	01	1	Standard Timing ID #2	PC Application
29	01	1		
2A	01	1	Standard Timing ID #3	PC Application
2B	01	1		
2C	01	1	Standard Timing ID #4	PC Application
2D	01	1		
2E	01	1	Standard Timing ID #5	PC Application
2F	01	1		
30	01	1	Standard Timing ID #6	PC Application
31	01	1		
32	01	1	Standard Timing ID #7	PC Application
33	01	1		
34	01	1	Standard Timing ID #8	PC Application
35	01	1		

Table 54 Standard Timing ID Block

A.2.10 Detailed Timing Descriptor Block

The detailed timing section is 72 bytes in length and can be divided into four descriptor blocks, which are each 18 bytes. In the following example, the address ranges for these four blocks are 36h-47h, 48h-59h, 5Ah-6Bh and 6Ch-7Dh. Each of these descriptors contains either detailed timing data (Detailed Timing Descriptor) or other specific types of data as described in the VESA E-EDID standard.

The VESA E-EDID standard allows various descriptor sequences, combinations, or repetitions and source devices should handle descriptors that may appear in any order. The only prescribed constraint is that Detailed Timing Descriptors precede the two required Monitor Descriptors in Block 0. The descriptors require the presence of valid data and no fill patterns are permitted in Block 0. Therefore, the source device should handle these possibilities and requirements accordingly. Blocks used for data, not detailed timing information, have a five byte identifier header that is formatted as follows: 00h, 00h, 00h, <Tag #>, 00h. For more detail regarding 18-byte descriptor tags, please refer to the VESA EDID standard section 3.10.3.

The example in this document configures the four blocks in this order: First Detailed Timing Descriptor, Second Detailed Timing Descriptor, First Monitor Descriptor (Monitor Name), and Second Monitor Descriptor (Monitor Range).

A.2.10.1 First Detailed Timing Descriptor

The VESA E-EDID Standard requires that the First Detailed Timing Descriptor be used for the most “preferred” video format and subsequent detailed timing descriptors are listed in order of decreasing preference.

Data locations within the Detailed Timing Descriptors are used to specify the video timing characteristics, image size, and contain flags for identifying interlace/non-interlace formats and sync signal polarities. Designers of source and sink device need to carefully consider these types of data in all implementations.

The example in Table 55 shows the data format for a “preferred” HDTV format 1920x1080i and the image size is matched to the screen size of approximately 36 inches diagonal. CEA-861-D recommends listing exact horizontal and vertical dimensions, but at least requires values that describe the aspect ratio. The source box should be capable of using these dimensions to determine aspect ratio. However, some EDID implementations that do not provide horizontal and vertical dimensions for non-CEA-861-D video formats may be encountered. The flags are set to convey an interlaced format and the syncs as separate and of positive polarity.

Address Hex	**Example Data Hex**	**Dec**	**Description**	**Remarks (Refer to note below for additional details)**
36	01	1	Pixel Clock	74.25 MHz
37	1D	29		
38	80	128	H Active	1920 pixels
39	18	24	H Blanking	280 pixels
3A	71	113	H Active: H Blanking	
3B	1C	28	V Active	540 lines
3C	16	22	V Blanking	22 lines
3D	20	32	V Active: V Blanking	
3E	58	88	H Sync Offset	88 pixels
3F	2C	44	H Sync Pulse Width	44 pixels
40	25	37	VS Offset: VS Pulse Width	2 lines, 5 lines
41	00	0	HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
42	20	32	H Image Size	800 mm (lower 8 bits)
43	C2	194	V Image Size	450 mm (lower 8 bits)
44	31	49	H&V Image Size	Upper 4 bits of H Size; Upper 4 bits of V Size
45	00	0	H Border	0 lines
46	00	0	V Border	0 pixels
47	9E	158	Flags	Interlaced, normal display no stereo, digital separate, V-sync polarity is positive, H-sync polarity is positive
NOTE—Some addresses above contain ‘composite’ bytes representing high and/or low order bits or “nibbles” (4 bits of an 8-bit byte). Please refer to section 3.10.2 of the VESA E-EDID standard for details on these fields.				

Table 55 First Detailed Timing Descriptor Block (1920x1080i Example)

A.2.10.2 Second Detailed Timing Descriptor

Table 56 contains an example for the second preferred timing using the Second Detailed Timing Descriptor block. This is the EDTV 720x480p format that has a 4:3 aspect ratio.

Address Hex	Example Data Hex	Dec	Description	Remarks (Refer to note below for additional details)
48	8C	140	Pixel Clock	27 MHz
49	0A	10		
4A	D0	208	H Active	720 pixels
4B	8A	138	H Blanking	138 pixels
4C	20	32	H Active: H Blanking	
4D	E0	224	V Active	480 lines
4E	2D	45	V Blanking	45 lines
4F	10	16	V Active: V Blanking	
50	10	16	H Sync Offset	16 pixels
51	3E	62	H Sync Pulse Width	62 pixels
52	96	150	VS Offset: VS Pulse Width	9 lines, 6 lines
53	00	0	HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
54	58	88	H Image Size	600 mm (lower 8 bits)
55	C2	194	V Image Size	450 mm (lower 8 bits)
56	21	33	H&V Image Size	Upper 4 bits of H Size; Upper 4 bits of V Size
57	00	0	H Border	0 lines
58	00	0	V Border	0 pixels
59	18	24	Flags	Non-interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative
NOTE—Some addresses above contain ‘composite’ bytes representing high and/or low order bits or “nibbles” (4 bits of an 8-bit byte). Please refer to section 3.10.2 of the VESA E-EDID standard for details on these fields.				

Table 56 Second Detailed Timing Descriptor Block (720x480p, 4:3 Example)

A.2.10.3 First Monitor Descriptor (Monitor Name)

The VESA Standard requires that one of the four 18-byte descriptors be a Monitor Name Descriptor. Here, it is recommended that the third 18-byte descriptor be used as the First Monitor Descriptor or Monitor Name. Examples of these bytes are located at addresses 5Fh through 6Bh. Each location is one byte in length and is used for ASCII character string. In the example contained in Table 57, a fictitious Monitor Name is listed.

Address Hex	Example Data Hex	Dec	Description	Remarks
5A	00	0	Flag (REQUIRED)	Flag = 0000h when block used as descriptor
5B	00	0		
5C	00	0	Flag (Reserved)	Flag = 00h when block used as descriptor
5D	FC	252	Data Type Tag	FCh denotes that last 13 bytes of this descriptor block contain Monitor name
5E	00	0	Flag	Flag = 00h when block used as descriptor
5F	4D	77	ASCII coded monitor name (13 bytes max). If name < 13 bytes, terminate name with 0Ah and fill remainder of 13 bytes with 20h.	Example monitor name: “MY HDTV”
60	59	89		
61	20	32		
62	48	72		
63	44	68		
64	54	84		
65	56	86		
66	0A	10		
67	20	32		
68	20	32		
69	20	32		
6A	20	32		
6B	20	32		

Table 57 First Monitor Descriptor Block (Monitor Name)

A.2.10.4 Second Monitor Descriptor (Monitor Range Limits)

The next and last 18-byte descriptor within Block 0 should be used as the Second Monitor Descriptor. In this example, it is the Monitor Range Limit, which is used to designate minimum and maximum parameters for horizontal and vertical frequencies and maximum pixel clock rate. In the following example, the block of data ranges from 6Ch through 7Dh. The data format is binary coded integer.

The first three locations, 6Ch (Flag), 6Dh (Flag), and 6Eh (Reserved Flag) are set to zero. Address 6Fh, a Data Type Flag, should be set to FDh, which means, “monitor range limits, binary coded”. For more detail, please refer to the VESA E-EDID standard section 3.10.3. Address 70h is another flag and loaded with zero.

Locations 71h through 75h are used to designate the minimum and maximum parameters for horizontal and vertical frequencies, and maximum pixel clock. Table 58 contains an example for a DTV that supports a 60 Hz vertical refresh rate, 15 kHz up to 46 kHz horizontal rates, which cover the frequencies required for 720 x 480i and 1280 x 720p formats, including 480 x 720p and 1920 x 1080i[15], and a maximum pixel clock of 80 MHz.

> NOTE—To reduce the possibility that a source device would mistakenly ignore the frequency range data if the minimum and maximum values were equal, a range of horizontal and vertical frequencies should be declared. For example, if a device supports only 15.75 kHz and 60 Hz timing, it is recommended to list the range as 15 to 16 kHz and 59 to 61 Hz. Source devices may encounter legacy devices that specify the same value for MIN and MAX horizontal and/or vertical ranges.

[15] This frequency range does not necessarily imply multi-scan capability. Due to the 1920x1080p format supported by CEA-861-C, a horizontal frequency of 67.5 kHz may be encountered and source devices should be capable of interpreting this information correctly

Address Hex	Example Data Hex	Dec	Description	Remarks
6C	00	0	Flag	Flag = 0000h when block used as descriptor
6D	00	0		
6E	00	0	Flag (Reserved)	Flag = 00h when block used as descriptor
6F	FD	253	Data Type Tag	FDh denotes that last 13 bytes of this descriptor block contain Monitor Range limits, binary coded
70	00	0	Flag	Flag = 00h when block used as descriptor
71	3B	59	Min Vertical Rate in Hz	59 HZ
72	3D	61	Max Vertical Rate in Hz	61 Hz
73	0F	15	Min Horizontal Rate in kHz	15 kHz
74	2E	46	Max Horizontal Rate in kHz	46 kHz
75	08	8	Max Supported pixel clock rate in MHz/10	80 MHz
76	00	0	Tag for secondary timing formula (00h=not used)	No secondary timing formula supported
77	0A	10	Put 0Ah after last data byte in block and fill remaining bytes with 20h.	Unused data address
78	20	32		
79	20	32		
7A	20	32		
7B	20	32		
7C	20	32		
7D	20	32		

Table 58 Second Monitor Descriptor Block (Monitor Range Limits)

Address 76h is used as a tag for a secondary generalized timing formula (GTF) and is not typically used for CE devices. In this case, the flag is set to zero. Addresses 77h through 7Dh are related to this tag. The E-EDID standard requires that address 77h contain 0Ah and addresses 78h ~ 7Dh contain 20h when no secondary GTF data is provided.

A.2.11 Extension Flag and Checksum

The Extension Flag and Checksum are defined as two-byte data located in address range 7Eh through 7Fh. The Extension Flag is used to indicate that additional blocks are present in the EDID that declare additional video formats and other monitor features.

The Extension Flag is used to declare the number of extensions that exist within the EDID tables. The total number of extensions actually present should equal the number of extensions declared within the base EDID. The number of extensions declared in the base EDID shall not include the base EDID, but shall include the block map. For example, if no extensions exist in the EDID data, then the Extension Flag shall be set to zero. If a single (e.g. CEA) extension is present, then the flag shall be set to one. If two (e.g. CEA) extensions are used, then a block map extension is also required by VESA EDID standard—increasing the total number of extensions to three. In this case, the extension flag is set to 3 and the sink product has an EDID containing a total of four 128-byte blocks: a base block plus three extensions—the first extension being a block map.

NOTE—Some devices have been incorrectly designed so that the block map is not counted in the extension count. Design of compliant devices should take compatibility with those non-compliant devices into consideration. For example, when a source finds an extension count of 2, it may

attempt to read 3 extensions on the chance that the sink has incorrectly set its count, or it may use the information in the block map as a more accurate guide.

The Checksum is set so that the sum of the entire 128-byte block modulus 256 equals 00h. Sink designers should calculate checksum using the following formula:

Checksum byte = (256-(S%256))%256

Where:

S is the sum of the first 127 bytes
% is modulus operator

Table 59 contains example data based upon the tables presented in this document. The Extension Flag at location 7Eh is set to one declaring that Block 1 is present. Since the Extension Flag equals 1 in the example, no other blocks exist. The Checksum is set so that the sum modulus 256 of the entire 128-byte block equals 00h.

Address Hex	**Example Data Hex**	**Dec**	**Description**	**Remarks**
7E	01	1	Extension Flag	Number of 128 bytes blocks to follow
7F	C3	195	Checksum	Block 0 sum (address 00h~7Eh) = 1B3Dh

Table 59 Extension Flag Block

A.2.11.1 Block One Details

Although there may be DTV implementations that do not include a CEA Extension or that include it in a block other than Block 1, it is recommended that for a CEA-861-D implementation, that the CEA Extension be included in Block 1. Therefore, the remainder of Annex A (through Section A.4) assumes that Block 1 is a CEA Extension.

The main purpose of the CEA Extension is to provide a place to add additional Detailed Timing Descriptors. However, other VESA-defined 18-byte descriptors are possible (e.g., Monitor Serial Number, Manufacturer Specific, etc.). Source boxes should ignore descriptors that they do not understand. The only descriptors that a CEA-861-D source is required to understand are the Detailed Timing Descriptors, the Monitor Range Limit descriptor, and the Monitor Name Descriptor. Note that the handling of unused descriptors is different in the CEA Extension than it is in Block 0. In Block 0, all four descriptor blocks are required by VESA EDID standard to be filled with valid data, even if it means repeating a timing descriptor. In the CEA Extension, unused descriptor locations are all collected at the end and filled with a fill pattern of 00h. Technically, a descriptor that has the first bytes being 00h would be a manufacturer-defined descriptor with a tag of 00h. It is recommended that manufacturers avoid the use of a 00h tag. Source boxes should verify that there are 18 00h bytes following the last valid descriptor if there is enough room for a descriptor. It is also recommended that the DTV place all of its remaining Detailed Timing Descriptors before other descriptors in the CEA Extension.

Within the CEA Extension, per CEA-861-D, up to six Detailed Timing Descriptors are allowed and may occur in any order. Therefore, source devices should be able to handle any combination or sequence that these Detailed Timing Descriptors may appear. According to CEA-861-D, the timing of highest priority is listed first and subordinate timings in descending order. Source devices should be capable of skipping additional extensions that they may not understand when encountered within Block 1.

A.2.12 Overview of Extensions

VESA has assigned Extension Tags to identify EDID extensions and source devices should anticipate encountering some of these extensions. Extensions are identified by the first byte (i.e., Tags). The Tags indicate the type of extension and its purpose. Table 60 lists the Extensions Tag numbers and their

description. CEA-861 implementations are required to use Tag = 02h for the CEA Extension Tag and source devices should ignore Tags that are not understood.

Tag	Description
01h	LCD Timings
02h	CEA Extension, previously reserved for VESA additional timing data, which now uses a different tag.
20h	EDID 2.0 Extension
30h	Color information Type 0
40h	DVI feature data
50h	Touch Screen Map
F0h	Block Map
FFh	Extension Defined by monitor manufacturer

Table 60 EDID Extension Tags

The structure of the CEA Extension (Version 1) block is shown in Table 61. Please note that other versions of CEA Extensions exist. See Section 7.1 for additional guidance.

Byte #	Value	Description	Format
0	02h	Tag (02h)	
1	01h	Revision Number	
2		Byte number offset ***d*** where 18-byte descriptors begin (typically Detailed Timing Descriptors)	***d*** = offset for the byte following the reserved data block. If no data is provided in the reserved data block, then ***d***=4. If no detailed timing descriptions are provided then ***d***=0.
3		Reserved	Set to 00h
4		Start reserved data block	This section was previously reserved for 8 byte-timing descriptors, but is currently a reserved data block.
d-1		End of reserved data block.	
d		Start of 18-byte descriptors (typically Detailed Timing Descriptors)	See Section 3.10.2 VESA E-EDID Standard.
d+(18**n*)-1		End of 18-byte descriptors where n is the number of descriptors included	
d+(18**n*)	00h	Beginning of Padding	
126	00h	End of Padding	
127		Checksum	xxh = This byte should be programmed such that a one-byte checksum (add all bytes together and modulus 256) of the entire 128 byte block equals “00h”.

Table 61 CEA Extension Version 1

A.2.13 Block One CEA Extension Header

The CEA Extension Header is defined as four-byte data located in the first four bytes of the EDID block. The first byte is the tag used to identify the extension. The number assigned by VESA to this tag is 02h. Following the CEA Extension Tag is the Revision Number location. The data for Revision Number was set according to which standard version the sink device was designed to support. CEA-861, CEA-861-A, and CEA-861-B all had unique number assignments for the Revision Number and this was used to differentiate the level of supported features, such as ”InfoPackets“, audio, etc. Incrementing the version number is no longer required. CEA-861 formerly required the revision number to be set to 01h, for CEA-861-A it was 02h, and for CEA-861-B it was 03h; however, this is no longer required in CEA-861-D, where only 03h is used. See Section 7.1 for further guidance. Versions 2 and 3 of the CEA Extension are

backward compatible with version 1, which is illustrated in this example. Source devices should be prepared to read versions later than version 1 and properly interpret the required 18-byte descriptors.

Following the Revision Number is the Byte Number Offset. This is used to tell where the Detailed Timing Data begins following the Reserved Data Block. The source device should use this byte offset to skip fields that it may not understand within the CEA Extension when encountering versions of this extension that may be newer than its own. CEA-861 DTV Monitors should load location 82 with d = 4 if the extension includes 18-byte descriptors. In the following example, the data is listed as 04h, which means there is no data present in the Reserved Data Block and that there are 18-byte descriptors present starting at the fifth byte of the EDID block.

Source devices should be aware that for later versions of the CEA Extension, ***d*** may be set to something other than 0 when no 18-byte descriptors are present. This is an indication that there is data in the reserved data block. In that case, ***d*** would be set to the location where 18-byte detailed timing descriptors would be located if present. That data should be skipped by a CEA-861-D source device. The presence of padding data for 18-byte descriptors can be used by the source box as an indication whether 18-byte descriptors are present or not.

The data at the next address location, 83h in this example, is reserved in the CEA Extension Version 1 (used for an 861 implementation) and is required in 861 to be set to 00h. Newer versions of the CEA Extension include flags in this field (see Sections 7.3 and 7.4). These flags can be ignored by a CEA-861-D source.

Table 62 contains example data based upon the tables presented in this document. In this example, the CEA Extension Tag is located at 80h followed by Revision Number, Byte Number Offset, and Reserved (i.e., 00h). The data is set as prescribed by CEA-861-D.

Address Hex	**Example Data Hex**	**Dec**	**Description**	**Remarks**
80	02	2	Tag per CEA-861	Tag 02h assigned by VESA to CEA for this extension
81	01	1	01h per CEA-861	Indicates revision of CEA-861 used by this device
82	04	4	04h per CEA-861	04h indicates no data present in Reserved Data Block; 18-byte descriptors ARE present
83	00	0	00h per CEA-861	These bits are utilized as flags in later versions of CEA-861

Table 62 Block One CEA Extension Header

A.2.14 Third Detailed Timing Descriptor

Following the Extension Flag Table is the next or Third Detailed Timing Descriptor. Table 63 follows the same format as with Table 55 and Table 56. This example is for HD format 1280x720p.

Address Hex	Example Data Hex	Dec	Description	Remarks (Refer to note below for additional details)
84	01	1	Pixel Clock	74.25 MHz
85	1D	29		
86	00	0	H Active	1280 pixels
87	72	114	H Blanking	370 pixels
88	51	81	H Active: H Blanking	
89	D0	208	V Active	720 lines
8A	1E	30	V Blanking	30 lines
8B	20	32	V Active: V Blanking	
8C	6E	110	H Sync Offset	110 pixels
8D	28	40	H Sync Pulse Width	40 pixels
8E	55	85	VS Offset: VS Pulse Width	
8F	00	0	HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
90	20	32	H Image Size	800 mm (lower 8 bits)
91	C2	194	V Image Size	450 mm (lower 8 bits)
92	31	49	H&V Image Size	Upper 4 bits of H Size; Upper 4 bits of V Size
93	00	0	H Border	0 pixels
94	00	0	V Border	0 lines
95	1E	30	Flags	Non-interlaced, normal display no stereo, digital separate, H and V sync polarity is positive
NOTE—Some addresses above contain ‘composite’ bytes representing high and/or low order bits or “nibbles” (4 bits of an 8-bit byte). Please refer to section 3.10.2 of the VESA E-EDID standard for details on these fields.				

Table 63 Third Detailed Timing Descriptor Block (720p, 16:9 Example)

A.2.15 Fourth Detailed Timing Descriptor

After the Third Detailed Timing Descriptor, the next Detailed Timing Descriptor follows, as indicated in Table 64. As with Table 55, Table 56 and Table 63, the same format is used. This table declares the SD 720x480i format, which requires doubling the horizontal pixel count to meet the DVI 1.0 minimum pixel clock frequency.

Address Hex	Example Data Hex	Dec	Description	Remarks (Refer to note below for additional details)
96	8C	140	Pixel Clock	27 MHz
97	0A	10		
98	A0	160	H Active	1440 pixels
99	14	20	H Blanking	276 pixels
9A	51	81	H Active: H Blanking	
9B	F0	240	V Active	240 lines
9C	16	22	V Blanking	22 lines
9D	00	0	V Active: V Blanking	
9E	26	38	H Sync Offset	38 pixels
9F	7C	124	H Sync Pulse Width	124 pixels
A0	43	67	VS Offset: VS Pulse Width	
A1	00	0	HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
A2	58	88	H Image Size	600 mm (lower 8 bits)
A3	C2	194	V Image Size	450 mm (lower 8 bits)
A4	21	33	H&V Image Size	Upper 4 bits of H Size; Upper 4 bits of V Size
A5	00	0	H Border	0 lines
A6	00	0	V Border	0 pixels
A7	98	152	Flags	Interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative,
NOTE—Some addresses above contain ‘composite’ bytes representing high and/or low order bits or “nibbles” (4 bits of an 8-bit byte). Please refer to section 3.10.2 of the VESA E-EDID standard for details on these fields.				

Table 64 Fourth Detailed Timing Descriptor Block (480i, 4:3 Example)

A.2.16 Descriptor Defined by Manufacturer

The Descriptor Defined by Manufacturer Table is placed after the last Detailed Timing Descriptor. The manufacturer defines the contents of this descriptor. The tag can be any value between 00h and 0Fh although the use of 00h is not recommended as explained in section 4.3. The example in Table 65 illustrates data that declares a revision number.

11dd00ddddd00ddd0dd00d01d1d00d00d00d00d111

Address Hex	Example Data Hex	Dec	Description	Remarks
A8	00	0	Flag	
A9	00	0	Flag	
AA	00	0	Reserved	
AB	01	1	Data Type 01-0F	
AC	00	0	Flag	
AD	52	82	R	
AE	45	69	E	
AF	56	86	V	
B0	31	49	1	
B1	2E	46	.	
B2	30	48	0	
B3	30	48	0	
B4	0A	10		
B5	00	0		
B6	00	0		
B7	00	0		
B8	00	0		
B9	00	0		

Table 65 Descriptor Defined by Manufacturer Block

A.2.17 Monitor Serial Number

13 bytes of this 18-byte table are allocated for the Monitor Serial number. This table can be used for the manufacturer's convenience. The monitor serial number descriptor uses FFh as the tag. Tags are described in Section 4.2.8. The data should be ASCII based. Table 66 contains a fictitious serial number as an example.

Address Hex	Example Data Hex	Dec	Description	Remarks
BA	00	0	Flag	Flag = 0000h when block used as descriptor
BB	00	0		
BC	00	0	Flag (Reserved)	Flag = 00h when block used as descriptor
BD	FF	255	Serial Number Tag	Refer to VESA E-EDID standard, section 3.10.3 for tag definitions
BE	00	0	Flag	
BF	39	57	ASCII serial number data	9
C0	39	57		9
C1	46	70		F
C2	43	67		C
C3	35	53		5
C4	30	48		0
C5	30	48		0
C6	30	48		0
C7	31	49		1
C8	0A	10		ASCII Line Feed
C9	20	32		Padding (ASCII space)
CA	20	32		Padding (ASCII space)
CB	20	32		Padding (ASCII space)

Table 66 Monitor Serial Number Block

A.2.18 Residual Byte Padding and Check Sum

CEA-861-D requires that residual addresses contain padding. In this case, 00h is used as padding. Address FFh should contain a one-byte checksum value such that when all bytes of the entire 128-byte block are added, the sum modulus 256 equals 00h. Table 67 illustrates these requirements.

Address Hex	Example Data Hex	Dec	Description	Remarks
CC	00	0	1st padding byte	Padding bytes should = 00h.
CD	00	0	Additional padding bytes	
CE	00	0		
CF	00	0		
D0	00	0		
D1	00	0		
D2	00	0		
D3	00	0		
D4	00	0		
D5	00	0		
D6	00	0		
D7	00	0		
D8	00	0		
D9	00	0		
DA	00	0		
DB	00	0		
DC	00	0		
DD	00	0		
DE	00	0		
DF	00	0		
E0	00	0		
E1	00	0		
E2	00	0		
E3	00	0		
E4	00	0		
E5	00	0		
E6	00	0		
E7	00	0		
E8	00	0		
E9	00	0		
EA	00	0		
EB	00	0		
EC	00	0		
ED	00	0		
EE	00	0		
EF	00	0		
F0	00	0		
F1	00	0		
F2	00	0		
F3	00	0		
F4	00	0		
F5	00	0		
F6	00	0		
F7	00	0		
F8	00	0		
F9	00	0		
FA	00	0		
FB	00	0		
FC	00	0		
FD	00	0		
FE	00	0	Last padding byte	
FF	84	132	Checksum	Block 1 sum (address 80h~FFh) = 0E7Ch

Table 67 Residual Byte Stuffing and Check Sum Block

A.2.19 Hot Plugging Sequence

An important element to proper interpretation of EDID is “Hot Plugging”. The following presents a recommendation for achieving consistent results during a Hot Plugging event.

DVI 1.0 defines a Hot Plug Detect (HPD) signal function that indicates to the host whether a monitor is connected. HPD is designed to be powered by the DDC + 5V coming from the host, and to be independent of whether the monitor is powered or not. In this way, a host device can detect the monitor and read its characteristics from EDID without the monitor being powered. On a PC, this feature allows the system to load the correct display configuration without delaying the boot process.

In short, in this context, HPD serves as an indication that the EDID is available to be read, however HPD may also have alternative uses. It does not imply any other state of readiness. The relevant definitions from the DVI 1.0 specification are:

a) Section 2.6: Hot Plug Detect (HPD) – Signal is driven by monitor to enable the system to identify the presence of a monitor.
b) Section 2.2.9.2: The monitor is required to provide a voltage of greater than +2.4V on the Hot Plug Detect (HPD) pin of the connector only when the EDID data structure is available to be read by the host.

Implementation Note: As an example for hot plug support, a simple monitor implementation of HPD support could be a pull up resistor to the EDID power supply. After HPD goes active, the host is only expected to read EDID and determine that a valid display mode is available and supported.

> NOTE—Whenever the EDID information in a device changes for any reason (e.g. if the EDID was updated, or is capable of dynamically changing its information content), the receiving device pulses HPD low for at least 100ms. This recommendation follows from the HDCP repeater implementation requirement that HDCP repeaters pulse HPD low for at least 100ms to indicate the connection of a new device or disconnection of an existing one.

A.3 Complete Example EDID Table (Informative)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
00	00	0	Block Zero Header		Fixed Value
01	FF	255			
02	FF	255			
03	FF	255			
04	FF	255			
05	FF	255			
06	FF	255			
07	00	0			
08	0C	12	Vendor / Product ID	Manufacturer Name	CEA
09	A1	161			
0A	00	00		Product Code	Used to differentiate between different models from the same manufacturer.
0B	00	0			
0C	00	00		Serial Number	Optional. The serial number can also be stored in a separate descriptor block
0D	00	00			
0E	00	00			
0F	00	00			
10	00	0		Week of Manufacture	Optional. If this field is unused, the value should be set to 0.
11	0C	12		Year of Manufacture	Year 2002
12	01	1	EDID Structure Version / Revision	Version #	1
13	03	3		Revision #	3
14	80	128	Basic Display Parameters / Features	Video Input Definition	Digital, VESA DFP1X : not compatible
15	50	80		Max. Horizontal Image Size in cm	Optional. The system should not make any assumption regarding display size
16	2D	45		Max. Vertical Image Size in cm	Optional. See above.
17	78	120		Gamma: (gamma x 100)-100 = value	Example is: (gamma = 2.2) (2.2 x 100)-100 = 120
18	0A	10		Feature Support	0x0A denotes: RGB color Display type, preferred timing: first detailed timing block. GTF timing: not supported. Standby mode: not supported, suspend mode: not supported, active off: not supported

Table 68 Complete EDID Example

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
19	0D	13	Color Characteristics	Red/Green Low Bits	
1A	C9	201		Blue/White Low Bits	
1B	A0	160		Red-x	0.625
1C	57	87		Red-y	0.340
1D	47	71		Green-x	0.280
1E	98	152		Green-y	0.595
1F	27	39		Blue-x	0.155
20	12	18		Blue-y	0.070
21	48	72		White-x	0.283
22	4C	76		White-y	0.298
23	20	32	Established Timings	Timing 1	640x480 @60Hz
24	00	0		Timing 2	None
25	00	0		Manufacturer's Reserved Timing	None
26	01	1	Standard Timing ID # 1-8	Standard Timing ID #1	PC Applications
27	01	1			
28	01	1		Standard Timing ID #2	PC Applications
29	01	1			
2A	01	1		Standard Timing ID #3	PC Applications
2B	01	1			
2C	01	1		Standard Timing ID #4	PC Applications
2D	01	1			
2E	01	1		Standard Timing ID #5	PC Applications
2F	01	1			
30	01	1		Standard Timing ID #6	PC Applications
31	01	1			
32	01	1		Standard Timing ID #7	PC Applications
33	01	1			
34	01	1		Standard Timing ID #8	PC Applications
35	01	1			
36	01	1	First Detailed Timing Descriptor (Preferred)	Pixel Clock	74.25 MHz
37	1D	29			
38	80	128		H Active	1920 pixels
39	18	24		H Blanking	280 pixels
3A	71	113		H Active: H Blanking	
3B	1C	28		V Active	540 lines
3C	16	22		V Blanking	22 lines
3D	20	32		V Active: V Blanking	
3E	58	88		H Sync Offset	88 pixels
3F	2C	44		H Sync Pulse Width	44 pixels
40	25	37		VS Offset: VS Pulse Width	2 lines, 5 lines
41	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
42	20	32		H Image Size	800 mm
43	C2	194		V Image Size	450 mm
44	31	49		H&V Image Size	
45	00	0		H Border	0 lines
46	00	0		V Border	0 pixels
47	9E	158		Flags	Interlaced, normal display no stereo, digital separate, V-sync polarity is positive, H-sync polarity is positive

Table 68 Complete EDID Example (Continued)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
48	8C	140	Second Detailed Timing Descriptor	Pixel Clock	27 MHz
49	0A	10			
4A	D0	208		H Active	720 pixels
4B	8A	138		H Blanking	138 pixels
4C	20	32		H Active: H Blanking	
4D	E0	224		V Active	480 lines
4E	2D	45		V Blanking	45 lines
4F	10	16		V Active: V Blanking	
50	10	16		H Sync Offset	16 pixels
51	3E	62		H Sync Pulse Width	62 pixels
52	96	150		VS Offset: VS Pulse Width	9 lines, 6 lines
53	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
54	58	88		H Image Size	600 mm
55	C2	194		V Image Size	450 mm
56	21	33		H&V Image Size	
57	00	0		H Border	0 lines
58	00	0		V Border	0 pixels
59	18	24		Flags	non interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative
5A	00	0	Monitor Descriptor Currently Mandatory (Monitor Name)	Flag	
5B	00	0			
5C	00	0		Flag (Reserved)	
5D	FC	252		Data Type Tag	Monitor name type
5E	00	0		Flag	
5F	4D	77		M	
60	59	89		Y	
61	20	32			
62	48	72		H	
63	44	68		D	
64	54	84		T	
65	56	86		V	
66	0A	10			
67	20	32			
68	20	32			
69	20	32			
6A	20	32			
6B	20	32			

Table 68 Complete EDID Example (Continued)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
6C	00	0	Second Monitor Descriptor Currently Mandatory (range limits, binary coded)	Flag	
6D	00	0			
6E	00	0		Flag (Reserved)	
6F	FD	253		Data Type Tag	Monitor Range limits, binary coded, mandatory block
70	00	0		Flag	
71	3B	59		Min Vertical Rate in Hz	59 HZ
72	3D	61		Max Vertical Rate in Hz	61 Hz
73	0F	15		Min Horizontal Rate in kHz	15 kHz
74	2E	46		Max Horizontal Rate in kHz	46 kHz
75	08	8		Max Supported pixel clock rate in MHz/10	80 MHz
76	00	0		Tag for secondary timing formula (00h=not used)	No secondary timing formula supported
77	0A	10		Fixed	
78	20	32		Fixed	
79	20	32		Fixed	
7A	20	32		Fixed	
7B	20	32		Fixed	
7C	20	32		Fixed	
7D	20	32		Fixed	
7E	01	1	Extension Flag	Number of 128 bytes blocks to follow	
7F	C3	195		Checksum	Block 0 sum = 1B3Dh
80	02	2	CEA Extension Header	Tag	Block One
81	01	1		01h by 861	Revision Number
82	04	4		04h, no data in Reserved	Byte Offset
83	00	0		00h by 861	

Table 68 Complete EDID Example (Continued)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
84	01	1	Third Detailed Timing Descriptor	Pixel Clock	74.25 MHz
85	1D	29			
86	00	0		H Active	1280 pixels
87	72	114		H Blanking	370 pixels
88	51	81		H Active: H Blanking	
89	D0	208		V Active	720 lines
8A	1E	30		V Blanking	30 lines
8B	20	32		V Active: V Blanking	
8C	6E	110		H Sync Offset	110 pixels
8D	28	40		H Sync Pulse Width	40 pixels
8E	55	85		VS Offset: VS Pulse Width	
8F	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
90	20	32		H Image Size	800 mm
91	C2	194		V Image Size	450 mm
92	31	49		H&V Image Size	
93	00	0		H Border	0 pixels
94	00	0		V Border	0 lines
95	1E	30		Flags	Non-interlaced, normal display no stereo, digital separate, H and V sync polarity is positive
96	8C	140	Fourth Detailed Timing Descriptor	Pixel Clock	27 MHz
97	0A	10			
98	A0	160		H Active	1440 pixels
99	14	20		H Blanking	276 pixels
9A	51	81		H Active: H Blanking	
9B	F0	240		V Active	240 lines
9C	16	22		V Blanking	22 lines
9D	00	0		V Active: V Blanking	
9E	26	38		H Sync Offset	38 pixels
9F	7C	124		H Sync Pulse Width	124 pixels
A0	43	67		VS Offset: VS Pulse Width	
A1	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
A2	58	88		H Image Size	600 mm
A3	C2	194		V Image Size	450 mm
A4	21	33		H&V Image Size	
A5	00	0		H Border	0 lines
A6	00	0		V Border	0 pixels
A7	98	152		Flags	interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative,

Table 68 Complete EDID Example (Continued)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
A8	00	0	Descriptor Defined by Manufacturer	Flag	
A9	00	0		Flag	
AA	00	0		Reserved	
AB	01	1		Data Type 01-0F	
AC	00	0		Flag	
AD	52	82		R	
AE	45	69		E	
AF	56	86		V	
B0	31	49		1	
B1	2E	46		.	
B2	30	48		0	
B3	30	48		0	
B4	0A	10			
B5	00	0			
B6	00	0			
B7	00	0			
B8	00	0			
B9	00	0			
BA	00	0	Monitor Serial Number (ASCII, 13 bytes max)		
BB	00	0			
BC	00	0			
BD	FF	255		Serial Number Tag	
BE	00	0			
BF	39	57		9	
C0	39	57		9	
C1	46	70		F	
C2	43	67		C	
C3	35	53		5	
C4	30	48		0	
C5	30	48		0	
C6	30	48		0	
C7	31	49		1	
C8	0A	10			
C9	20	32			
CA	20	32			
CB	20	32			

Table 68 Complete EDID Example (Continued)

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
CC	00	0	Residual Byte Padding		
CD	00	0			
CE	00	0			
CF	00	0			
D0	00	0			
D1	00	0			
D2	00	0			
D3	00	0			
D4	00	0			
D5	00	0			
D6	00	0			
D7	00	0			
D8	00	0			
D9	00	0			
DA	00	0			
DB	00	0			
DC	00	0			
DD	00	0			
DE	00	0			
DF	00	0			
E0	00	0			
E1	00	0			
E2	00	0			
E3	00	0			
E4	00	0			
E5	00	0			
E6	00	0			
E7	00	0			
E8	00	0			
E9	00	0			
EA	00	0			
EB	00	0			
EC	00	0			
ED	00	0			
EE	00	0			
EF	00	0			
F0	00	0			
F1	00	0			
F2	00	0			
F3	00	0			
F4	00	0			
F5	00	0			
F6	00	0			
F7	00	0			
F8	00	0			
F9	00	0			
FA	00	0			
FB	00	0			
FC	00	0			
FD	00	0			
FE	00	0			
FF	84	132	Checksum		Block 1 sum = 0E7Ch

Table 68 Complete EDID Example (Continued)

A.4 Example EDID Detailed Timing Descriptors

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	01		Pixel Clock = 74.25 MHz
37		1D		
38	Horizontal Active Pixels (lower 8 bits)	00		hor. active pixels = 1280 = 500h
39	Horizontal Blanking Pixels (lower 8 bits)	72		hor. blanking pixels = 370 = 172h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51		
3B	Vertical Active Lines, lower 8 bits	D0		vert. active lines = 720 = 2D0h
3C	Vertical Blanking Lines, lower 8 bits	1E		vert. blanking lines = 30 = 1Eh
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	6E		offset = 110 pixels = 6Eh
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	28		width = 40 pixels = 28h
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55		vert sync. offset = 5 lines vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	1E	00011110	Flag = non- interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table 69 Example EDID Detailed Timing Descriptor for 1280x720p (60 Hz, 16:9)

Byte# (Hex)	Function	Value (Hex)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	01		Pixel Clock = 74.25 MHz
37		1D		
38	Horizontal Active Pixels (lower 8 bits)	80		hor. active pixels = 1920 = 780h
39	Horizontal Blanking Pixels (lower 8 bits)	18		hor. blanking pixels = 280 = 118h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	71		
3B	Vertical Active Lines, lower 8 bits	1C		vert. active lines = 540 = 21Ch
3C	Vertical Blanking Lines, lower 8 bits	16		vert. blanking lines = 22 = 16h[16]
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	58		offset = 88 pixels = 58h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	2C		width = 44 pixels = 2Ch
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	25		vert sync. offset = 2 lines[17] vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h[18]
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	9E	10011110	Flag = interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table 70 Example EDID Detailed Timing Descriptor for 1920x1080i (60 Hz, 16:9)

[16] For interlaced display: Field 1 vertical blanking = Vertical Blanking Lines. Field 2 vertical blanking = Vertical Blanking Lines + 1 line.
[17] For interlaced display: Field 1 vertical offset = Vertical Sync Offset. Field 2 vertical offset = Vertical Sync Offset + 0.5 lines.
[18] Image size is display dependent. Ratio of Horizontal Image Size to Vertical Image Size shall be 16:9 or 4:3.

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	D0		hor. active pixels = 720 = 2D0h
39	Horizontal Blanking Pixels (lower 8 bits)	8A		hor. blanking pixels = 138 = 8Ah
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3B	Vertical Active Lines, lower 8 bits	E0		vert. active lines = 480 = 1E0h
3C	Vertical Blanking Lines, lower 8 bits	2D		vert. blanking lines = 45 = 2Dh
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10		offset = 16 pixels = 10h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	3E		width = 62 pixels = 3Eh
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	96		vert sync. offset = 9 lines vert. sync width = 6 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	13		Hor. Image size = 531 mm = 213h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (4:3 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	00011000	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 71 Example EDID Detailed Timing Descriptor for 720x480p (59.94 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	D0		hor. active pixels = 720 = 2D0h
39	Horizontal Blanking Pixels (lower 8 bits)	8A		hor. blanking pixels = 138 = 8Ah
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3B	Vertical Active Lines, lower 8 bits	E0		vert. active lines = 480 = 1E0h
3C	Vertical Blanking Lines, lower 8 bits	2D		vert. blanking lines = 45 = 2Dh
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10		offset = 16 pixels = 10h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	3E		width = 62 pixels = 3Eh
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	96		vert sync. offset = 9 lines vert. sync width = 6 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (16:9 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	00011000	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 72 Example EDID Detailed Timing Descriptor for 720x480p (59.94Hz, 16:9)

11dd00ddddd00ddd0d00d01d1d00d00d00d00d111
Gst}vklx$Fsrwyq ivSFpigpxsrngw$Ewwsgmexsr$
Tvszmihs$F}9LW$yrhivqmqirwi${ md$GIE$ Wsph3es+HMKMXEP^S R I $ S 2 0PXH 2 0$[4868846
Rs$vitvshygpxsr$svqrix{ svxmrk$tivq mxihs${ mdlsyxqmqirwi$jvsq 9LW Rsx$jsv$Viwepi0544;3;36$9><374$QX

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	A0		hor. active pixels = 1440 = 5A0h
39	Horizontal Blanking Pixels (lower 8 bits)	14		hor. blanking pixels = 276 = 114h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51		
3B	Vertical Active Lines, lower 8 bits	F0		vert. active lines = 240 = F0h
3C	Vertical Blanking Lines, lower 8 bits	16		vert. blanking lines = 22 = 16h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	00		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	26		offset = 38 pixels = 26h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7C		width = 124 pixels = 7Ch
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	43		vert sync. offset = 4 lines vert. sync width = 3 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	13		Hor. Image size = 531 mm = 213h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (4:3 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	10011000	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 73 Example EDID Detailed Timing Descriptor for 720x480i (59.94Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	A0		hor. active pixels = 1440 = 5A0h
39	Horizontal Blanking Pixels (lower 8 bits)	14		hor. blanking pixels = 276 = 114h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51		
3B	Vertical Active Lines, lower 8 bits	F0		vert. active lines = 240 = F0h
3C	Vertical Blanking Lines, lower 8 bits	16		vert. blanking lines = 22 = 16h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	00		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	26		offset = 38 pixels = 26h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7C		width = 124 pixels = 7Ch
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	43		vert sync. offset = 4 lines vert. sync width = 3 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (16:9 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	10011000	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 74 Example EDID Detailed Timing Descriptor for 720x480i (59.94Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	01		Pixel Clock = 74.25 MHz
37		1D		
38	Horizontal Active Pixels (lower 8 bits)	00		hor. active pixels = 1280 = 500h
39	Horizontal Blanking Pixels (lower 8 bits)	BC		hor. blanking pixels = 700 = 2BCh
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	52		
3B	Vertical Active Lines, lower 8 bits	D0		vert. active lines = 720 = 2D0h
3C	Vertical Blanking Lines, lower 8 bits	1E		vert. blanking lines = 30 = 1Eh
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	B8		offset = 440 pixels = 1B8h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	28		width = 40 pixels = 28h
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55		vert sync. offset = 5 lines vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	40	01000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	1E	00011110	Flag = non- interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table 75 Example EDID Detailed Timing Descriptor for 1280x720p (50 Hz, 16:9)

11dd00ddddd00ddd0d00d01d1d00d00d00d111

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	01		Pixel Clock = 74.25 MHz
37		1D		
38	Horizontal Active Pixels (lower 8 bits)	80		hor. active pixels = 1920 = 780h
39	Horizontal Blanking Pixels (lower 8 bits)	D0		hor. blanking pixels = 720 = 2D0h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	72		
3B	Vertical Active Lines, lower 8 bits	1C		vert. active lines = 540 = 21Ch
3C	Vertical Blanking Lines, lower 8 bits	16		vert. blanking lines = 22 = 16h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	10		offset = 528 pixels = 210h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	2C		width = 44 pixels = 2Ch
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	25		vert sync. offset = 2 lines vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	80	10000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	9E	10011110	Flag = interlaced; non-stereo; digital separate; positive V sync; positive H sync

Table 76 Example EDID Detailed Timing Descriptor for 1920x1080i (50 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	D0		hor. active pixels = 720 = 2D0h
39	Horizontal Blanking Pixels (lower 8 bits)	90		hor. blanking pixels = 144 = 90h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3B	Vertical Active Lines, lower 8 bits	40		vert. active lines = 576 = 240h
3C	Vertical Blanking Lines, lower 8 bits	31		vert. blanking lines = 49 = 31h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	0C		offset = 12 pixels = 0Ch
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	40		width = 64 pixels = 40h
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55		vert sync. offset = 5 lines vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	13		Hor. Image size = 531 mm = 213h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (4:3 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	00011000	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 77 Example EDID Detailed Timing Descriptor for 720x576p (50 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	D0		hor. active pixels = 720 = 2D0h
39	Horizontal Blanking Pixels (lower 8 bits)	90		hor. blanking pixels = 144 = 90h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3B	Vertical Active Lines, lower 8 bits	40		vert. active lines = 576 = 240h
3C	Vertical Blanking Lines, lower 8 bits	31		vert. blanking lines = 49 = 31h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	20		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	0C		offset = 12 pixels = 0Ch
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	40		width = 64 pixels = 40h
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	55		vert sync. offset = 5 lines vert. sync width = 5 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (16:9 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	18	00011000	Flag = non-interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 78 Example EDID Detailed Timing Descriptor for 720x576p (50 Hz, 16:9)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	A0		hor. active pixels = 1440 = 5A0h
39	Horizontal Blanking Pixels (lower 8 bits)	20		hor. blanking pixels = 288 = 120h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51		
3B	Vertical Active Lines, lower 8 bits	20		vert. active lines = 288 = 120h
3C	Vertical Blanking Lines, lower 8 bits	18		vert. blanking lines = 24 = 18h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	18		offset = 24 pixels = 18h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7E		width = 126 pixels = 7Ch
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	23		vert sync. offset = 2 lines vert. sync width = 3 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	13		Hor. Image size = 531 mm = 213h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (4:3 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	10011000	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 79 Example EDID Detailed Timing Descriptor for 720x576i (50 Hz, 4:3)

Byte# (HEX)	Function	Value (HEX)	Value (binary)	Notes
36	Pixel Clock/10,000 (LSB stored first)	8C		Pixel Clock = 27.00 MHz
37		0A		
38	Horizontal Active Pixels (lower 8 bits)	A0		hor. active pixels = 1440 = 5A0h
39	Horizontal Blanking Pixels (lower 8 bits)	20		hor. blanking pixels = 288 = 120h
3A	Horizontal Active and Blanking Pixels (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	51		
3B	Vertical Active Lines, lower 8 bits	20		vert. active lines = 288 = 120h
3C	Vertical Blanking Lines, lower 8 bits	18		vert. blanking lines = 24 = 18h
3D	Vertical Active: Vertical Blanking (upper nibble = upper 4 bits of active) (lower nibble = upper 4 bits of blanking)	10		
3E	Horizontal sync. offset (pixels) (from blanking starts, lower 8 bits)	18		offset = 24 pixels = 18h
3F	Horizontal sync pulse width (pixels) (lower 8 bits)	7E		width = 126 pixels = 7Eh
40	Vert sync offset; Vert sync pulse width (upper nibble = lines, lower 4 bits of vertical sync offset) (lower nibble = lines, lower 4 bits of vertical sync pulse width)	23		vert sync. offset = 2 lines vert. sync width = 3 lines
41	bits 7,6: upper 2 bits of Hor. sync. offset bits 5,4: upper 2 bits of Hor. sync pulse width bits 3,2: upper 2 bits of vert sync offset bits 1,0: upper 2 bits of vert. sync pulse width	00	00000000	
42	Horizontal Image Size (mm, lower 8 bits)	C4		Hor. Image size = 708 mm = 2C4h
43	Vertical Image Size (mm, lower 8 bits)	8E		Vert. Image Size = 398 mm = 18Eh (16:9 in this case).
44	Horizontal and Vertical Image Size (upper nibble = upper 4 bits of horiz.) (lower nibble = upper 4 bits of vert.)	21		
45	Horizontal Border (pixels)	0		Shall be 0
46	Vertical Border (pixels)	0		Shall be 0
47	Flags (bit 7 = non-interlaced; bit 5,6 = normal display; bit 1, 2, 3,4 = sync description; bit 0 = don't care)	98	10011000	Flag = interlaced; non-stereo; digital separate; negative V sync; negative H sync

Table 80 Example EDID Detailed Timing Descriptor for 720x576i (50 Hz, 16:9)

Annex B Application to DVI 1.0 (Normative)

All mandatory aspects of DVI 1.0 [3] shall be implemented with the exception of those expressly identified as optional or informative when DVI 1.0 is used to implement CEA-861-D. DVI does not support transport of CEA InfoFrames, audio or YC_BC_R pixel data. However, CEA-861-D can still be implemented on DVI 1.0 (with reduced functionality) as explained in Section 6.

All sections in Annex B are normative when DVI 1.0 is used to implement CEA-861-D except as otherwise noted.

B.1 Connector and Cable

The connector used shall be DVI-Digital, Single Link [3].

The cable, if supplied with the product, shall be compliant with the DVI specification at maximum pixel clock frequency compatible with the product.

B.2 Digital Content Protection

High -bandwidth Digital Content Protection (HDCP) [2] is available to authenticate display devices and encrypt content transmitted across the DVI interface.

B.2.1 Additional Information

DVI 1.0: www.ddwg.org
HDCP: www.digital-cp.com

Gst}vmklx$Gsrwyq ivGrpigpuxsrmgw$Ewwsgmexmsr$
Tvszmihf}WLWyrhivqmirwi{mdGIE
Rs$vitvshygpmxr$sv$rix{svomrk$tivqmxihf{mdsyxqmirwivsqWLW
Wsph3es+HMKMKEP^SRI$JS2D$PXH2D$[4868846
RsxsvViwepi0644;3;36$9><374$QX

Annex C Application to Open LDI (Normative)

All mandatory aspects of OpenLDI 0.95 [7] shall be implemented with the exception of those expressly identified as optional or informative in that standard when OpenLDI 0.95 is used to implement CEA-861-D. It should be noted that at the time of this writing, a version of OpenLDI that supports transport of CEA InfoFrames was not available. However, CEA-861-D can still be implemented on OpenLDI 0.95 (with reduced functionality) as explained in Section 6.

All sections in this Annex are normative when OpenLDI 0.95 is used to implement CEA-861-D except as otherwise noted.

C.1 Open LDI Data and Control Signals

OpenLDI has two options for display synchronization:

a) DC Balance Mode:
b) Non DC Balance Mode:

In DC Balance mode synchronization is accomplished by transmitting control signals during the Display blanking intervals as shown in Figure 39.

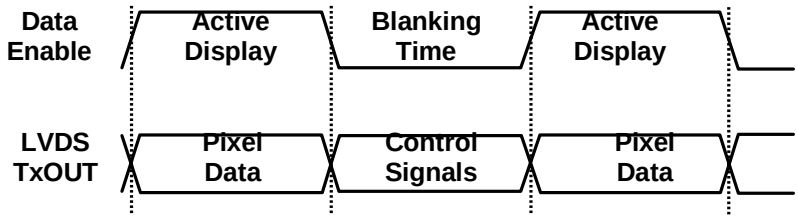


Figure 39 OpenLDI Synchronization

In the single or dual LVDS bus mode (24 or 48 bit Total), the control signals are transmitted over 7 transition words on specific output signals during the blanking period as indicated in Table 81.

Control Signal	Signal Level	Output Signal	Data Pattern
DE	High	CLK1 and CLK2	1111000 or 1110000
	Low		1111100 or 1100000
HSYNC	High	A0	1100000 or 1111100
	Low		1110000 or 1111000
VSYNC	High	A1	1100000 or 1111100
	Low		1110000 or 1111000

Table 81 OpenLDI Control Signals

C.2 Non DC Balanced Mode

Control signals are transmitted as part the LVDS serialized data stream. The controls signals are then de-serialized and regenerated at the receiver outputs to the EDTV/HDTV Monitor.

C.3 OpenLDI Cabling Information

An OpenLDI cable assembly shall consist of a cable meeting the requirements of this section with an OpenLDI plug on each end or an OpenLDI plug on one end and the other end permanently affixed to the display device. Acceptable cables for OpenLDI may use either shielded or unshielded twisted pairs. It is up to the manufacturer of the OpenLDI equipment to use the grade and type of cable required to meet applicable regulatory requirements. Adherence to CEA-861-D does not guarantee regulatory compliance.

When the OpenLDI is an interface internal to an assembly and not accessible externally, the OpenLDI cable may be replaced with any cable or connection means appropriate to the requirements of the assembly.

C.3.1 Cable Length
The maximum cable length shall be 10m.

C.3.2 Number of Signal Conductors
The OpenLDI cable shall comprise 11 twisted pairs and 10 individual conductors.

C.3.3 Wire Gauge
Each conductor in an OpenLDI cable shall be no less than 28AWG.

C.3.4 Conductor Resistance
The resistance of a single conductor of an OpenLDI cable shall not exceed 4Ω when the conductor is of the maximum length specified in CEA-861-D.

C.3.5 Insulation
Each conductor in the cable shall be separately insulated. The minimum insulation resistance shall be 1GΩ.

C.3.6 Shield Requirement
The OpenLDI cable shall be encompassed by a single shield, surrounding all conductors in the cable. The shield shall provide a minimum of 90% coverage.

For shielded twisted pair cable, each twisted pair shall be shielded individually. Each shield shall provide a minimum of 90% coverage.

C.3.7 Single Twisted Pair Transmission Skew
The differential time of transmission (single pair transmission skew) of a pulse through a single differential pair in an OpenLDI cable shall not exceed 300ps.

C.3.8 Multiple Twisted Pair Transmission Skew
The differential time of transmission (pair to pair transmission skew) of a pulse through any two differential pairs in an OpenLDI cable shall not exceed 1 bit time.

C.3.9 USB Cable Requirements
The conductors used for transmission of USB signals on the OpenLDI cable shall meet the requirements stated in the Universal Serial Bus Specification, Version 1.0, January 15, 1996.

C.3.10 DDC Cable Requirements
The conductors used for transmission of DDC signals on the OpenLDI cable shall meet the requirements stated in the VESA Display Data Channel Command Interface (DDC/CI) Standard, Version 1, August 14, 1998 [42].

More information on the connector is available in Section 7.2 of the OpenLDI specification [7].

OpenLDI .95 website Location:

http://www.National.com/appinfo/fpd

Annex D Application to HDMI (Informative)

In Annex D, the characters 0x preceding numbers or letters A through F designate the following values as hexidecimal notation.

D.1 InfoPackets

HDMI carries each InfoFrame in its own HDMI packet. The HDMI packet type for an InfoFrame packet is equal to 0x80+InfoFrame Type, therefore, only InfoFrames with Types less than 0x80 may be transmitted. Including Type, Version and Length fields, InfoFrames of at most 30 bytes are supported. A checksum is present in each InfoFrame.

Refer to the HDMI Specification for more detail on the packetization of InfoFrames.

D.2 EDID

A DTV monitor using an HDMI input shall contain an EDID consisting of a single E-EDID version 1.3 (or newer) block and at least one CEA Extension version 3.

A DTV monitor that supports either type of YC_bC_r pixel data (4:2:2 or 4:4:4) shall support both types and therefore shall set both bits 4 and 5 of byte 3 of all CEA EDID Extensions within the EDID. A DTV monitor that does not support YC_bC_r pixel data shall have both bits 4 and 5 clear. See D.6 for an example.

If the DTV Monitor supports any type of digital audio on this interface, then it shall also support Basic Audio and shall indicate this by setting the Basic Audio bit (bit 6).

Bit 7 of byte 3 shall be set if the DTV Monitor underscans IT formats by default.

D.3 Audio

HDMI [29] is capable of supporting a variety of audio formats, including uncompressed digital audio (PCM), in an IEC 60958-compliant stream at up to 8 channels, up to 192 kHz and up to 24 bits/sample, and compressed digital audio, in an IEC 61937-compliant stream, up to 192 kHz.

HDMI [29] relies on the defined audio discovery mechanisms present in the CEA EDID Extension version 3.

The Audio InfoFrame, the IEC 60958 “Channel Status” bits, and the IEC 61937 “Burst Info” bits are used to describe the transmitted audio stream. The Audio InfoFrame CT (coding type), SS (sample size) and SF (sample frequency) fields are required to be 0 (“Refer to Stream Header”) to avoid redundancy with the same data already contained within the IEC 60958 stream data.

D.4 HDCP

High-bandwidth Digital Content Protection (HDCP) version 1.1 or later, is available to protect the audio and video data carried on an HDMI link.

D.5 Additional Information

HDMI information is available from HDMI Licensing, LLC at www.hdmi.org .

HDCP information is available from Digital-CP, LLC at www.digital-cp.com .

D.6 Example EDID Using Elements of CEA Block Tag Extension (Applicable to HDMI)

Table 87 contains an example implementation of EDID utilizing elements of the CEA Block Tag Extension that were not addressed in Annex A. These elements are Short Video Descriptors, Audio Descriptors, Speaker Allocation Block, and a Vendor-Specific Data Block. This example is applicable to HDMI implementations. Elements of the Example EDID are addressed individually, in the following subsections.

D.6.1 First Monitor Descriptor (Monitor Name) and Second Monitor Descriptor (Monitor Range Limits)

Although Annex A requires that two of the four 18-byte detailed timing descriptors be a Monitor Name Descriptor and a Monitor Descriptor, it is possible that implementations designed for Personal Computers (e.g., multimedia applications), may contain a different set of data. For that reason, source devices

adhering to CEA-861-D should be designed without dependency upon specific data within these blocks that prevent collection and interpretation of subsequent data blocks.

D.6.2 Extension Flag and Checksum

The Extension Flag and Checksum are defined the same as in Annex A.

D.6.3 CEA Extension Header (Block 1)

The CEA Extension Header is a four-data bytes located in address range 80h through 83h. The first byte is the tag used to identify the extension. The number assigned by VESA to this tag is 02h. Following the CEA Extension Tag is the Revision Number location. In this example, the Revision Number is set to 03h. Please note that all Revision numbers are backward compatible. Source devices should not have a dependency upon Revision Numbers.

Table 82 contains data based upon the tables presented in this Annex. In this example, the CEA Extension Tag is located at address 80h followed by Revision Number, Byte Number Offset, and Reserved (i.e., 00h). The data is set as prescribed by CEA-861-D.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
80	02	2	CEA Extension Header	Tag	Block One
81	03	3		Revision Number	Start of CEA Block Tag Extension
82	1A				Byte Offset
83	71	113		Global Declarations	DTV, YCbCr (4:4:4), YCbCr (4:2:2)

Table 82 CEA Extension Header (Block 1)

D.6.4 CEA Data Block Collection

The CEA Data Block Collection is within the CEA Extension Block and declares CEA Short Video Descriptors, Audio capabilities, Speaker configuration, a Vendor Specific Block that requires an Identifier code, and a Vendor Specific Payload bock that is used to carry additional and optional data. As noted in Section 7.5, the Data Block ordering sequence is not constrained and various combinations are possible; and therefore, the examples provided herein are based upon one possible combination.

D.6.5 Video Data Block

The purpose of this block is for listing Short Video Descriptors (SVDs). Short Video Descriptors are used to declare video formats with one byte as contrasted with 18 bytes for Detailed Timing Descriptors, which is useful in economizing memory space. The preferred SVD is listed first. Subsequent SVDs are of decreasing preference..

As defined in Table 29 (General Tag Format), the first byte is used to signify a Video Tag Code and Payload Length. Bits 5 to 7 designate the Tag Code and payload length is defined by bits 0 to 4.

The payload byte structure is defined in Table 33. Bits 0 through 6 are used for a Video Identification Codes as defined in Table 3; and bit 7 (MSB) is a marker bit called “Native.” If bit 7 is set to ‘1’, the format is a “Native format” (see Section 2.2), and if set to ‘zero’ the format is not “Native.”

In the example, as shown in Table 83, bits 5 through 7 located in address 84h are set to Tag Code 2 (04h) designating a Video Data Block; and bits 0 to 4 is set to 7h indicating seven bytes of data payload. Addresses 85h through 8Bh contain one discrete Short Video Descriptor code per byte.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
84	47		**Video Data Block**	Start of data block collection. Includes Tag Code and length of following data block payload	47h = Video Block (code = 2) and seven bytes of data payload
85	85			1st Short Video Descriptor	1920x1080i @ 59.94/60 Hz 16:9 Native Mode
86	02			2nd Short Video Descriptor	720x480p 59.94/60 Hz 4:3
87	03			3rd Short Video Descriptor	720x480p 59.94/60 Hz 16:9
88	04			4th Short Video Descriptor	1280x720p 59.94/60 Hz 16:9
89	06			5th Short Video Descriptor	720(1440)x480i 59.94/60 Hz 4:3
8A	07			6th Short Video Descriptor	720(1440)x480i 59.94/60 Hz 4:3
8B	01			7th Short Video Descriptor	640x480p 59.94/60 Hz 4:3

Table 83 Video Data Block

D.6.6 CEA Audio Block

The Audio Data Block is used to declare format, frequency and bit-rate. The structure of this table is defined in Table 26 with subsequent tables addressing the General Tag Format, Short Audio Descriptors, and Audio Format Codes. Multiple, Short Audio Descriptors may be used in this block.

The first byte in this block is the General Format Tag and is the same structure as the Video Data Block as defined in Table 27, General Tag Format. The Tag Code occupies bits 5 and 7; and Payload Length is placed in bits 0 through 4. Audio Tag Codes are listed in Table 34, Audio Format Codes. Three bytes of data are used for each Short Audio Descriptor.

Short Audio Descriptors are defined in Table 34, Table 35, Table 36 and Table 37; with Table 34 dealing with Linear PCM Audio and compressed audio formats in the remaining tables. Each Descriptor consists of three data bytes.

In Table 84, as with the Video Data Block, the first byte (8Ch) is used to indicate block type and payload length in bytes. Audio Tag Code 1 (02h) is placed in bits 3 and 7; and bits 0 to 4 contains 3h for a payload of three bytes. The Short Audio Descriptor begins at address 8Dh and ends with 8Fh. In the first byte of the descriptor, bit 7 is reserved and set to ‘zero’. Bits 3 through 6 contain the Audio Format code as defined in Table 34; in this example Code 1 for Linear PCM is indicated with bit 6…3 set to ‘0001’. Bits 0 through 2 designate the maximum number of channels as one channel audio (1h). The second descriptor byte uses seven bits to declare frequency characteristics. Frequencies of 32 kHz, 44.1 kHz, and 48 kHz are indicated by the 07h as defined in Table 34. In address 8Eh; and in the next address 07h is used to declare bit-rates of 16, 20 and 24 bit audio per Table 34. This example does not illustrate Short Audio Descriptors for compressed audio formats.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
8C	23		Audio Data Block	Start of Audio Block	23h = Audio Block (code = 1) and three bytes of data payload.
8D	09			Audio Format	Code 1 = Linear PCM (IEC 60985)
8E	07			Frequency	07h = 32 kHz, 44.1 kHz, 48 kHz
8F	07			Bit Rate	07h = 16 bit, 20 bit, 24 bit

Table 84 Audio Data Block

D.6.7 Speaker Allocation Block

The Speaker Allocation Data Block is used to declare number of speakers and configuration. As with preceding blocks a Tag Code and payload length are designated in the first data byte. The second byte is the first byte of the data block payload and consists of seven bits and one reserved bit. These are used to indicate speaker count and configuration. The remaining two data payload bytes are set to zero (see Table 37).

In Table 85, address 90h contains a value 83h which designates the beginning of the Speaker Allocation Block and data payload. In this example, the Speaker Allocation Data Block is indicated by Code 4 per Table 29. The data payload is set to three bytes. At address 91 FL/FR (2 Channel Stereo) is chosen by setting the bits to 01h. The two remaining addresses have the bits set to zero as required by Table 37.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
90	83		Speaker Allocation Block	Start of Speaker Allocation	83h =Speaker Allocation Data Block (code = 4) and three bytes of data payload.
91	01			Speaker Designation	01 = FL / FR (2 Channel Stereo.)
92	00			Reserved	Always zero
93	00			Reserved	Always zero

Table 85 Speaker Data Block

D.6.8 Vendor Specific Block

The Vendor Specific Data Block was originally intended as an option to place data not specified by CEA-861-D; data that a manufacturer may care to use. However, the HDMI specification makes requirements that are addressed below. Users are advised to treat this data block with care.

The first address requires a Tag Code and data payload length in the first byte. The next three addresses house a 24-bit IEEE Registration Identifier (three bytes); and a Vendor Specific Payload in the remaining bytes. In the case of HDMI compliant devices the IEEE Registration is used as an 'HDMI Identifier.' After the HDMI Identifier two bytes are used to identify the port configuration. Users are advised to refer to the HDMI specification for details. For the purposes of this example the HDMI Identifier and Physical Source Address are presented.

As shown in Table 86, the first address, 94h, the Tag Code is listed as '3' and the payload length is set to '5' bytes. The second, third and fourth bytes, addresses 95, 96 and 97h, contain the HDMI LLC's 24-bit IEEE registration Organizationally Unique Identifier (OUI) 00030Ch, which is coded least significant byte first. The Physical Source Address is found in address 98 and 99h and according to the HDMI specification, the two bytes are used as Identity Port Configuration with 1000h indicating a single port sink device. The last byte in the data payload or Vendor Specific Payload address is set to zero.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
94	65		Vendor Specific Data Block	Start of Vendor Specific Block	65h = Vendor Specific Block (code = 3) and five bytes of data payload.
95	03			24-bit IEEE Registration	HDMI Identifier = 000C03h (The big-endian HDMI-LLC's 24-bit OUI Registration Identifier 0x000C03 is placed into the EDID in little-endian order.)
96	0C				
97	00				
98	10			Components of Source Physical Address	Sink identifies location of source in signal path relative to root display as ABCDh. Example shows input '1' of root display (A=1, B=0, C=0, D=0 or 1000h).
99	00				

Table 86 Vendor Specific Data Block

D.6.9 Complete CEA-861-D Example with Block Tag Extension

Table 87 contains an example implementation of E-EDID utilizing elements of the CEA Block Tag Extension that were not addressed in Annex A. These elements are Short Video Descriptors, Audio Descriptors, Speaker Allocation Block, and a Vendor-Specific Data Block. This example is applicable to HDMI implementations.

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
00	00	0	Block Zero Header		Fixed Value
01	FF	255			
02	FF	255			
03	FF	255			
04	FF	255			
05	FF	255			
06	FF	255			
07	00	0			
08	0C	12	Vendor / Product ID	Manufacturer Name	CEA
09	A1	161			
0A	00	0		Product Code	Used to differentiate between different models from the same manufacturer.
0B	00	0			
0C	00	0		Serial Number	Optional. The serial number can also be stored in a separate descriptor block
0D	00	0			
0E	00	0			
0F	00	0			
10	00	0		Week of Manufacture	Optional. If this field is unused, the value should be set to 0.
11	0F	15		Year of Manufacture	Year 2005
12	01	1	EDID Structure Version / Revision	Version #	1
13	03	3		Revision #	3
14	80	128	Basic Display Parameters / Features	Video Input Definition	Digital, VESA DFP1X : not compatible
15	50	80		Max. Horizontal Image Size in cm	Optional. The system should not make any assumption regarding display size
16	2D	45		Max. Vertical Image Size in cm	Optional. See above.
17	78	120		Gamma: (gamma x 100)-100 = value	Example is: (gamma = 2.2) (2.2 x 100)-100 = 120
18	0A	10		Feature Support	0x0A denotes: RGB color Display type, preferred timing: first detailed timing block. GTF timing: not supported. Standby mode: not supported, suspend mode: not supported, active off: not supported

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
19	0D	13	Color Characteristics	Red/Green Low Bits	
1A	C9	201		Blue/White Low Bits	
1B	A0	160		Red-x	0.625
1C	57	87		Red-y	0.340
1D	47	71		Green-x	0.280
1E	98	152		Green-y	0.595
1F	27	39		Blue-x	0.155
20	12	18		Blue-y	0.070
21	48	72		White-x	0.283
22	4C	76		White-y	0.298
23	20	32	Established Timings	Timing 1	640x480 @ 60Hz
24	00	0		Timing 2	None
25	00	0		Manufacturer's Reserved Timing	None
26	01	1	Standard Timing ID # 1-8	Standard Timing ID #1	PC Application
27	01	1			
28	01	1		Standard Timing ID #2	PC Application
29	01	1			
2A	01	1		Standard Timing ID #3	PC Application
2B	01	1			
2C	01	1		Standard Timing ID #4	PC Application
2D	01	1			
2E	01	1		Standard Timing ID #5	PC Application
2F	01	1			
30	01	1		Standard Timing ID #6	PC Application
31	01	1			
32	01	1		Standard Timing ID #7	PC Application
33	01	1			
34	01	1		Standard Timing ID #8	PC Application
35	01	1			

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
36	01	1	First Detailed Timing Descriptor (Preferred)	Pixel Clock	74.25 MHz
37	1D	29			
38	80	128		H Active	1920 pixels
39	18	24		H Blanking	280 pixels
3A	71	113		H Active: H Blanking	
3B	1C	28		V Active	540 lines
3C	16	22		V Blanking	22 lines
3D	20	32		V Active: V Blanking	
3E	58	88		H Sync Offset	88 pixels
3F	2C	44		H Sync Pulse Width	44 pixels
40	25	37		VS Offset: VS Pulse Width	2 lines, 5 lines
41	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
42	20	32		H Image Size	800 mm (lower 8 bits)
43	C2	194		V Image Size	450 mm (lower 8 bits)
44	31	49		H&V Image Size	Upper 4 bits of H & V size
45	00	0		H Border	0 lines
46	00	0		V Border	0 pixels
47	9E	158		Flags	Interlaced, normal display no stereo, digital separate, V-sync polarity is positive, H-sync polarity is positive
48	8C	140	Second Detailed Timing Descriptor (Next Preferred)	Pixel Clock	27 MHz
49	0A	10			
4A	D0	208		H Active	720 pixels
4B	8A	138		H Blanking	138 pixels
4C	20	32		H Active: H Blanking	
4D	E0	224		V Active	480 lines
4E	2D	45		V Blanking	45 lines
4F	10	16		V Active: V Blanking	
50	10	16		H Sync Offset	16 pixels
51	3E	62		H Sync Pulse Width	62 pixels
52	96	150		VS Offset: VS Pulse Width	9 lines, 6 lines
53	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
54	58	88		H Image Size	600 mm (lower 8 bits)
55	C2	194		V Image Size	450 mm (lower 8 bits)
56	21	33		H&V Image Size	Upper 4 bits of H & V size
57	00	0		H Border	0 lines
58	00	0		V Border	0 pixels
59	18	24		Flags	non interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
5A	00	0	Monitor Descriptor Currently Mandatory (Monitor Name)	Flag	
5B	00	0			
5C	00	0		Flag (Reserved)	
5D	FC	252		Data Type Tag	Monitor name type
5E	00	0		Flag	
5F	4D	77		M	
60	59	89		Y	
61	20	32			
62	48	72		H	
63	44	68		D	
64	54	84		T	
65	56	86		V	
66	0A	10			
67	20	32			
68	20	32			
69	20	32			
6A	20	32			
6B	20	32			
6C	00	0	Second Monitor Descriptor Currently Mandatory (range limits, binary coded)	Flag	
6D	00	0			
6E	00	0		Flag (Reserved)	
6F	FD	253		Data Type Tag	Monitor Range limits, binary coded, mandatory block
70	00	0		Flag	
71	3B	59		Min Vertical Rate in Hz	59 Hz
72	3D	61		Max Vertical Rate in Hz	61 Hz
73	0F	15		Min Horizontal Rate in kHz	15 kHz
74	2E	46		Max Horizontal Rate in kHz	46 kHz
75	08	8		Max Supported pixel clock rate in MHz/10	80 MHz
76	00	0		Tag for secondary timing formula, GTF (00h=not used)	No secondary timing formula supported
77	0A	10		Fixed	
78	20	32		Fixed	
79	20	32		Fixed	
7A	20	32		Fixed	
7B	20	32		Fixed	
7C	20	32		Fixed	
7D	20	32		Fixed	

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
7E	01	1	Extension Flag	Number of 128 bytes blocks to follow	
7F	C0	192	Checksum	Checksum	Block 0 sum = FFh&(100h-(1B40h&FFh) = C0h
80	02	2	CEA Extension Header	Tag	Block One
81	03	3		05h 03h (reserved in CEA-861-B)	Revision Number (Start of VESA CEA Block Tag Extension)
82	1A	26		04h, no data in Reserved	Byte Offset
83	71	113		Global Declarations	Content depends on implementation DTV, YCbCr (4:4:4), YCbCr (4:2:2)

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
84	47	71	CEA Data Block Collection Video Data Block	Start of data block collection. Includes Tag Code and length of following data block payload	47h = Video Block (code = 2) and seven bytes of data payload
85	85	133		1st Short Video Descriptor	1920x1080i @ 59.94/60 Hz 16:9 Native Mode
86	02	2		2nd Short Video Descriptor	720x480p 59.94/60 Hz 4:3
87	03	3		3rd Short Video Descriptor	720x480p 59.94/60 Hz 16:9
88	04	4		4th Short Video Descriptor	1280x720p 59.94/60 Hz 16:9
89	06	6		5th Short Video Descriptor	720 (1440)x480i 59.94/60 Hz 4:3
8A	07	7		6th Short Video Descriptor	720 (1440)x480i 59.94/60 Hz 4:3
8B	01	1		7th Short Video Descriptor	640x480p 59.94/60 Hz 4:3
8C	23	35	Audio Data Block	Start of Audio Block	23h = Audio Block (code = 1) and three bytes of data payload.
8D	09	9		Audio Format	Code 1 = Linear PCM (IEC 60985)
8E	07	7		Frequency	07h = 32 kHz, 44.1 kHz, 48 kHz
8F	07	7		Bit Rate	07h = 16 bit, 20 bit, 24 bit
90	83	131	Speaker Allocation Block	Start of Speaker Allocation	83h =Speaker Allocation Data Block (code = 4) and three bytes of data payload.
91	01	1		Speaker Designation	01 = FL / FR (2 Channel Stereo.)
92	00	0		Reserved	Always zero
93	00	0		Reserved	Always zero
94	65	101	Vendor Specific Data Block	Start of Vendor Specific Block	65h = Vendor Specific Block (code = 3) and five bytes of data payload.
95	03	3		24-bit IEEE Registration	HDMI Identifier = 000C03h (The big-endian HDMI-LLC's 24-bit OUI Registration Identifier 0x000C03 is placed into the EDID in little-endian order.)
96	0C	12			
97	00	0			
98	10	16		Components of Source Physical Address	Sink identifies location of source in signal path relative to root display as ABCDh. Example shows input ‘1’ of root display (A=1, B=0, C=0, D=0 or 1000h).
99	00	0			

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
9A	01	1	Third Detailed Timing Descriptor	Pixel Clock	74.25 MHz
9B	1D	29			
9C	00	0		H Active	1280 pixels
9D	72	114		H Blanking	370 pixels
9E	51	81		H Active: H Blanking	
9F	D0	208		V Active	720 lines
A0	1E	30		V Blanking	30 lines
A1	20	32		V Active: V Blanking	
A2	6E	110		H Sync Offset	110 pixels
A3	28	40		H Sync Pulse Width	40 pixels
A4	55	85		VS Offset: VS Pulse Width	Sync Offset = 5 lines, Sync width = 5 lines
A5	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
A6	20	32		H Image Size	800 mm (lower 8 bits)
A7	C2	194		V Image Size	450 mm (lower 8 bits)
A8	31	49		H&V Image Size	Upper 4 bits of H & V size
A9	00	0		H Border	0 pixels
AA	00	0		V Border	0 lines
AB	1E	30		Flags	Non-interlaced, normal display no stereo, digital separate, H and V sync polarity is positive
AC	8C	140	Fourth Detailed Timing Descriptor	Pixel Clock	27 MHz
AD	0A	10			
AE	A0	160		H Active	1440 pixels
AF	14	20		H Blanking	276 pixels
B0	51	81		H Active: H Blanking	
B1	F0	240		V Active	240 lines
B2	16	22		V Blanking	22 lines
B3	00	0		V Active: V Blanking	
B4	26	38		H Sync Offset	38 pixels
B5	7C	124		H Sync Pulse Width	124 pixels
B6	43	67		VS Offset: VS Pulse Width	Sync Offset = 4 lines, Sync width = 3 lines
B7	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
B8	58	88		H Image Size	600 mm (lower 8 bits)
B9	C2	194		V Image Size	450 mm (lower 8 bits)
BA	21	33		H&V Image Size	Upper 4 bits of H & V size
BB	00	0		H Border	0 lines
BC	00	0		V Border	0 pixels
BD	98	152		Flags	interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative,

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
BE	8C	140	Fifth Detailed Timing Descriptor	Pixel Clock	27 MHz
BF	0A	10			
C0	D0	208		H Active	720 pixels
C1	8A	138		H Blanking	138 pixels
C2	20	32		H Active: H Blanking	
C3	E0	224		V Active	480 lines
C4	2D	45		V Blanking	45 lines
C5	10	16		V Active: V Blanking	
C6	10	16		H Sync Offset	16 pixels
C7	3E	62		H Sync Pulse Width	64 pixels
C8	96	150		VS Offset: VS Pulse Width	Sync Offset= 9 lines, Sync width = 6
C9	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
CA	20	32		H Image Size	800 mm (lower 8 bits)
CB	C2	194		V Image Size	450 mm (lower 8 bits)
CC	31	49		H&V Image Size	Upper 4 bits of H&V size
CD	00	0		H Border	0 lines
CE	00	0		V Border	0 pixels
CF	18	24		Flags	Non-interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative,
D0	8C	140	Sixth Detailed Timing Descriptor	Pixel Clock	27 MHz
D1	0A	10			
D2	A0	160		H Active	1440 pixels
D3	14	20		H Blanking	276 pixels
D4	51	81		H Active: H Blanking	
D5	F0	240		V Active	240 lines
D6	16	22		V Blanking	22 lines
D7	00	0		V Active: V Blanking	
D8	26	38		H Sync Offset	38 pixels
D9	7C	124		H Sync Pulse Width	124 pixels
DA	43	67		VS Offset: VS Pulse Width	Sync Offset = 4 lines, Sync Width = 3 lines
DB	00	0		HS Offset: HS Pulse Width: VS Offset: VS Pulse Width	
DC	20	32		H Image Size	800 mm (lower 8 bits)
DD	C2	194		V Image Size	450 mm (lower 8 bits)
DE	31	49		H&V Image Size	Upper 4 bits of H & V size
DF	00	0		H Border	0 lines
E0	00	0		V Border	0 pixels
E1	98	152		Flags	interlaced, normal display no stereo, digital separate, V. and H. sync polarity is negative

Table 87 CEA-861-D EDID Example with Block Tag Extension

Address Hex	Example Data Hex	Dec	Name of Block	Description	Remarks
E2	00	0	Padding Bytes		
E3	00	0			
E4	00	0			
E5	00	0			
E6	00	0			
E7	00	0			
E8	00	0			
E9	00	0			
EA	00	0			
EB	00	0			
EC	00	0			
ED	00	0			
EE	00	0			
EF	00	0			
F0	00	0			
F1	00	0			
F2	00	0			
F3	00	0			
F4	00	0			
F5	00	0			
F6	00	0			
F7	00	0			
F8	00	0			
F9	00	0			
FA	00	0			
FB	00	0			
FC	00	0			
FD	00	0			
FE	00	0			
FF	7A	122	Checksum		Block 1 sum = FFh&(100h-(1686h&FFh) = 7Ah

Table 87 CEA-861-D EDID Example with Block Tag Extension

Annex E [Reserved for Future Use]

Annex F Format Conversion Examples (Informative)

In the example shown below in Figure 40, the DTV Monitor indicates by its EDID data that it has a preferred format of 1080i, and that it can accept 1080i, 720p, 480i, or 480p. In the cases labeled (a), the conversion from the source material (which may be received and decoded as 1080i, 720p, 480i or 480p) to 1080i is happening in the source box. In the other case, labeled (b), the source does no format conversion and delivers the as-decoded format across the interface. Conversion to 1080i is happening in the Display. If the Display indicates it has a single 1080i native format, it may not matter where the conversion takes place. If the Display is multi-scan and indicates the other formats are supported natively also, the best image presentation probably results if the conversion takes place in the Display.

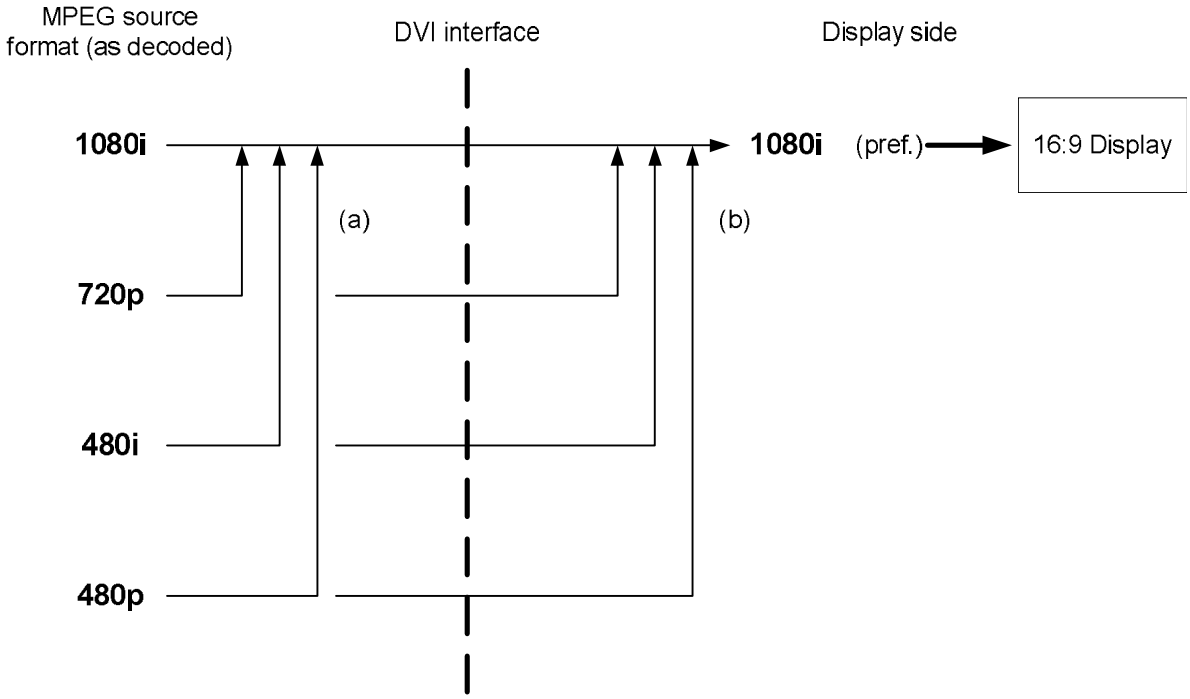


Figure 40 Example of Options for Format Conversion

In the example in Figure 41, the DTV Monitor can once again support 1080i, 720p, 480i, or 480p. In this case, the display is a 1024 by 576 LCD panel so none of these formats is native, and 720p is indicated as being “preferred.” The illustration shows conversions either taking place in the source device, in the Display, or in both. Any conversion performed in the source box is to 720p because 720p is indicated as the preferred format. This is a situation where at least one conversion takes place. In general, format conversions introduce errors and display artifacts. In the optimum system, at most one format conversion should be done between the MPEG-2 decoder and visual presentation.

In Figure 41, MPEG-2 video in 1080i format is decoded, and can be converted (c) into the display’s preferred 720p format. In this case, the Display re-converts 720p into its native 1024x576 LCD format. Alternatively, the 1080i video can be delivered un-converted across the interface (d) where the Display performs one conversion to its native format. The cases marked (e) are similar, in that two conversions result if the source re-formats into 720p before delivering the data across the interface, but just one conversion results if the video is delivered in the same format as it was decoded. These cases illustrate that the best visual presentation may result when the source device transports (passes through) the video to the Display in the same basic format as the decoded MPEG2 stream (assuming the ultimate source is MPEG2).

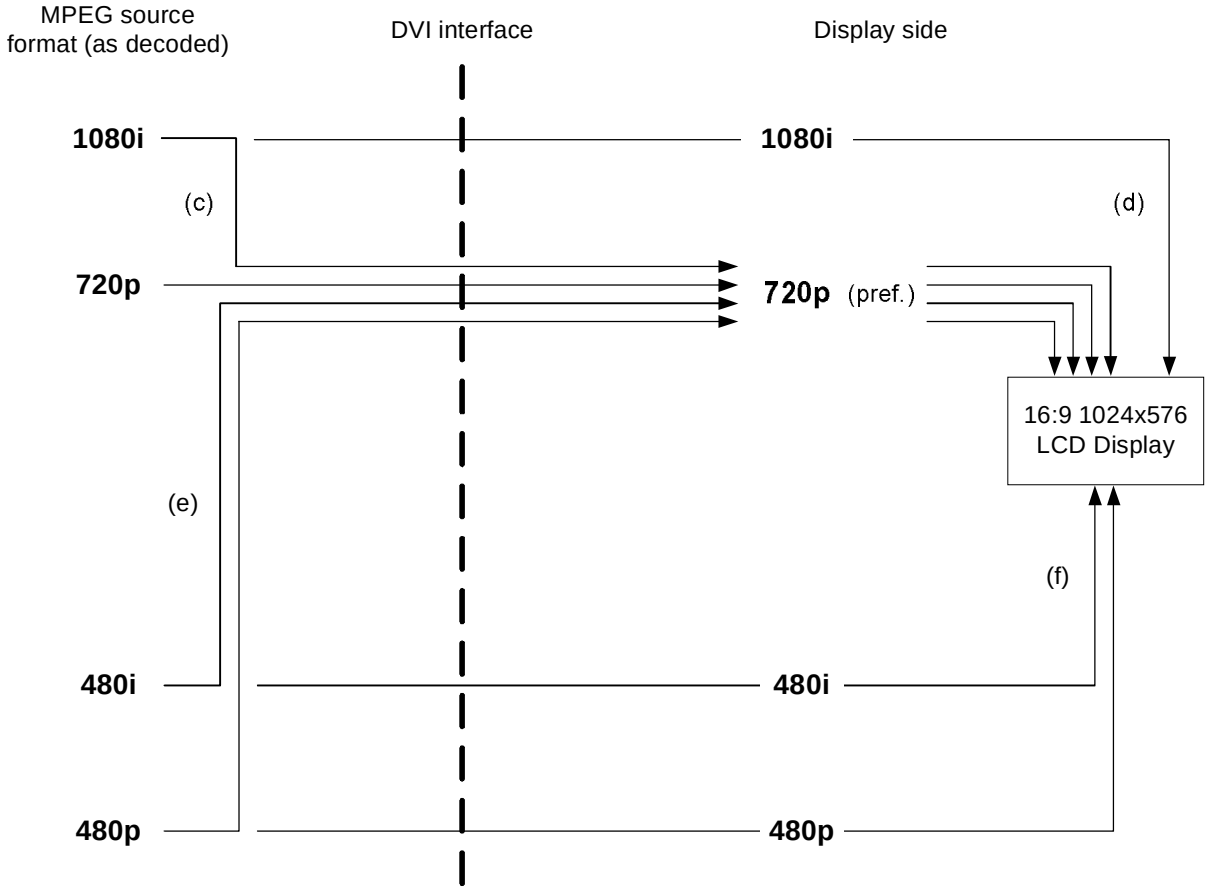


Figure 41 Multiple Conversions Example

Annex G InfoPacket Framework (Informative)

Previous versions of CEA-861-D defined an InfoPacket data structure that could be used to bundle one or more InfoFrames together for transmission across an existing digital interface. The InfoPacket mechanism is not used in any current interface and is not expected to be used in any future interface and so has been deprecated.

11dd00ddddd00ddd0d00d01d1d00d00d00d00d111

Gst}vklx$Gsrwyq ivGipigpuxsrngw$Ewwsgmexmsr$
Tvszmihf{}9MLW3yrhivqmqirwi${ md$GIE$
Rs$vitvshygpmsr$sv9rix{ svomrk$tivq mxih${ mdsyxqmqirwi$jusq9MLW

Wsph3es>HMKMKEP^S R I$JS 2D$PXH 2D$[4868846
Rsx6$sv5Viwepi0544;3;36$9><s74$KQ X

Annex H DVB Active Format Description (Informative)
Annex H is extracted from Annex B of the DVB Guidelines document [26].

Figure 42 illustrates the meanings of the bounding rectangles, gray areas, and white circles as used in Table 88.

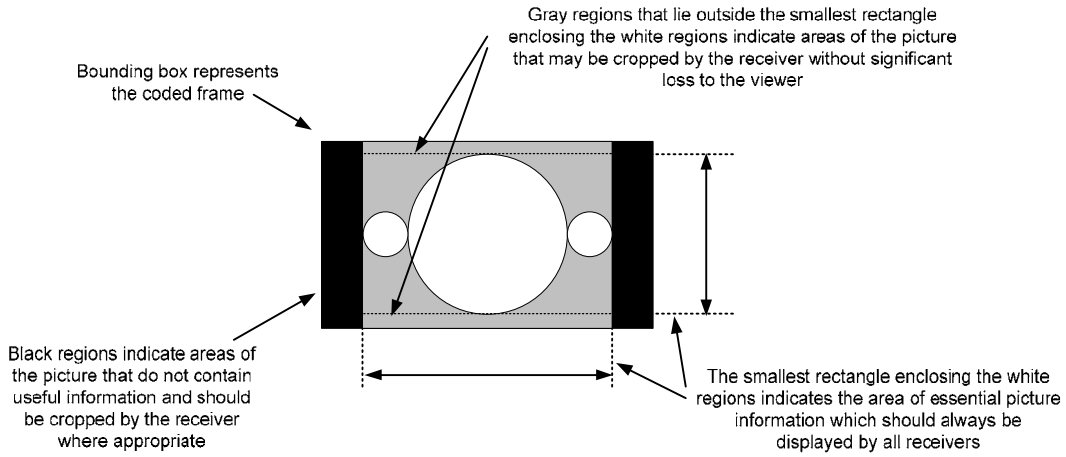


Figure 42 Active Format Illustration

Definitions:

Coded Frame	A picture within a compressed video stream such as MPEG2 that is coded as a single frame or as two fields.
Coded Frame Aspect Ratio	The picture aspect ratio associated with the coded frame of a compressed video stream such as MPEG2. It is either 4:3 or 16:9.

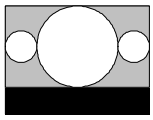
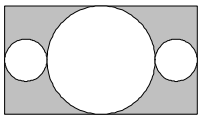
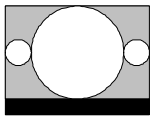
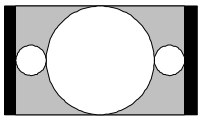
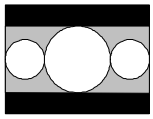
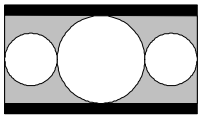
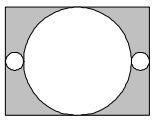
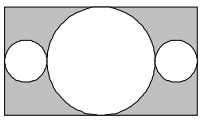
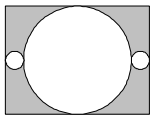
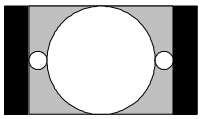
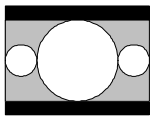
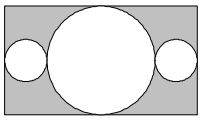
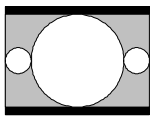
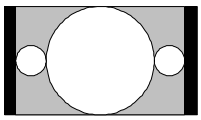
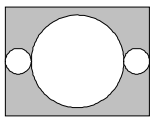
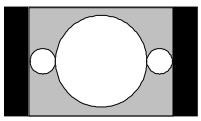
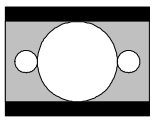
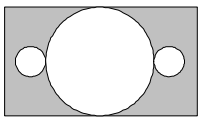
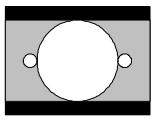
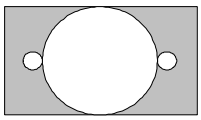
active_format		illustration of described format	
value	description	in 4:3 coded frame	in 16:9 coded frame
0000 - 0001	reserved		
0010	box 16:9 (top)		
0011	box 14:9 (top)		
0100	box > 16:9 (center)		
0101 - 0111	reserved		
1000	As the coded frame		
1001	4:3 (center)		 18
1010	16:9 (center)		
1011	14:9 (center)		
1100	reserved		
1101	4:3 (with shoot & protect 14:9 center)		 18
1110	16:9 (with shoot & protect 14:9 center)		
1111	16:9 (with shoot & protect 4:3 center)		

Table 88 AFD Coding

Annex I Picture Aspect Ratio Conversion Example (Informative)

Figure 43 illustrates a possible problem if both the source and DTV Monitor stretch the video horizontally to fit into a picture with a larger aspect ratio.

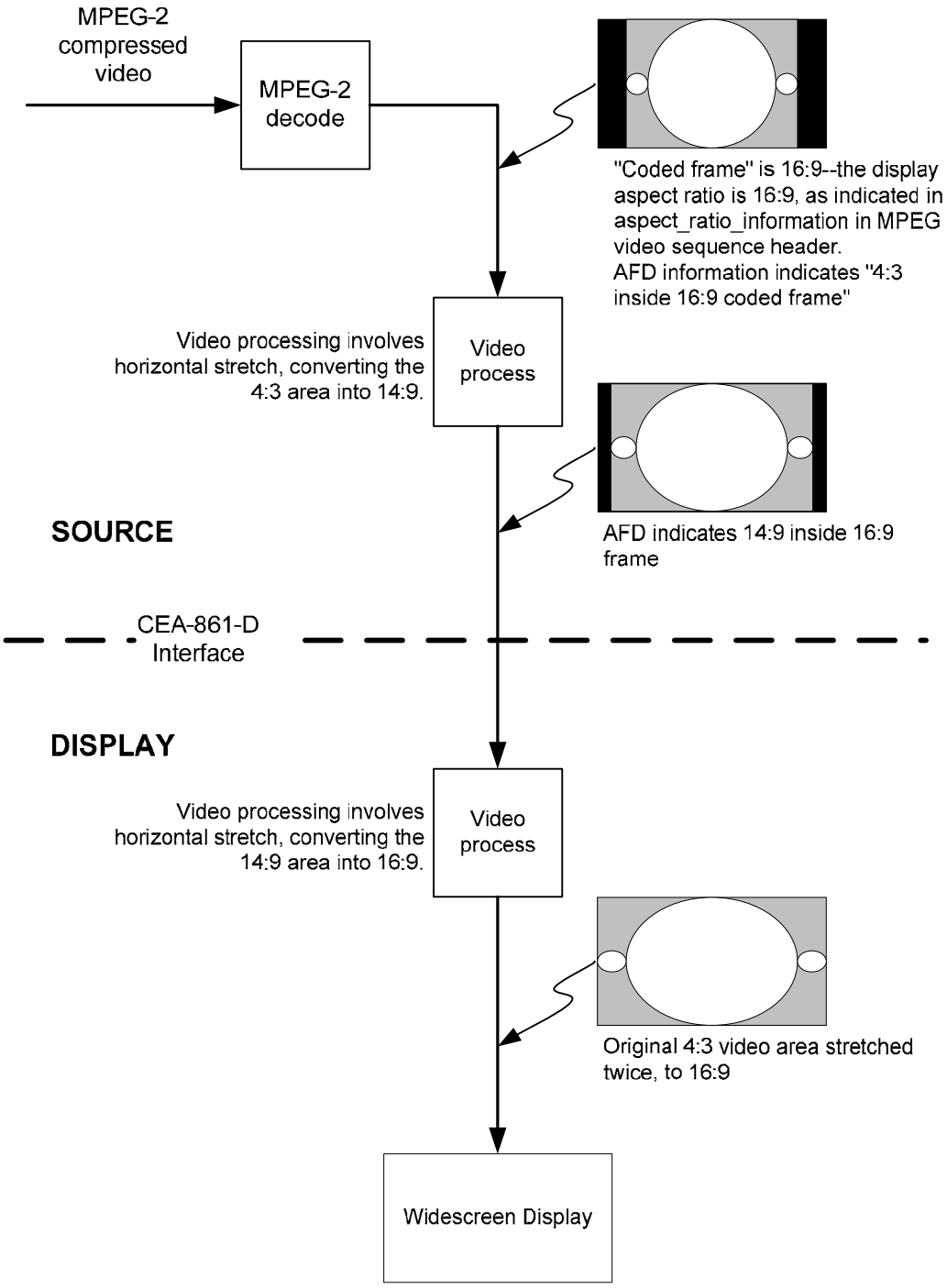


Figure 43 Example of Problem Resulting from Double Stretch

Annex J Typical Audio Applications (Informative)

Table 89 illustrates some typical audio applications.

Audio Type	Application	Constraints	References
LPCM	DVD-Video	Sample Rate = 48 kHz or 96kHz. Sample Size = 16, 20, 24 bits Max Channels = 8	24
LPCM	DVD-Audio	Sample Rate = 44.1, 48, 88.2, 176.4, 192 kHz Sample Size = 16, 20, 24 bits Max Channels = 6	25
One-Bit Audio	Super Audio CD	Sampling Rate = 2.8224 MHz xx (DSD) (=64 x 44.1 kHz) Sample Size = 1 bit Max Channels = 6	42
AC-3	ATSC/SCTE	Sample Rate = 48 kHz Max Bit Rate = 128, 192, 384, 448, 512 kbps	21, 34
AC-3	DVD-Video	Sample Rate = 48 kHz Max Bit Rate = 64, 448 kbps	24
MPEG1 (layers 1 & 2)	MPEG Satellite	Sample Rate = 32, 44.1, 48 kHz Max Bit Rate (layer 1) = 32, 64, 96, 128, 160, 192, 224, 256, 288, 320, 352, 384 kbps Max Bit Rate (layer 2) = 32, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384 kbps	21, 34
MPEG1 (layers 1 & 2)	DVD-Video	Sample Rate = 48 kHz Max Bit Rate = 384 kbps	24, 34
MPEG1 (layers 1 & 2)	DVB	Same as “MPEG Satellite”	26, 34
MPEG2	DVD-Video	Sample Rate = 48 kHz Max Bit Rate = 528 kbps, 912 kbps for main plus extension.	24, 35
MPEG2	DVB	Max Bit Rate of Extension = 682 kbps	26, 35
MP3 (MPEG1 - layer 3)	MP3 Players	Sample Rate = 32, 44.1, 48 kHz Max Bit Rate = 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320 kbps	34
AAC (MPEG4)	Natural Audio Profile	Sampling Rate = 48, 96 kHz	36
DST	Super Audio CD	Sampling Rate = 2.8224 MHz (compressed DSD) (=64 * 44.1 kHz); Sample Size = 1 bit; Number of Channels = 6	37

Table 89 Some Typical Audio Applications

CEA Document Improvement Proposal

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