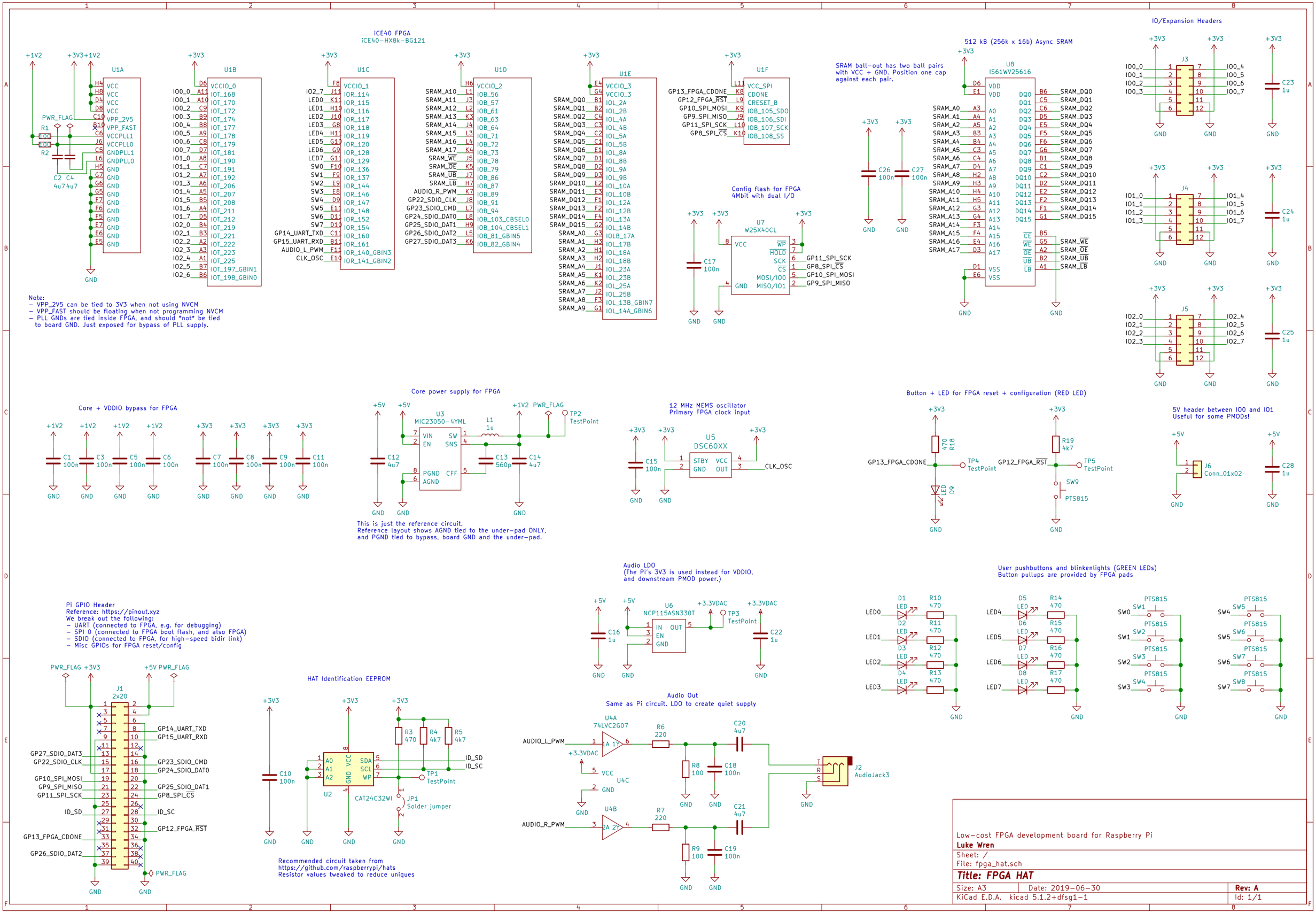
iCE40 FPGA
iCE40-HX8k-BG121
U1A
U1B
U1C
U1D
U1E
U1F
Note:
– VPP_2V5 can be tied to 3V3 when not using NVCM
– VPP_FAST should be floating when not programming NVCM
– PLL GNDs are tied inside FPGA, and should *not* be tied to board GND. Just exposed for bypass of PLL supply.
512 kB (256k x 16b) Async SRAM
U8
IS61WV25616
SRAM ball-out has two ball pairs with VCC + GND. Position one cap against each pair.
IO/Expansion Headers
J3
J4
J5
Config flash for FPGA
4Mbit with dual I/O
U7
W25X40CL
Core + VDDIO bypass for FPGA
Core power supply for FPGA
U3
MIC23050-4YML
This is just the reference circuit.
Reference layout shows AGND tied to the under-pad ONLY,
and PGND tied to bypass, board GND and the under-pad.
12 MHz MEMS oscillator
Primary FPGA clock input
U5
DSC60XX
Button + LED for FPGA reset + configuration (RED LED)
5V header between IO0 and IO1
Useful for some PMODs!
J6
Conn_01x02
Pi GPIO Header
Reference: https://pinout.xyz
We break out the following:
– UART (connected to FPGA, e.g. for debugging)
– SPI 0 (connected to FPGA boot flash, and also FPGA)
– SDIO (connected to FPGA, for high-speed bidir link)
– Misc GPIOs for FPGA reset/config
J1
2x20
HAT Identification EEPROM
U2
CAT24C32WI
JP1
Solder jumper
Recommended circuit taken from
https://github.com/raspberrypi/hats
Resistor values tweaked to reduce uniques
Audio LDO
(The Pi's 3V3 is used instead for VDDIO,
and downstream PMOD power.)
U6
NCP115ASN330T
Audio Out
Same as Pi circuit. LDO to create quiet supply
U4A
74LVC2G07
U4B
U4C
J2
AudioJack3
User pushbuttons and blinkenlights (GREEN LEDs)
Button pullups are provided by FPGA pads
Low-cost FPGA development board for Raspberry Pi
Luke Wren
Sheet: /
File: fpga_hat.sch
Title: FPGA HAT
Size: A3
Date: 2019-06-30
Rev: A
KiCad E.D.A. kicad 5.1.2+dfsg1-1
Id: 1/1