North South University
Department of Electrical & Computer Engineering

Course Code: CSE231L.8

Course Title: Digital Logic Design

Faculty Name: Prof. Dr. M. A. Razzak (Azz)

Project Report of

"Design a Combinational and Sequential Circuit to display "DL2-31D230S12" on a 7 Segment Display including"

Section: 08

Group Number: 06

Submitted To: Jannatul Ferdaous

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Introduction:

This project is about displaying "DL2-31D230S12" with the help of a seven-segment display, including combinational and sequential circuits.

Phase 1: Combinational Part

Truth Table:

Displays	Inputs				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
D	0	0	0	0	1	1	1	1	1	1	0
L	0	0	0	1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0	1	1	0	1
-	0	0	1	1	0	0	0	0	0	0	1
3	0	1	0	0	1	1	1	1	0	0	1
1	0	1	0	1	0	1	1	0	0	0	0
D	0	1	1	0	1	1	1	1	1	1	0
2	0	1	1	1	1	1	0	1	1	0	1
3	1	0	0	0	1	1	1	1	0	0	1
0	1	0	0	1	1	1	1	1	1	1	0
S	1	0	1	0	1	0	1	1	0	1	1
1	1	0	1	1	0	1	1	0	0	0	0
2	1	1	0	0	1	1	0	1	1	0	1
	1	1	0	1	X	X	X	X	X	X	X
	1	1	1	0	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X

Canonical SOP form:

a = A’B’C’D’ + A’B’CD’ + A’BC’D’ + A’BCD’ + A’BCD + AB’C’D’ + AB’C’D + A’BC’D + ABC’D’

b = A’B’C’D’ +A’B’CD’ +A’BC’D’ +A’BC’D +A’BCD’ +A’BCD + AB’C’D’ + AB’C’D + AB’CD + ABC’D’

c = A’B’C’D’ +A’BC’D’ +A’BC’D +A’BCD’+ AB’C’D’ + AB’C’D + AB’CD’+ AB’CD

d = A’B’C’D’ +A’B’C’D +A’B’CD’+ A’BC’D’+A’BCD’ + A’BCD + AB’C’D’ + AB’C’D + AB’CD’

e = A’B’C’D’ +A’B’C’D +A’B’CD’ + A’BCD’ + A’BCD + AB’C’D + ABC’D’

f = A’B’C’D’ +A’B’C’D + A’BCD’ + AB’C’D + AB’CD’

g = A’B’CD’ + A’B’CD + A’BC’D’ + A’BCD + AB’C’D’ + AB’CD’ + ABC’D’

Canonical POS form:

a = (A’+B’+C’+D). (A’+B’+C+D). (A’+B+C’+D). (A+B’+C+D)

b = (A’+B’+C’+D). (A’+B’+C+D). (A+B’+C+D’)

c = (A’+B’+C’+D)(A’+B’+C+D’)(A’+B’+C+D)(A’+B+C+D). (A+B+C’+D’)

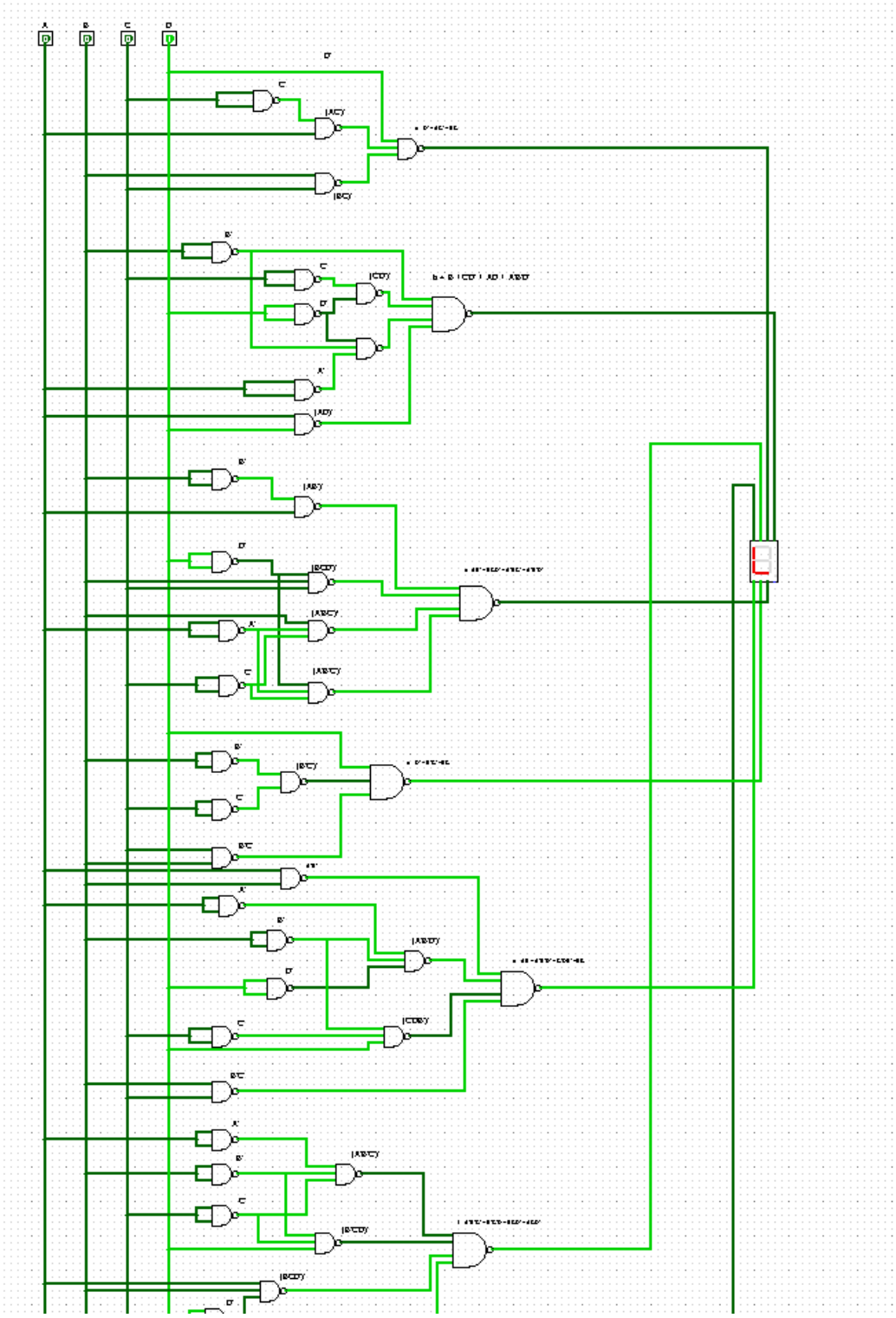
d = (A’+B’+C+D)(A’+B+C’+D)(A+B’+C+D)

e = (A’+B’+C+D)(A’+B+C’+D’)(A’+B+C’+D)(A+B’+C’+D’)(A+B’+C+D’)(A+B’+C+D)

f = (A’+B’+C+D’)(A’+B’+C+D)(A’+B+C’+D’)(A’+B+C’+D)(A’+B+C+D)(A+B’+C’+D’) (A+B’+C+D)(A+B+C’+D’)

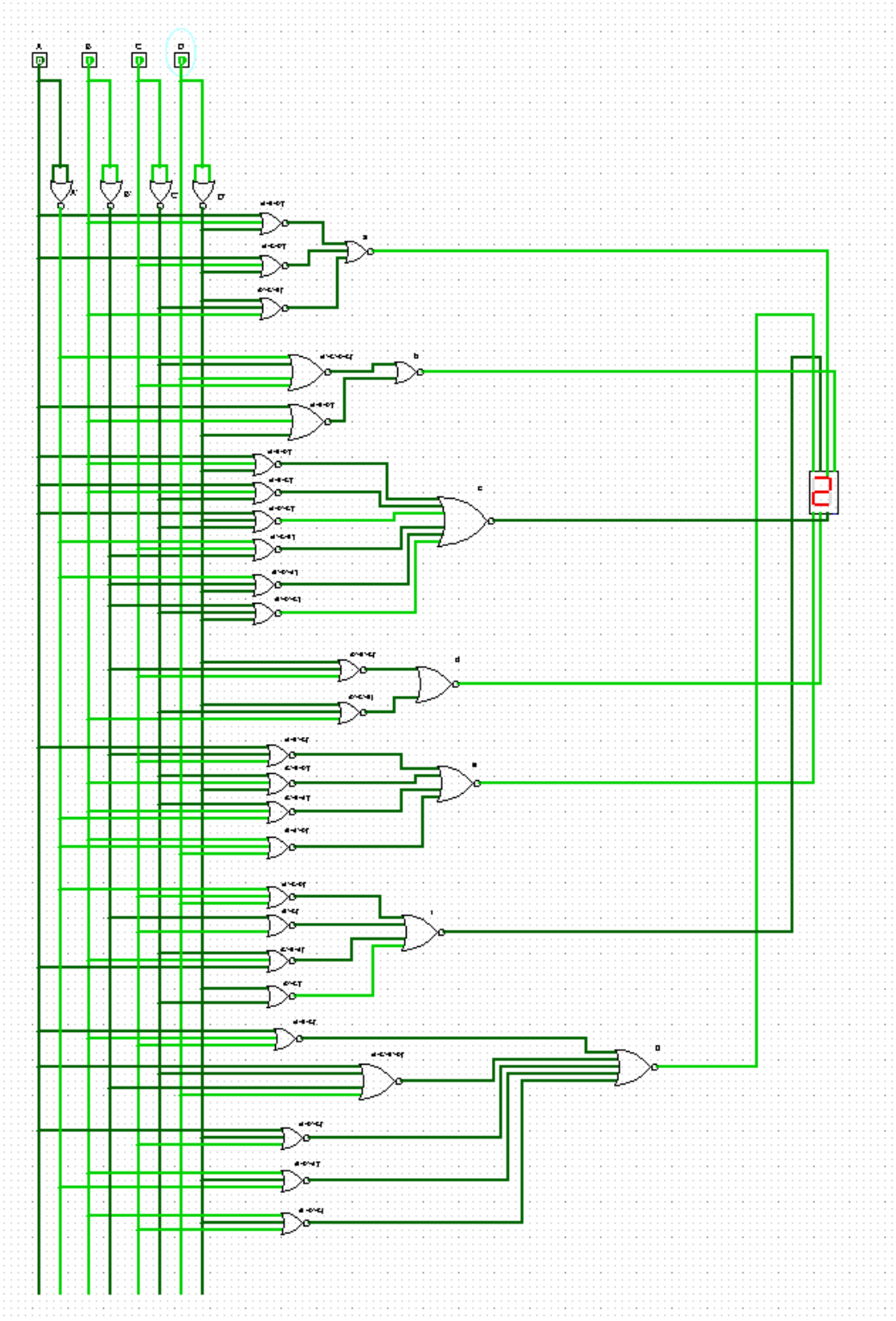
g = (A’+B’+C’+D’)(A’+B’+C’+D)(A’+B+C’+D)(A’+B+C+D’)(A+B’+C’+D)(A+B’+C+D)

Using NAND gates:



0001 Displaying - “L”

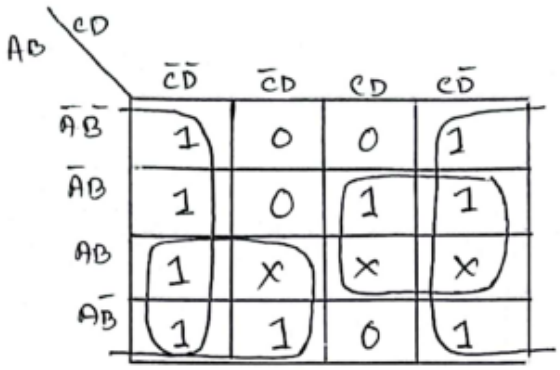
Using NOR gates:



0111 Displaying - “2”

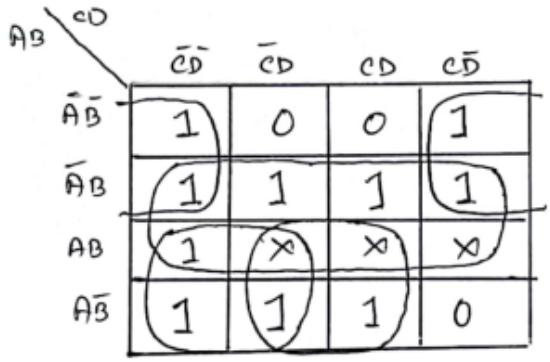
Using SOP:

SOP Kmaps



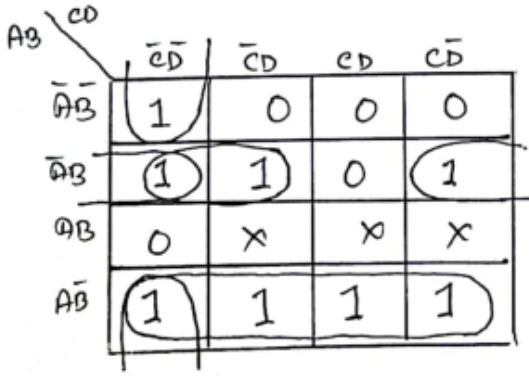
K-Map for "a"

$a = \bar{D} + A\bar{C} + BC$



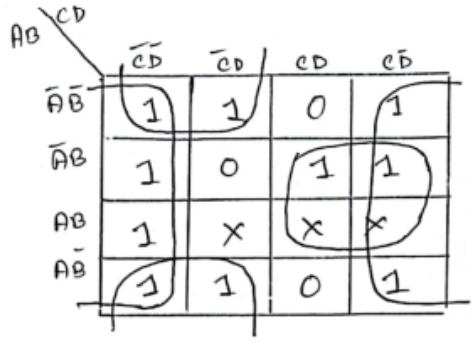
K-Map for "b"

$b = B + \bar{A}\bar{D} + A\bar{C} + AD$



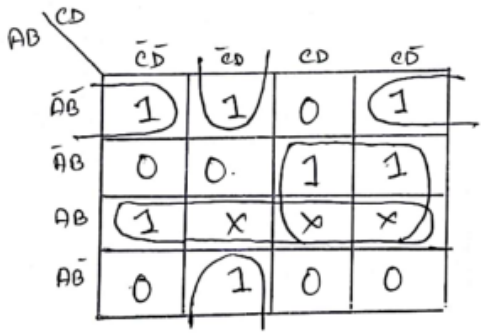
K-Map for "c"

$c = A\bar{B} + \bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C} + \bar{A}B\bar{D}$



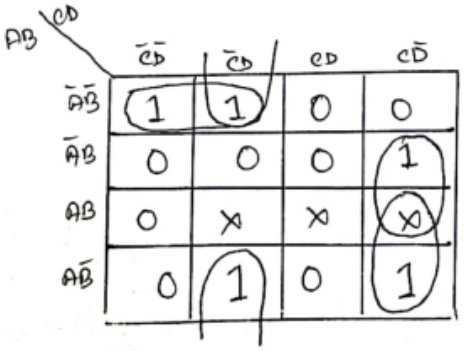
K-Map for "d"

$d = \bar{D} + BC + \bar{B}\bar{C}$



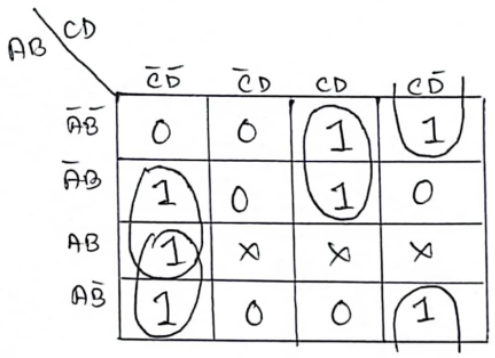
K-Map for "e"

$e = BC + AB + \bar{B}\bar{C}D + \bar{A}\bar{B}\bar{D}$



K-Map for "f"

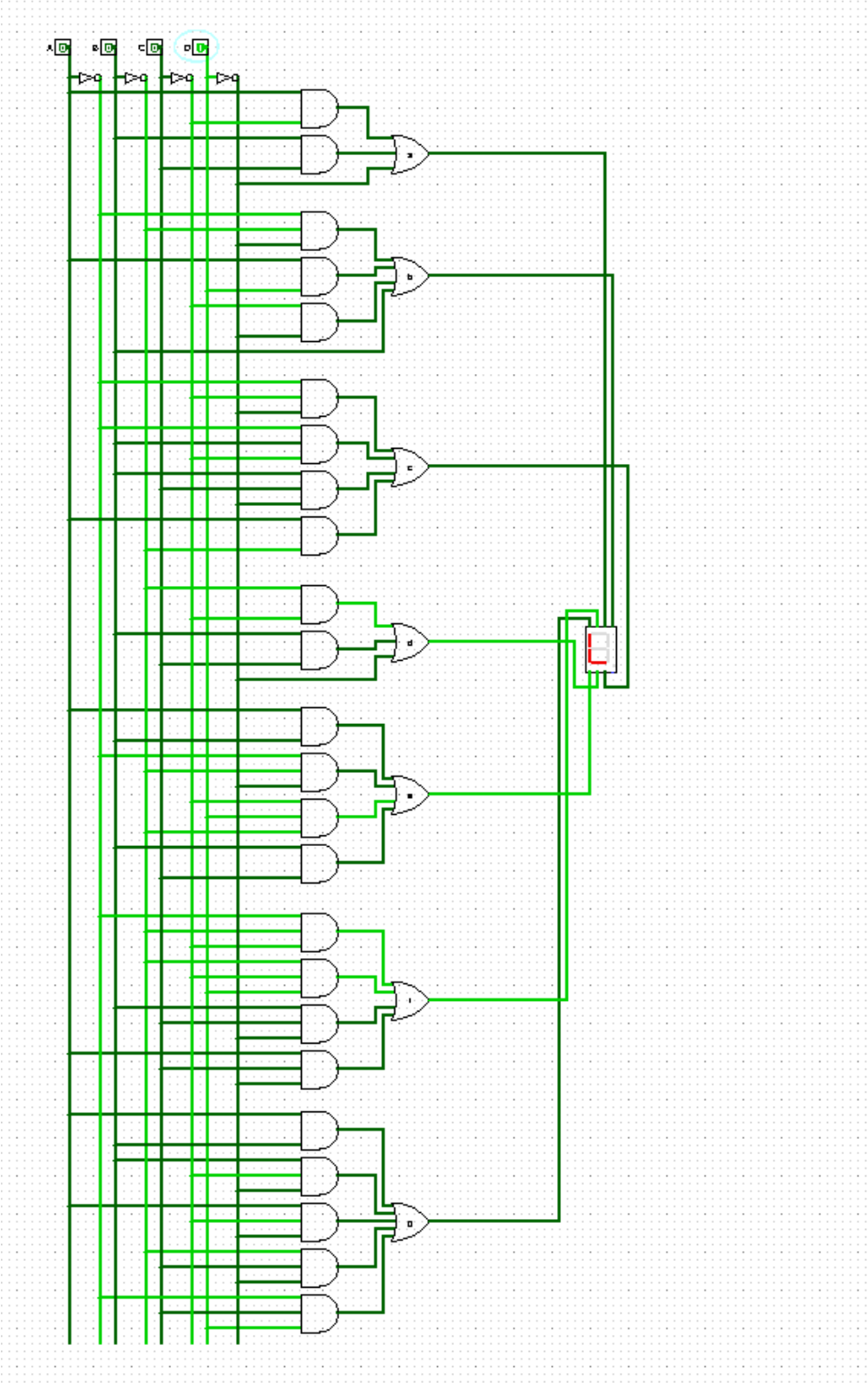
$f = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}D + BC\bar{D} + AC\bar{D}$



K-Map for "g"

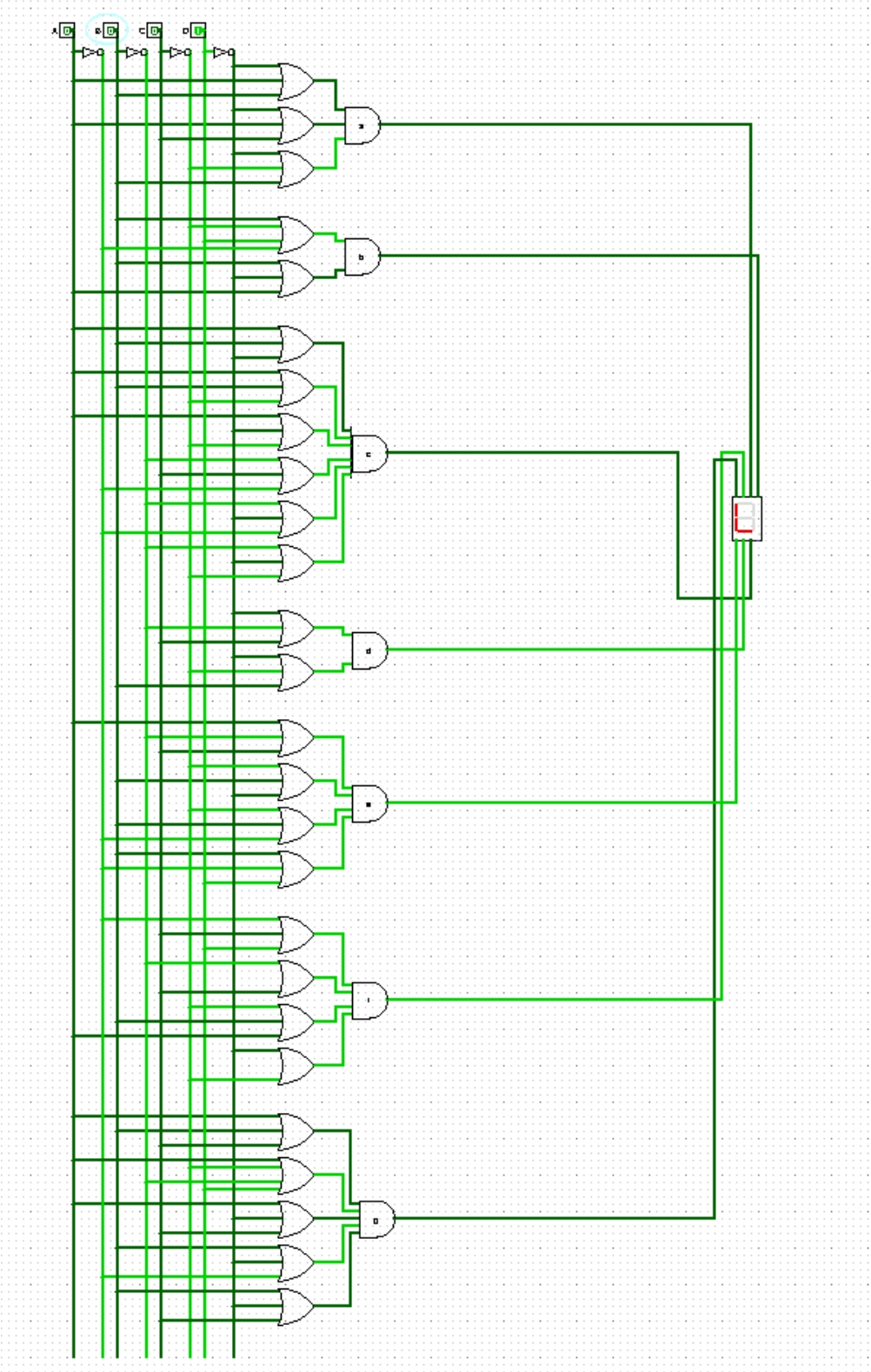
$g = \bar{B}C\bar{D} + \bar{A}CD + B\bar{C}\bar{D} + A\bar{C}\bar{D}$.

SOP Simulation



0001 Displaying - “L”

POS Simulation



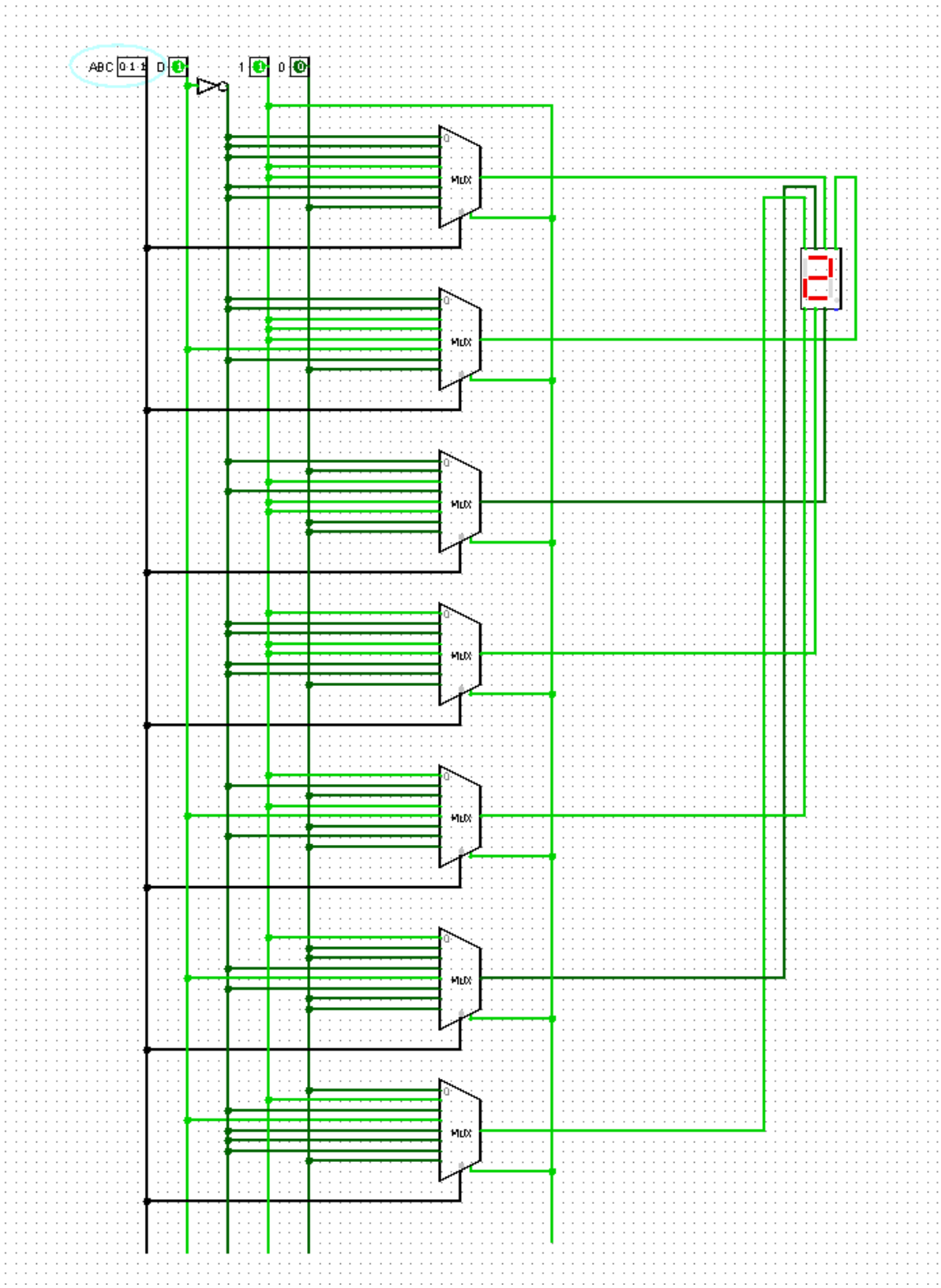
0001 Displaying - “L”

MUX

16 to 1 mux using 8 to 1 mux

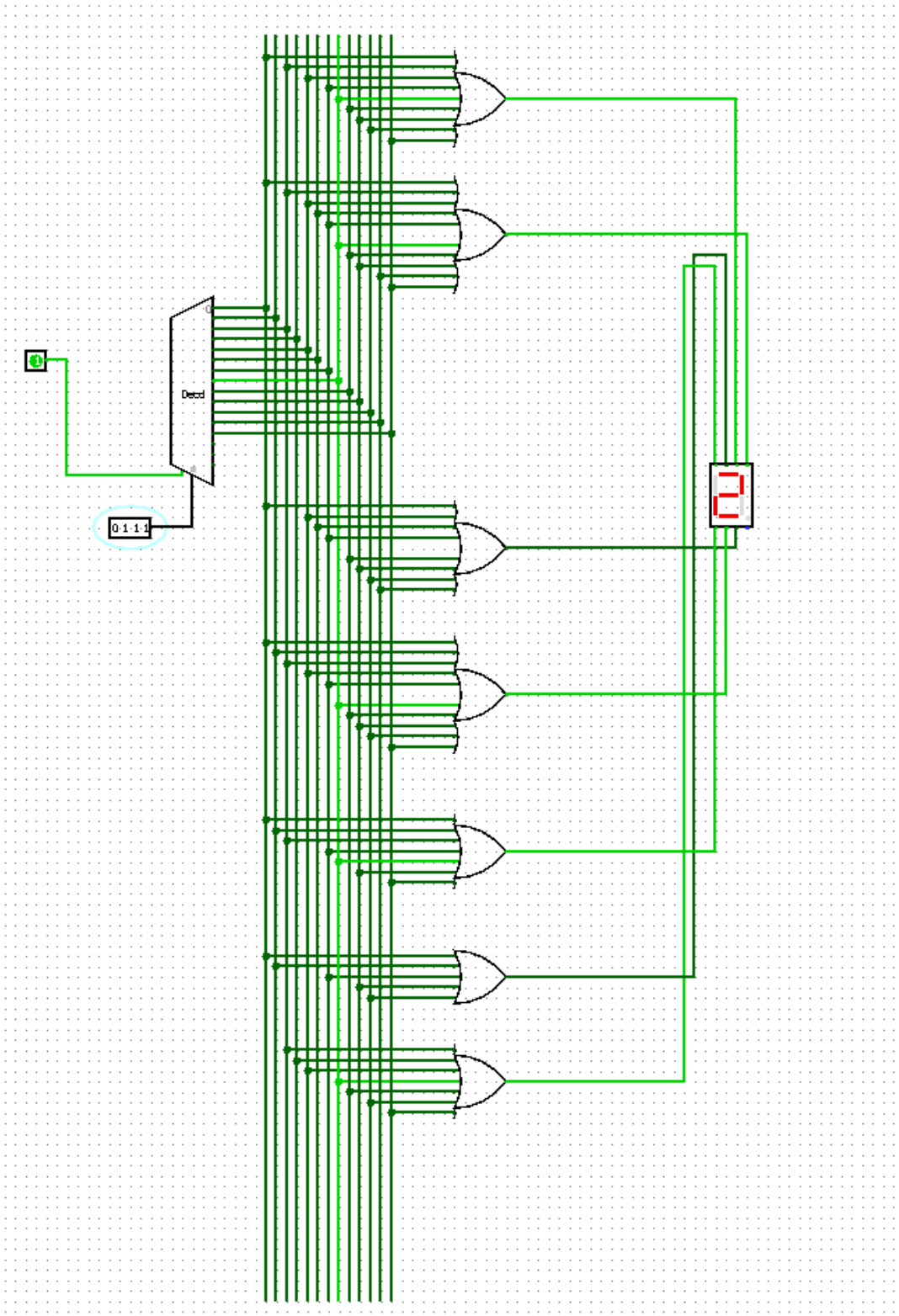
A	B	C	D	F	a		b		c		d		e		f		g	
0	0	0	0	D	1		1		1		1		1		1		0	
0	0	0	1	L	0	$I_0=D'$	0	$I_0=D'$	0	$I_0=D'$	1	$I_0=1$	1	$I_0=1$	1	$I_0=1$	0	$I_0=0$
0	0	1	0	2	1		1		0		1		1		0		1	
0	0	1	1	-	0	$I_1=D'$	0	$I_1=D'$	0	$I_1=0$	0	$I_1=D'$	0	$I_1=D'$	0	$I_1=0$	1	$I_1=1$
0	1	0	0	3	1		1		1		1		0		0		1	
0	1	0	1	1	0	$I_2=D'$	1	$I_2=1$	1	$I_2=1$	0	$I_2=D'$	0	$I_2=0$	0	$I_2=0$	0	$I_2=D'$
0	1	1	0	D	1		1		1		1		1		1		0	
0	1	1	1	2	1	$I_3=1$	1	$I_3=1$	0	$I_3=D'$	1	$I_3=1$	1	$I_3=1$	0	$I_3=D'$	1	$I_3=D$
1	0	0	0	3	1		1		1		1		0		0		1	
1	0	0	1	0	1	$I_4=1$	1	$I_4=1$	1	$I_4=1$	1	$I_4=1$	1	$I_4=D$	1	$I_4=D$	0	$I_4=D'$
1	0	1	0	S	1		0		1		1		0		1		1	
1	0	1	1	1	0	$I_5=D'$	1	$I_5=D$	1	$I_5=1$	0	$I_5=D'$	0	$I_5=0$	0	$I_5=D'$	0	$I_5=D'$
1	1	0	0	2	1		1		0		1		1		0		1	
1	1	0	1		0	$I_6=D'$	0	$I_6=D'$	0	$I_6=0$	0	$I_6=D'$	0	$I_6=D'$	0	$I_6=0$	0	$I_6=D'$

MUX Simulation



0111 Displaying - “2”

Decoder Simulation



0111 Displaying - “2”

Budget for the project (Without Flip Flop):

As we are using Multiplexer to display “DL2-31D230S12”, we require

1-Cathode 7-Segment Display = 12 Tk
7-IC 74HC151N (8:1 MUX) = 224 Tk
1-IC NOT 7404 (2-input NOT) = 26 TK
2 Breadboard = 260 TK
Wires = 90 TK

Total Cost = 612 TK