North South University
Department of Electrical & Computer Engineering

Course Code: CSE231L.8

Course Title: Digital Logic Design

Faculty Name: Prof. Dr. M. A. Razzak (Azz)

Project Report of

"Design a Combinational and Sequential Circuit to display "DL2-31D230S12" on a 7 Segment Display including"

Section: 08

Group Number: 06

Submitted To: Jannatul Ferdaous

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Introduction:

This project is about displaying "DL2-31D230S12" with the help of a seven-segment display, including combinational and sequential circuits.

Phase 1: Combinational Part

Truth Table:

Displays	Inputs				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
D	0	0	0	0	1	1	1	1	1	1	0
L	0	0	0	1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0	1	1	0	1
-	0	0	1	1	0	0	0	0	0	0	1
3	0	1	0	0	1	1	1	1	0	0	1
1	0	1	0	1	0	1	1	0	0	0	0
D	0	1	1	0	1	1	1	1	1	1	0
2	0	1	1	1	1	1	0	1	1	0	1
3	1	0	0	0	1	1	1	1	0	0	1
0	1	0	0	1	1	1	1	1	1	1	0
S	1	0	1	0	1	0	1	1	0	1	1
1	1	0	1	1	0	1	1	0	0	0	0
2	1	1	0	0	1	1	0	1	1	0	1
	1	1	0	1	X	X	X	X	X	X	X
	1	1	1	0	X	X	X	X	X	X	X
	1	1	1	1	X	X	X	X	X	X	X

Canonical SOP form:

a = A’B’C’D’ + A’B’CD’ + A’BC’D’ + A’BCD’ + A’BCD + AB’C’D’ + AB’C’D + A’BC’D + ABC’D’

b = A’B’C’D’ +A’B’CD’ +A’BC’D’ +A’BC’D +A’BCD’ +A’BCD + AB’C’D’ + AB’C’D + AB’CD + ABC’D’

c = A’B’C’D’ +A’BC’D’ +A’BC’D +A’BCD’+ AB’C’D’ + AB’C’D + AB’CD’+ AB’CD

d = A’B’C’D’ +A’B’C’D +A’B’CD’+ A’BC’D’+A’BCD’ + A’BCD + AB’C’D’ + AB’C’D + AB’CD’

e = A’B’C’D’ +A’B’C’D +A’B’CD’ + A’BCD’ + A’BCD + AB’C’D + ABC’D’

f = A’B’C’D’ +A’B’C’D + A’BCD’ + AB’C’D + AB’CD’

g = A’B’CD’ + A’B’CD + A’BC’D’ + A’BCD + AB’C’D’ + AB’CD’ + ABC’D’

Canonical POS form:

a = (A’+B’+C’+D). (A’+B’+C+D). (A’+B+C’+D). (A+B’+C+D)

b = (A’+B’+C’+D). (A’+B’+C+D). (A+B’+C+D’)

c = (A’+B’+C’+D)(A’+B’+C+D’)(A’+B’+C+D)(A’+B+C+D). (A+B+C’+D’)

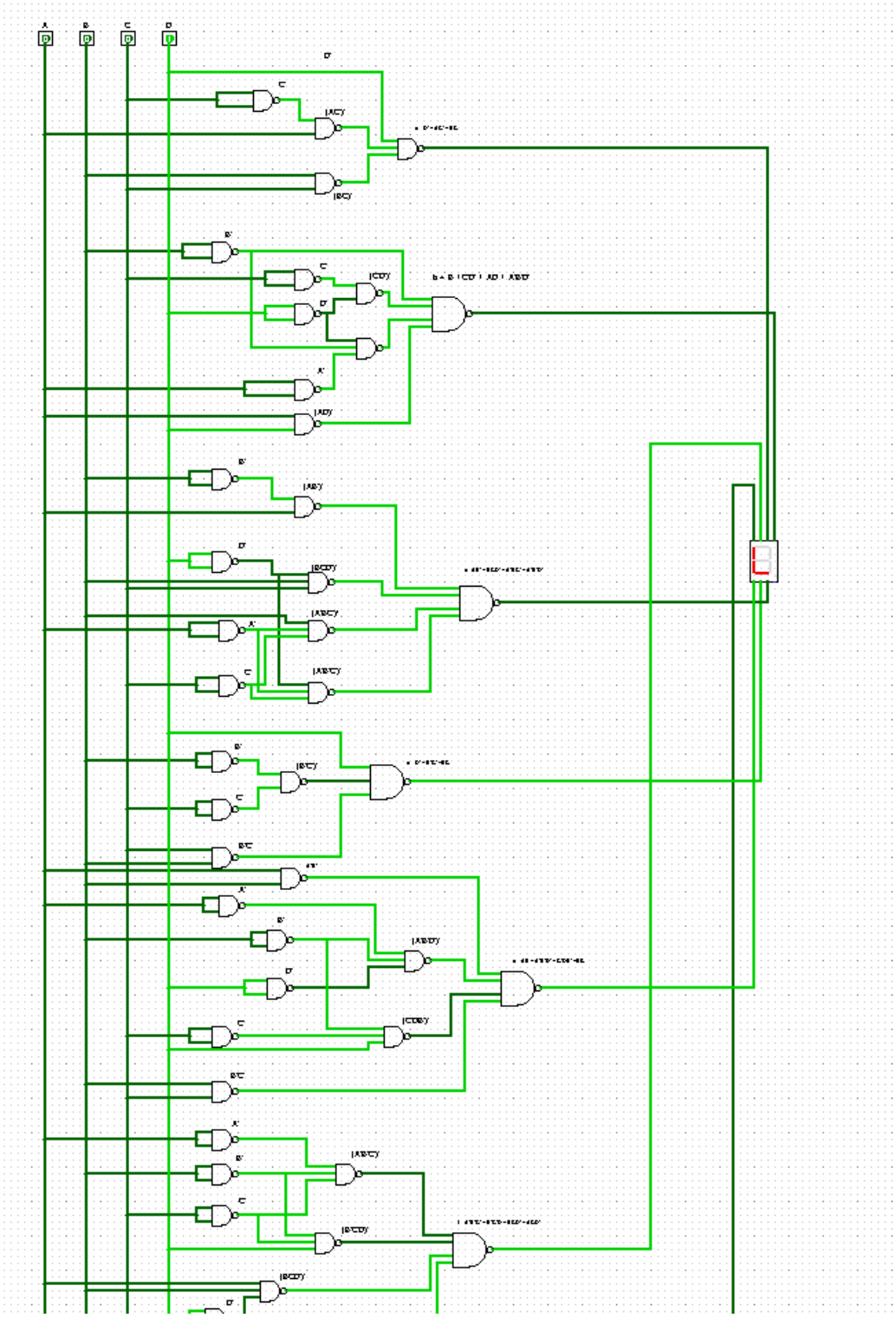
d = (A’+B’+C+D)(A’+B+C’+D)(A+B’+C+D)

e = (A’+B’+C+D)(A’+B+C’+D’)(A’+B+C’+D)(A+B’+C’+D’)(A+B’+C+D’)(A+B’+C+D)

f = (A’+B’+C+D’)(A’+B’+C+D)(A’+B+C’+D’)(A’+B+C’+D)(A’+B+C+D)(A+B’+C’+D’) (A+B’+C+D)(A+B+C’+D’)

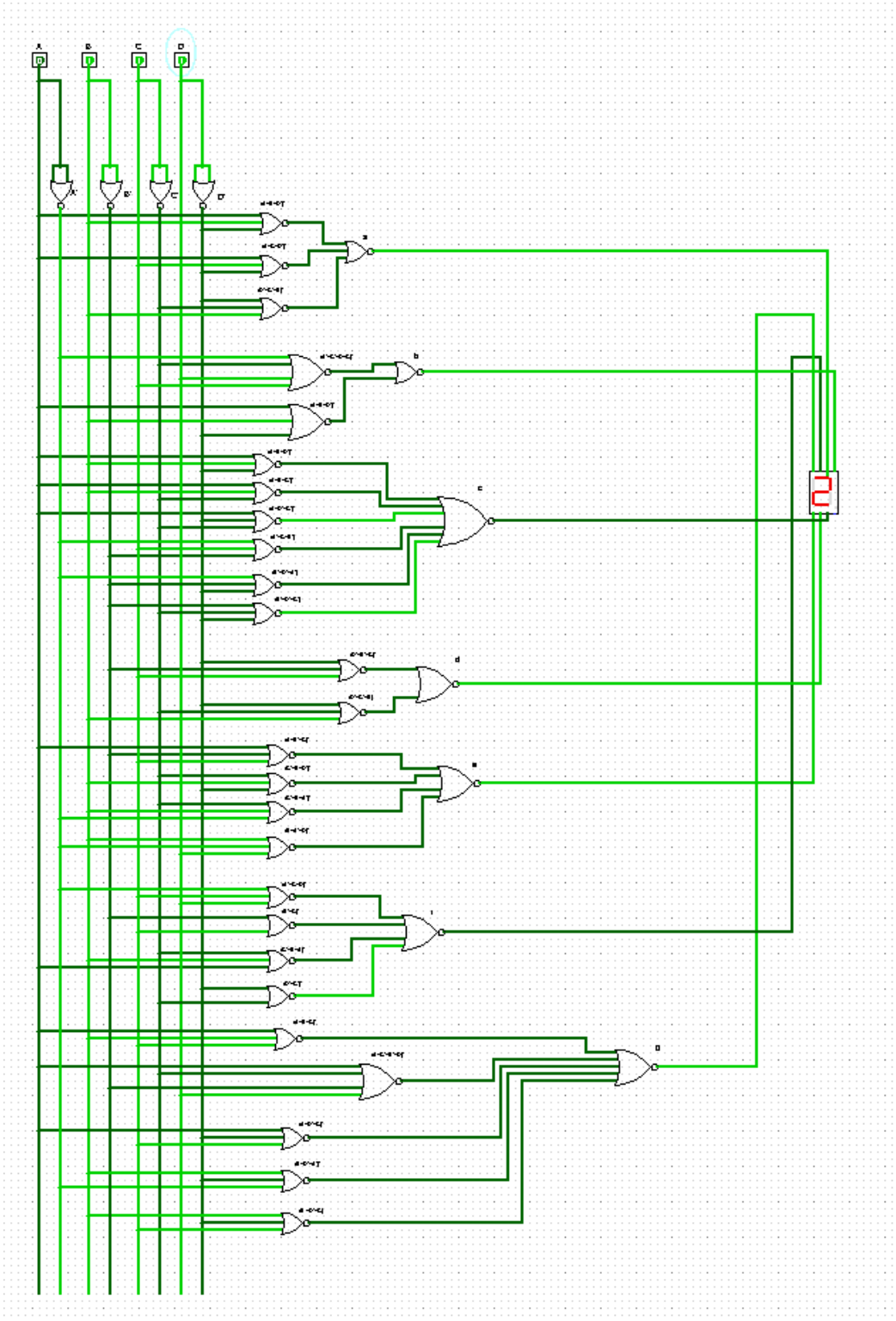
g = (A’+B’+C’+D’)(A’+B’+C’+D)(A’+B+C’+D)(A’+B+C+D’)(A+B’+C’+D)(A+B’+C+D)

Using NAND gates:



0001 Displaying - “L”

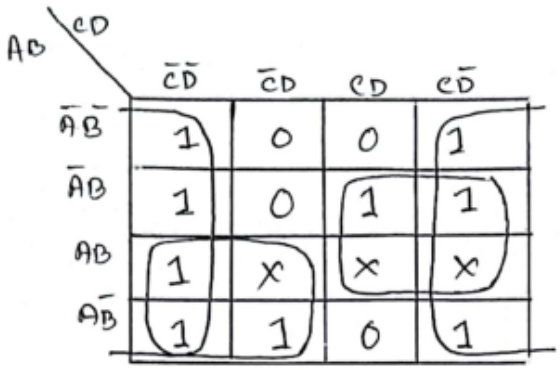
Using NOR gates:



0111 Displaying - “2”

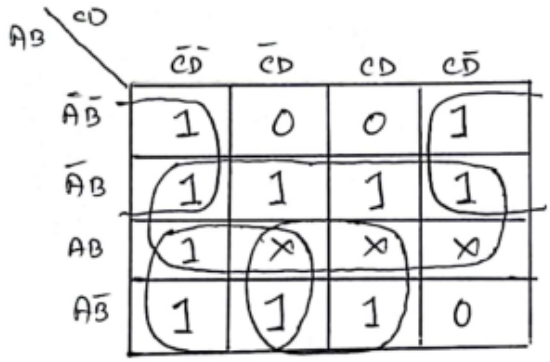
Using SOP:

SOP Kmaps



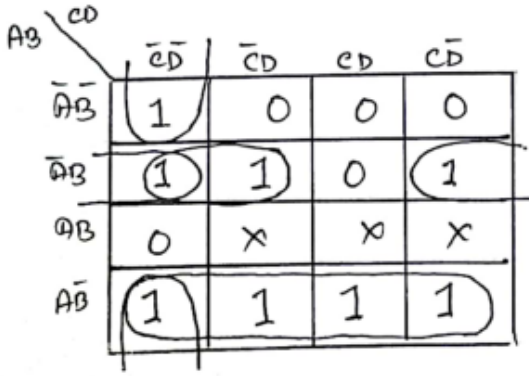
K-Map for "a"

$a = \bar{D} + A\bar{C} + BC$



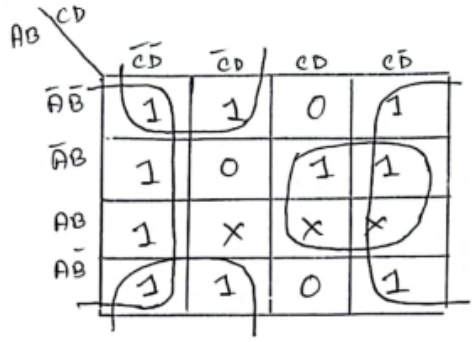
K-Map for "b"

$b = B + \bar{A}\bar{D} + A\bar{C} + AD$



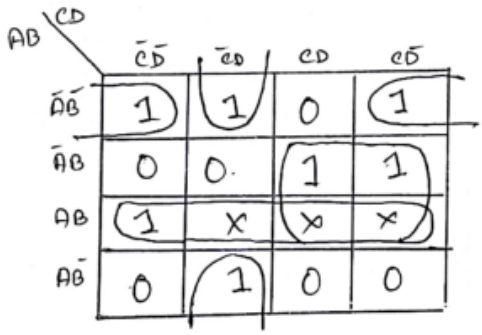
K-Map for "c"

$c = A\bar{B} + \bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C} + \bar{A}B\bar{D}$



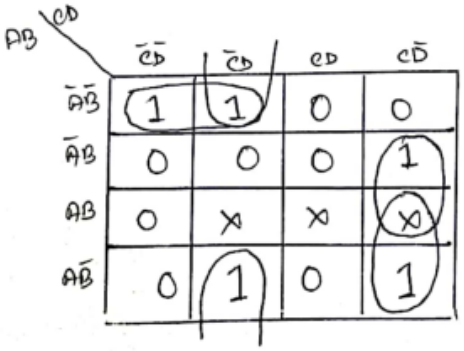
K-Map for "d"

$d = \bar{D} + BC + \bar{B}\bar{C}$



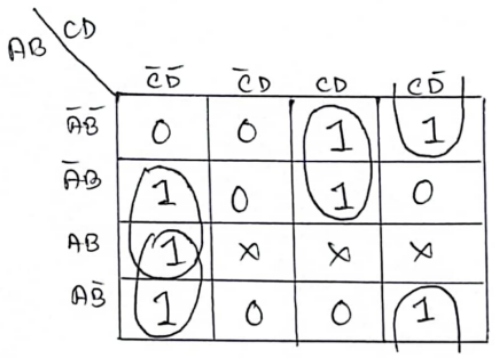
K-Map for "e"

$e = BC + AB + \bar{B}\bar{C}D + \bar{A}\bar{B}\bar{D}$



K-Map for "f"

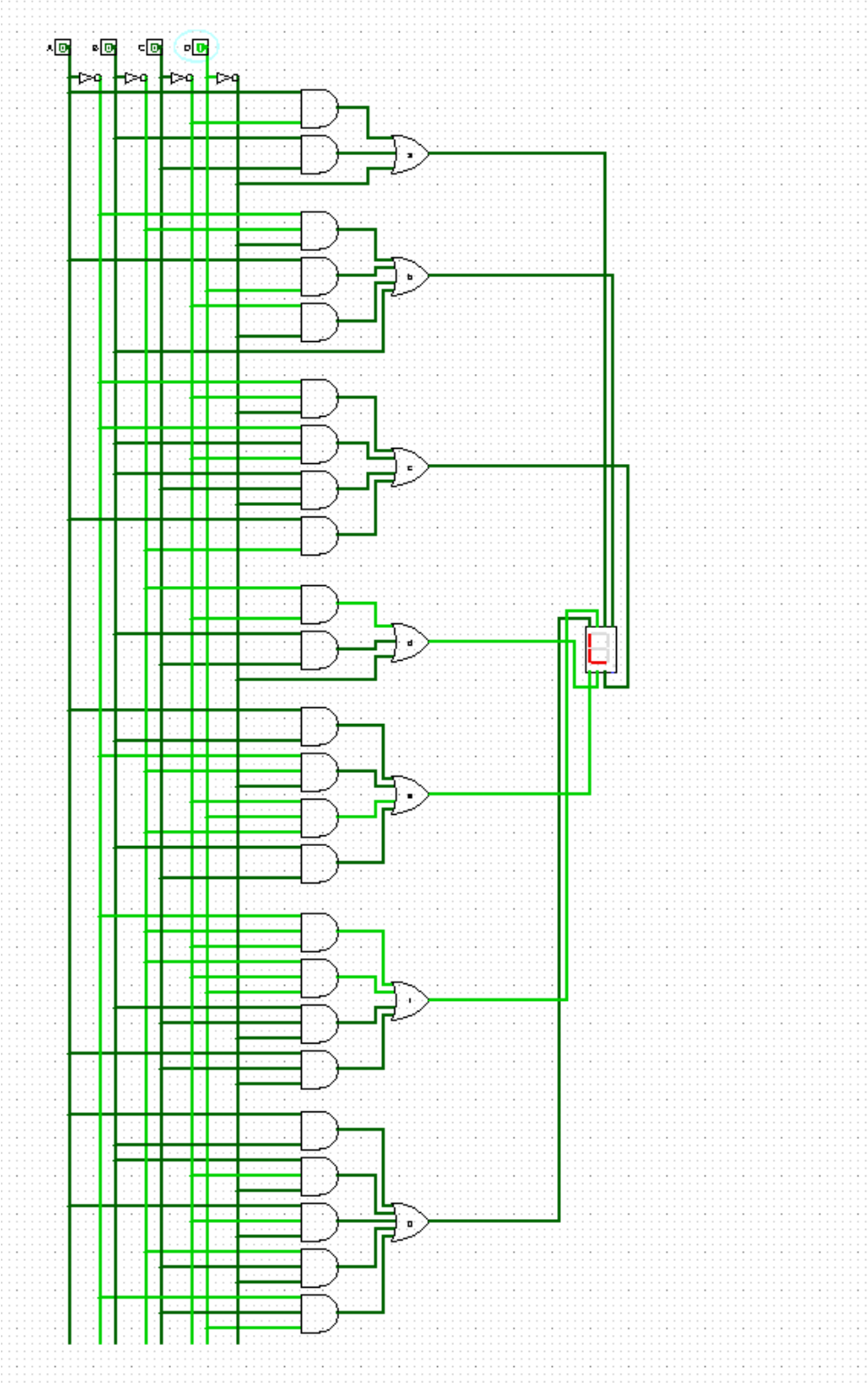
$f = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}D + BC\bar{D} + AC\bar{D}$



K-Map for "g"

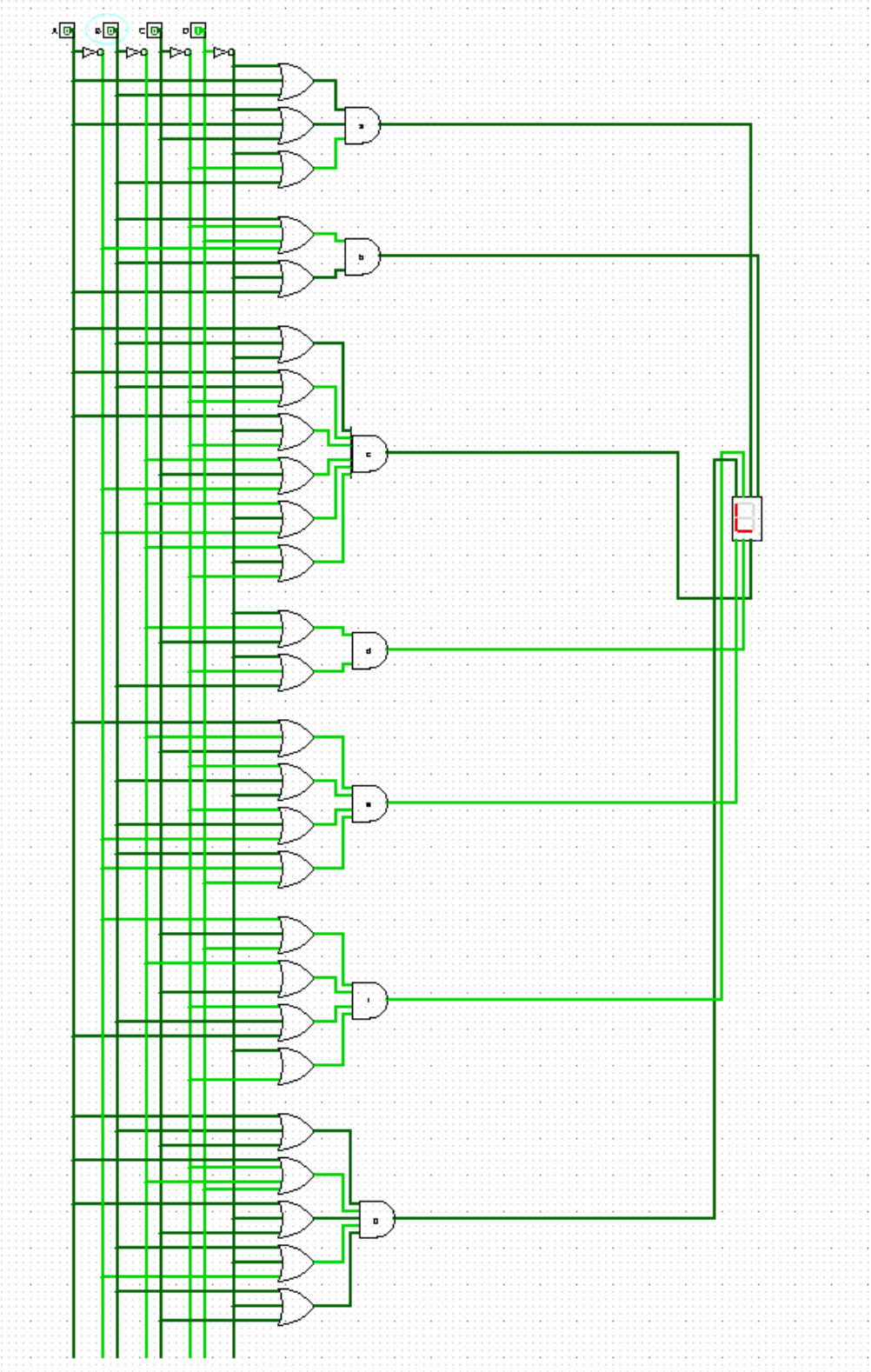
$g = \bar{B}C\bar{D} + \bar{A}CD + B\bar{C}\bar{D} + A\bar{C}\bar{D}$.

SOP Simulation



0001 Displaying - “L”

POS Simulation



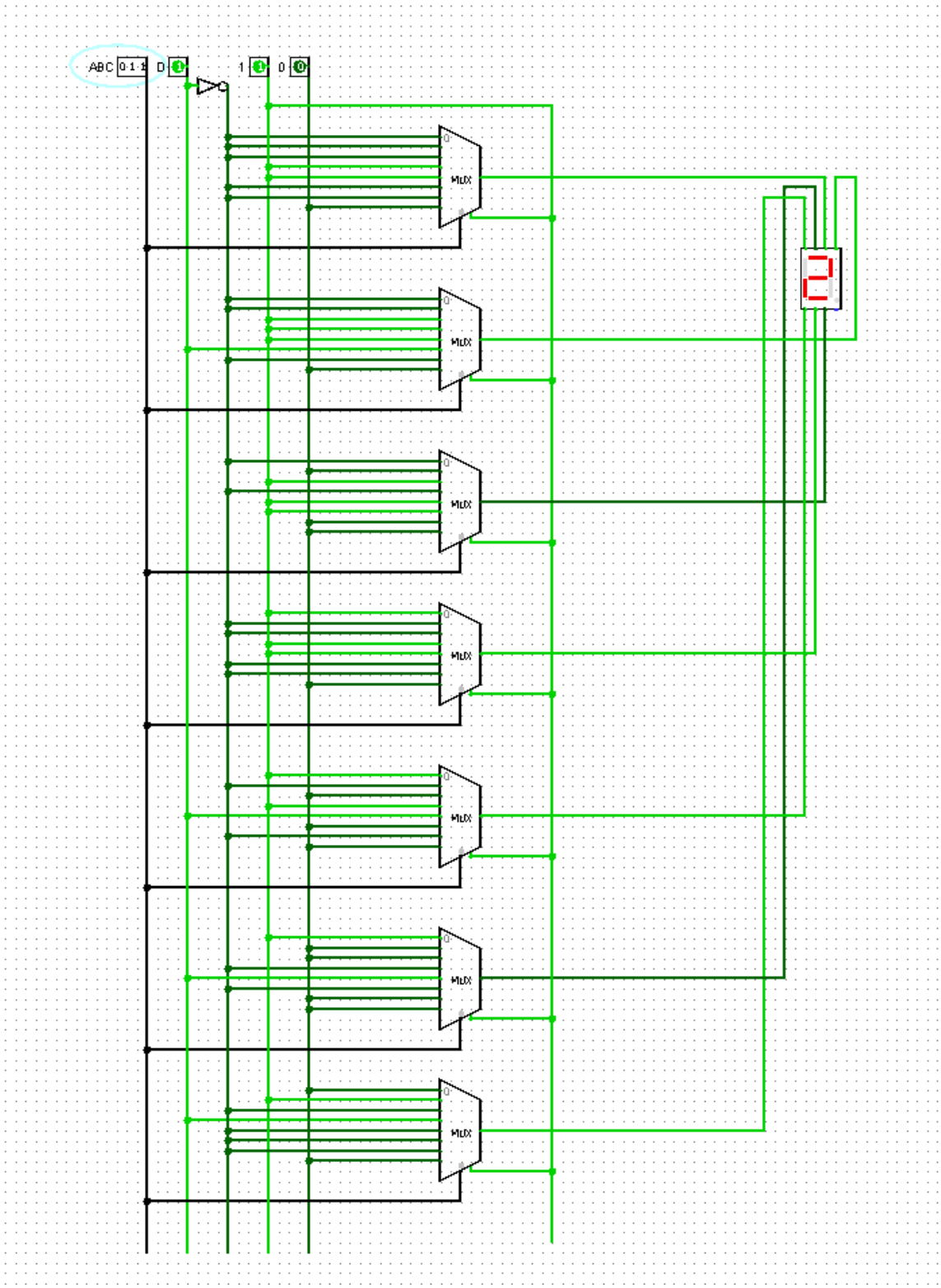
0001 Displaying - “L”

MUX

16 to 1 mux using 8 to 1 mux

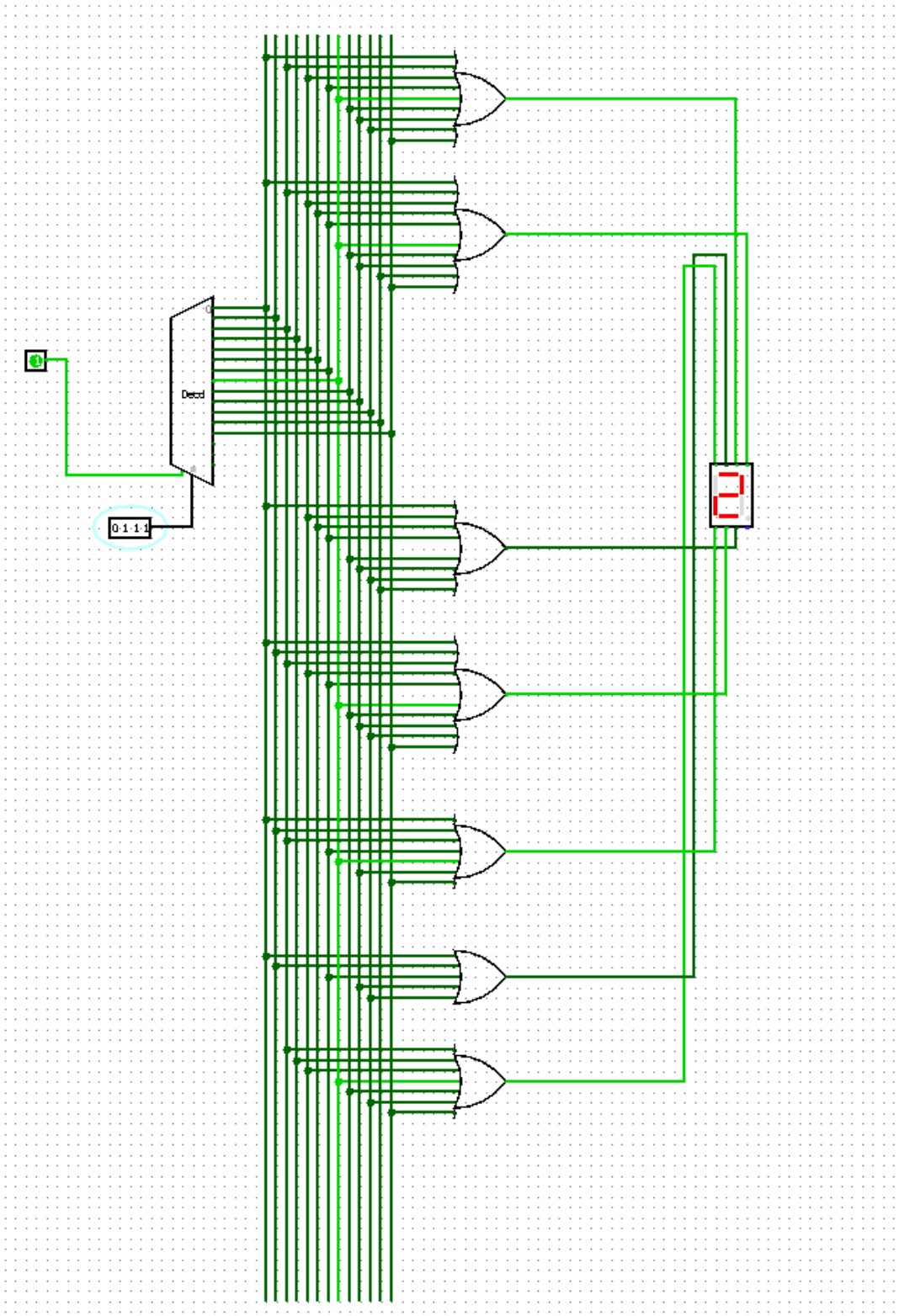
A	B	C	D	F	a		b		c		d		e		f		g	
0	0	0	0	D	1		1		1		1		1		1		0	
0	0	0	1	L	0	$I_0=D'$	0	$I_0=D'$	0	$I_0=D'$	1	$I_0=1$	1	$I_0=1$	1	$I_0=1$	0	$I_0=0$
0	0	1	0	2	1		1		0		1		1		0		1	
0	0	1	1	-	0	$I_1=D'$	0	$I_1=D'$	0	$I_1=0$	0	$I_1=D'$	0	$I_1=D'$	0	$I_1=0$	1	$I_1=1$
0	1	0	0	3	1		1		1		1		0		0		1	
0	1	0	1	1	0	$I_2=D'$	1	$I_2=1$	1	$I_2=1$	0	$I_2=D'$	0	$I_2=0$	0	$I_2=0$	0	$I_2=D'$
0	1	1	0	D	1		1		1		1		1		1		0	
0	1	1	1	2	1	$I_3=1$	1	$I_3=1$	0	$I_3=D'$	1	$I_3=1$	1	$I_3=1$	0	$I_3=D'$	1	$I_3=D$
1	0	0	0	3	1		1		1		1		0		0		1	
1	0	0	1	0	1	$I_4=1$	1	$I_4=1$	1	$I_4=1$	1	$I_4=1$	1	$I_4=D$	1	$I_4=D$	0	$I_4=D'$
1	0	1	0	S	1		0		1		1		0		1		1	
1	0	1	1	1	0	$I_5=D'$	1	$I_5=D$	1	$I_5=1$	0	$I_5=D'$	0	$I_5=0$	0	$I_5=D'$	0	$I_5=D'$
1	1	0	0	2	1		1		0		1		1		0		1	
1	1	0	1		0	$I_6=D'$	0	$I_6=D'$	0	$I_6=0$	0	$I_6=D'$	0	$I_6=D'$	0	$I_6=0$	0	$I_6=D'$

MUX Simulation



0111 Displaying - “2”

Decoder Simulation



0111 Displaying - “2”

Budget for the project (Without Flip Flop):

As we are using Multiplexer to display “DL2-31D230S12”, we require

1-Cathode 7-Segment Display = 12 Tk
7-IC 74HC151N (8:1 MUX) = 224 Tk
1-IC NOT 7404 (2-input NOT) = 26 TK
2 Breadboard = 260 TK
Wires = 90 TK

Total Cost = 612 TK

Phase 02: Sequential part

J-K Flip Flop

Truth Table:

J-K Inputs								Clk	Outputs			
JA	**KA**	**JB**	**KB**	**JC**	**KC**	**JD**	**KD**		**QA***	**QB***	**QC***	**QD***
X	X	X	X	X	X	X	X	0	0	0	0	0
0	X	0	X	0	X	1	X	1	0	0	0	1
0	X	0	X	1	X	X	1	1	0	0	1	0
0	X	0	X	X	0	1	X	1	0	0	1	1
0	X	1	X	X	1	X	1	1	0	1	0	0
0	X	X	0	0	X	1	X	1	0	1	0	1
0	X	X	0	1	X	X	1	1	0	1	1	0
0	X	X	0	X	0	1	X	1	0	1	1	1
1	X	X	1	X	1	X	1	1	1	0	0	0
X	0	0	X	0	X	1	X	1	1	0	0	1
X	0	0	X	1	X	X	1	1	1	0	1	0
X	0	0	X	X	0	1	X	1	1	0	1	1
X	0	1	X	X	1	X	1	1	1	1	0	0
X	1	X	1	0	X	0	X	1	0	0	0	0

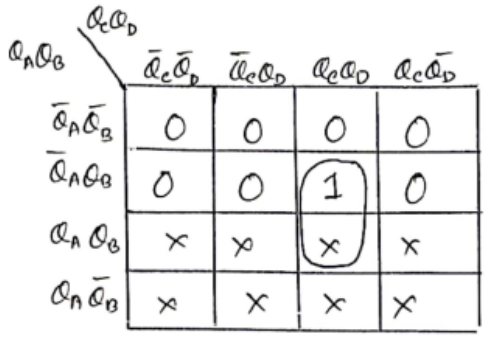
Characteristic Table:

Present				J-K Inputs								Next			
QA	**QB**	**QC**	**QD**	**JA**	**KA**	**JB**	**KB**	**JC**	**KC**	**JD**	**KD**	**QA***	**QB***	**QC***	**QD***
0	0	0	0	0	X	0	X	0	X	1	X	0	0	0	1
0	0	0	1	0	X	0	X	1	X	X	1	0	0	1	0
0	0	1	0	0	X	0	X	X	0	1	X	0	0	1	1
0	0	1	1	0	X	1	X	X	1	X	1	0	1	0	0
0	1	0	0	0	X	X	0	0	X	1	X	0	1	0	1
0	1	0	1	0	X	X	0	1	X	X	1	0	1	1	0
0	1	1	0	0	X	X	0	X	0	1	X	0	1	1	1
0	1	1	1	1	X	X	1	X	1	X	1	1	0	0	0
1	0	0	0	X	0	0	X	0	X	1	X	1	0	0	1
1	0	0	1	X	0	0	X	1	X	X	1	1	0	1	0
1	0	1	0	X	0	0	X	X	0	1	X	1	0	1	1
1	0	1	1	X	0	1	X	X	1	X	1	1	1	0	0
1	1	0	0	X	1	X	1	0	X	0	X	0	0	0	0

Excitation Table:

Present				Next				J-K Inputs							
QA	**QB**	**QC**	**QD**	**QA***	**QB***	**QC***	**QD***	**JA**	**KA**	**JB**	**KB**	**JC**	**KC**	**JD**	**KD**
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	1	0	1	0	X	0	0	X	1	X	X	1
1	0	1	0	1	0	1	1	X	0	0	X	X	0	1	X
1	0	1	1	1	1	0	0	X	0	1	X	X	1	X	1
1	1	0	0	0	0	0	0	X	1	X	1	0	X	0	X

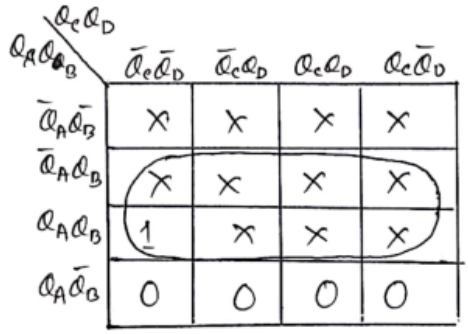
K-Maps for J-K flip flop:



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	0	0
$\bar{Q}_A Q_B$	0	0	1	0
$Q_A Q_B$	×	×	×	×
$Q_A\bar{Q}_B$	×	×	×	×

K-Map for J_A

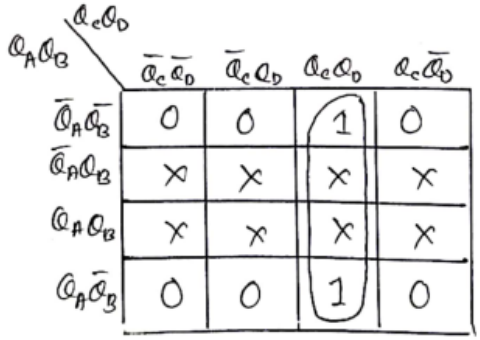
$J_A = Q_B Q_C Q_D$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	×	×	×	×
$\bar{Q}_A Q_B$	×	×	×	×
$Q_A Q_B$	1	×	×	×
$Q_A\bar{Q}_B$	0	0	0	0

K-Map for K_A

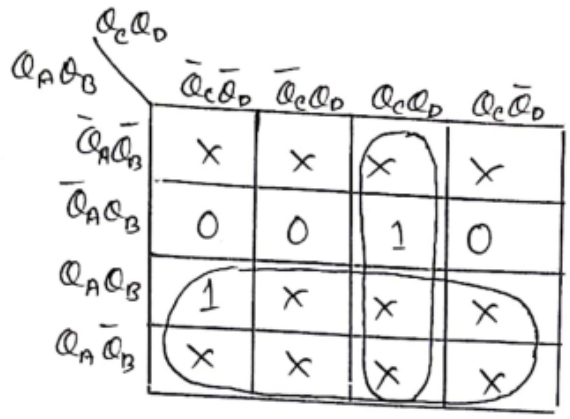
$K_A = Q_B$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	1	0
$\bar{Q}_A Q_B$	×	×	×	×
$Q_A Q_B$	×	×	×	×
$Q_A\bar{Q}_B$	0	0	1	0

K-Map for J_B

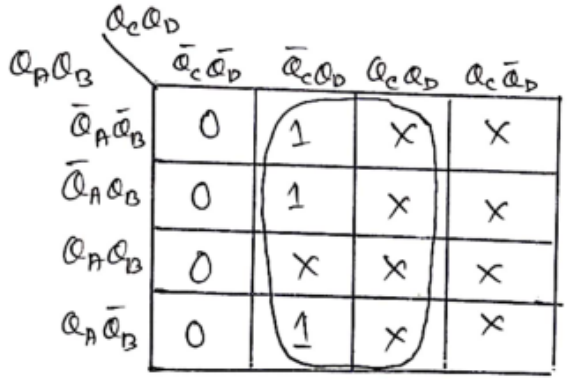
$J_B = Q_C Q_D.$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	X	X	X	X
$\bar{Q}_A Q_B$	0	0	1	0
$Q_A Q_B$	1	X	X	X
$Q_A\bar{Q}_B$	X	X	X	X

K-Map for K_B

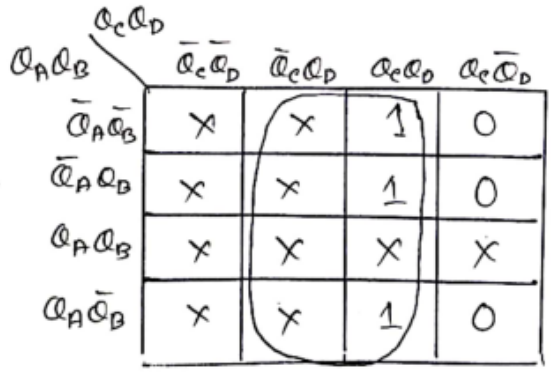
$K_B = Q_C Q_D + Q_A$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	1	X	X
$\bar{Q}_A Q_B$	0	1	X	X
$Q_A Q_B$	0	X	X	X
$Q_A\bar{Q}_B$	0	1	X	X

K-Map for J_C

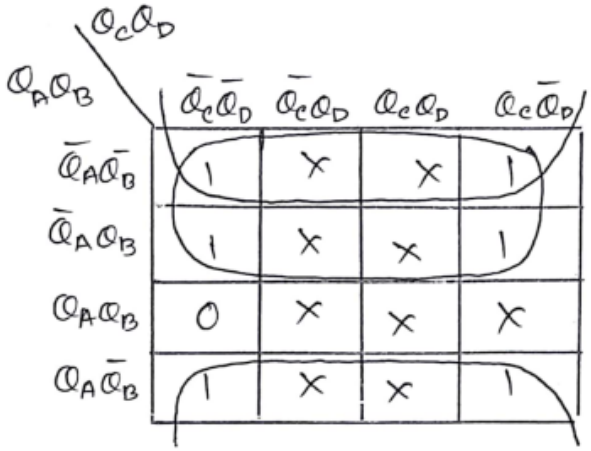
$J_C = Q_D$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	X	X	1	0
$\bar{Q}_A Q_B$	X	X	1	0
$Q_A Q_B$	X	X	X	X
$Q_A\bar{Q}_B$	X	X	1	0

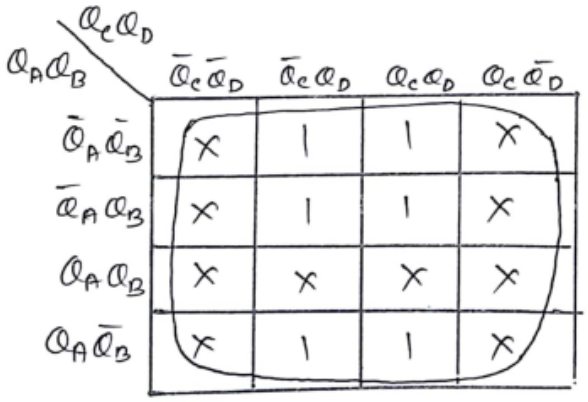
K-Map for K_C

$K_C = Q_D$



K-Map for J_D

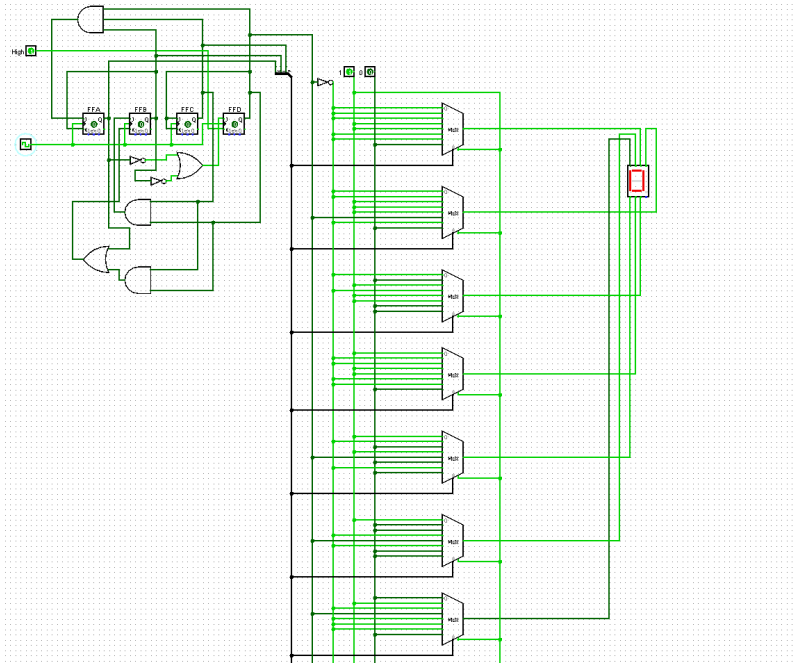
$J_D = \bar{Q}_A + \bar{Q}_B$



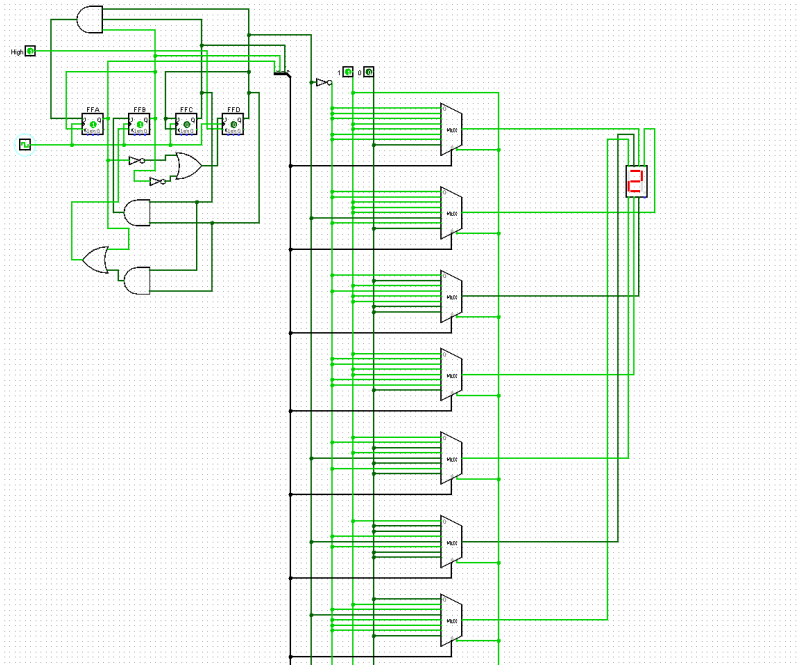
K-Map for K_D

$K_D = 1$

Logisim Simulation



Screenshot 1: State - 0000 Displaying - "**D**"



Screenshot 2: State - 1100 Displaying - "**2**"

Note: We can avoid the NOT gates in the flip flop part because it's built-in.

T Flip Flop

Truth Table:

T Inputs				Clk	Outputs			
TA	**TB**	**TC**	**TD**		**QA***	**QB***	**QC***	**QD***
X	X	X	X	0	0	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0	1
0	0	1	1	1	0	0	1	0
0	0	0	1	1	0	0	1	1
0	1	1	1	1	0	1	0	0
0	0	0	1	1	0	1	0	1
0	0	1	1	1	0	1	1	0
0	0	0	1	1	0	1	1	1
1	1	1	1	1	1	0	0	0
0	0	0	1	1	1	0	0	1
0	0	1	1	1	1	0	1	0
0	0	0	1	1	1	0	1	1
0	1	1	1	1	1	1	0	0
1	1	0	0	1	0	0	0	0

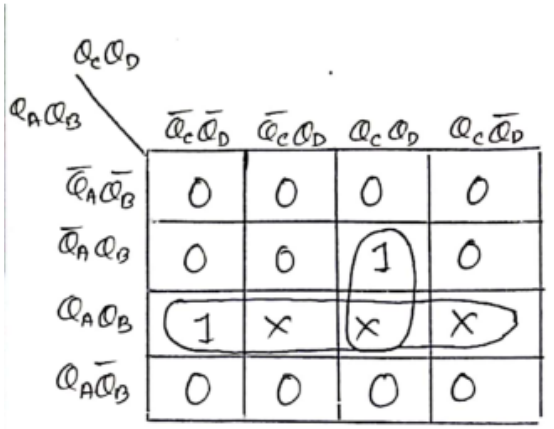
Characteristic Table:

Present				T Inputs				Next			
QA	**QB**	**QC**	**QD**	**TA**	**TB**	**TC**	**TD**	**QA***	**QB***	**QC***	**QD***
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1	0
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	1	0	1	1	1	0	1	0	0
0	1	0	0	0	0	0	1	0	1	0	1
0	1	0	1	0	0	1	1	0	1	1	0
0	1	1	0	0	0	0	1	0	1	1	1
0	1	1	1	1	1	1	1	1	0	0	0
1	0	0	0	0	0	0	1	1	0	0	1
1	0	0	1	0	0	1	1	1	0	1	0
1	0	1	0	0	0	0	1	1	0	1	1
1	0	1	1	0	1	1	1	1	1	0	0
1	1	0	0	1	1	0	0	0	0	0	0

Excitation Table:

Present				Next				T Inputs			
QA	**QB**	**QC**	**QD**	**QA***	**QB***	**QC***	**QD***	**TA**	**TB**	**TC**	**TD**
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	0	0	0	0	1	1	0	0

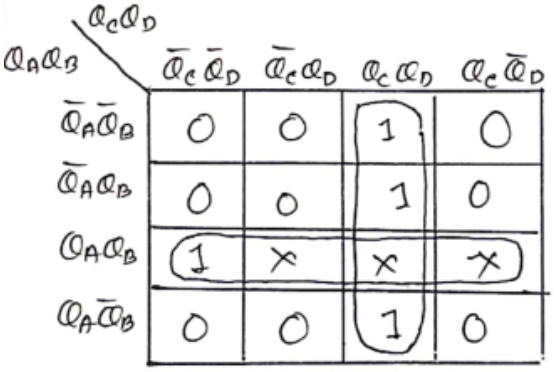
K-Maps for T flip flop:



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	0	0
$\bar{Q}_A Q_B$	0	0	1	0
$Q_A Q_B$	1	×	×	×
$Q_A\bar{Q}_B$	0	0	0	0

K-Map for T_A

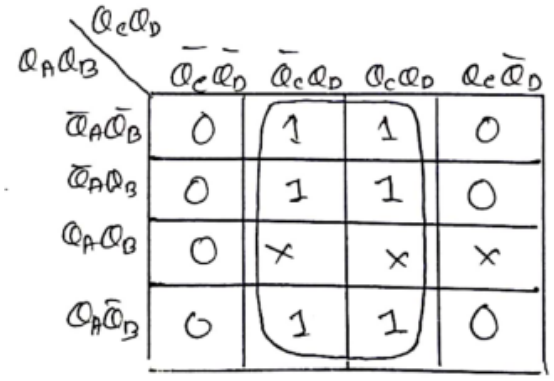
$T_A = Q_A Q_B + Q_B Q_C Q_D$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	1	0
$\bar{Q}_A Q_B$	0	0	1	0
$Q_A Q_B$	1	×	×	×
$Q_A\bar{Q}_B$	0	0	1	0

K-Map for T_B

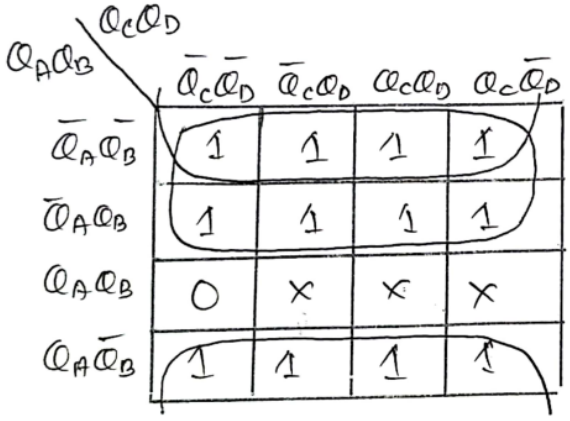
$T_B = Q_A Q_B + Q_C Q_D$.



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	1	1	0
$\bar{Q}_A Q_B$	0	1	1	0
$Q_A Q_B$	0	×	×	×
$Q_A\bar{Q}_B$	0	1	1	0

K-Map for T_C

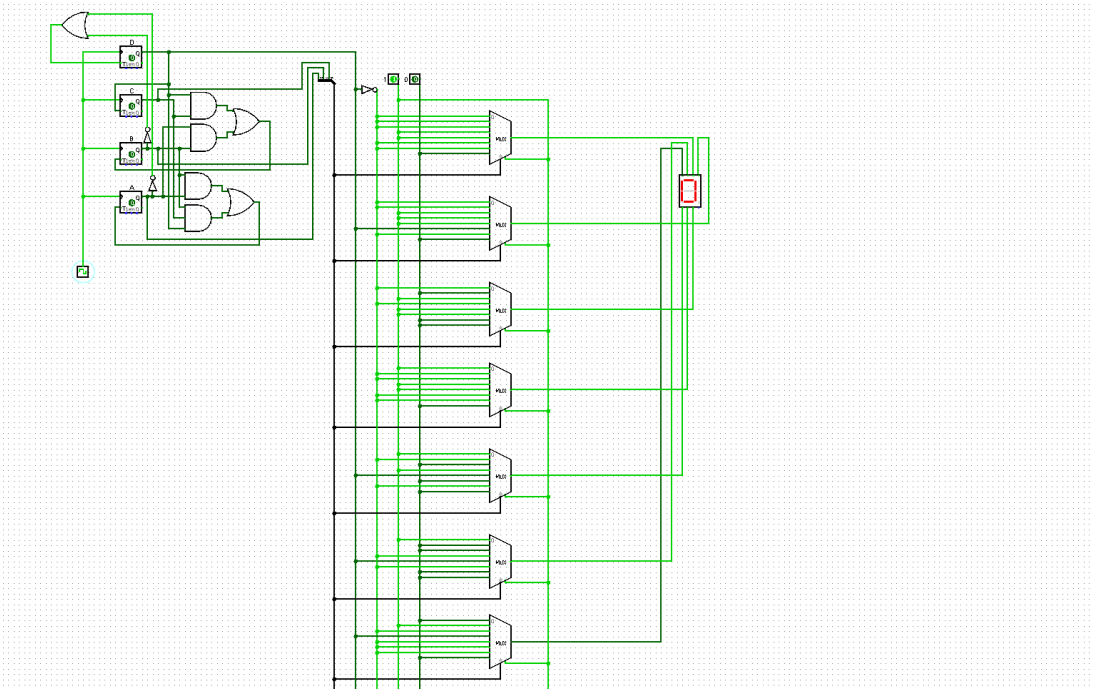
$T_C = Q_D$.



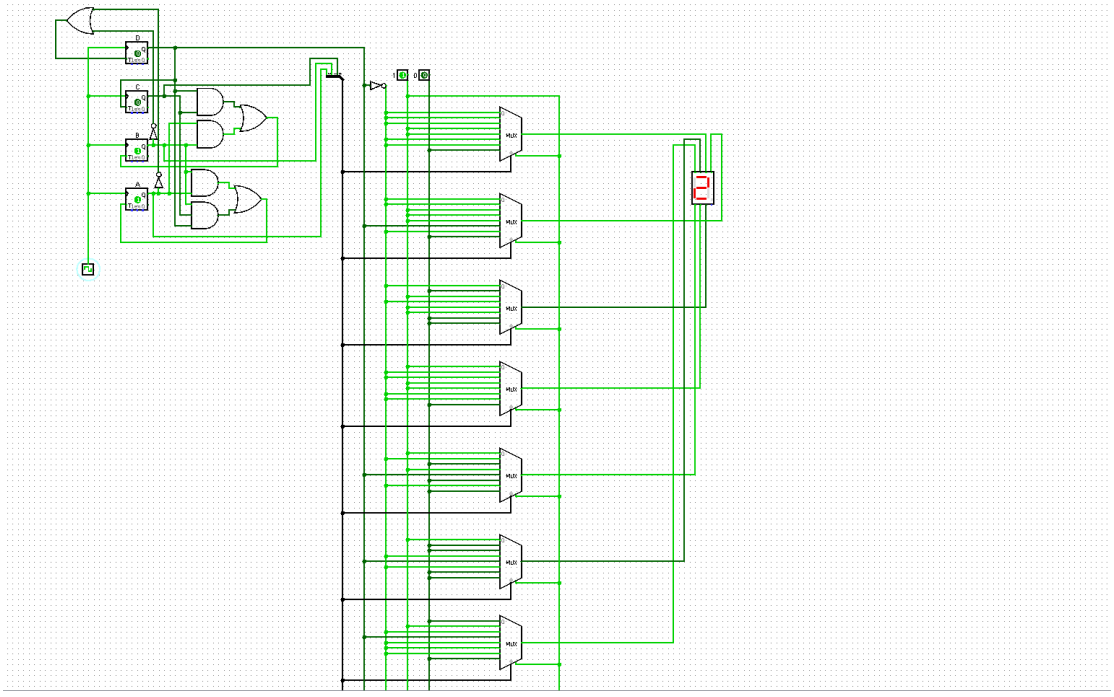
K-Map for T_D

$T_D = \bar{Q}_A + \bar{Q}_B$

Logisim Simulation



Screenshot 1: State - 0000 Displaying - "**D**"



Screenshot 2: State - 1100 Displaying - "**2**"

Note: We can avoid the NOT gates in the flip flop part because it's built-in.

D Flip Flop

Truth Table:

D Inputs				Clk	Next			
DA	**DB**	**DC**	**DD**		**QA***	**QB***	**QC***	**QD***
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0
0	0	0	1	0	0	0	0	0
0	0	0	1	1	0	0	0	1
0	0	1	0	0	0	0	0	1
0	0	1	0	1	0	0	1	0
0	0	1	1	0	0	0	1	0
0	0	1	1	1	0	0	1	1
0	1	0	0	0	0	0	1	1
0	1	0	0	1	0	1	0	0
0	1	0	1	0	0	1	0	0
0	1	0	1	1	0	1	0	1
0	1	1	0	0	0	1	0	1
0	1	1	0	1	0	1	1	0
0	1	1	1	0	0	1	1	0
0	1	1	1	1	0	1	1	1
1	0	0	0	0	0	1	1	1
1	0	0	0	1	1	0	0	0
1	0	0	1	0	1	0	0	0
1	0	0	1	1	1	0	0	1
1	0	1	0	0	1	0	0	1

1	0	1	0	1	1	0	1	0
1	0	1	1	0	1	0	1	0
1	0	1	1	1	1	0	1	1
1	1	0	0	0	1	0	1	1
1	1	0	0	1	1	1	0	0
0	0	0	0	0	1	1	0	0
0	0	0	0	1	0	0	0	0

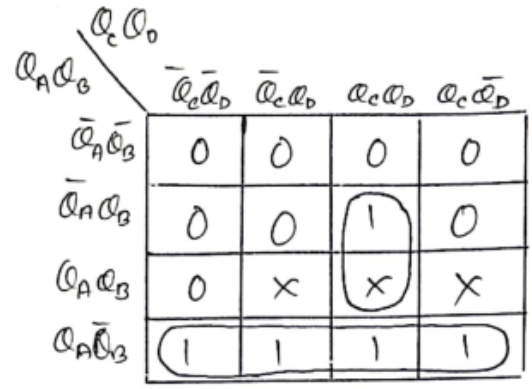
Characteristic Table:

Present				D Inputs				Next			
QA	**QB**	**QC**	**QD**	**DA**	**DB**	**DC**	**DD**	**QA***	**QB***	**QC***	**QD***
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	0	0	0	0	0	0	0	0

Excitation Table:

Present				Next				D Inputs			
QA	**QB**	**QC**	**QD**	**QA***	**QB***	**QC***	**QD***	**DA**	**DB**	**DC**	**DD**
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	1	1	0	1	1
1	0	1	1	1	1	0	0	1	1	0	0
1	1	0	0	0	0	0	0	0	0	0	0

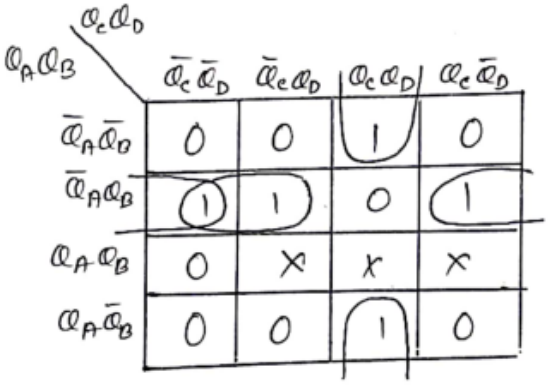
K-Maps for D flip flop:



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	0	0
$\bar{Q}_A Q_B$	0	0	1	0
$Q_A Q_B$	0	×	×	×
$Q_A\bar{Q}_B$	1	1	1	1

K-Map for D_A

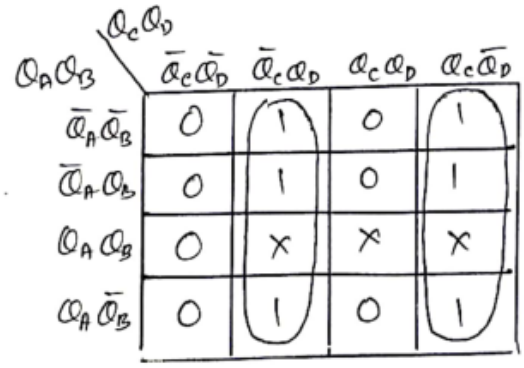
$D_A = Q_A\bar{Q}_B + Q_B Q_C Q_D$.



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	0	1	0
$\bar{Q}_A Q_B$	1	1	0	1
$Q_A Q_B$	0	×	×	×
$Q_A\bar{Q}_B$	0	0	1	0

K-Map for D_B

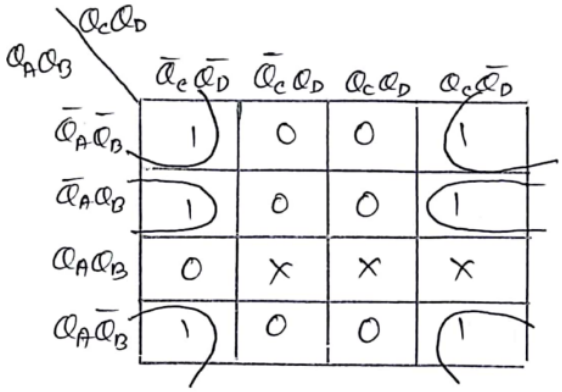
$D_B = \bar{Q}_A Q_D\bar{Q}_C + \bar{Q}_A Q_B\bar{Q}_D + \bar{Q}_B Q_C Q_D$



$Q_A Q_B$ \ $Q_C Q_D$	$\bar{Q}_C\bar{Q}_D$	$\bar{Q}_C Q_D$	$Q_C Q_D$	$Q_C\bar{Q}_D$
$\bar{Q}_A\bar{Q}_B$	0	1	0	1
$\bar{Q}_A Q_B$	0	1	0	1
$Q_A Q_B$	0	×	×	×
$Q_A\bar{Q}_B$	0	1	0	1

K-Map for D_C

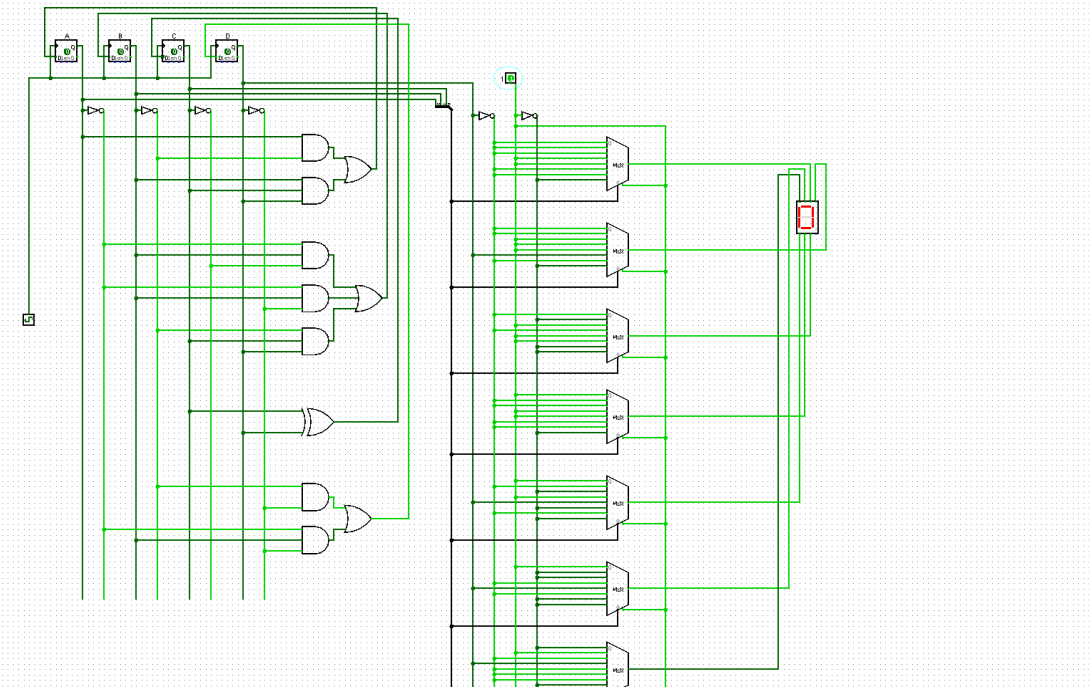
$D_C = \bar{Q}_C Q_D + Q_C\bar{Q}_D$



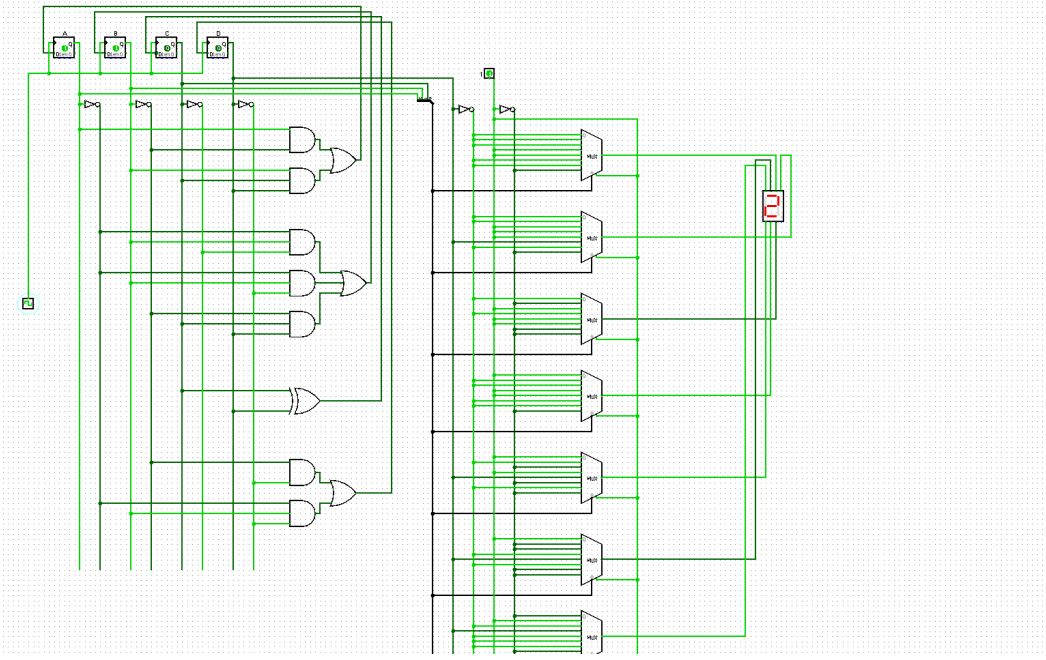
K-Map for D_D

$$D_D = \bar{Q}_B \bar{Q}_D + \bar{Q}_A Q_B \bar{Q}_D$$

Logisim Simulation



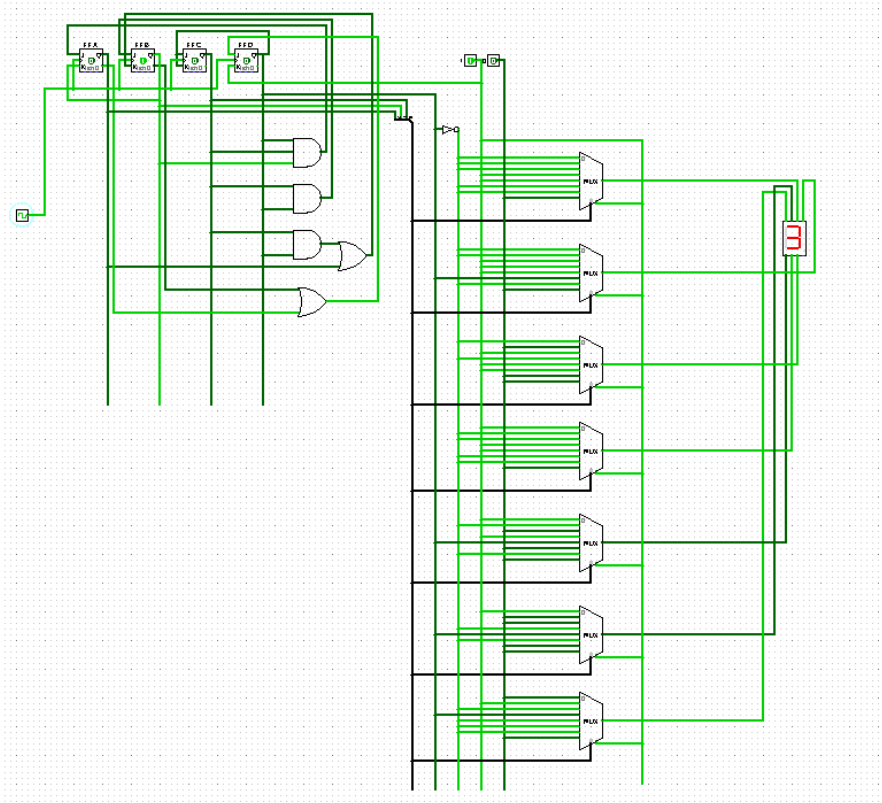
Screenshot 1: State - 0000 Displaying - “D”



Screenshot 2: State - 1100 Displaying - “2”

Note: We can avoid the NOT gates in the flip flop part because it's built-in.

The optimized flip flop for the project:



The **J-K Flip Flop** is the optimized one because for our project we can see that this flip flop configuration required the least amount of gates and complexity. Whereas D and T Flip Flops require more gates.

Unlike other flip-flop types, JK flip-flops do not have invalid or forbidden states. They can be in any of the four possible states (00, 01, 10, 11), which simplifies state analysis and reduces the risk of unintended behavior. When configured as a toggle flip-flop, a JK flip-flop typically requires fewer gates than other flip-flop types designed for toggling. This can result in a more compact and efficient design.

Thus J-K Flip Flop is the most optimized one for this project.

Budget for the project:

As we are using Multiplexer to display “**DL2-31D230S12**”, we require

1-Cathode 7-Segment Display = 12 Tk
7-IC 74HC151N (8:1 MUX) = 224 Tk
1-IC NOT 7404 (2-input NOT) = 26 Tk
1-IC 7408 (2-input AND) = 31 Tk
1-IC 7432 (2-input OR) = 28 Tk
2-IC 4027 (Dual J-k Flip-Flop) = 70 Tk
1-IC 555 Timer = 18 Tk
5 Breadboards = 650
13 resistors = 20 Tk
1 capacitor = 5 Tk
Jumper cables = 300 Tk

Total Cost = 1384 Tk