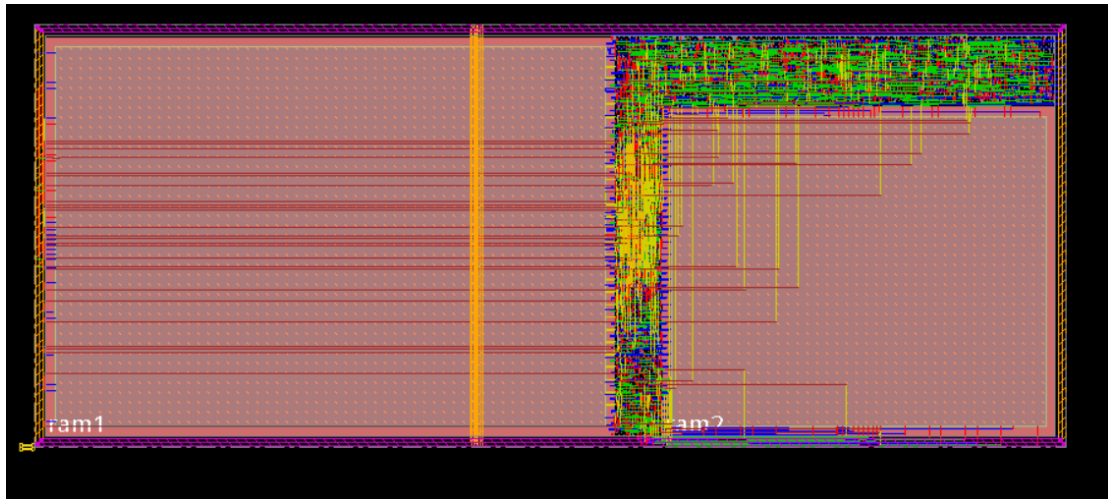


# CVSD Final report

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若要用 innovus 重建，請開 DBS/corefiller

## 1.APR 後的 Lauout 圖



## 2.Verify

### Verify DRC

```
innovus 107> *** Starting Verify Geometry (MEM: 1666.8) ***

**WARN: (IMPVFG-257): verifyGeometry command is replaced by verify_drc command. It still works in this release but will be removed in future releases. Please update your script to use the new command.
VERIFY GEOMETRY ..... Starting Verification
VERIFY GEOMETRY ..... Initializing
VERIFY GEOMETRY ..... Deleting Existing Violations
VERIFY GEOMETRY ..... Creating Sub-Areas
                        ..... bin size: 8320
**WARN: (IMPVFG-198): Area to be verified is small to see any runtime gain from multi-cpus. Use setMultiCpuUsage command to adjust the number of CPUs.
VERIFY GEOMETRY ..... SubArea : 1 of 1
VERIFY GEOMETRY ..... Cells : 0 Viols.
VERIFY GEOMETRY ..... SameNet : 0 Viols.
VERIFY GEOMETRY ..... Wiring : 0 Viols.
VERIFY GEOMETRY ..... Antenna : 0 Viols.
VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 2.00
Begin Summary ...
Cells : 0
SameNet : 0
Wiring : 0
Antenna : 0
Short : 0
Overlap : 0
End Summary

Verification Complete : 0 Viols. 0 Wrngs.

*****End: VERIFY GEOMETRY*****
*** verify geometry (CPU: 0:00:01.4 MEM: 35.1M)
innovus 107> █
```

## Verify Geometry

```
innovus 107> #-report LEDDC.drc.rpt # string, default="", user setting
*** Starting Verify DRC (MEM: 1679.3) ***

VERIFY DRC ..... Starting Verification
VERIFY DRC ..... Initializing
VERIFY DRC ..... Deleting Existing Violations
VERIFY DRC ..... Creating Sub-Areas
VERIFY DRC ..... Using new threading
VERIFY DRC ..... Sub-Area: {0.000 0.000 152.320 125.120} 1 of 8 Thread : 3
VERIFY DRC ..... Sub-Area: {0.000 125.120 152.320 249.280} 5 of 8 Thread : 3
VERIFY DRC ..... Sub-Area: {304.640 0.000 456.960 125.120} 3 of 8 Thread : 0
VERIFY DRC ..... Sub-Area: {152.320 0.000 304.640 125.120} 2 of 8 Thread : 0
VERIFY DRC ..... Sub-Area: {456.960 0.000 608.120 125.120} 4 of 8 Thread : 3
VERIFY DRC ..... Sub-Area: {152.320 125.120 304.640 249.280} 6 of 8 Thread : 0
VERIFY DRC ..... Sub-Area: {456.960 125.120 608.120 249.280} 8 of 8 Thread : 3
VERIFY DRC ..... Thread : 0 finished.
VERIFY DRC ..... Thread : 2 finished.
VERIFY DRC ..... Thread : 5 finished.
VERIFY DRC ..... Sub-Area: {304.640 125.120 456.960 249.280} 7 of 8 Thread : 3
VERIFY DRC ..... Thread : 3 finished.

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.3 ELAPSED TIME: 1.00 MEM: 21.3M) ***

innovus 107>
```

## Verify Connectivity

```
innovus 107> VERIFY_CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****
Start Time: Fri Jan 11 14:48:28 2019

Design Name: LEDDC
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (608.1200, 249.2800)
Error Limit = 1000; Warning Limit = 50
Check all nets
Use 8 pthreads

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Fri Jan 11 14:48:28 2019
Time Elapsed: 0:00:00.0

***** End: VERIFY CONNECTIVITY *****
Verification Complete : 0 Viols. 0 Wrngs.
(CPU Time: 0:00:00.1 MEM: 2.516M)

innovus 107>
```

### 3.Layout area

最後 analyzeFloorplan 面積 15.15 萬

```
innovus 107> analyzeFloorplan
**WARN: (IMPAPFU-9006): Command 'analyzeFloorplan' is obsolete. Please use commands 'placeDesign + trialRoute + create_ps_per_micron_model + timeDesi
gn' 'proto + load_timing_debug_report' 'proto' to analyze congestion and timing for the floorplan.
Start to collect the design information.
Build netlist information for Cell LEDDC.
Finished collecting the design information.
Average module density = 1.000.
Density for the design = 1.000.
= stdcell area 9448 sites (16037 um^2) / alloc_area 9448 sites (16037 um^2).
Pin Density = 0.04616.
= total # of pins 3823 / total area 82816.
***** Analyze Floorplan *****
Die Area(um^2) : 151592.15
Core Area(um^2) : 140571.88
Chip Density (Counting Std Cells and MACROs and IOs): 85.037%
Core Density (Counting Std Cells and MACROs): 91.703%
Average utilization : 100.000%
Number of instance(s) : 1631
Number of Macro(s) : 2
Number of IO Pin(s) : 23
Number of Power Domain(s) : 0
***** Estimation Results *****
innovus 108> █
```

下圖為本次 RTL 設計使用到的資源

```
output reg[15:0] OUT;
reg [63:0] read_data,read_data_temp;
reg [15:0] ram2_data_in,read_data_count,first_data_OUT;
reg [8:0] ram1_r_addr,ram2_r_addr,ram1_w_addr;//0~511
reg [7:0] ram2_w_addr;//0~255
reg [4:0] read_scanline_count;
reg [3:0] write_data_count;
reg ram1_r_en,ram1_w_en,ram2_w_en,ram2_r_en,round;

sram_512x16 ram1(
.AA(ram1_r_addr[8:0]),
.AB(ram1_w_addr[8:0]),
.DB(ram1_data_in),
.CLKA(GCK),
.CLKB(GCK),
.CENA(ram1_r_en),
.CENB(ram1_w_en),
.QA(ram1_data_out)
);

sram_256x16 ram2(
.AA(ram2_r_addr[7:0]),
.AB(ram2_w_addr),
.DB(ram2_data_in),
.CLKA(GCK),
.CLKB(DCK),
.CENA(ram2_r_en),
.CENB(ram2_w_en),
.QA(ram2_data_out)
);
```

為了要減少面積，所以盡量不使用自己宣告的 reg 而是用 sram，在這個 design 中 ram2 作為接收 data，並在特定時間把 data 傳到 ram1，讀取 data 固定從 ram1，因 sram 只有一個 output port，故必要對於目前輸出的 scanline 上 16 個 pixel 做暫存，並把讀到的數值和 Vsync 計數器做比較，決定 output 的值是多少

比較要注意的是 ram2 寫至 ram1 時的 address 不能衝突，需經過調整，此外，需自製有號數的減法才可以正確將讀到的數值和 Vsync 計數器做比較。

#### Synthesis 後的面積

```
Number of ports:                23
Number of nets:                  1101
Number of cells:                  968
Number of combinational cells:    730
Number of sequential cells:       236
Number of macros/black boxes:     2
Number of buf/inv:                71
Number of references:             91

Combinational area:              6312.630557
Buf/Inv area:                     409.073396
Noncombinational area:            7626.417969
Macro/Black Box area:            122983.527344
Net Interconnect area:           128800.656189

Total cell area:                  136922.575869
Total area:                       265723.232058
```