3GPP TSG RAN WG1 Meeting #86-BIS **R1- 1609708**

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Agenda item: 8.1.3.1
Source: National Taiwan University
Title: Discussion of QC-LDPC code design with regular degree-3 for NR
Document for: Discussion

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1. Introduction

The quasi-cyclic low density parity check (QC-LDPC) code has been identified as one of the promising channel coding candidates for NR in RAN1#86 meeting. Way forward on Channel Coding Evaluation for 5G New Radio has been agreed for study the next step [1]. In this document, we provide a low complexity Double QC-LDPC (DQC-LDPC) code design with regular degree-3 for NR. The parity-check matrices supporting flexible rates are provided for performance evaluation.

2. Double QC-LDPC code design

The QC-LDPC code can be represented by the parity-check matrix **H** that consists of small square blocks (or submatrices) of size Q x Q which are the null matrix or circulant permutation (right-shifted identity) matrices. The QC-LDPC codes are designed with the following parameters.

1. Circulant permutation matrix size Q. For easier implementation, $Q = 2^q$ is usually selected. In this contribution $Q = 64$ is selected for illustration purpose, other sizes of Q are viable.
2. Codeword length $N = Q \cdot n_q$, information block $K = Q \cdot k_q$,
3. Code rate $r = K/N = k_q/n_q$. However, these codes are not classified by rate but by parity check size. It can be more flexible with varying information bits.
4. Shift value s_q (sub-block size or lift size).
5. Column degree d_v (the same as variable degree), which is strictly regular-3 for each matrix without any exception. To put it again, it is not average 3 with dv=2 or 4.
6. Row degree r_v (the same as check degree), designed as nearly regular. Due to code rate, it is ranged from 5 to 32.

The circulant permutation matrix $\mathbf{P}_{\boldsymbol{k}} = (p_{ij})$ $(0 \le i, j < Q)$ is obtained from the Q x Q identity matrix by cyclically shifting the columns to the right by k columns.

For example, for Q = 5, the following show example matrices,

$$\mathbf{P}_0 = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \mathbf{P}_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{bmatrix}, \mathbf{P}_3 = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix}.$$

Using the above notation, parity-check matrices for large block sizes can be represented in a compact form. For example, an expanded matrix $\mathbf{H}_M$ (of size m_q x n_q) can be used to denote the $m_q Q$ x $n_q Q$ binary parity-check matrix obtained by using a compact base matrix $\mathbf{H}_{bm}$ (of size m_q x n_q) and a shift size value s_q.

Encoding

In this contribution, a DQC-LDPC code is presented. The DQC-LDPC is a special form of the classical QC-LDPC codes in the parity check matrix. The DQC code features double layers of circulant matrices (or circulant of circulants). Fig. 1 shows an example of double circulant in the parity matrix. For convenience, "*" is used to denote the null matrix of size Q x Q. As in QC-LDPC code, each small square blocks (or submatrices) of size Q x Q are the null matrix (denoted by "*") or circulant permutation (right-shifted identity) matrices. A square collection of the small square blocks forms the outer layer of circulant matrix in **H**. The unique feature helps to encode the parity with double shift register array.

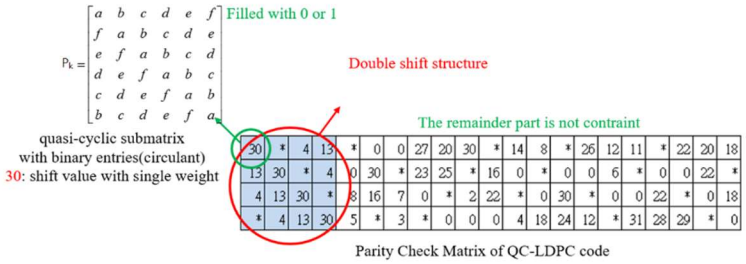

Fig. 1. Example of DQC-LDPC

The DQC codes with different rates have advantage in encoder implementation. The error correction performance is not affected by the DQC structure at all.

Decoding

The scalar min-sum decoder is used to evaluate block error rate (BLER). The scalar min-sum decoder has general column shuffle architecture with early termination. The convergence is achieved by checking whether the syndrome vector is all-zero. Within decoding process, the scalar is 3/4 due to bit-shift-adder hardware implementation. In principle, the parity check matrix generally determines the error correction performance. In general, the classical QC-LDPC decoding strategies are all suitable to the DQC-LDPC codes.

Block size support

Similar to the LTE turbo codes, the block size selection needs to consider underlying code structure. We select several parity-check matrix sizes such as 256, 512, 768, 1024, 1536, 2048 to meet various user cases. Each parity-check matrix size could construct 3~7 base matrices with the best correction performance. In the following step, a flexible matrix size can be obtained by column-truncation from the base matrix if necessary. The number of column truncation is the multiples of circulant matrix size (e.g. 64). In principle, DQC-LDPC codes can be designed to support any arbitrary information/code block size.

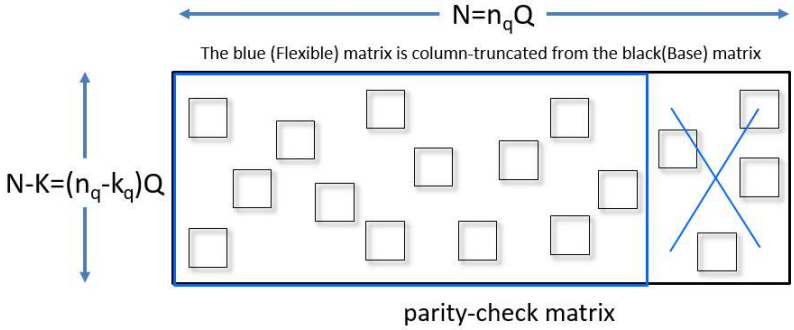

Fig. 2. Column truncation of DQC-LDPC for flexible code rate support

In the illustration example, all the base matrices are designed by column-degree 3, QC block size 64, and DQC encoding feature.

3. Performance evaluation

RAN1 agreed for initial evaluations of different channel coding schemes in RAN1#84bis. In the attached text file (R1_dqc_ldpc.xls), we provide DQC-LDPC parity-check matrices capable of supporting coding parameters applicable to eMBB scenarios. The evaluation are presented in the companion contribution.

The example DQC-LDPC code designs is listed in Table 1. The code rates covers from 0.111 to 0.889 with variable-degree-3. We utilize scalar min-sum decoder to evaluate the block error rate (BLER) versus SNR (E_s/N_0). The simulation results for parity size 256, 512, 768, 1024, 1536, and 2048 are shown in Fig. 3 to Fig. 8 respectively. All the figures are under maximum iterations=31 with 10 soft-bits to behave as nearly-floating input. The input quantization could be further discussed in the future.

Table 1. Parameters of the proposed parity-check matrices for evaluations.

Parity	Base Codeword Length N	Flexible Codeword Length N	Code Rate
256	{1280, 768, 512}	256+64*i, i in{1,2⋯,16}	0.5~0.8
512	{4608, 3584, 2560, 1536, 1024, 768, 640}	512+64*i, i in{1,2⋯,64}	0.2~0.889
768	{4864, 4096, 3072, 1792, 1280, 1024}	768+64*i, i in{1,2⋯,64}	0.25~0.842
1024	{5120, 4096, 3072, 2048, 1536, 1280}	1024+64*i, i in{1,2⋯,64}	0.2~0.8
1536	{5632, 4096, 3584, 2560, 2048}	1536+64*i, i in{1,2⋯,64}	0.25~0.727
2048	{6144, 5120, 4096, 3072, 2560, 2304}	2048+64*i, i in{1,2⋯,64}	0.111~0.667

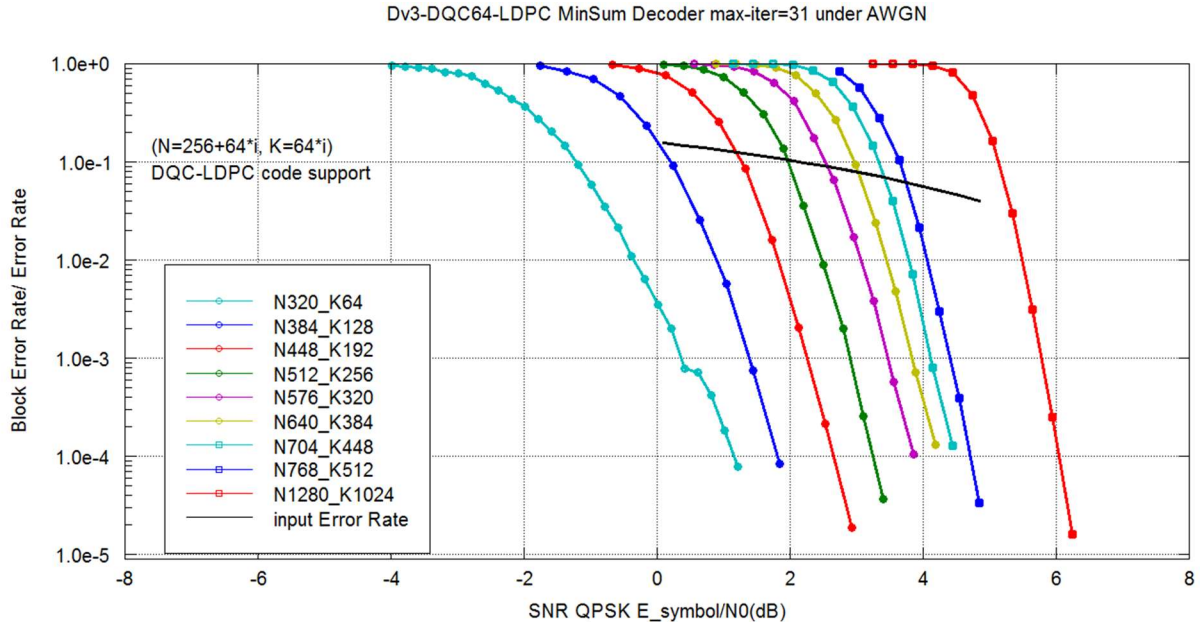

Fig. 3.The performance results of codes with 256-bit parity are shown in the companion contribution.

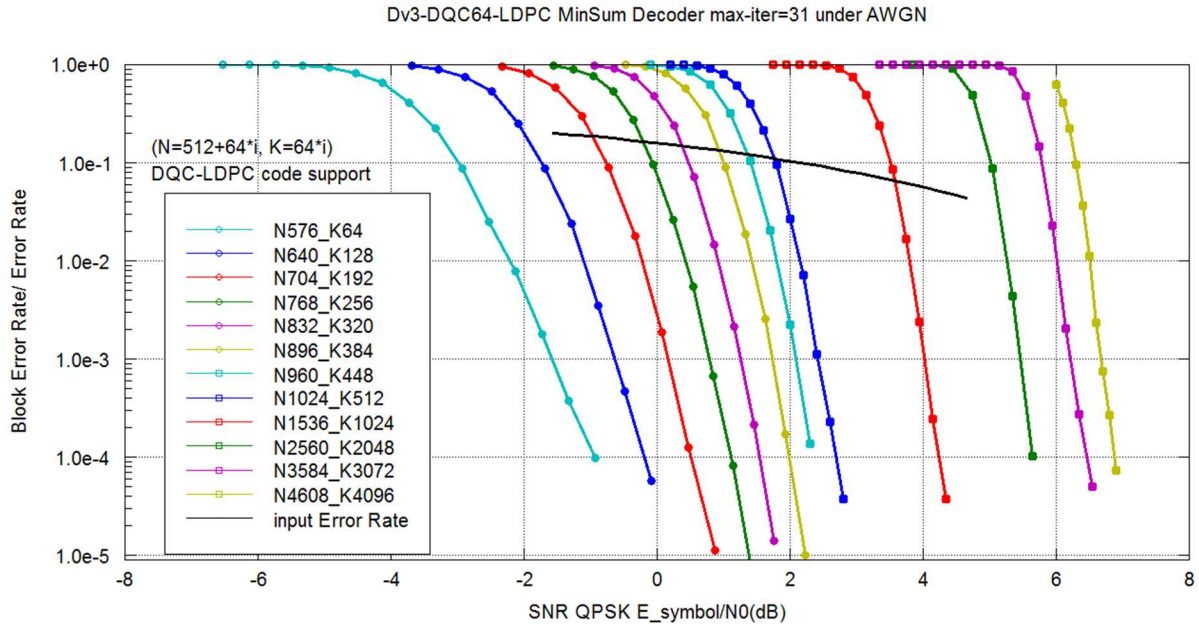

Fig. 4. The performance results of codes with 512-bit parity are shown in the companion contribution.

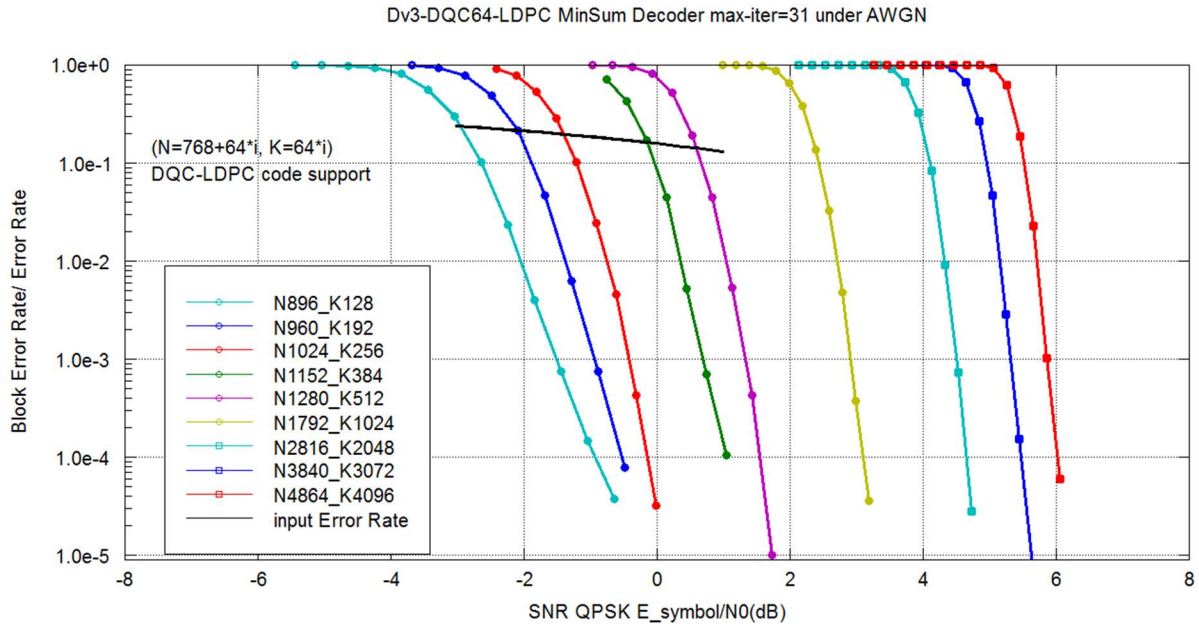

Fig. 5. The performance results of codes with 768-bit parity are shown in the companion contribution.

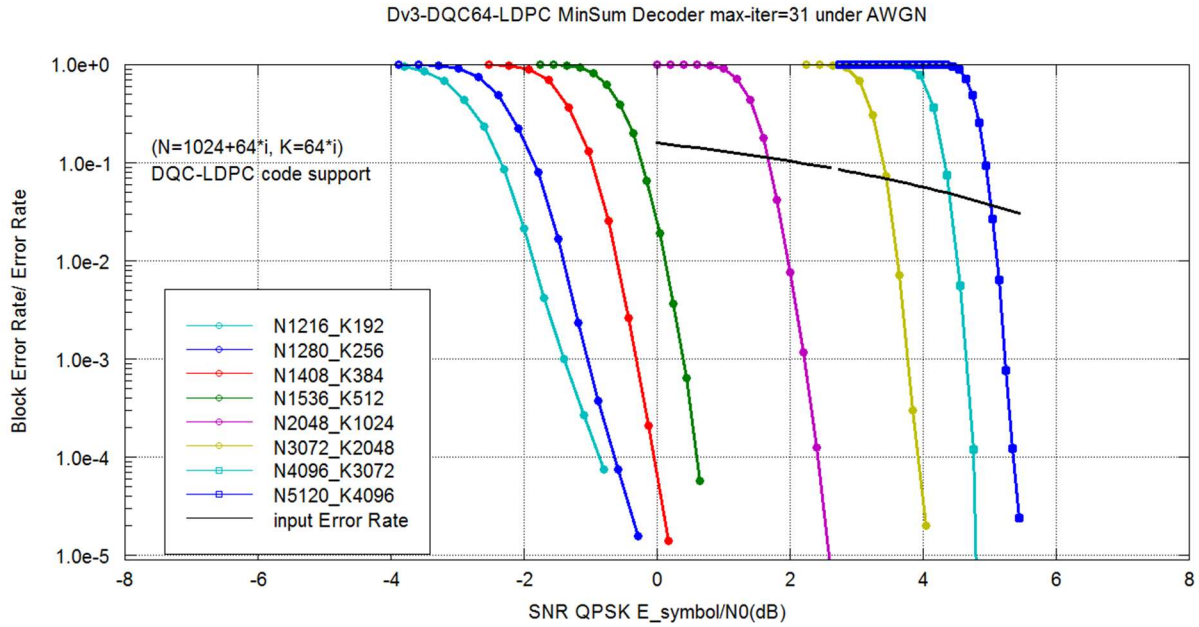

Fig. 6. The performance results of codes with 1024-bit parity are shown in the companion contribution.

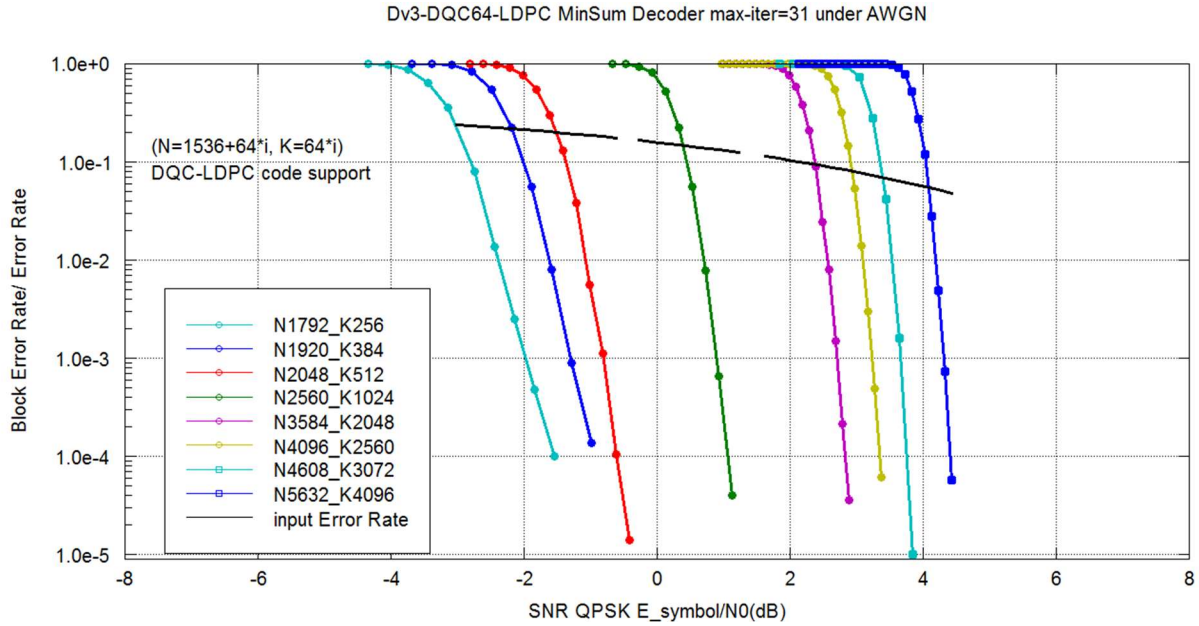

Fig. 7. The performance results of codes with 1536-bit parity are shown in the companion contribution.

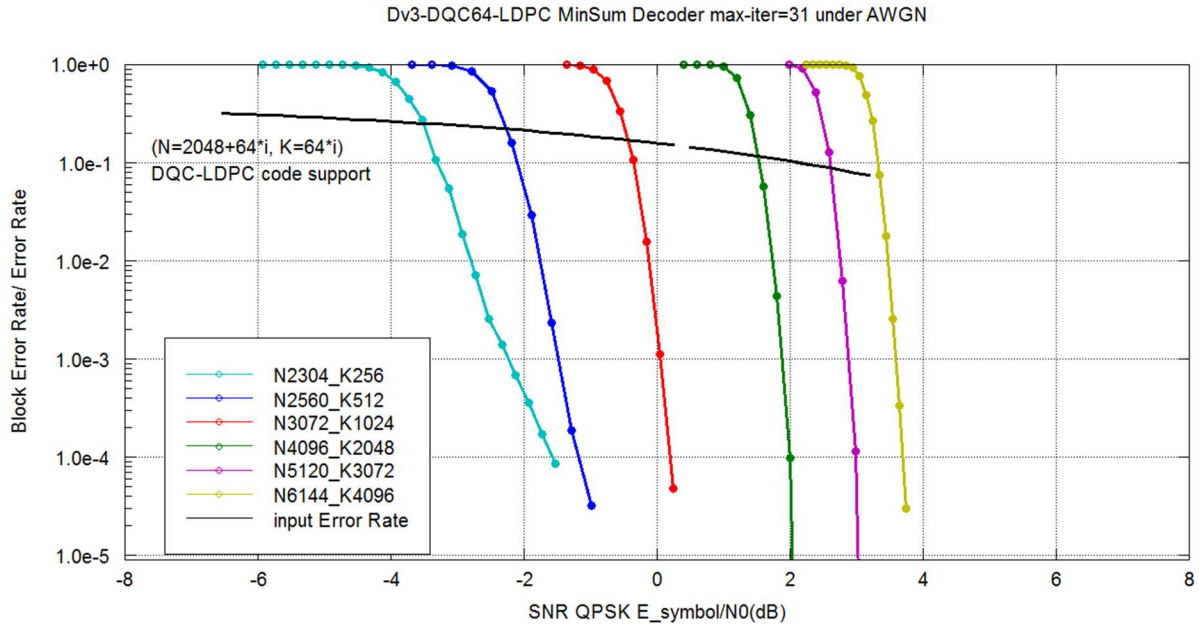

Fig. 8. The performance results of codes with 2048-bit parity are shown in the companion contribution

4. Complexity Analysis

In this section, the hardware implementation with DQC-LDPC code with degree-3 is studied. The codec design is based on DQC encoder and column-shuffle decoder. For efficient processing, the encoder is designed as B_{enc}-bit encoder and the decoder would process P_{dec}-bit nodes per cycle. The B_{enc} and P_{dec} could be chosen as one of Q, Q/2, Q/4…, if matching processor and DRAM data bus size is needed. The complexity analysis is summarized in Table 2. The table emphasizes that the variable degree of parity check matrix would affect parallel processing. The regular degree-3 property facilitates parallel processing efficiency and reduce the complexity of codec design.

Table **2**. Decoder complexity analysis.

	Design complexity	Note
Parameter for parity check matrix	N: codeword length K: information bit length Q: circulant size = 64 d_v = 3	Column-shuffle architecture. Variable-degree polynomial $\lambda(x) = x^{dv-1}$ [5].
Rom for Each parity check matrix	Width: d_v*(log2(N-K)) bits Depth: n_q	
Encoder - B_{enc} bit parallel encoder		
Syndrome FFs	(N-K) bits	
Shifter and mux for syndrome update	d_v barrel shifter, d_v*B_{enc} muxs	
Syndrome calculator	d_v*B_{enc} xor gates	
Parity calculator	B_{enc}*(N-K) xor gates	B_{enc} would be one of Q, Q/2, Q/4,…as system design to meet throughput requirement.
Parity shifter	d_v barrel shifter, 1 DQC shifter	DQC shifter will reduce encoding rom regardless of storing multiple vectors.
ROM for DQC code parity	(N-K) bits	Different from each codes
Decoder - P_{dec} bit parallel decoder		

Degrees of whole matrix	d_v*N	This decides how many nodes should be decoded per iteration.
Degree processed per cycle	d_v*P_{dec}	This would decide (N/P_{dec}) as cycle number per iteration.
Check node storage	(2*B_{chk}+B_{loc})*(N-K)	B_{chk} means LLR quantization for min1, min2. B_{loc} means bits that expressess min1 location. FFs or sram is possible depending on system request.
Check node operation	P_{dec} * d_v units	P_{dec} would be one of Q, Q/2, Q/4,…as system design to meet throughput balance. This means hardware for min and sign-mag operation
Shifter and mux between check node and variable node	d_v barrel shifter, d_v* P_{dec} muxs	
Variable node operation	(1+d_v)*P_{dec} adder	signed adders
SRAM for variable bits	Width: P_{dec} bits Depth: N/P_{dec}	Sram shape depend on P_{dec} -parallel
SRAM for check node sign	Width: d_v*P_{dec} bits Depth: N/P_{dec}	Sram shape depend on P_{dec} -parallel
Percentage of redundant hardware design that match outside system bus.	0 %	Q=64 match cpu and dram bus size that do not waste any hardware to queue or resize output results.

5. Conclusion

In this document, we provide DQC-LDPC code design with various parity size to satisfy flexible use scenarios. The contribution also includes the aspects related to encoding/decoding/flexibility in terms of block-sizes/code-rate support. We also provide the parity-check matrices for performance evaluations. We propose to further study LDPC code for NR, including the following statements:

Proposal 1: The QC-LDPC code is flexible in supporting low to high code rates.

Proposal 2: The circulant structure of DQC-LDPC in parity matrix is hardware friendly to the encoder.

Proposal 3: The regular degree property facilitates the decoding efficiency with low complexity.

References

[1] R1-163757, WF on Channel Coding Evaluation for 5G New Radio
[2] RP-160671, New SID Proposal: Study on New Radio Access Technology
[3] R1-164697, “LDPC Design Overview”, R1-164697, Qualcomm Inc., 3GPP TSG RAN WG1 #85, Nanjing, China, May 23-25, 2016.
[4] R1-165164, "Discussion on LDPC Code Design and Performance Evaluation," MediaTek Corp., 3GPP TSG RAN WG1 #85, Nanjing, China, May 23-25, 2016.
[5] T. Richardson, A. Shokrollahi, R. Urbanke, "Design of capacity-approaching irregular low-density parity-check codes," *IEEE Trans. Information Theory*, vol.47, pp. 619-637, Feb. 2001.