GPP TSG-RAN WG1 #NR **R1-1700644**
16th – 20th Jan 2017
Spokane, US

Agenda item: 5.1.5.1

Source: National Taiwan University

Title: IR-HARQ scheme support with double QC-LDPC codes of degree-3

Document for: Discussion

1 Introduction

In the RAN1-#87, LDPC has been adopted as the channel coding scheme for the eMBB data channel [1]. In the agreements [2],

Agreement:

- Code extension of a parity-check matrix is used for IR HARQ/rate-matching support
    - Use lower-triangular extension, which includes diagonal-extension as a special case
- For the QC-LDPC design, the non-zero sub-blocks have circulant weight <=2
    - Circulant weight is the number of superimposed circularly shifted Z×Z identity matrices
- In parity check matrix design, the highest code rate ($R_{max,j}$) to design j-th H matrix for is
    - $R_{max,j}$ <=8/9
    - $R_{max,j}$ is the code rate of the j-th H matrix before code extension is applied ($0 \le j < J$)
    - $R_{max,j}$ is the code rate after accounting for the built-in puncturing, if this is applied in H matrix design
    - Rate matching to support transmission code rate higher than $R_{max,j}$ is not precluded

In this article, we present support to the IR-HARQ scheme with double quasi-cyclic low-density parity check code (DQC-LDPC) of degree-3[3]. The code design leads to well support of IR-HARQ decoding process with constraint of the same circulant size and optimal decoding hardware efficiency.

2 Flexibility and Performance

Observation 1 (IR-Hydrid ARQ):

The double QC-LDPC codes support IR-HARQ scheme by stacking multiple parity check matrix. The stack of multiple parity check matrices of degree-3 would form a larger matrix with degree >=3. The decoding process in the larger matrix utilizes the longer parity which sums up multiple parity retransmission. The log-likelihood ratio (LLR) summation crossing multiple degree-3 double-QC matrices in variable nodes benefits correction improvement. And the incremental check nodes provide helpful information exchange and speed up decoding convergence. The Fig. 1 shows the process of IR-HARQ with DQC-LDPC codes.

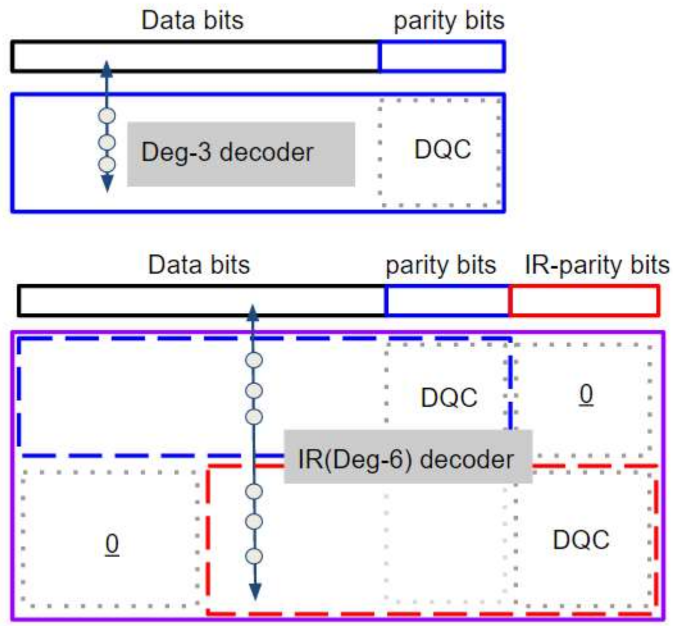

Fig. 1. The IR-HARQ scheme for DQC-LDPC codes

The parity bits (blue part) and data bits (black part) comprises the codeword for the first transmission. When channel error occurs, the LDPC decoder reports uncorrectable status. The system launch IR-HARQ to ask for IR parity (red part). So the IR decoder will utilize the longer codeword (data bits +blue part +red part) and the bigger matrix (purple box). The partial region in the larger matrix will have larger column degree where bits located in are re-encoded. The multiple parity part will not be overlaped due to behaving info bits as the next encoding. As a result, the longer parity has joint belief-propagating decoding to enhance error correction.

Observation 2 (Parity-Selection and IR Options):

The base matrices selection of double QC-LDPC codes is discussed in R1-1609708 [3]. The DQC-LDPC PCM can be used to offer IR-HARQ by the combination of multiple matrix. Each matrix guarantees codeword error rate down to 10^{-5}. The lower decoding failure probability implies lower excessive errors.

IR decoding have two choices for further studies. One is the total bits (black data bits+1st parity+ IR parity) using purple matrix. The other is partial (overlapped data bits++1st parity+ IR parity) using red matrix. These two kinds of decoding is bidding where the errors are located in. We recommend that the length of IR-parity should be longer than the length of the previous parity to avoid often decoding failure. Moreover, too many IR-HARQ ping-pong retransmissions waste the system resource and degrade user experience. By simulation experience, system should re-consider the TYPE-I HARQ (the whole data-bit retransmission) and CC-HARQ if failing decoding at the third time.

3 Implementation advantages

Observation 3 (Compatible Hardware Design for ARQ):

The IR-HARQ scheme is easily merged into the DQC-LDPC hardware design with degree-3. Supposed that codec is ready for degree-3 LLR-value exchange, the decoding control flow needs re-arrangement when starting IR-decoding. The pointer of reading PCMs, and SRAM address of variable nodes and check nodes should be shuffled between two matrices. The variable node will sum up the total LLRs as a joint decoding. The decoding iteration cycles become longer and time-consuming for syndrome convergence. Overall, there are much less hardware problem for IR-HARQ support using double QC-LDPC codes with degree-3.

Observation 4 (IR-Decoder Improvement):

We show a simple example for DQC-LDPC code effectiveness below. Code-1 is (N=3584, K3072) is for the original parity check matrix, and code-2 (N=2048, K=1024) is for IR-ARQ scheme. The figure show that IR provides almost 1.2 dB coding gain.

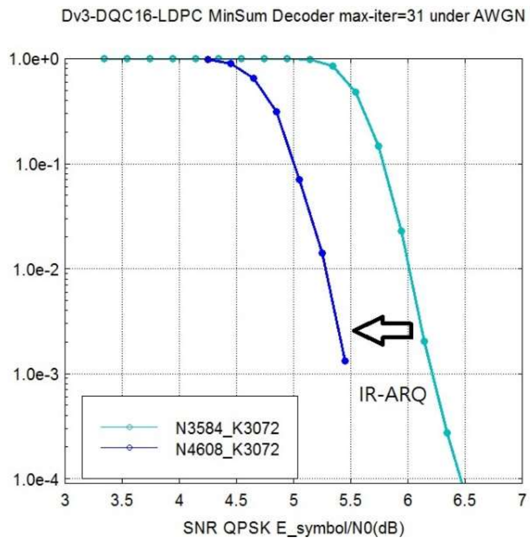

Fig2. BLER curve to show IR coding gain.

4 Conclusions

<u>Proposal 1:</u> Double QC-LDPC codes with degree-3 can support IR-HARQ scheme with rate matching.

5 References

[1] R1-1613710, Chairman's Notes of AI 7.1.5 on channel coding and modulation for NR, 3GPP RAN1 meeting #87, Reno, Nevada, Nov. 2016.

[2] R1-1613093 "WF on Basics of LDPC Design," 3GPP RAN1 meeting #87, Reno, Nevada, Nov. 2016.

[3] R1-1609708, "Discussion of QC-LDPC code design with regular degree-3 for NR", 3GPP RAN1 meeting #86bis, Lisbon, Portugal, Oct. 2016.