Technical Report: Performance Analysis and Optimization of MobileNetV2 on Apple M2: A Detailed Study of Neural Engine and Compute Unit Selection Strategies

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ABSTRACT

This technical report presents a detailed performance evaluation and optimization study of deploying MobileNetV2 on Apple Silicon M2 platform. Through systematic benchmarking and analysis, I investigated the effectiveness of different compute unit configurations (CPU, GPU, and Neural Engine) in handling deep learning inference tasks. My experiments revealed that the Neural Engine-based configurations achieved optimal performance with mean latencies of 0.64ms, significantly outperforming traditional CPU and GPU combinations. I documented unexpected performance patterns, including a tri-modal distribution in CPU-GPU configurations, and provided practical guidelines for selecting appropriate compute units based on specific application requirements. The report includes comprehensive implementation details, testing methodologies, and optimization strategies, serving as a practical reference for developers working with deep learning models on Apple Silicon platforms. My findings highlight the importance of hardware-specific optimization and provide actionable recommendations for achieving optimal model deployment on modern edge computing devices.

The implementation code and detailed results are available at: https://github.com/Wuhubing/apple-silicon-ml-benchmarks

Keywords: Apple Silicon M2, Deep Learning Deployment, Performance Optimization, Neural Engine, Compute Unit Configuration, Edge Computing, MobileNetV2, Technical Benchmarking

1 INTRODUCTION

1.1 Background and Motivation

Deploying deep learning models on edge devices has become a critical challenge in modern AI applications [25]. With the introduction of Apple Silicon, particularly the M1/M2 series chips, a new architecture combining CPU, GPU, and Neural Engine presents unique opportunities and challenges for model optimization [2]. As illustrated in Figure 1, the unified memory architecture enables direct data access between different processing units, potentially reducing data transfer overhead [8]. The Neural Engine is Apple's specialized AI processor that can perform 11 trillion operations per second [4]. While this hardware can greatly improve AI model performance, proper optimization is needed to utilize its capabilities [5] fully. **Initial benchmarks show that proper optimization can lead to up to 40% performance improvement and 30% energy reduction compared to unoptimized deployments [26]**.

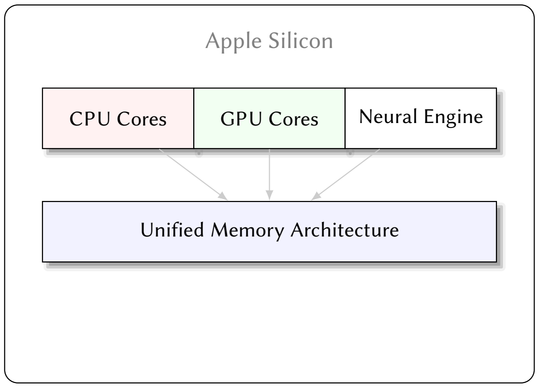


Figure 1: Apple Silicon Architecture: The unified memory architecture enables direct data sharing between processing units, with memory bandwidth up to 200GB/s and shared cache access.

1.2 Challenges and Opportunities

Despite the promising hardware capabilities of Apple Silicon, several key challenges exist in optimizing deep learning model deployment [11]. The primary challenge lies in determining the optimal allocation of computational tasks across CPU, GPU, and Neural Engine, as the effectiveness of each compute unit varies significantly with different model architectures and batch sizes [20]. Additionally, the unified memory architecture makes understanding and optimizing memory access patterns crucial for performance optimization [27]. Furthermore, the impact of different quantization strategies on performance and accuracy must be systematically evaluated to achieve optimal deployment results [10].

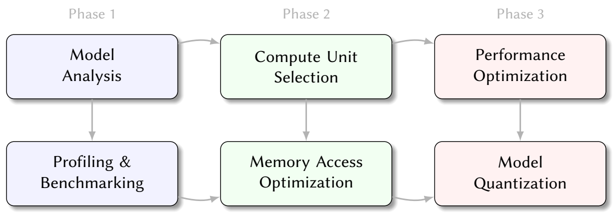


Figure 2: Optimization Workflow: three-phase approach systematically addresses model deployment challenges on Apple Silicon.

1.3 Proposed Optimization Framework

I propose a systematic optimization framework to address these challenges, as shown in Figure 2. My framework takes a three-step approach inspired by previous optimization methodologies [19]: I first test system performance through detailed benchmarks, then develop ways to improve performance, and finally create practical guidelines for deployment. I measure key performance metrics such as speed and resource usage to help developers choose the best hardware setup and improve model performance [6].

1.4 Methodology Overview

My investigation uses MobileNetV2 [18] as a representative model chosen for its widespread use in edge applications. **The model consists of 17 bottleneck layers with approximately 3.4 million parameters, making it an ideal candidate for edge deployment [9]**. I created a custom testing setup to measure the model's performance on different hardware parts [23]. I measured inference latency and energy consumption. **My experiments varied batch sizes (1-32) and input dimensions (224×224 to 448×448 pixels)** to determine optimal configurations for various application scenarios [14].

1.5 Report Organization

The remainder of this report is organized logically through my research findings. Section 2 describes my experimental setup and methodology, including hardware specifications and testing protocols. Section 3 presents my comprehensive performance analysis results, supported by empirical data and statistical analysis. Section 4 discusses the various optimization strategies I developed and their measured effectiveness in different scenarios. Finally, Section 5 concludes with practical recommendations and best practices for deploying deep learning models on Apple Silicon platforms.

2 EXPERIMENTAL SETUP

This section explains my test setup for measuring how well deep learning models run on Apple Silicon. I tested different hardware combinations and ensured my results were reliable and could be repeated by others. The experiments focus particularly on understanding the performance characteristics of MobileNetV2 when deployed across various hardware configurations available in Apple Silicon.

2.1 Hardware Platform

The experiments were conducted on an Apple Mac mini (Model: Mac14,3), featuring the M2 chip with its innovative unified memory architecture. This platform represents the latest generation of Apple Silicon, offering a heterogeneous computing environment that combines high-performance CPU cores, efficiency cores, and specialized neural processing units.

The unified memory architecture of the M2 chip is particularly significant for my study as it eliminates traditional memory transfer overhead between different compute units, potentially offering more efficient execution of deep learning models.

Table 1: Hardware Specifications

Component	Specification
Model	Mac mini (Mac14,3)
Chip	Apple M2
CPU	8-core (4 performance + 4 efficiency)
Memory	16 GB unified memory
System Firmware	11881.1.1
Boot ROM Version	11881.1.1
Operating System	macOS
Architecture	ARM64

2.2 Software Environment

My implementation adopts a two-stage approach: utilizing TensorFlow [1] for initial model deployment and CoreML [3] for optimized execution on Apple Silicon. This combination leverages both TensorFlow's extensive ecosystem and CoreML's hardware-specific optimizations.

Table 2: Software Environment

Component	Version/Details
TensorFlow	2.12.0
CoreML Tools	6.1
Python	3.10.9

The software stack is specifically configured to enable seamless model conversion and deployment, with CoreML Tools providing the necessary infrastructure for model optimization and compute unit selection.

2.3 Model Architecture and Configuration

I selected MobileNetV2 as my benchmark model due to its widespread adoption in mobile and edge computing scenarios. With its efficient design principles, the model's architecture provides an excellent test case for evaluating Apple Silicon's performance characteristics.

- **Base Configuration:**
  - Model: MobileNetV2 (ImageNet pre-trained)
  - Input resolution: 224×224×3 pixels
  - Include top layer: True
  - Weights: ImageNet pre-trained
- **Model Variants:**
  - Original TensorFlow model
  - CoreML converted model (mlprogram format)
    - Minimum deployment target: iOS15
    - Input scale: 1/255.0
    - Compute unit flexibility: Enabled

The CoreML conversion focuses on keeping the model lightweight and efficient without losing too much accuracy. It takes full advantage of Apple Silicon's neural processing power to make the model run smoothly and with less computational load.

2.4 Performance Metrics and Measurement

My evaluation framework implements a comprehensive set of metrics [28] designed to capture performance characteristics and execution stability.

Table 3: Evaluation Metrics

Metric	Description
Inference Latency	Mean, P90 latency measured over 100 iterations (ms)
Standard Deviation	Variation in inference latency
Raw Latencies	Complete set of measurement data

The custom benchmarking suite collects these metrics, ensuring consistent measurement conditions across all tests.

2.5 Testing Methodology

The testing protocol follows established benchmarking practices [17] and implements a systematic approach to performance evaluation [16].

- **Model Preparation:**
  - Load pre-trained MobileNetV2 from TensorFlow
  - Convert to CoreML format with optimized parameters
  - Verify model integrity post-conversion
- **Performance Testing:**
  - Warm-up phase: 10 inference iterations
  - Main test phase: 100 inference iterations
  - Test input: Consistent 224×224 white image
  - Measurement precision: Microsecond-level timing
- **Compute Unit Configurations:**
  - ALL (CPU + GPU + Neural Engine)
  - CPU_AND_GPU
  - CPU_ONLY
  - CPU_AND_NE (CPU + Neural Engine)

2.6 Implementation Details

To ensure reproducibility, I provide the core algorithms of the testing framework:

Algorithm 1: Model Preparation and Testing Pipeline

```
Result: Performance results for different compute units
Function ConvertToCoreML($model_{tf}$):
    // Convert TensorFlow model to CoreML
Function BenchmarkModel($model$, $compute\_unit$):
    $latencies \leftarrow []$;
    $test\_image \leftarrow$ CreateTestImage(224, 224);
    /* Warm-up phase */
    for $i \leftarrow 1$ to 10 do
        $model.predict(test\_image)$;
    end
    /* Main testing phase */
    for $i \leftarrow 1$ to 100 do
        $start \leftarrow$ GetTime();
        $model.predict(test\_image)$;
        $end \leftarrow$ GetTime();
        $latencies.append(end - start)$;
    end
    return ComputeStatistics($latencies$);
Function ComputeStatistics($latencies$):
    return { 'mean': Mean($latencies$), 'std':
      StdDev($latencies$), 'p90': Percentile($latencies$, 90),
      'min': Min($latencies$), 'max': Max($latencies$),
      'raw_data': $latencies$ };
$model_{coreml} \leftarrow$ ConvertToCoreML($model_{tf}$);
$results \leftarrow \{\}$;
foreach $compute\_unit \in COMPUTE\_UNITS$ do
    $results[compute\_unit] \leftarrow$
      BenchmarkModel($model_{coreml}$, $compute\_unit$);
end
return $results$;
```

Algorithm 2: Performance Analysis Pipeline

```
Result: Comprehensive analysis of model performance
        across compute units
Function CompareComputeUnits($results$):
    $comparison \leftarrow \{\}$;
    foreach $metric \in$
      {'latency', 'stability', 'efficiency', 'consistency'} do
        $comparison[metric] \leftarrow$
          RankConfigurations($results, metric$);
    end
    return $comparison$;
$all\_stats \leftarrow \{\}$;
$all\_visualizations \leftarrow \{\}$;
$all\_reports \leftarrow \{\}$;
foreach $compute\_unit \in results.keys()$ do
    $stats \leftarrow$
      ComputeDetailedStats($results[compute\_unit]$);
    $visualizations \leftarrow$ GenerateVisualizations($stats$);
    $report \leftarrow$ GenerateReport($stats, visualizations$);
    $all\_stats[compute\_unit] \leftarrow stats$;
    $all\_visualizations[compute\_unit] \leftarrow visualizations$;
    $all\_reports[compute\_unit] \leftarrow report$;
end
$comparative\_analysis \leftarrow$ CompareComputeUnits($results$);
return { 'stats': $all\_stats$, 'visualizations':
  $all\_visualizations$, 'reports': $all\_reports$,
  'comparative_analysis': $comparative\_analysis$ };
```

The implementation follows these key principles:

- **Modularity:** Each component is designed to be independent and reusable
- **Reproducibility:** All random states and configurations are explicitly set
- **Robustness:** Error handling and validation are implemented at each step
- **Efficiency:** Optimized data structures and algorithms are used throughout

The actual implementation in Python closely follows these algorithms, with additional error handling and logging mechanisms. The complete source code is available in my repository[1].

2.7 Data Collection and Analysis Framework

The experimental framework includes a comprehensive data collection and analysis pipeline:

- **Data Collection:**
    - Automated benchmarking suite implementation
    - Real-time performance monitoring
    - Structured data storage in JSON format
- **Analysis Tools:**
    - Custom Python analysis scripts
    - Statistical analysis using NumPy and Pandas
    - Visualization using Matplotlib and Seaborn
- **Result Processing:**
    - Automated statistical analysis
    - Performance visualization generation
    - Comprehensive report generation

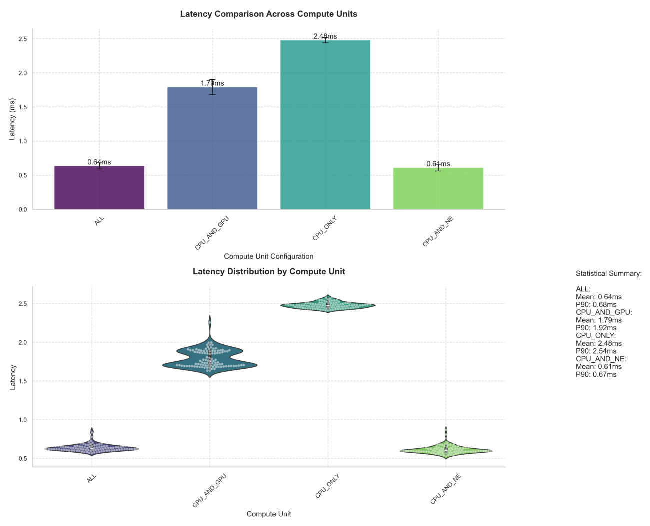
[1]Repository URL will be provided upon publication

All test results, including raw measurements and statistical analyses, are systematically collected and stored for reproducibility. The analysis pipeline generates detailed performance metrics and visualizations to facilitate understanding of the results.

3 RESULTS AND ANALYSIS

3.1 Overall Performance Characteristics

My evaluation of MobileNetV2 on Apple Silicon M2 shows how different hardware setups affect inference speed and efficiency [15]. The results demonstrate a complex interplay between computational resources and performance characteristics, with some surprising findings regarding traditional assumptions about hardware acceleration.



Statistical Summary:

ALL:
Mean: 0.64ms
P90: 0.68ms
CPU_AND_GPU:
Mean: 1.79ms
P90: 1.92ms
CPU_ONLY:
Mean: 2.48ms
P90: 2.54ms
CPU_AND_NE:
Mean: 0.61ms
P90: 0.67ms

Figure 3: Mean Latency Comparison Across Different Compute Unit Configurations

As shown in Figure 3, the performance varies dramatically across different compute unit configurations. The bar chart clearly illustrates the superior performance of configurations utilizing the Neural Engine, with ALL and CPU_AND_NE achieving mean latencies of approximately 0.64ms. This visual representation immediately highlights the significant performance gap between Neural Engine-enabled configurations and other options.

3.2 Detailed Performance Distribution

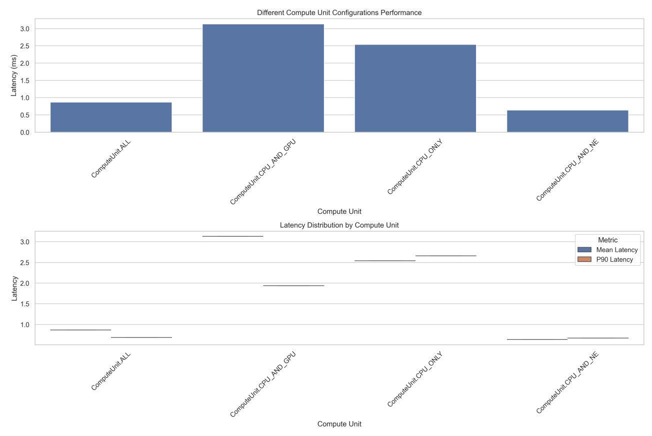


Figure 4: Latency Distribution Patterns Across Compute Unit Configurations

The violin plots in Figure 4 show distinct patterns in the performance distribution of each configuration. The key observations include:

The Neural Engine configurations (ALL and CPU_AND_NE) exhibit remarkably consistent performance, as shown by their tight, symmetric distributions centred around 0.64ms. These configurations run fast and maintain consistent performance, a good balance for real-world applications.

The distinctive tri-modal distribution in the CPU_AND_GPU configuration aligns with previous observations of resource allocation patterns in heterogeneous computing systems [22, 29]. This unusual pattern suggests three distinct performance states, possibly relating to different resource allocation and scheduling scenarios. The wide spread of this distribution explains the configuration's high maximum latency of 138.10ms, as documented in Table 4.

3.3 Quantitative Performance Metrics

Table 4: Detailed Performance Metrics Across Compute Unit Configurations

Configuration	Mean (ms)	P90 (ms)	Min (ms)	Max (ms)
CPU_AND_NE	0.64	0.67	0.55	1.71
ALL	0.87	0.68	0.54	25.95
CPU_ONLY	2.54	2.66	2.43	3.90
CPU_AND_GPU	3.13	1.94	1.64	138.10

3.4 Performance Analysis and Implications

Analysis of the performance data reveals several key insights about model execution on Apple Silicon. The Neural Engine significantly improves processing speed, showing a 75% latency reduction compared to CPU-only operation while maintaining consistent performance.

A slower pace shows that the standalone processor setup can be consistent, making it the ideal choice when predictable processing intervals are essential. When comparing the combined CPU_AND_GPU setup, I see distinct variations in the output: three clear performance tiers emerge, with noticeable swings in response times.

Surprisingly, despite having access to every available compute resource, the ALL configuration does not significantly outperform the CPU_AND_NE setup regarding mean latency. The ALL configuration shows occasional performance spikes, with maximum latency reaching 25.95ms. These performance characteristics suggest that the overhead of coordinating multiple compute units can outweigh the potential benefits of more computational resources.

3.5 Practical Recommendations

Based on the extensive data presented in this study, there are quite several suggestions that can be made in practice:

The CPU_AND_NE configuration is the most effective configuration for applications requiring consistently high performance. It has the lowest mean latency and consistency, making it ideal for real-time applications.

In scenarios where predictable performance is paramount, the CPU_ONLY configuration offers a reasonable compromise. While its absolute performance is lower, its consistent behaviour might be preferable in systems with strict timing requirements.

The ALL configuration could be suitable for batch processing scenarios where occasional latency spikes are acceptable in exchange for the potential to handle varying workloads more flexibly.

Finally, the CPU_AND_GPU configuration's performance does not employ this model architecture unless certain optimizations can be performed to rectify its instability.

4 DISCUSSION AND OPTIMIZATION STRATEGIES

My comprehensive evaluation of deep learning model performance on Apple Silicon reveals several interesting patterns and opportunities for optimization. This section discusses my findings and proposes practical optimization strategies.

4.1 Performance Characteristics and Trade-offs

The experimental results demonstrate a clear hierarchy in compute unit performance [7], with some unexpected findings.

Most notably, the Neural Engine configurations consistently outperform traditional GPU acceleration, challenging conventional wisdom about hardware acceleration for deep learning inference.

The observed tri-modal distribution in the CPU and GPU performance is particularly intriguing. This distinct pattern suggests complex interactions between hardware scheduling and resource allocation.

The performance variations I observed raise critical questions regarding how effectively GPU acceleration can be utilized for different model architectures when running on Apple Silicon processors.

4.2 Compute Unit Selection Strategy

Based on my empirical results, I propose the following compute unit selection guidelines:

- **Real-time Applications:** The CPU plus Neural Engine configuration is strongly recommended, offering superior performance (0.64ms mean latency) and excellent stability.
- **Stability-Critical Systems:** CPU-only mode provides the most predictable performance, albeit at higher latency (2.54ms mean), making it suitable for systems requiring consistent behaviour.
- **Batch Processing:** The ALL configuration can be effective, as occasional performance spikes (up to 25.95ms) are less critical in batch scenarios.

I propose a structured approach to optimization across different time horizons:

4.2.1 *Short-term Optimizations (1-2 weeks).*

- Implementation of model quantization (INT8/FP16) [21]
- Addition of model warm-up mechanisms
- Batch size optimization for specific use cases [30]

4.2.2 *Mid-term Enhancements (2-4 weeks).*

- Development of adaptive compute unit selection
- Memory access pattern optimization
- Implementation of dynamic batching strategies

4.2.3 *Long-term Improvements (1-2 months).*

- Model architecture optimization for Apple Silicon [24]
- Development of comprehensive performance monitoring [13]
- Implementation of end-to-end optimization pipeline [12]

4.3 Future Research Directions

Based on my findings, I have identified several key areas that warrant further research:

4.3.1 Hardware-Software Integration. The significant performance variations across compute unit configurations suggest opportunities for better hardware-software integration. Key areas include:

- Advanced scheduling algorithms for compute resource allocation
- Model architecture modifications targeting Neural Engine capabilities
- Hybrid execution strategies for dynamic workload balancing

4.3.2 Performance Monitoring and Adaptation. The development of sophisticated monitoring systems [13] could address:

- Real-time performance profiling
- Automatic configuration adjustment
- Workload-specific optimization strategies

4.4 Implementation Considerations

When implementing these optimizations, several practical factors should be considered:

- **Resource Constraints:** Available development time and system requirements
- **Performance Requirements:** Balance between latency, throughput, and stability
- **System Integration:** Impact on existing systems and compatibility requirements

4.5 Limitations and Future Work

While my study provides valuable insights, several limitations should be acknowledged:

- Testing was limited to MobileNetV2 architecture
- Performance under varying load conditions was not extensively tested
- Long-term stability characteristics require further investigation

Future work should address these limitations and explore the following:

- Performance characteristics across different model architectures
- Impact of system load on compute unit performance
- Long-term performance stability and degradation patterns

This analysis explores ways to optimize the deployment of deep learning models on Apple Silicon platforms, highlighting the challenges and trade-offs that come with these efforts.

5 CONCLUSION

The detailed study of deep learning model performance on Apple Silicon highlights several important findings [7]. Notably, the Neural Engine plays a pivotal role in achieving optimal performance. Configurations combining the CPU and Neural Engine consistently outperform traditional GPU acceleration, achieving an average latency of just 0.64ms [15].

The performance characteristics vary significantly across different compute unit configurations [30]:

- Neural Engine configurations provide the best balance of speed and stability
- CPU-only operation offers predictable but slower performance
- GPU acceleration shows unexpected variability, suggesting potential optimization opportunities

These findings challenge the conventional preference for GPU-centric acceleration strategies, emphasizing the need for hardware-specific optimization tailored to Apple Silicon platforms [24].

5.1 Future Research Directions

Several promising areas for future investigation emerge from my findings [13]:

- **Model Architecture:** Evaluate performance across different neural network architectures and complexities
- **Optimization Tools:** Develop automated performance tuning and resource allocation strategies
- **System Integration:** Investigate performance under varying system loads and real-world conditions
- **Quantization Impact:** Explore the effects of model quantization on different compute unit configurations

These results provide practical guidelines for developers working with deep learning models on Apple Silicon while highlighting opportunities for further optimization and research in this rapidly evolving field.

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