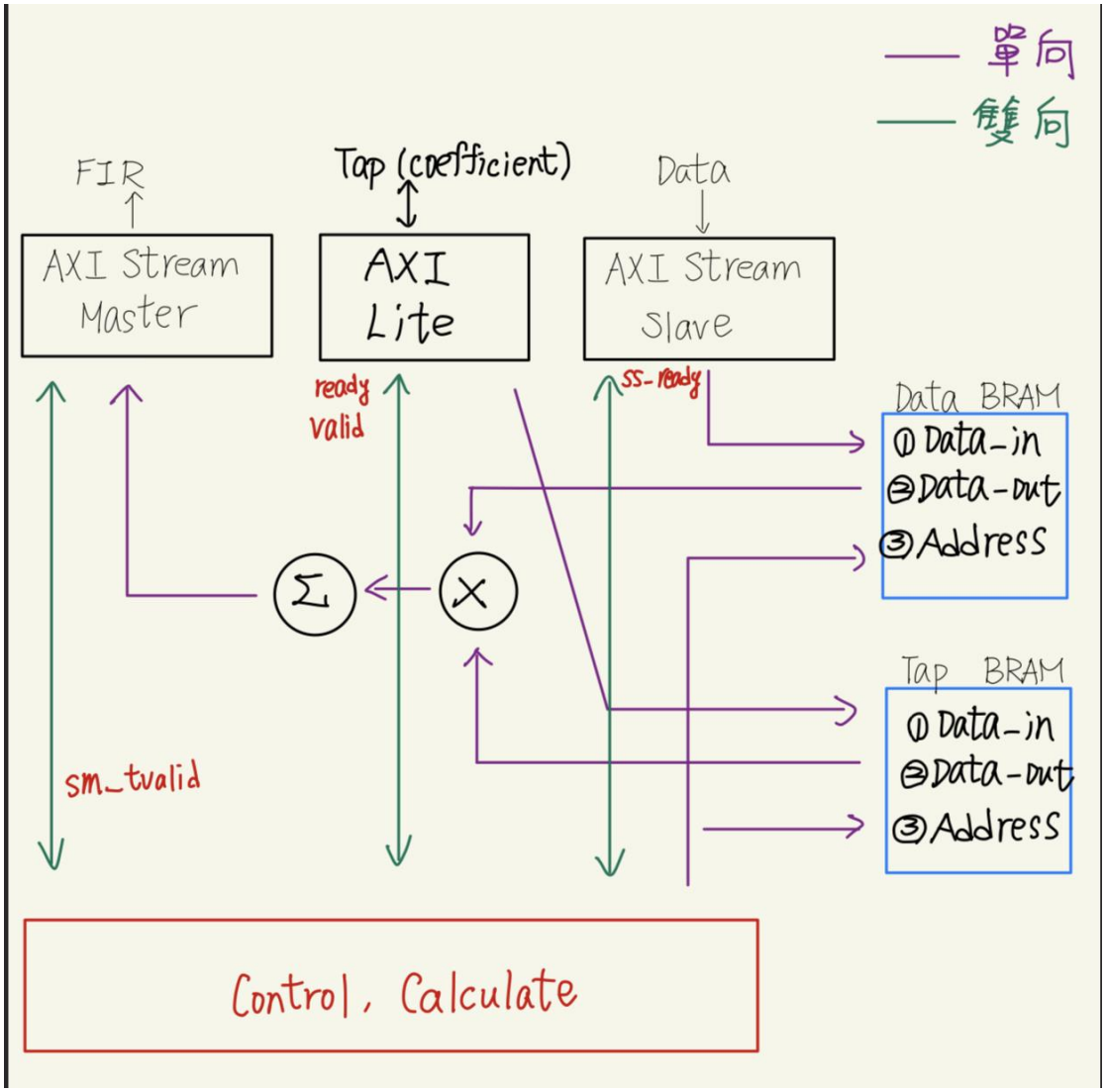
2023 SOC Lab3 Report

1.Overview:

本次實驗要求利用 Stream 進行資料的傳輸，其他如 ap_start 等其他通訊協定則要求利用 Axilite 傳輸，在 FIR 方面要求只能利用一個加法器和一個乘法器。

2.Block Diagram:



3.Operation:

從y[t] = Σ (h[i] *x[t -i])這個式子，我們可以觀察到 FIR filter 運算的規律如下：(h[1] *x[t -1])+ (h[2] *x[t -2])…，每次需要讀入一筆新的 data，而這筆 data 需要與 h[0]相乘，而上次讀入的 data 則是與 coef[1]相乘，以此類推，直到計算完11個相乘，故y[t]的累加最後一項為(h[11] *x[0])。假如data是依照讀入順序存在各個 address，我們就只需要用一個 pointer 指向最新的 data address，從此 pointer 開始依序 accesses data BRAM，將讀出的 data 依序與coef[1]…, coef[11]相乘累加，即可完成 FIR filter運算。

4.Resourace Usage:

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	194	0	0	53200	0.36
LUT as Logic	194	0	0	53200	0.36
LUT as Memory	0	0	0	17400	0.00
Slice Registers	116	0	0	106400	0.11
Register as Flip Flop	113	0	0	106400	0.11
Register as Latch	3	0	0	106400	<0.01
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	140	0.00
RAMB36/FIFO*	0	0	0	140	0.00
RAMB18	0	0	0	280	0.00

5.Timing Report:

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.111 ns	Worst Hold Slack (WHS):	0.151 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	150	Total Number of Endpoints:	150	Total Number of Endpoints:	114

All user specified timing constraints are met.

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Max Delay Paths
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Slack (MET) :             6.111ns  (required time - arrival time)
  Source:                 sm_tdata_reg_reg[1]/C
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Destination:            sm_tdata_reg_reg[31]/D
                            (rising edge-triggered cell FDCE clocked by axis_clk  {rise@0.000ns fall@5.000ns period=10.000ns})
  Path Group:             axis_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            10.000ns  (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
  Data Path Delay:        3.753ns  (logic 2.638ns (70.290%)  route 1.115ns (29.710%))
  Logic Levels:           10  (CARRY4=8 LUT2=2)
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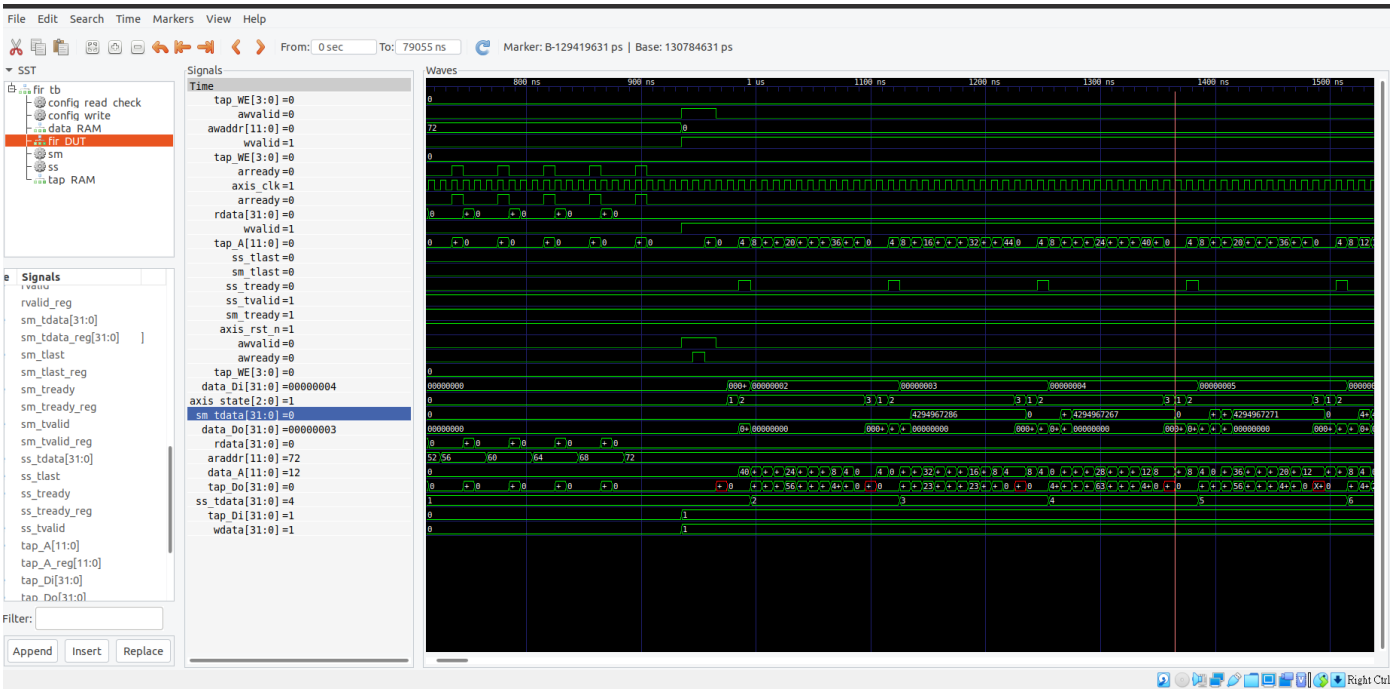
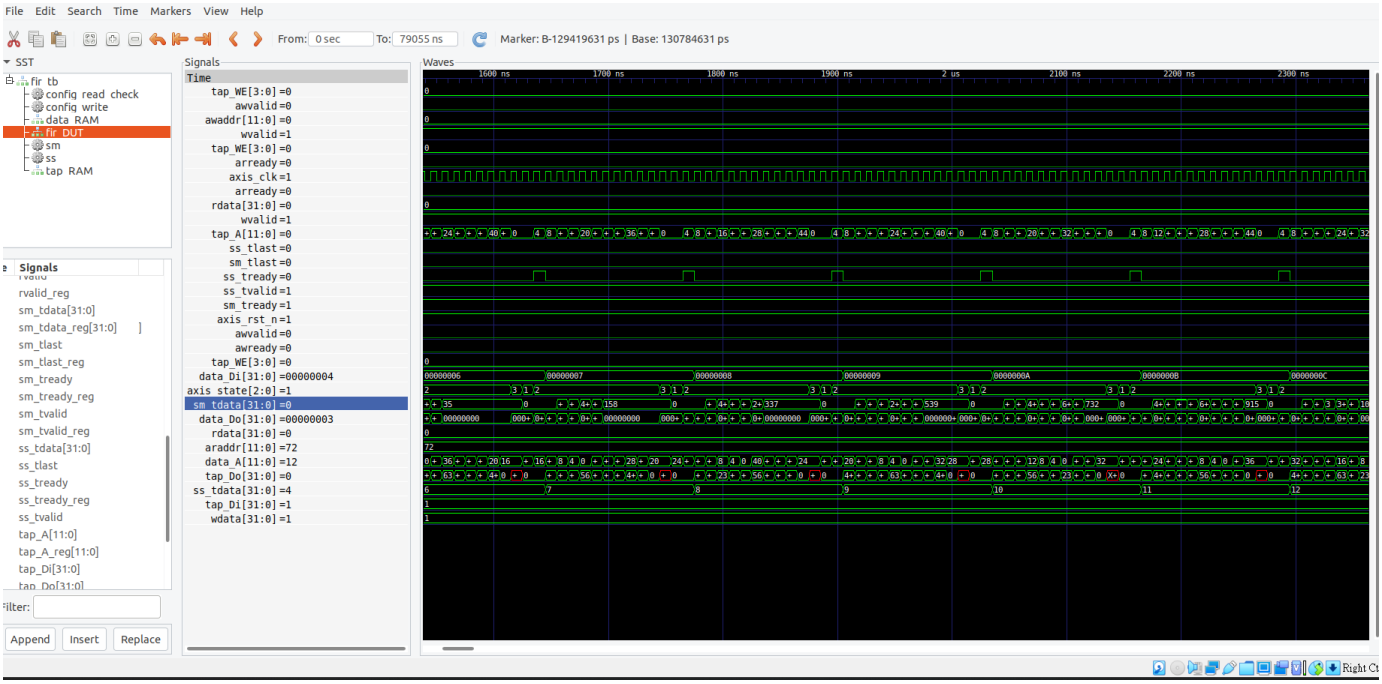
6.Simulation Waveform:

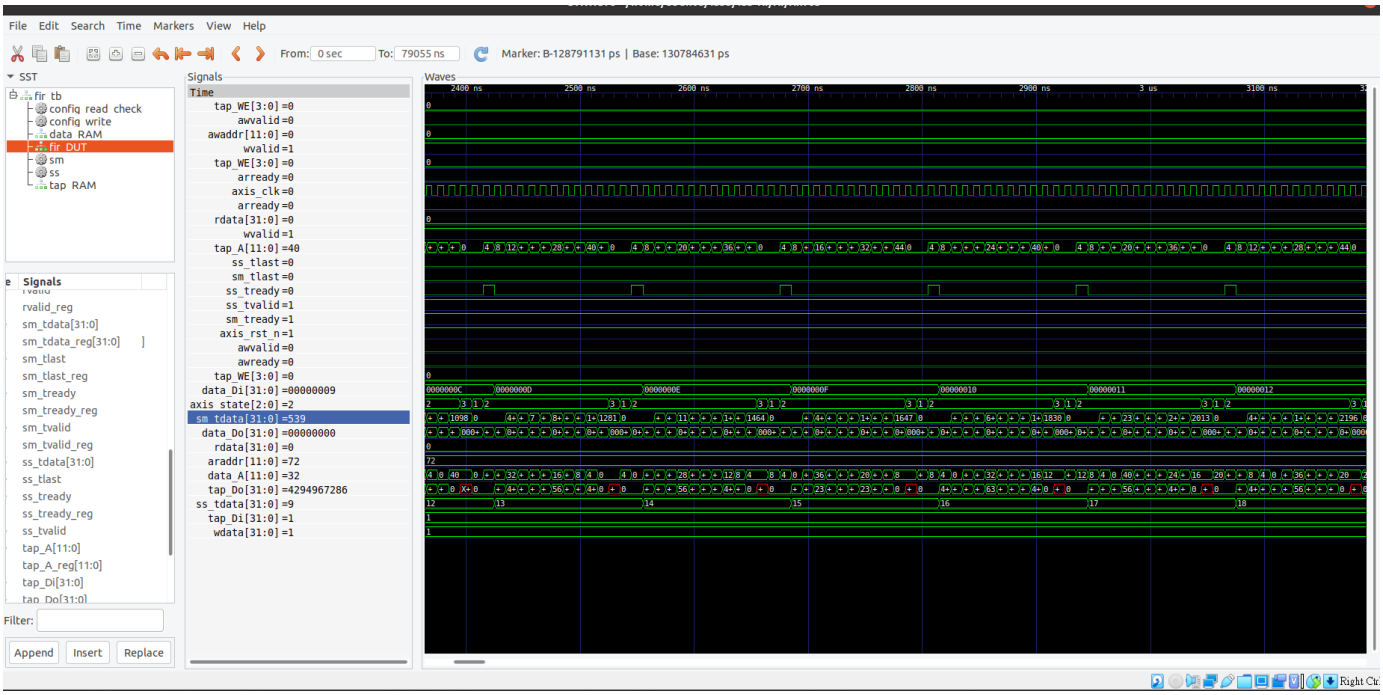
0~1500ns:



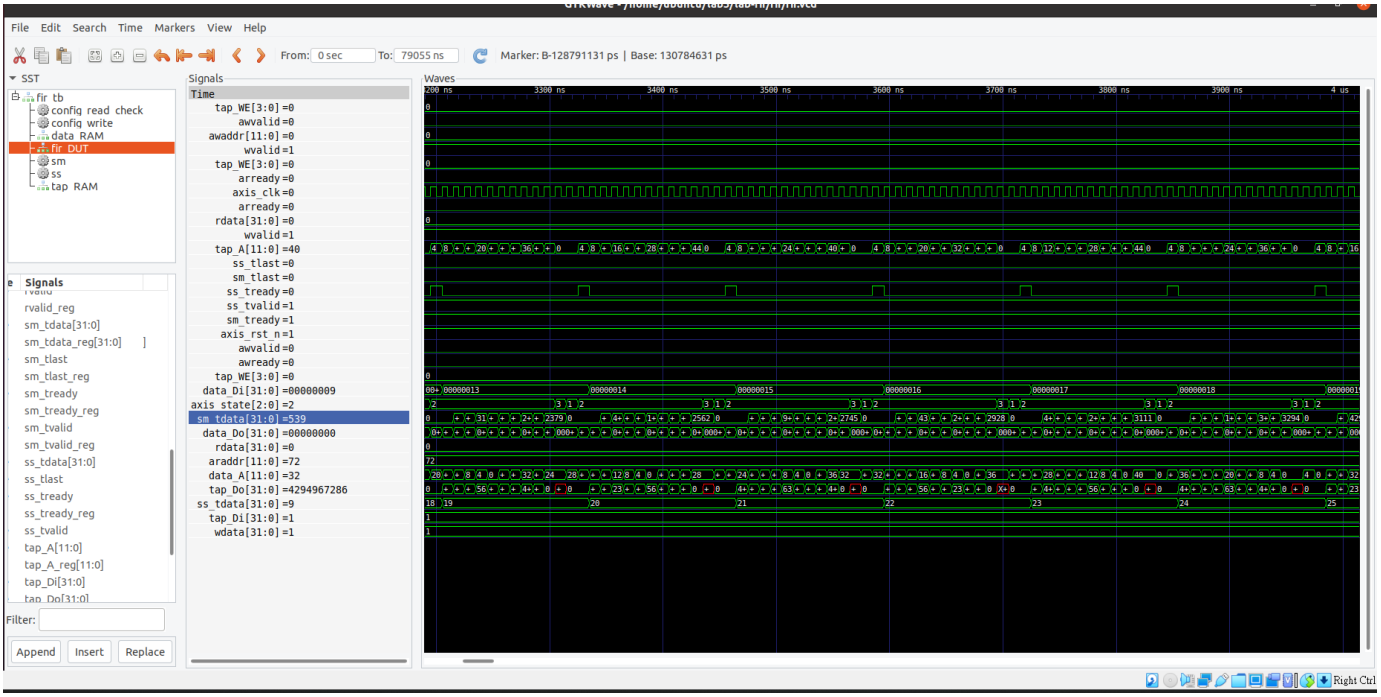
1500~2300ns:



2300~3100ns:



3100~4000ns:



4100~5000ns: