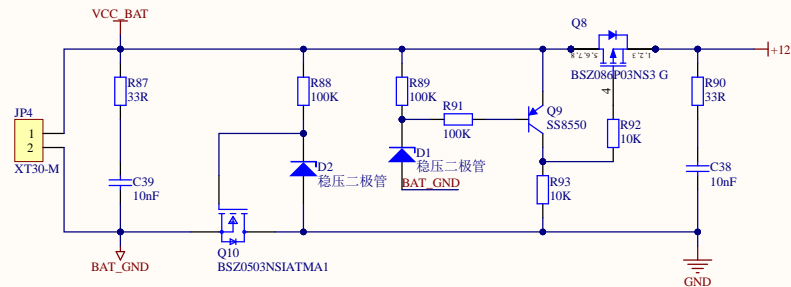
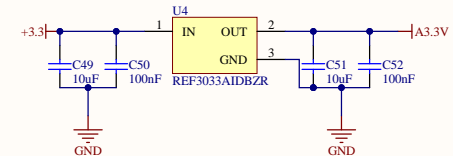




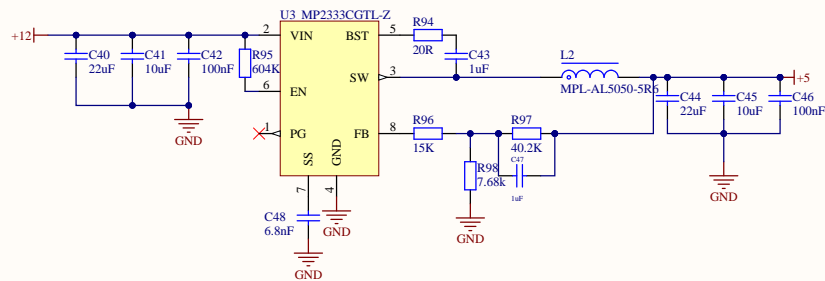
## Anti-Reverse Connection and Soft Start



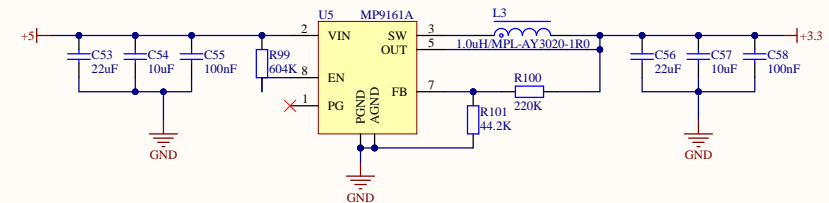
## Reference Voltage Source



## 12V->5V 3A Buck Converter



## 5V->3.3V 2A Buck Converter

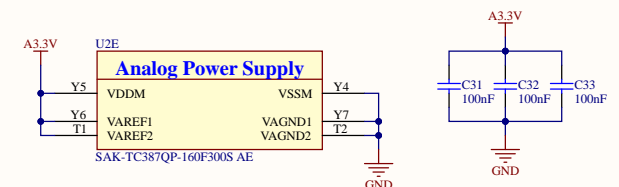


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Size	Number	Revision
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Date:	6/06/2024	Sheet of
File:	G:\Projects\...\PWR.SchDoc	Drawn By:



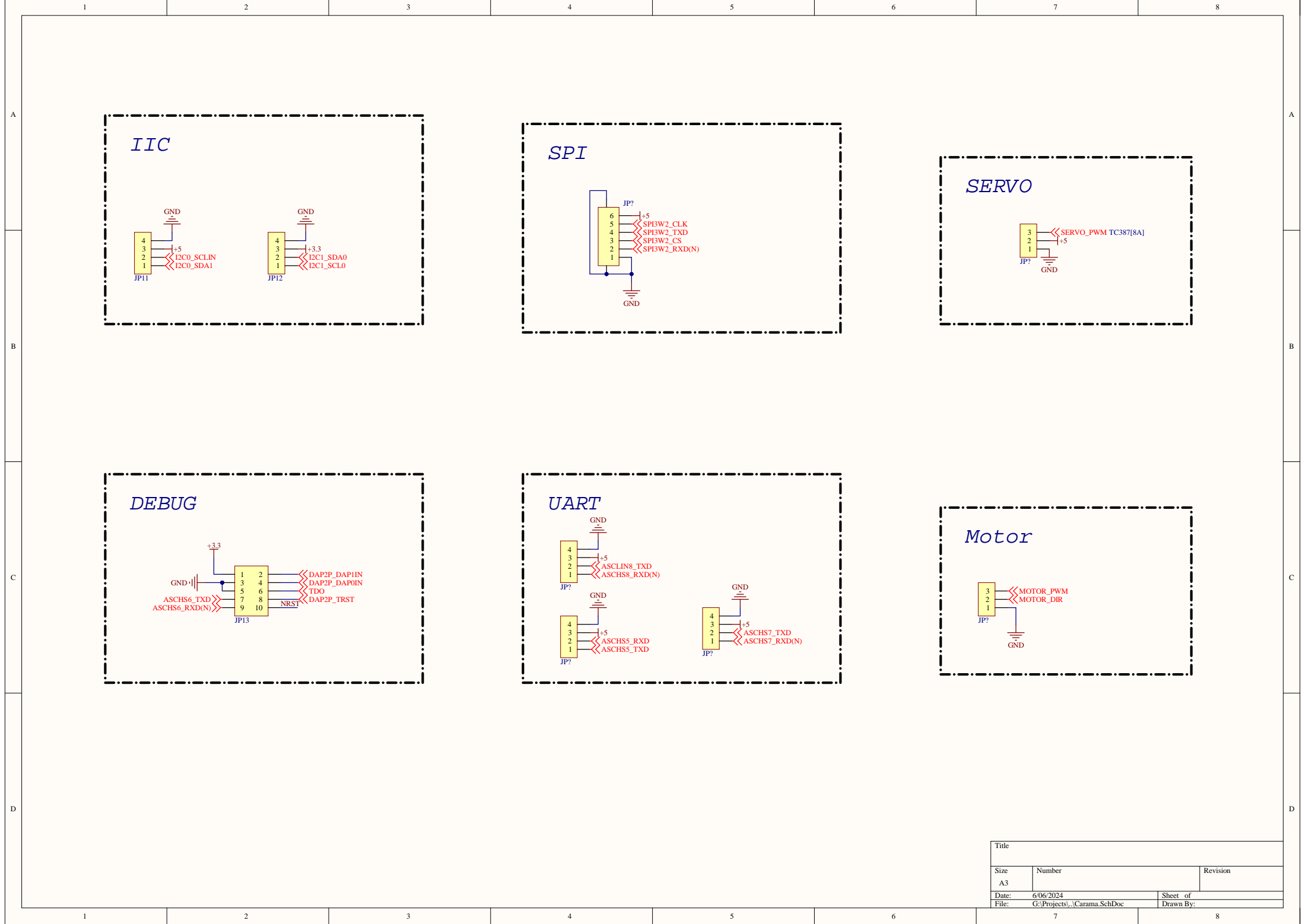
**Figure 105 EVR Switch mode topology (e) - 3.3 V single supply**

No.	HWCFG [2,1] <sup>1)</sup>	VGATE1P <sup>2)</sup> VGATE1N <sup>3)</sup>	Supply Pin Voltage Level / Source <sup>4)</sup>	Selected Supply Scheme
e.)	10 <sub>B</sub>	VGATE1P/ VGATE1N connected to gate of P- /N-ch. MOSFET.	VEXT,VEVRSB,VDDP3, VFLEX/VFLEX2 and VDDFL3 = 3.3V external supply. VDDM = VAREF <sub>x</sub> = 5V or 3.3V external supply. VDD supplied by EVRC.	3.3 V single source supply. EVRC in SMPS mode. EVR33 inactive. 5 V or 3.3 V ADC domain. 3.3 V Flexport domain. Standby Mode supported.



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SPI

JP?

6

5

4

3

2

1

+

5

SPI3W2\_CLK

SPI3W2\_TXD

SPI3W2\_CS

SPI3W2\_RXD(N)

GND

SERVO

JP?

3

2

1

+

5

SERVO\_PWM TC387[8A]

GND

DEBUG

JP13

1

2

3

4

5

6

7

8

9

10

+

3.3

GND

ASCHS6\_TXD

ASCHS6\_RXD(N)

DAP2P\_DAP11IN

DAP2P\_DAP01IN

TDO

DAP2P\_TRST

NRST

UART

JP?

4

3

2

1

+

5

ASCLIN8\_TXD

ASCHS8\_RXD(N)

GND

JP?

4

3

2

1

+

5

ASCHS5\_RXD

ASCHS5\_TXD

GND

JP?

4

3

2

1

+

5

ASCHS7\_TXD

ASCHS7\_RXD(N)

GND

Motor

JP?

3

2

1

+

5

MOTOR\_PWM

MOTOR\_DIR

GND

1

2

3

4

5

6

7

8

1

2

3

4

5

6

7

8

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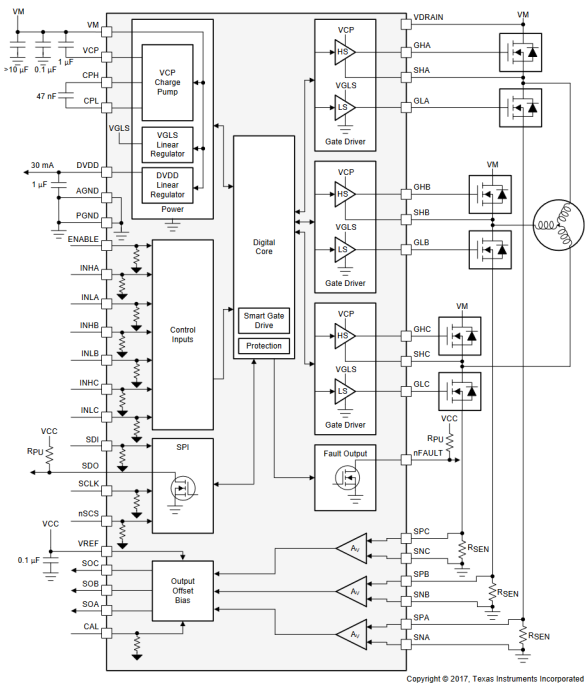
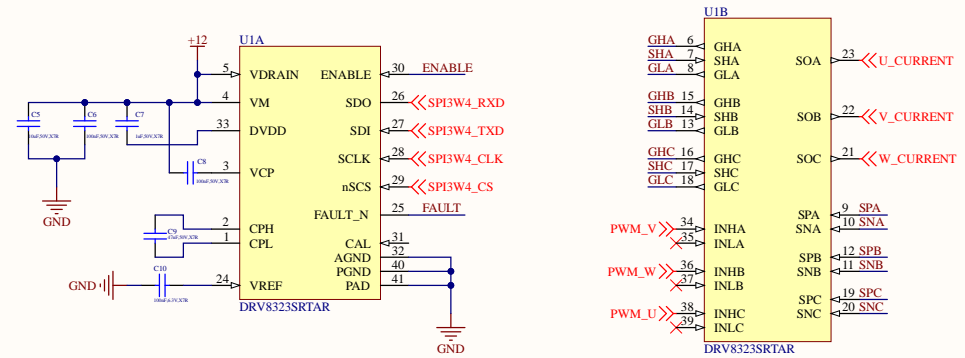


Figure 15. Block Diagram for DRV8323S

## DRV8323 Three-Phase Pre-Driver



## Power Circuit And Current Sampling

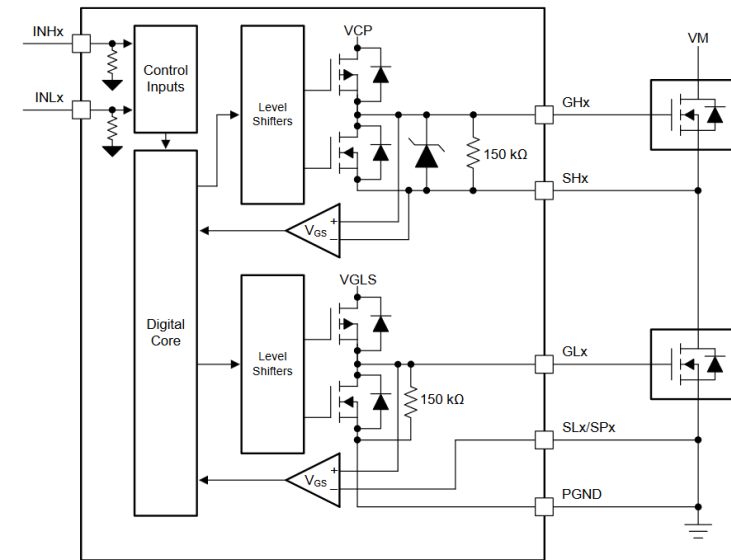
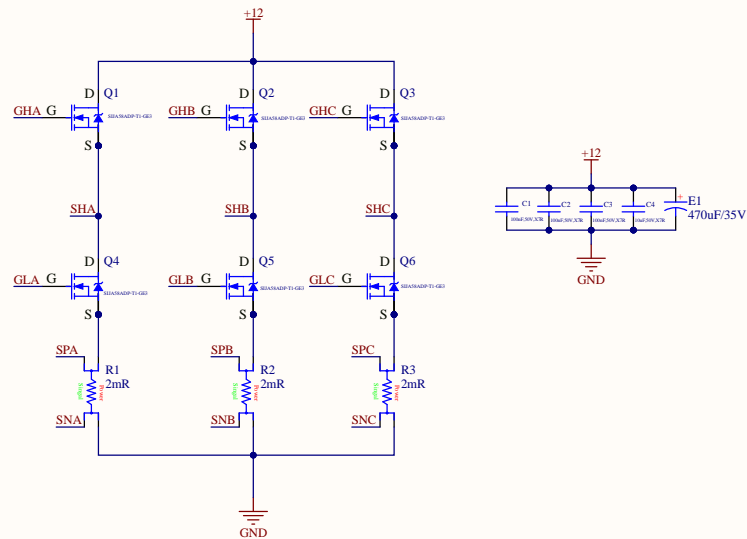


Figure 26. Gate Driver Block Diagram

Title		
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File:	G:\Projects\...\FOC.SchDoc	Drawn By:

A

B

C

D

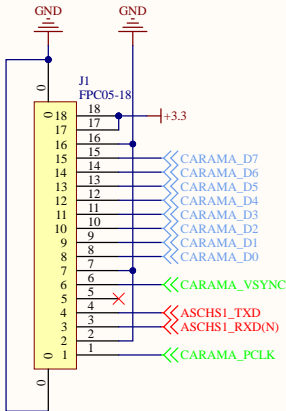
A

B

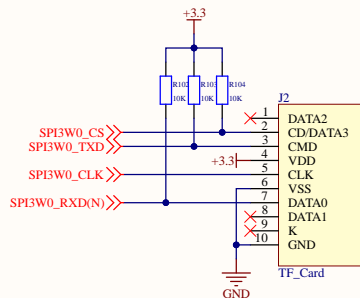
C

D

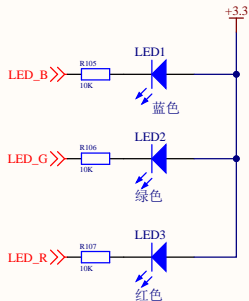
### MT9V034



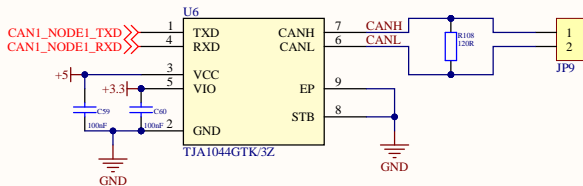
### TF CARD(SPI Mode)



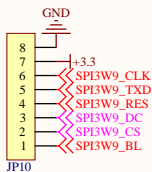
### LED



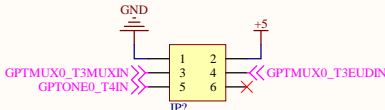
### FDCAN



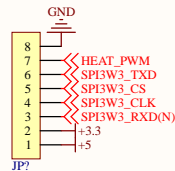
### TFT Screen



### ABZ Encoder



### IMU



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