Designator
ZYNQ-PS

Designator
ZYNQ-PL

Designator
ZYNQ-DDR3L

Designator
ZYNQ-Power

Designator
ZYNQ-JTAG

Designator
Board-Power

Designator
ZYNQ-Connecters

Designator
Others

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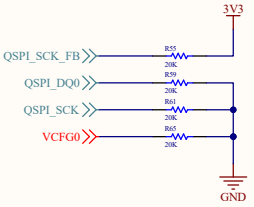
ZYNQ Boot and Configure

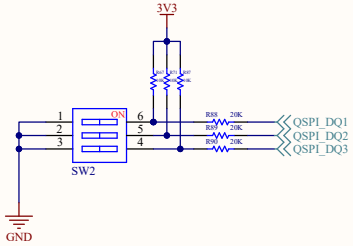
Table 6-4: Boot Mode MIO Strapping Pins

Pin-signal / Mode	MIO[8]	MIO[7]	MIO[6]	MIO[5]	MIO[4]	MIO[3]	MIO[2]
	VMODE[1]	VMODE[0]	BOOT_MODE[3]	BOOT_MODE[2]	BOOT_MODE[1]	BOOT_MODE[0]	BOOT_MODE[3]
Boot Devices							
JTAG Boot Mode; cascaded is most common[1]			0	0	0		JTAG Chain Routing[2]
NOR Boot[3]			0	0	1		0: Cascade mode
NAND			0	1	0		1: Independent mode
Quad-SPI[3]			1	0	0		
SD Card			1	1	0		
Mode for all 3 PLLs							
PLL Enabled			0	Hardware waits for PLL to lock, then executes BootROM.			
PLL Bypassed			1	Allows for a wide PS_CLK frequency range.			
MIO Bank Voltage[4]							
	Bank 1	Bank 0	Voltage Bank 0 includes MIO pins 0 thru 15.				
2.5 V, 3.3 V	0	0	Voltage Bank 1 includes MIO pins 16 thru 53.				
1.8 V	1	1					

Notes:
1. JTAG cascaded mode is most common and is the assumed mode in all the references to JTAG mode except where noted.
2. For secure mode, JTAG is not enabled and MIO[2] is ignored.
3. The Quad-SPI and NOR boot modes support execute-in-place (this support is always non-secure)
4. Voltage Banks 0 and 1 must be set to the same value when an interface spans across these voltage banks. Examples include NOR, 16-bit NAND, and a wide TPIU test port. Other interface configuration may also span the two banks.

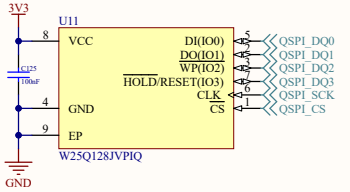
MIO[8](QSPI_SCK_FB) = 1 ---- MIO BANK 1 use 1V8
MIO[7](VCFG0) = 0 ---- MIO BANK 0 use 3V3
MIO[6](QSPI_SCK) = 0 ---- PLL Enabled
MIO[2](QSPI_DQ0) = 0 ---- JTAG In Cascade Mode

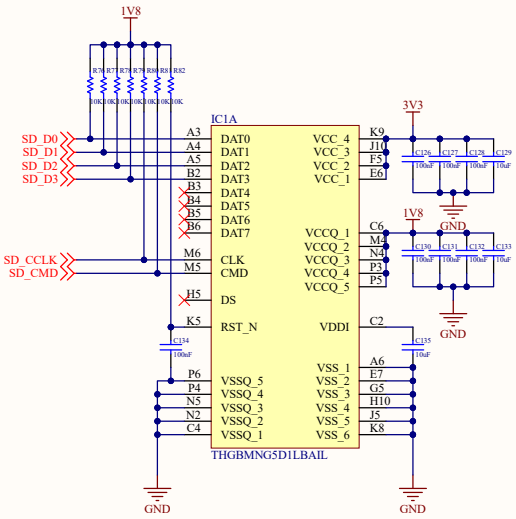




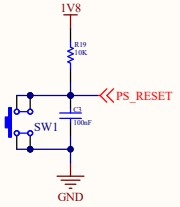
MIO[5] ---- QSPI_DQ1
MIO[4] ---- QSPI_DQ2
MIO[3] ---- QSPI_DQ3

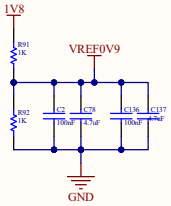
QSPI FLASH / EMMC

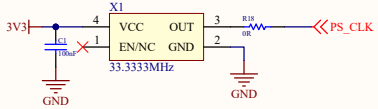




MIO VREF / RESET / CLK







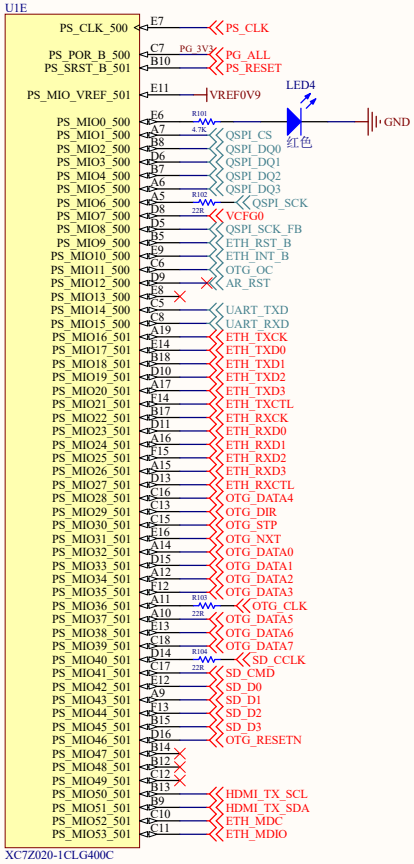


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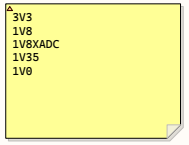
Table 2-1: **Power Pins**

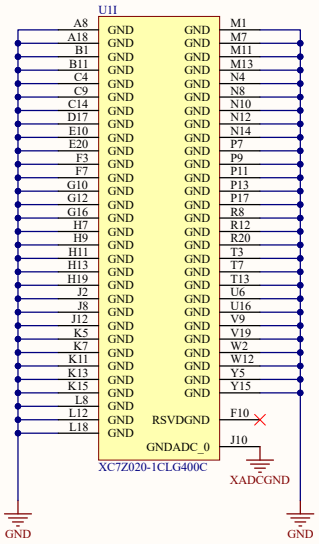
Type	Pin Name	Nominal Voltage	Power Pin Description
PS Power	V_{CCPINT}	1.0V	Internal logic
	V_{CCPAUX}	1.8V	I/O buffer pre-driver
	V_{CCO_DDR}	1.2V to 1.8V	DDR memory interface
	V_{CCO_MIO0}	1.8V to 3.3V	MIO bank 0, pins 0:15
	V_{CCO_MIO1}	1.8V to 3.3V	MIO bank 1, pins 16:53
	V_{CCPLL}	1.8V	Three PLL clocks, analog
PL Power	V_{CCINT}	1.0V	Internal core logic
	V_{CCAUX}	1.8V	I/O buffer pre-driver
	$V_{CCO\_\#}$	1.2V to 3.3V	I/O buffers drivers (per bank)
	V_{CC_BATT}	1.5V	PL decryption key memory backup
	V_{CCBRAM}	1.0V	PL block RAM
	$V_{CCAUX\_IO\_G\#}$	1.8V to 2.0V	PL auxiliary I/O circuits
XADC	VCCADC, GNDADC	N/A	Analog power and ground.
Ground	GND	Ground	Digital and analog grounds

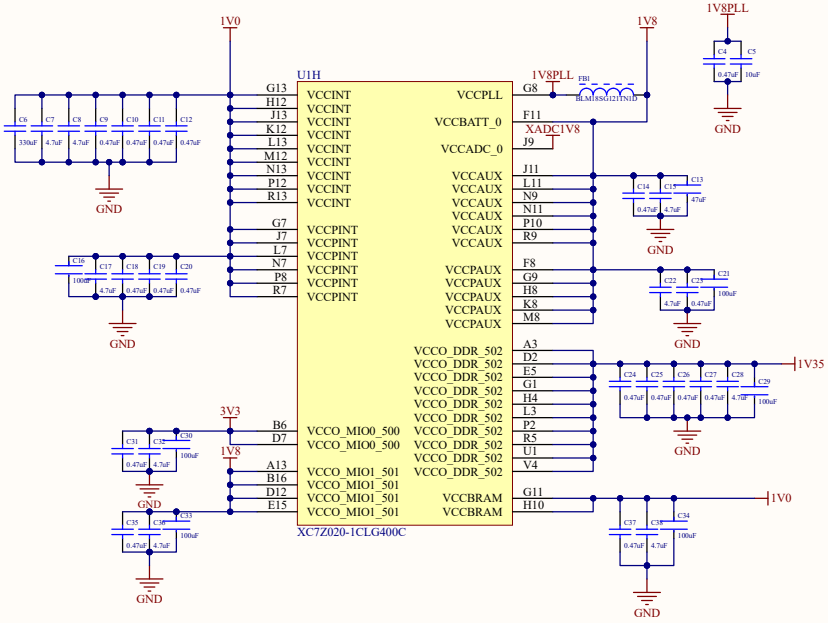
Note: Refer to the respective data sheet for recommended operating conditions.

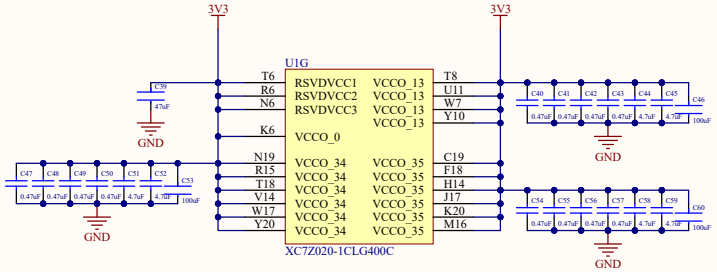
Reserved	RSVDVCC	Dedicated	Tie to V_{CCO_0}.
	RSVDGND	Dedicated	Do not connect.

XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V









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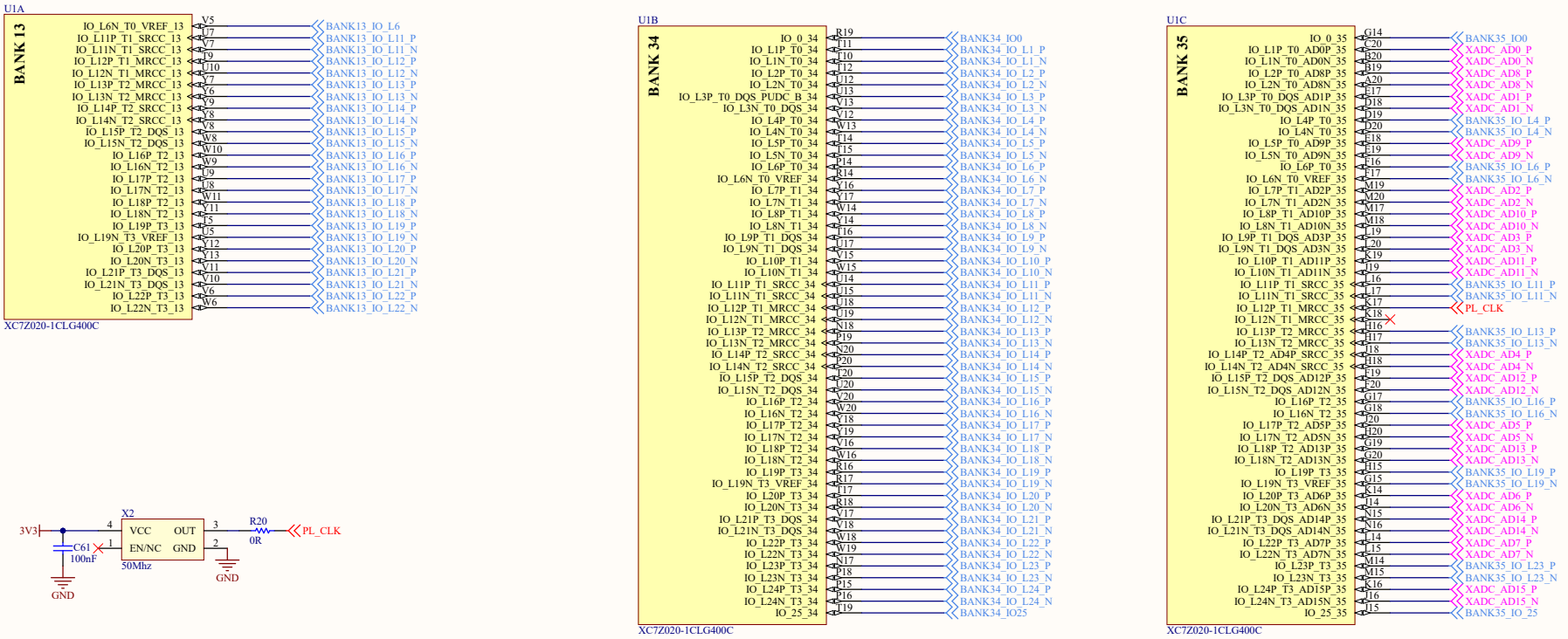

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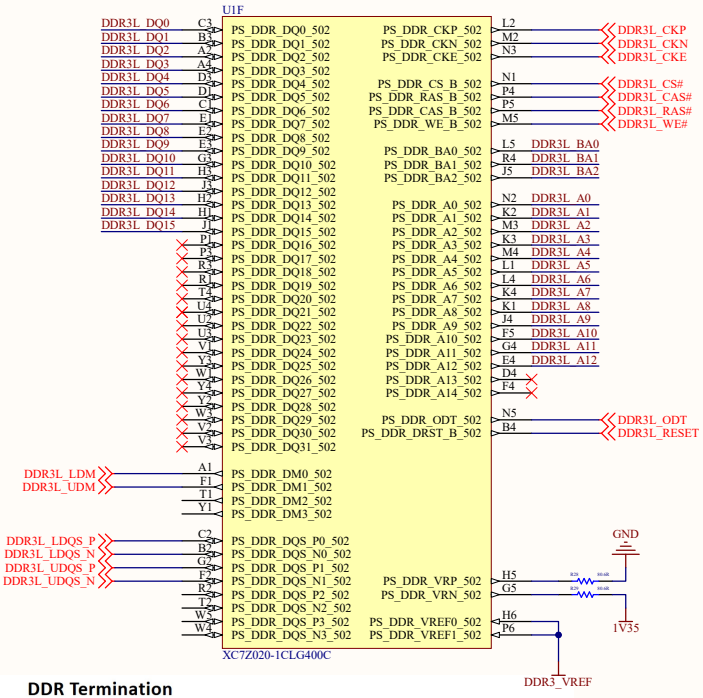

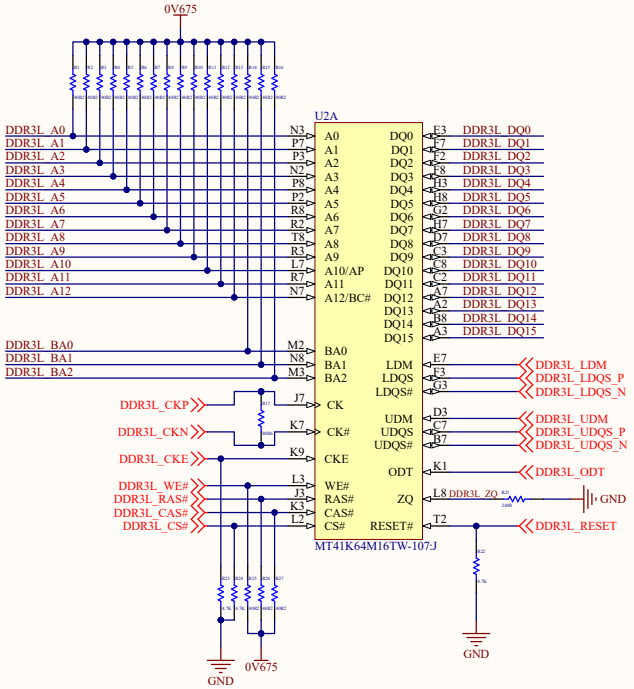

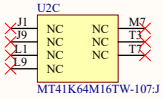

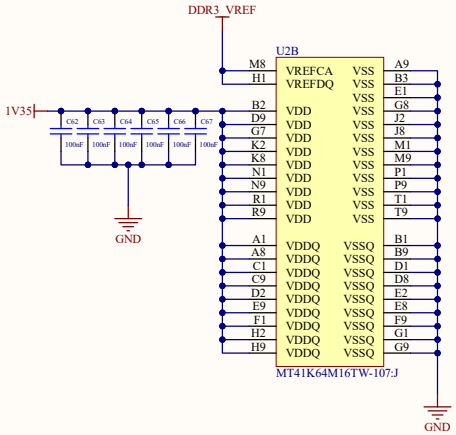

DDR Termination

For better signal integrity, DDR2 and DDR3 clock, address, command and control signals need to be terminated. For DDR2, ODT and CKE are not terminated and should be pulled down during memory initialization with a 4.7 kΩ resistor to GND. For DDR3, the DRST_B signal is not terminated and should be pulled down during memory initialization with a 4.7 kΩ resistor to GND.

LPDDR2 does not require termination.

Table 5-7 shows the DDR termination requirements.

Table 5-7: **DDR Termination**

Termination	LPDDR2	DDR2	DDR3/3L	Comments
Rterm	N/A	50Ω	40Ω	
Rclk	N/A	100Ω	80Ω	
Rdown	4.7 KΩ	4.7 KΩ	4.7 KΩ	There is no DDR_DRST_B in LPDDR2/DDR2 device side

Note: DDR3 memory also supports terminated DQS signals through the TDQS_P and TDQS_N pins. This feature is not supported on Zynq-7000 SoC devices and those pins should be left floating.

PS_DDR_VRN, PS_DDR_VRP – PS DDR Termination Voltage

PS_DDR_VRN and PS_DDR_VRP provide a reference for digitally controlled impedance (DCI) calibration. For memory types that require termination (DDR2, DDR3) VRP must be pulled Low to GND and VRN needs to be pulled High to V_{CCO_DDR}. For DDR2/3, the resistor value on VRP and VRN should be twice the memory's trace and termination impedance. For example, for a DDR3 memory with a 40Ω termination and board impedance, an 80Ω resistor must be used to pull-up/down VRP and VRN. For LPDDR2, the DCI tunes the output impedance of the driver and therefore the resistor value on VRP and VRN should be equal to the transmission line impedance, typically set to 40Ω.

Table 5-2 shows the required values for the DCI VRN/VRP pull-down/pull-up resistors.

Table 5-2: **DCI VRP and VRN Values**

	LPDDR2	DDR2	DDR3/3L
VRP/VRN	40Ω	100Ω	80Ω
	(type I DCI trace impedance 40Ω)	(type III DCI trace impedance 50Ω)	(type III DCI trace impedance 40Ω)

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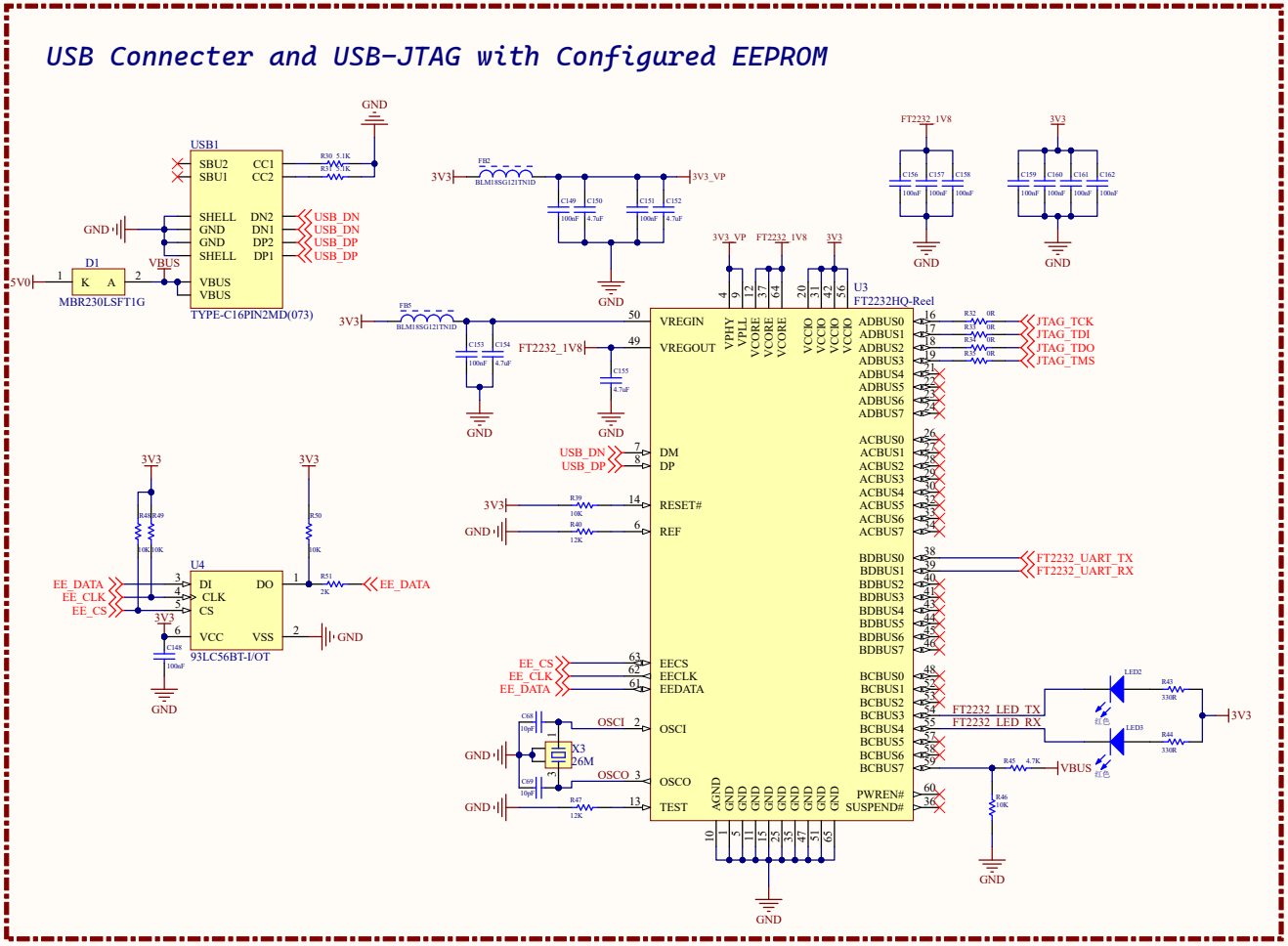
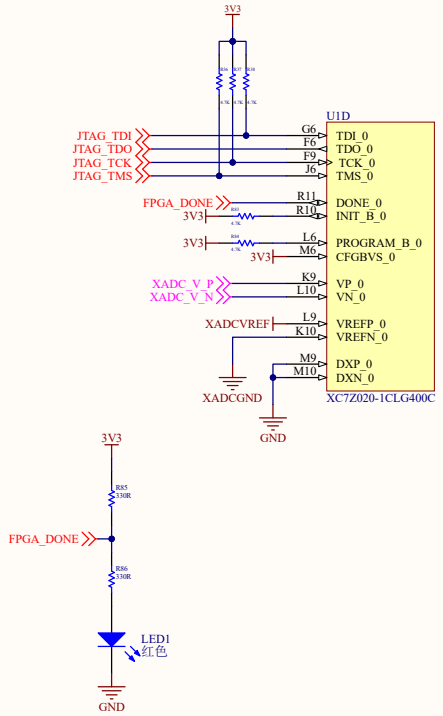
USB Connecter and USB-JTAG with Configured EEPROM



ZYNQ JTAG and FPGA Congfigure



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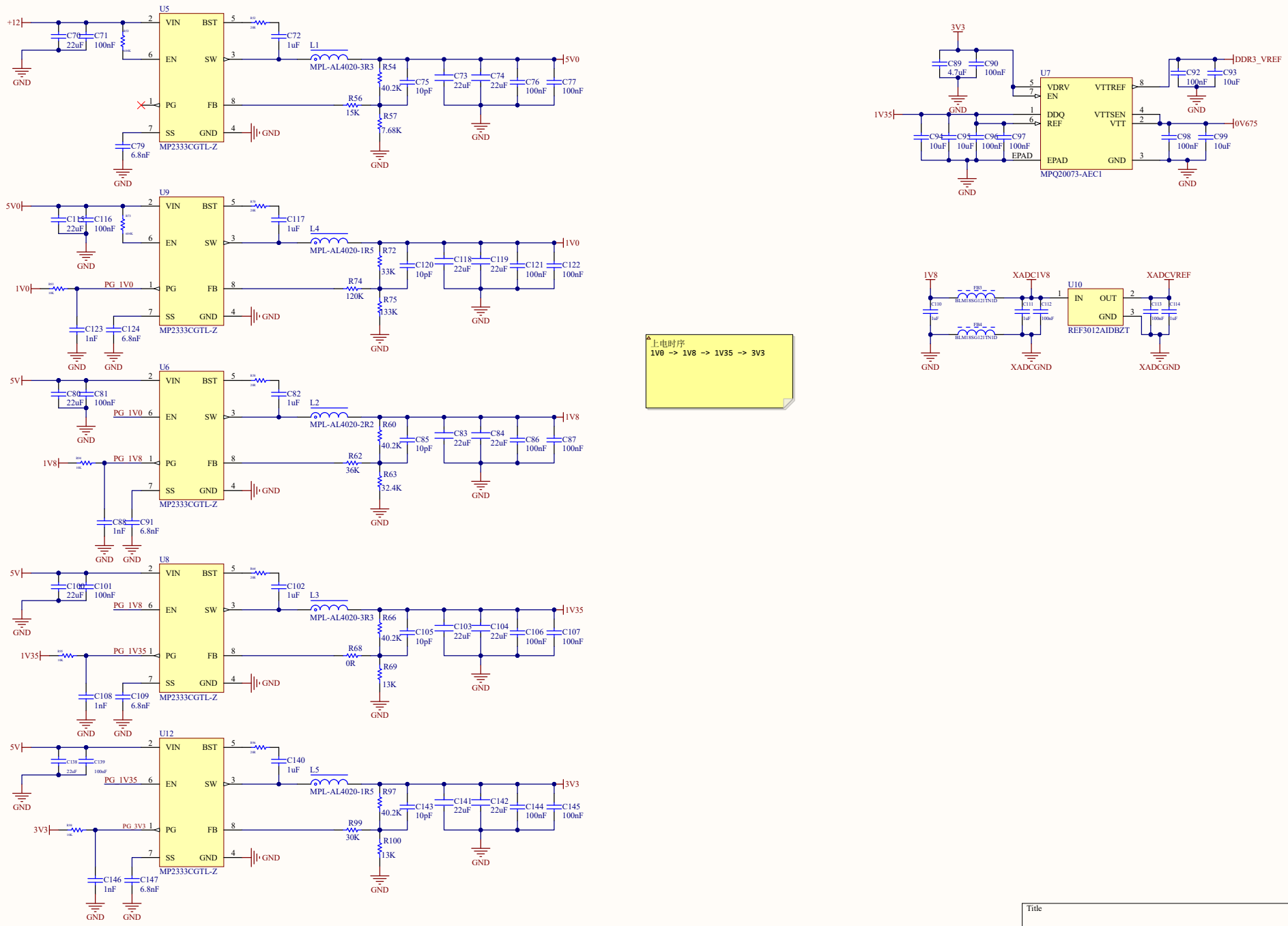

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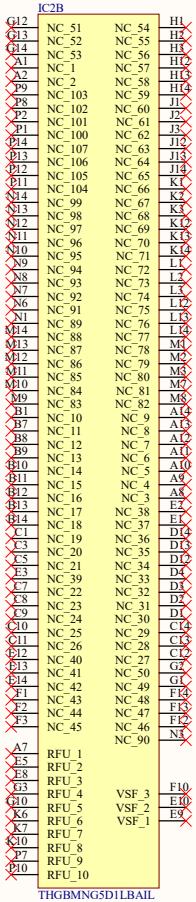

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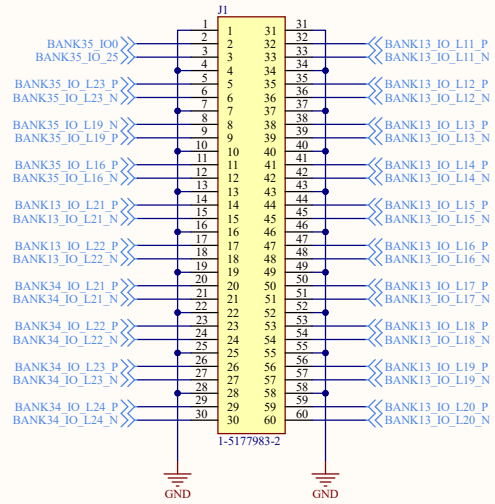

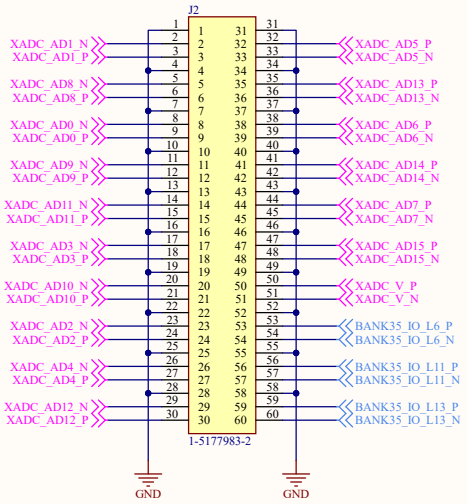

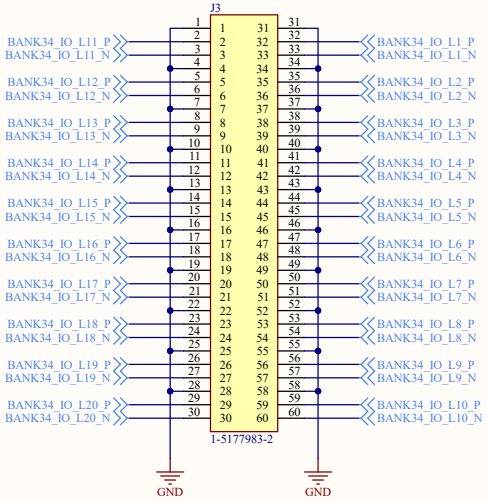

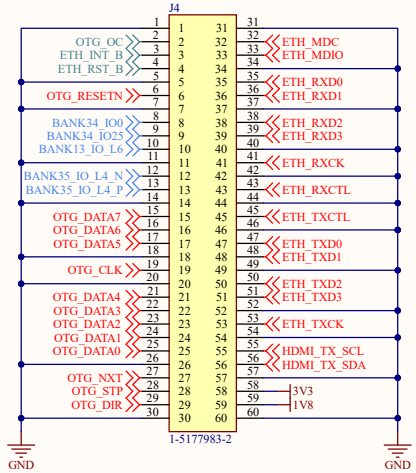

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