9. 0.500087, 2301

13. 21447.035 μ m^2, 728ps

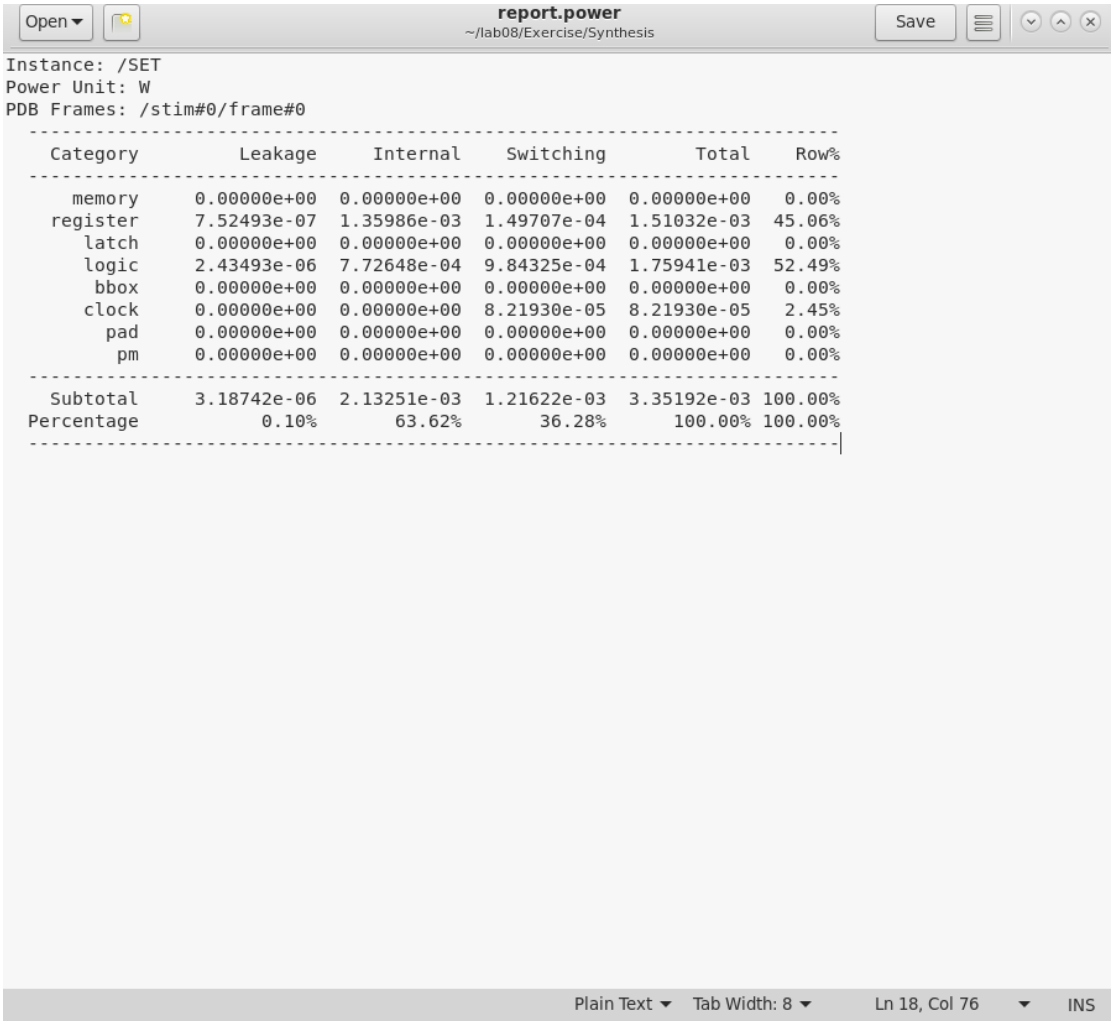
19. 3.66608 x 10^{-3} W

24. 20686.788 μ m^2, 0ps

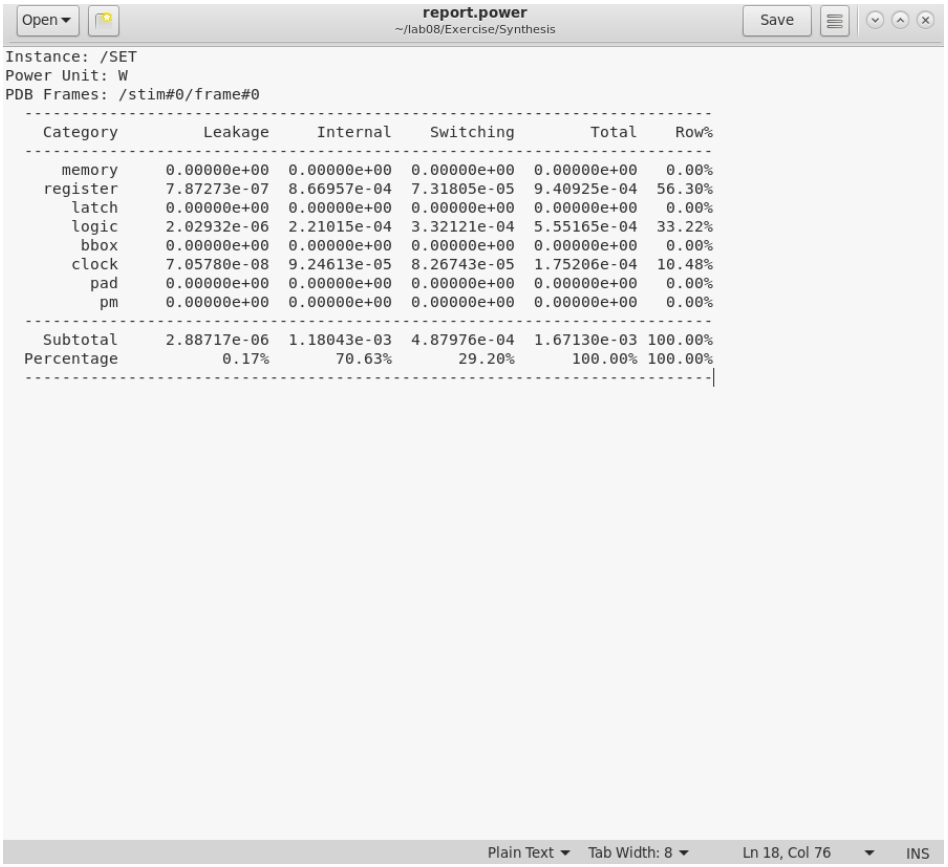
29. 1.95052 x 10^{-3} W

30. many of flip-flops are clock gated

40. 3.35192 x 10^{-3} W



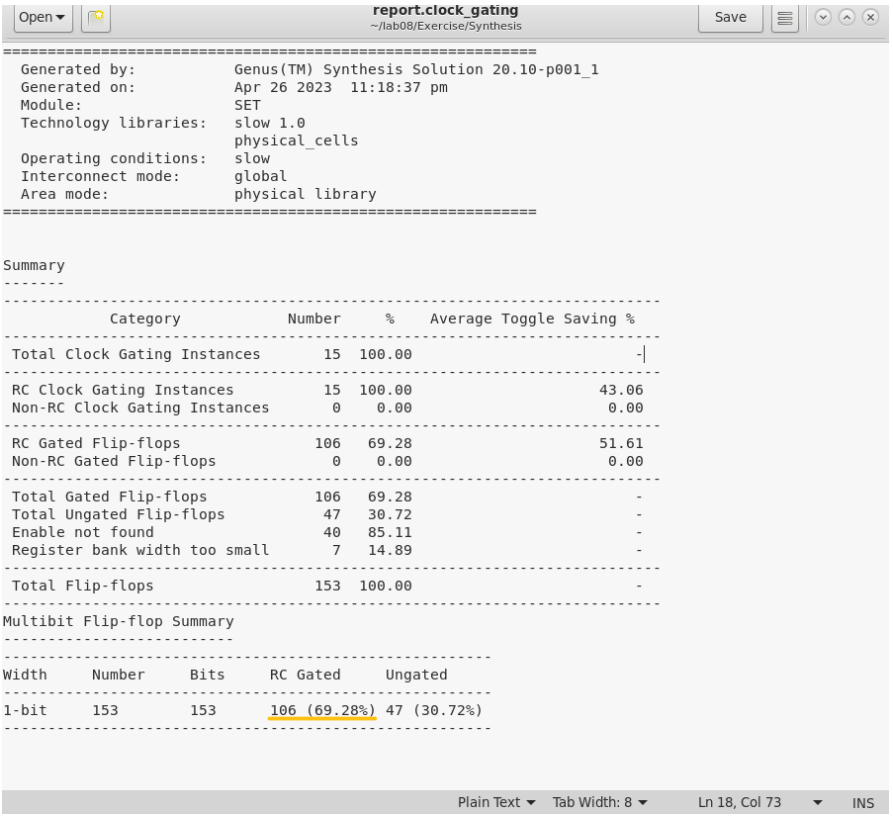
42. 1.67130 x 10^{-3} W




```
Instance: /SET
Power Unit: W
PDB Frames: /stim#0/frame#0
  ---------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ---------------------------------------------------------------------------
       memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
     register     7.87273e-07  8.66957e-04  7.31805e-05  9.40925e-04  56.30%
        latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        logic     2.02932e-06  2.21015e-04  3.32121e-04  5.55165e-04  33.22%
         bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
        clock     7.05780e-08  9.24613e-05  8.26743e-05  1.75206e-04  10.48%
          pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
           pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ---------------------------------------------------------------------------
      Subtotal     2.88717e-06  1.18043e-03  4.87976e-04  1.67130e-03 100.00%
    Percentage           0.17%       70.63%       29.20%      100.00% 100.00%
  ---------------------------------------------------------------------------
```

Plain Text Tab Width: 8 Ln 18, Col 76 INS

43. many of flip-flops are clock gated




```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 20.10-p001_1
  Generated on:           Apr 26 2023  11:18:37 pm
  Module:                 SET
  Technology libraries:   slow 1.0
                          physical_cells
  Operating conditions:   slow
  Interconnect mode:      global
  Area mode:              physical library
============================================================


Summary
-------
--------------------------------------------------------------------------------
           Category            Number     %    Average Toggle Saving %
--------------------------------------------------------------------------------
 Total Clock Gating Instances       15  100.00                          -
--------------------------------------------------------------------------------
 RC Clock Gating Instances          15  100.00                       43.06
 Non-RC Clock Gating Instances       0    0.00                        0.00
--------------------------------------------------------------------------------
 RC Gated Flip-flops               106   69.28                       51.61
 Non-RC Gated Flip-flops             0    0.00                        0.00
--------------------------------------------------------------------------------
 Total Gated Flip-flops            106   69.28                          -
 Total Ungated Flip-flops           47   30.72                          -
 Enable not found                   40   85.11                          -
 Register bank width too small       7   14.89                          -
--------------------------------------------------------------------------------
 Total Flip-flops                  153  100.00                          -
--------------------------------------------------------------------------------
Multibit Flip-flop Summary
--------------------------
-----------------------------------------------------
Width     Number     Bits     RC Gated     Ungated
-----------------------------------------------------
1-bit     153        153      106 (69.28%) 47 (30.72%)
-----------------------------------------------------
```

Plain Text Tab Width: 8 Ln 18, Col 73 INS