CSIE DIC Lab 2023

Lab14. Post-Layout STA and Verifications

In this exercise, using the layout file (**CHIP.gds**) and LVS netlist file (**CHIP_LVS.v**) in your previous lab: lab12 to check about the design's DRC and LVS by Calibre.

Data Preparation

1. Extract file from TA's directory:
   % tar xzvf ~dicta/lab14_IC61.tar.gz
2. The extracted LAB directory (**lab14_IC61**) contains.
   a. **Democase/Opus/** : Demo case Cadence DFII library for layout edition and generating GDS files for Calibre DRC/LVS.
   b. **Democase/Calibre/** : Demo case Calibre DRC and LVS command files for design rule check (DRC) and layout vs. schematic (LVS) check.
   c. **Exercise/** : Exercise directory for DRC/LVS check.

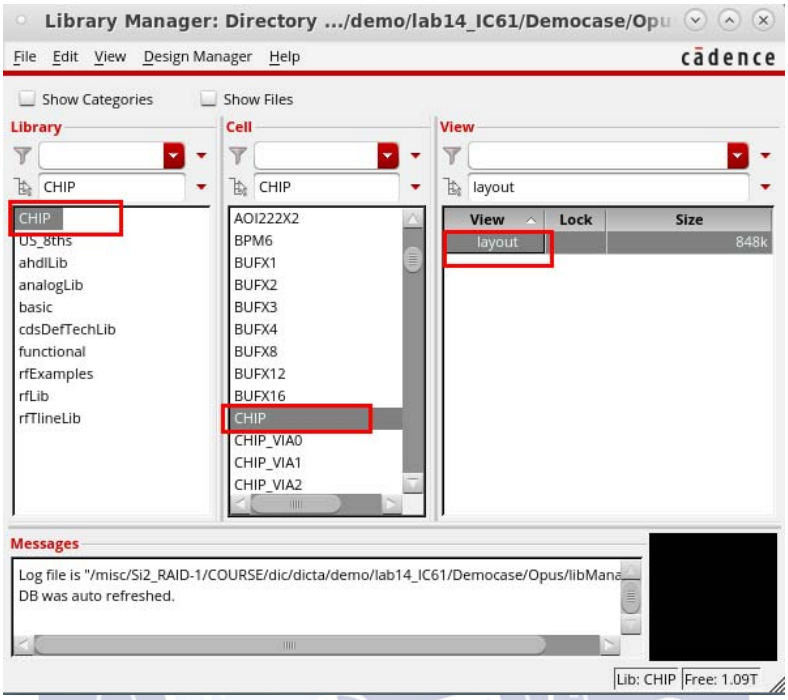
(Demo Case): Using TA provided CHIP.gds and CHIP_LVS.gds

Please follow these commands step-by-step.

Virtuso Layout Editor and DFII Environment

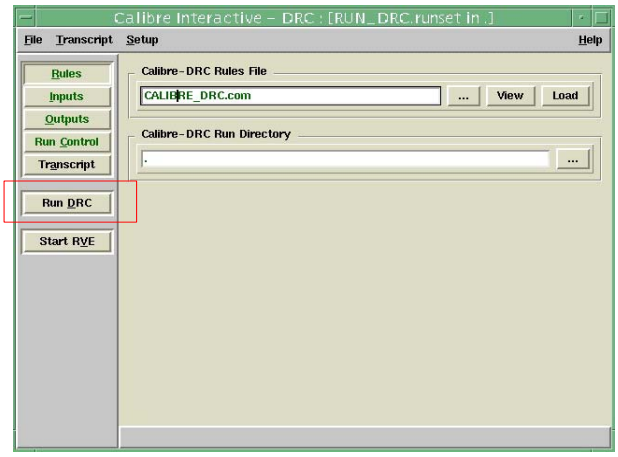
3. Change to directory: **Democase/Opus/**
4. Type **"./01_GDS_in"**.
   This script will stream-in **"CHIP.gds"** with top cell name: **"CHIP"** into DFII library (directory named: **"CHIP"**).
5. Type **"./02_GDS_out"**.
   This script will stream-out your design from Virtuoso library (Library name: **CHIP**, Cell name: **"CHIP"** and View name: **"layout"**) to GDS stream file: **"CHIP_LVS.gds"** for Calibre DRC/LVS.
   (In this step, because we didn't modify the layout, thus the generated **CHIP_LVS.gds** is the same as the **CHIP.gds**.
6. **!! Remember !!** Whenever you modified your design in DFII library for fixing some DRC/LVS errors, you must stream-out your design again to regenerate the newest **CHIP_LVS.gds** for DRC/LVS check.
7. Type **"virtuoso &"**
   to start Cadence Virtuoso environment, and then open the design layout view in Virtuoso Layout Editor.

8. In **Library Manager**, click ″**CHIP**″ in Library field → Select ″**CHIP**″ in Cell field → Double click ″**layout**″ in View field → then you will see the layout of your design.
9. You can use Virtuoso layout editor to modify your design layout if needed.



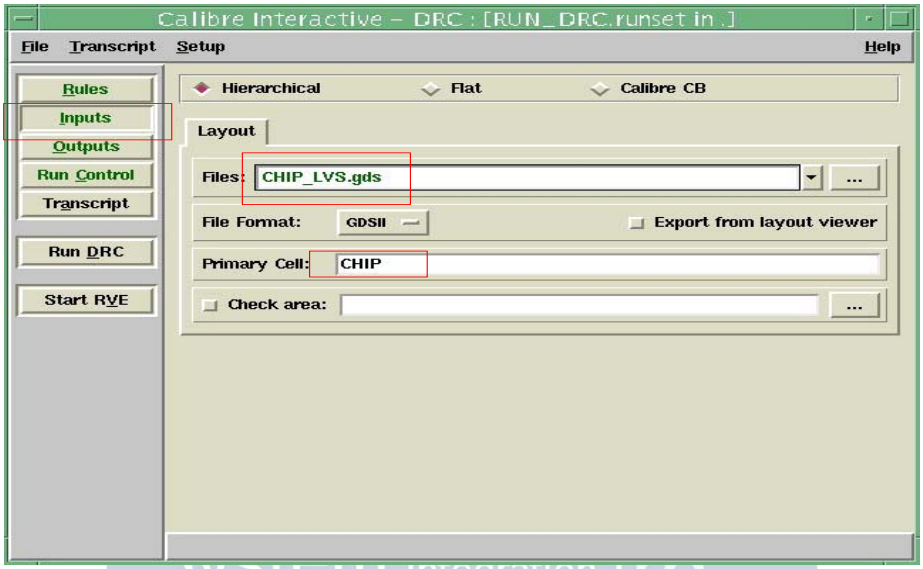
Design Rule Check (DRC)

10. Change to directory : **Democase/Calibre/DRC**
11. You must prepare your design in GDS format (**CHIP_LVS.gds**) in this directory.
12. Type ″**./01_run_drc**″
    and click on ″**RUN DRC**″ button to run Calibre DRC.

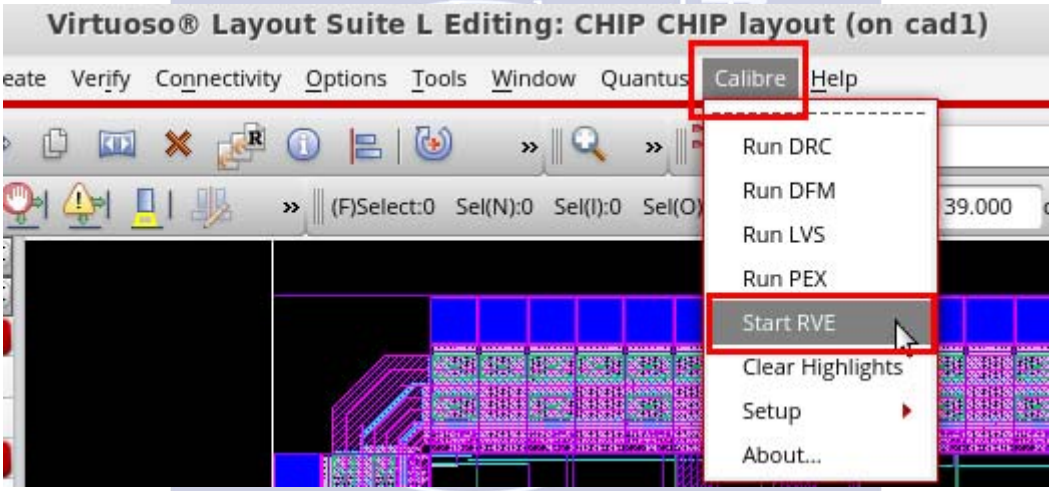


13. If you want to change the input file name and top cell name, you can click ″**Inputs**″ from left pane, and change the filename and top cell name of your design.

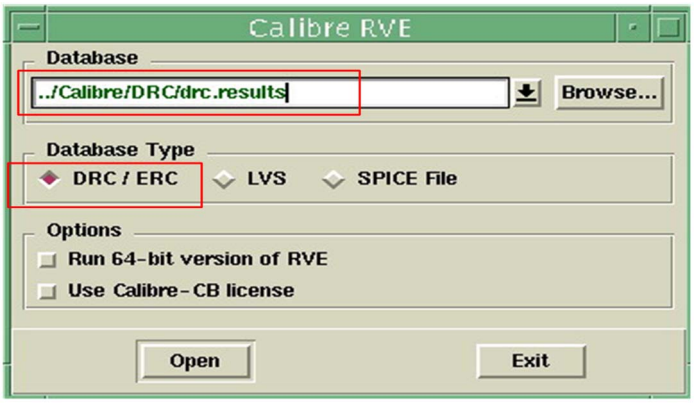
And then click on the "**RUN DRC**" to run Calibre DRC

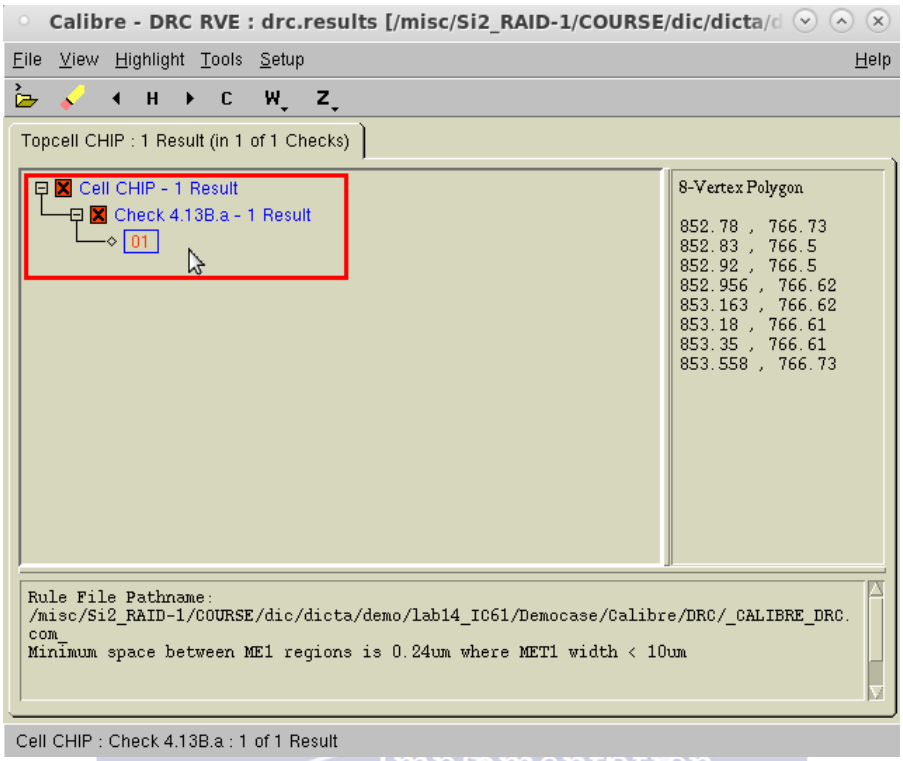


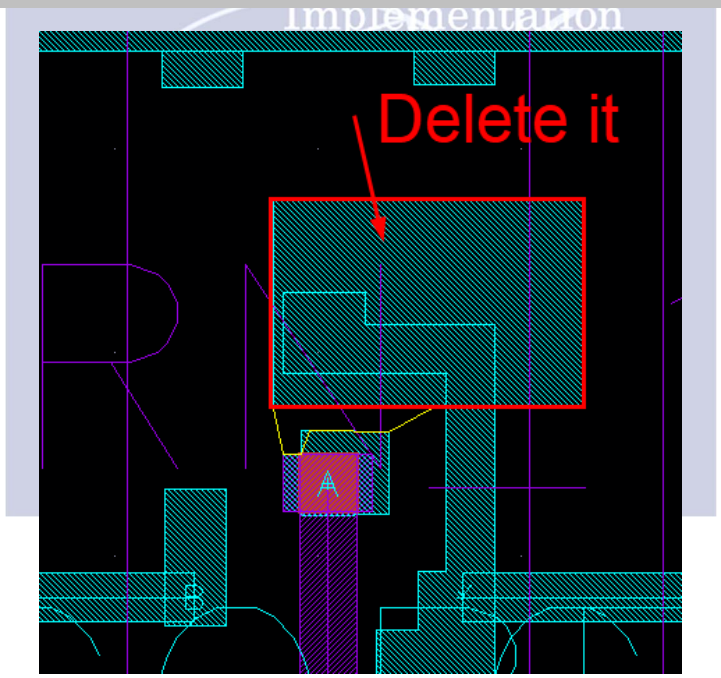
14. After DRC check is finished, close Calibre Interactive window and return to Virtuoso layout editor. In Virtuoso menu bar, select ***Calibre -> Start RVE***.



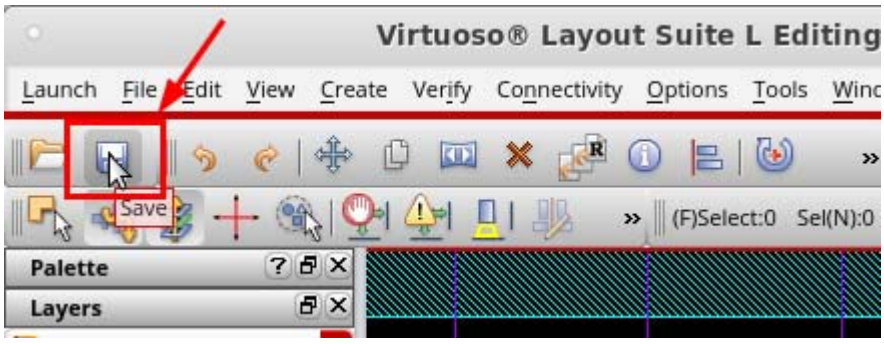
15. In RVE, open DRC results (**drc.results**) in **Democase/Calibre/DRC** directory, and then double click on each DRC errors to zoom to the location of DRC error in layout editor.







16. You can use Virtuoso layout editor to edit your layout, then save and stream out your design again after fixing DRC errors. (Execute **./02_GDS_out** again)



17. Then run the Calibre DRC again to make sure there has no DRC errors in the design.

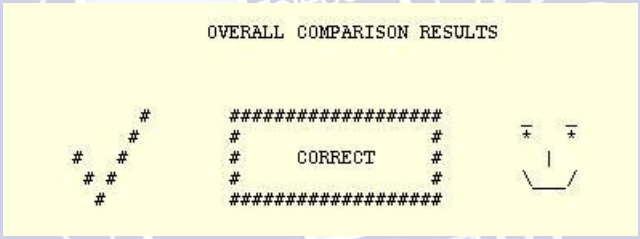
Layout versus Schematic (LVS) Check

18. Change to directory: **Democase/Calibre/LVS**
19. Before you start LVS check, you must convert your netlist (**CHIP_LVS.v**) into the SPICE netlist format.

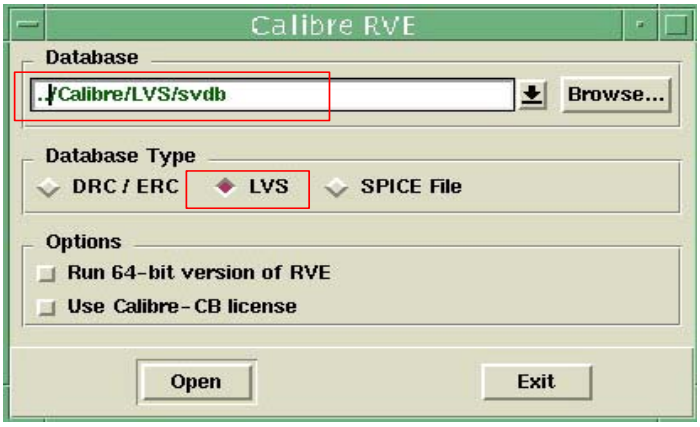
    Type **″./01_run_v2lvs″**

    to generate the SPICE netlist (**CHIP.netlist**) of your design.
20. Type **″./02_run_lvs″**

    to open Calibre Interactive Window, and then click on **″RUN LVS″** to start the LVS check.
21. If you want to change the input file name and top cell name, you can click **″Inputs″** from left pane, and change the filename and top cell name of your design. And then click on the **″RUN LVS″** to run Calibre LVS.
22. If your design passes LVS check, you will see this smile face in front of **lvs.report** file.



23. After LVS check is finished, close Calibre Interactive window and return to Virtuoso layout editor. In Virtuoso menu bar, select ***Calibre -> Start RVE***.
24. In RVE, open LVS results (**svdb**) in **Democase/Calibre/LVS** directory, and then click on each LVS errors to zoom to the location of LVS error.



25. You can use Virtuso layout editor to edit your layout and stream out your design again after fixing LVS errors. Then run the Calibre LVS check again.

Exercise

Using the layout file (**CHIP.gds**) and LVS netlist file (**CHIP_LVS.v**) of the previous lab: lab12 to verify the DRC and LVS by Calibre. Open your layout and explain your DRC report and LVS report to TAs.

You must put your layout file (**CHIP.gds**) in the directory: **Exercise/Opus**. Then follows the step 4 and step 5 to stream-in and stream-out your design to generate the GDS stream file: **CHIP_LVS.gds** for Calibre DRC/LVS.

In addition, you also need to put your LVS netlist file (**CHIP_LVS.v**) in the directory: **Exercise/Calibre/LVS** for Calibre LVS.