CSIE DIC Lab 2023

Lab10. Scan Chain Insertion and ATPG Training

Data Preparation

1. Extract LAB data from TA's directory:
   % tar xzvf ~dicta/lab10.tar.gz
2. The extracted LAB directory (**lab10**) contains:
   a. **RTL/** :RTL source code of design
   b. **Synthesis/** :Synthesis script and scan chain insertion
   c. **Netlist/** :Synthesized netlist and test pattern for gate-level simulation
   d. **TMAX/** : TestMAX working directory for ATPG

Lab Note

The design used in this lab is an image smoothing engine circuit. The following steps will explain how to run scan chain insertion and ATPG. The requirement of this lab is to complete the entire flow and answer the listed questions.

Prepare the design netlist and STIL file

3. Change to the directory: **RTL/**
4. Run RTL simulation
   % ncverilog –f run.f
5. Change to the directory: **Synthesis/**
6. Open the cell library datasheet (**evince ~dicta/lab01c_lib/umc18.pdf &**) and understand the functionality of scan-type cell ***SDFFXL***.
7. Perform logic synthesis
   % ./01_run_synthesis
8. Open and read the synthesis script with scan chain insertion and timing/area reports
   % gedit SYN018_RC_DFT.tcl &
   % gedit report.area &
   % gedit report.timing &
9. Change to the directory: **Netlist/**
10. Open and read the generated standard test interface language (STIL) file
    % gedit ISE.stil &
11. In the "Signal Groups" section, what is the signal name for "_si" and "_so" groups?

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12. In the "ScanStructures" section, what is the length of the scan chain? _____
13. In the "ScanStructures" section, what is the signal name for the ScanEnable signal?_____
14. Open and read the test bench, in the normal mode, the value of the ScanEnable signal should be set to 0.
    % gedit TEST_gate.v &
15. Run gate-level simulation,
    % ncverilog –f run.f

TestMAX: ATPG

16. Change to the directory: **TMAX/**
17. Open and read the script for TestMAX
    % gedit ATPG018.tcl &
18. Execute command **01** to run TestMAX and generate fault coverage report and test patterns
    % ./01_run_tmax
19. Open and read the log file of TestMAX.
    % gedit run.log &
20. In the "Uncollapsed Stuck Fault Summary Report," what are the total faults?
    _____
21. What is the test coverage?_____
22. How many patterns are generated?_____
23. Open and read the generated test patterns in STIL format
    % gedit patterns.stil &

TestMAX: Fault Simulation

24. Before run fault simulation, execute command **02** to convert the test pattern file to the Verilog test bench.
    % ./02_stil2verilog
    (test_bench.v and test_bench.dat are generated)
25. Run Verilog fault simulation
    % ncverilog –f run.f
26. How many mismatches is in this simulation?_____
27. Open ***ISE_syn.v*** and search for any buffer cell, for example, ***BUFX12*** (instance name: g17020). Find the wire name of port ***A***. Add one stuck-at-1 (S-A-1) fault to this cell input by replace ***n_11*** as ***1'b1***:
    BUFX12 g17020(.A (**n_11**), .Y (n_84));
    to

BUFX12 g17020(.A (**1'b1**), .Y (n_84));

28. Run Verilog fault simulation again

    % ncverilog –f run.f

29. How many mismatches are in this simulation?_____