CSIE DIC Lab 2023

LAB01C. APR Data Preparation

Data Preparation

1. Extract LAB data from TA's directory:
   % tar xzvf ~dicta/lab01c.tar.gz
2. The extracted LAB directory (**lab01c**) contains:
   a. **p0/** : Cell library database and datasheet for APR
   b. **p1/** : Capacitance table for APR

Reading Cell Library Datasheet

3. Change to the directory: **p0/**
4. Open and read the CORE cell library datasheet.
   % evince umc18.pdf &
5. Search for cell: **CLKBUFXL** and cell: **BUFXL**, and find out what is the major difference between these cells?

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6. Search for cell: **CLKBUFXL** and cell: **BUFXL**. If these cells both have 0.1pF loading. What is the T_{PHL} and T_{PLH} delay for these cells?

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7. Suppose 10 **CLKBUFXL** cells are connected in series to build up a buffer chain. In addition, a 100MHz clock with a 50% duty cycle is input in this buffer chain input. What is the duty cycle of this buffer chain's output?

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8. Suppose 10 **BUFXL** cells are connected in series to build a buffer chain. In addition, a 100MHz clock with a 50% duty cycle is input in this buffer chain input. What is the duty cycle of this buffer chain's output?

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9. Open and read the I/O PAD cell library datasheet.
   % evince umc18io3v5v.pdf &
10. Search for cell: ***POC16C***. If this cell have a 20pF loading. What is the T_{PHL} and T_{PLH} delay for this cell? _____

Reading Timing and Power Model (.lib)

11. Change to the directory: **p0/**
12. Open and reading timing && power model file in worst-case condition.
    % gedit slow.lib &
13. Search for cell: ***INVXL***, and find out the non-linear delay/power model of output pin: Y, and find out the max capacitance and leakage power value of this cell:

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14. Open and read the timing && power model file in best-case condition.
    % gedit fast.lib &
15. Search for cell: ***INVXL***, and find out the non-linear delay/power model of output pin: Y, and find out the max capacitance and leakage power value of this cell:

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Reading Verilog Model (.v)

16. Change to the directory: **p0/**
17. Open and read the Verilog model file of the CORE cell library.
    % gedit umc18_neg.v &
18. Open and read the Verilog model file of the I/O PAD cell library.
    % gedit umc18io3v5v.v &

Reading Cell Library Information for APR (.lef)

19. Change to the directory: **p0/**
20. Open and reading the technology information file (.lef)
    % gedit umc18_6lm_tech.lef &
    In umc18_6lm_tech.lef, try to find out the max width for met1 to met6 and find out the pitch setup for met1 to met6? _____
21. Open and read the .lef file of the CORE cell library.
    % gedit umc18_6lm_core.lef &
    Search for cell: ***INVX20***, and find out the obstruction information of this cell.

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22. Open and read the .lef file of the I/O PAD cell library.
    % gedit umc18io3v5v_6lm.lef &

Reading and Generating Capacitance Table (.captbl)

23. Change to directory: **p1/**
24. Open the process definition file (.ict).
    % ./01_run_viewict
25. In ViewICT GUI, click on the button: "**Process**," "**Conductor**," "**Dielectric**," and "**Vias**" to see the detail of this process.
26. Execute generateCapTbl to build up the 3D capacitance model for APR.
    % ./02_run_gencap
27. Because the generation for the capacitance model takes a long time to be finished, y**ou can skip step 26** and directly see the run log file: **generateCapTbl.log** and the generated capacitance model file: **umc18_1p6m.captbl**.