A Pulsed UWB Receiver SoC for Insect Motion Control

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Abstract—A 2.5 mW wireless flight control system for cyborg moths is presented, consisting of a 3-to-5 GHz non-coherent pulsed ultra-wideband receiver system-on-chip with an integrated 4-channel pulse-width modulation stimulator mounted on a 1.5 cm by 2.6 cm printed circuit board. The highly duty cycled, energy detection receiver requires 0.5-to-1.4 nJ/bit and achieves a sensitivity of -76 dBm at a data rate of 16 Mb/s (10^{-3} BER). A multi-stage inverter-based RF front end with resonant load and differential signal chain allow for robust, low energy operation. Digital calibration is used in the baseband amplifier, ADC and DLL to cancel voltage and timing offsets. Through the use of a flexible PCB and 3-D die stacking, the total weight of the electronics is kept to 1 g, within the carrying capacity of an adult *Manduca sexta* moth. Preliminary wireless flight control of a moth in a wind tunnel is demonstrated.

Index Terms—CMOS integrated circuits, low-power electronics, neural interface, pulse-position modulation, receivers, RF, ultra-wideband (UWB).

I. INTRODUCTION

SCIENTISTS and engineers have been fascinated by cybernetic organisms, or cyborgs, that fuse artificial and natural systems. Cyborgs enable harnessing biological systems that have been honed by evolutionary forces over millennia. An emerging cyborg application is hybrid-insect flight control, where electronics and microelectromechanical systems (MEMS) devices are placed on and within insects to alter flight direction. Compared to existing micro- and nano-air vehicles used by the military and other government agencies, insects are appealing because they are small, can travel significant distances, and can carry relatively large payloads. Such a hybrid-insect system would take the best qualities of biology: energy storage, efficient flight control, highly adapted sensing—and combine them with the best qualities of electronics: low weight, small size, deterministic control,

and interfacing with computation. A critical component of the hybrid-insect system is the communication link, which provides flight control commands to the insect. A wireless communication link is required for maximum system range and versatility.

Ultra-wideband (UWB) communication, technology that was first demonstrated by Marconi with spark gap transmitters, has shown much promise for the highly integrated, energy efficient low data rate radios that are required by hybrid-insect systems. UWB technology is a form of wireless communication in which signals occupy a wide bandwidth, greater than the lesser of 500 MHz or 20% of the center frequency of the signal, according to the United States Federal Communications Commission (FCC). In 2007, the IEEE 802.15.4a amendment to the 802.15.4 wireless personal area network (WPAN) standard was approved, adding UWB signaling as a physical layer option [1]. Due to the wide bandwidth of UWB signals, they can be efficiently amplified and processed with wide-bandwidth, low Q circuits, which can be easily integrated on-chip with minimal area [2]. One specific method of UWB communication, termed impulse radio ultra-wideband (IR-UWB), is to encode data in short pulses, on the order of nanoseconds. IR-UWB signaling is highly compatible with digital architectures, and very simple digital pulse transmitters consisting of only digital logic and delay elements have been successfully demonstrated [3].

This paper presents work on a hybrid-insect wireless system for flight control of a *Manduca sexta* hawkmoth (Fig. 1). A basestation wireless transmitter sends directional commands to the moth, and a wireless UWB receiver on the moth decodes these commands and sends pulses to the moth's central nervous system (CNS) via tungsten probes to influence flight direction. The system employs a unidirectional wireless link to reduce the complexity and power consumption of the electronics on the moth. The electronics on the moth are powered by a miniature battery.

The paper focuses on the UWB receiver system-on-chip (SoC) as well as the system integration of the receiver printed circuit board (PCB) on the moth. First, in Section II, background on hybrid-insect systems is provided and the *Manduca sexta* hawkmoth is introduced. Next, in Sections III and IV, the UWB receiver SoC is described in detail. Finally, in Section V, system results of untethered flight in a wind tunnel are presented.

II. HYBRID-INSECT FLIGHT CONTROL SYSTEMS

For millennia, humans have been able to control the motion or flight of animals through a variety of techniques. Horses are
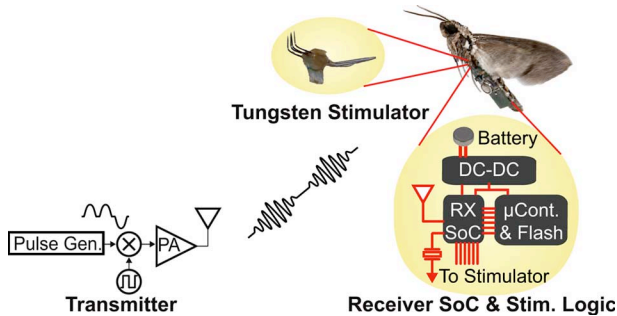
Fig. 1.   Hybrid-insect flight control system.

provided directional commands from humans by reins. Homing pigeons have been selectively bred to be able to find their way home over extremely long distances and are used to deliver messages. Hybrid-insect flight control systems are an example of these existing motion control systems pushed to the micro-scale. A pivotal, early development leading to hybrid-insect systems was the discovery of electrophysiology by Luigi Galvani in the late 1700s; he discovered that electrical sparks caused leg motion in a dead frog. The electrical properties of biological cells and tissues make it possible to interface electronic devices with cells and tissues to deliver electrical stimulation and to obtain electrical recordings.

In the last few decades, due to ongoing miniaturization of electronics, researchers have developed "backpacks" to place on animals, for both electrical stimulation and recording. Demonstrated systems include a stimulator for cockroaches [4], a discrete wireless transmitter for transmitting muscle potentials of a flying locust [5], a discrete frequency modulation (FM) telemetry system for recording electromyogram (EMG) signals from moths [6], [7], and an integrated FM telemetry system for recording neural activity of monkeys [8]. The majority of published work involves electrical recorders and wireless transmitters rather than electrical stimulators and wireless receivers, because recording neural activity has historically been more important than stimulating neurons.

Through ongoing study of the electrical properties of organisms, it is becoming increasingly feasible to control motion through electrical stimulation. In [4], directional locomotion control of a cockroach is achieved through electrical stimulation of afferent nerve fibers on the antennae. Recent work has controlled the wing flapping of a moth through electrical stimulation of muscle groups [9]. A similar stimulation approach has been used to control the flight of a beetle [10]. An alternative to muscle stimulation is to directly stimulate the CNS, which was demonstrated for moth flight control in [11].

A. Manduca Sexta Hawkmoth

In this work, we attempt to control flight of the hawkmoth *Manduca sexta*, a species that is widely distributed in the Americas. During their lifespan, moths undergo complete metamorphosis, going from egg, to larva, to pupa, and then finally to adult moth, which can live in captivity for up to two weeks. There are multiple reasons why moths are ideal for insect flight control systems. First, moths are easily reared in laboratories; the moth

colonies used in this research have existed for decades. Second, an adult hawkmoth has a wingspan of 10 cm and a carrying capacity of approximately 1 g, which is large enough to carry the required electronics. In addition, moths have been studied extensively by neurobiologists and physiologists for decades, and thus there is extensive data on their flight control mechanisms. The moth flaps its wings at ca. 25 Hz, and subtle variations in body geometry can alter the direction of flight.

Given the extreme weight and volume constraints imposed by the moth, the electronics to be carried need to be extremely lightweight, low power, and to occupy minimal volume. The total weight must be less than 1 g, the power consumption must be on the order of a few milliwatts, and the volume needs to be on the order of 1 cm^3. In addition, a wireless range of tens of meters is required. To meet these stringent specifications requires a high performance, highly integrated, energy efficient receiver SoC. As flight control commands are relatively simple, only low data rate communication (kb/s) is needed.

B. Flight Control Through Abdominal Deflection

A promising approach to altering the flight direction of a moth is to elicit abdominal movements via neural stimulation. The moth's abdomen plays an important role in flight stabilization. For instance, the moth can initiate a downward trajectory by moving its abdomen downward. It has been shown that pulsed stimulation of the nervous system can generate abdominal movements and thereby bias flight direction [11].

In our system, stimulation pulses are delivered to the nervous system via a 4-electrode tungsten probe. The electrodes are implanted at the ventral junction between the abdomen and thorax. Tungsten wire is used because of its combination of tensile strength, resistance to corrosion, and conductive properties. The electrodes consist of $\sim$ 15 mm long, 0.004$''$ diameter tungsten tines electrically coupled to 0.002$''$ diameter steel wire, which in turn interfaces with the probe. The steel-tungsten junction is encapsulated in hardened-resin epoxy which facilitates handling. The four stimulation sites of the tungsten probe enable multi-directional flight control.

To elicit abdominal deflections, simple monopolar pulses with pulse duration of 1 ms are applied to the CNS via the tungsten probe. Of the four electrodes, at least one electrode needs to be grounded and at least one electrode needs to be provided pulses. Fig. 2(a) plots the abdominal deflection of a moth versus pulse amplitude. The direction of this abdominal deflection depends on the specific electrode which is pulsed and its placement relative to the nervous system, which varies from moth to moth. Generally, the maximum amount of abdominal deflection that can be introduced is on the order of 7° to 10°. A pulse amplitude of approximately 1.5 V or above is required to introduce abdominal deflections. Fig. 2(b) plots the abdominal deflection versus pulse frequency of a different moth. By varying the pulse frequency from 2 Hz to 200 Hz, the amount of abdominal deflection can be varied from 0° to 7°. Based on a transient current measurement, the CNS connection between two tungsten electrodes can be modeled as a resistor with impedance of approximately 25 kΩ.
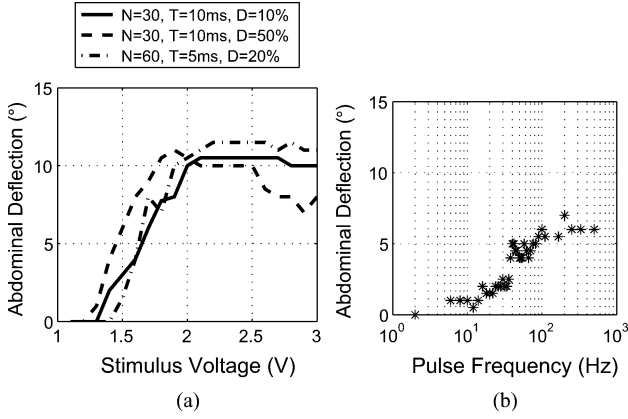
Fig. 2. Measured abdominal deflection of moths in response to pulse stimuli of varying voltage and frequency. In (a), the voltage of stimulation pulses is varied. T represents the pulse period, N represents the number of pulses and D represents the duty cycle. In (b), for a different moth, the frequency of stimulation pulses is varied, for a 0.5 s burst of 2.5 V, 1 ms pulses.
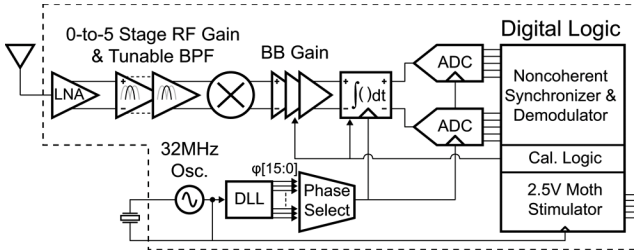

Fig. 3. Detailed block diagram of receiver SoC.

III. UWB RECEIVER SoC: ARCHITECTURE AND CIRCUITS

A. Architecture

In the flight control system, the key electronic component is the wireless receiver, which is subject to stringent constraints on weight, volume and power consumption. Fig. 3 shows a block diagram of the wireless receiver. The receiver is a non-coherent, energy detection based IR-UWB receiver designed for the 802.15.4a wireless standard. The receiver operates at a peak data rate of 16 Mb/s in the 3-to-5 GHz UWB band, communicating in one of three 500 MHz channels at 3.5, 4.0, and 4.5 GHz. Through duty cycling, the receiver can operate at lower data rates, thereby reducing average power consumption.

Noncoherent signaling is employed to reduce power consumption on the receiver as it allows for a simple, energy detection architecture without any high frequency clocks. The receiver mixes the received signal with itself at radio-frequency (RF), and a windowed integrator and analog-to-digital converter (ADC) at baseband generate a digital signal representing the total energy received in a given time window. This architecture allows for demodulation of both on-off keying (OOK) and pulse-position modulation (PPM) signals.

The first stage of the receiver signal chain is a RF front end that amplifies the received signal by up to 40 dB while attenuating out-of-band interferers. This amplified RF signal is then squared, resulting in the RF signal being mixed to baseband. Following the squarer is a baseband amplifier, and then the amplified signal is integrated and quantized by an ADC. The

ADC values are passed to a digital backend, which performs packet detection, synchronization and decoding. Also included in the receiver SoC is a crystal oscillator and a delay-locked loop (DLL). The entire receiver is clocked by a fixed, 32 MHz clock. After synchronization, the appropriate (DLL) phase is selected and is used by the windowed integrator and ADC. Each of the specific components of the receiver SoC is described in the following subsections, except for the digital synchronizer and demodulator, which is described in [12].

B. RF Front End

For noncoherent receivers, significant gain is required prior to the squarer to obtain a sufficient signal swing such that semiconductor device nonlinearity can be exploited in the squaring element. Passive and active squarers require input voltages on the order of millivolts whereas low noise amplifier (LNA) input voltages can be on the order of tens of microvolts, thus requiring voltage gain of approximately 40 dB. To achieve such large gain, noncoherent receivers typically employ one of two methods: a super-regenerative architecture [13] or a multi-stage linear amplifier [14]. Although a multi-stage linear amplifier requires more power than a super-regenerative amplifier, it allows for simple support of any arbitrary squaring and integration interval. Moreover, a multi-stage linear amplifier is less subject to RF leakage out of the antenna, which can potentially result in FCC spectrum violations or require the use of an RF isolation amplifier. Based on these advantages, a multi-stage linear amplifier topology is selected, with a per-stage gain of approximately 8 dB.

A key design choice is whether to implement the multi-stage amplifier with single-ended or differential circuits. As the RF front end is integrated on the same chip as digital logic and baseband analog circuits, a differential architecture offers significant advantages in terms of substrate noise and power supply immunity. In addition, reduced decoupling capacitance is required, and a differential structure allows for higher quality factor inductors and virtual ground "center-tap" nodes. Thus, a differential RF architecture is selected; however, as all commercially available UWB antennas are single ended, the LNA has a single ended input. Single-ended to differential conversion is realized by the LNA and all later stages are differential. Resonant *LC* loads are used instead of non-resonant loads as they offer superior gain in the 3-to-5 GHz frequency band at the same power consumption and also have a second order bandpass characteristic which rejects out-of-band interferers [14].

1) Core Amplifier Structure: Given the design choice of a differential amplifier with resonant load, the final key design choice is what amplifier structure to use. One of the most common topologies is the differential pair, shown in Fig. 4(a). This amplifier can operate at very low supply voltages to maximize energy efficiency. The amplifier shown in Fig. 4(a), but with source degeneration, has been demonstrated operating at a supply voltage as low as 0.5 V [14]. In a practical system, however, there are several reasons why such a low supply voltage is not ideal. In mixed signal SoCs with RF, baseband analog and digital logic all on a single chip, additional complexity is required to generate multiple supply voltages. Moreover, there are voltage headroom advantages to operating both RF and baseband analog circuits at higher voltages. For example, nMOS switches operating off a higher supply voltage have an improved I_{on} to I_{off} ratio. Thus, it is preferred to select an
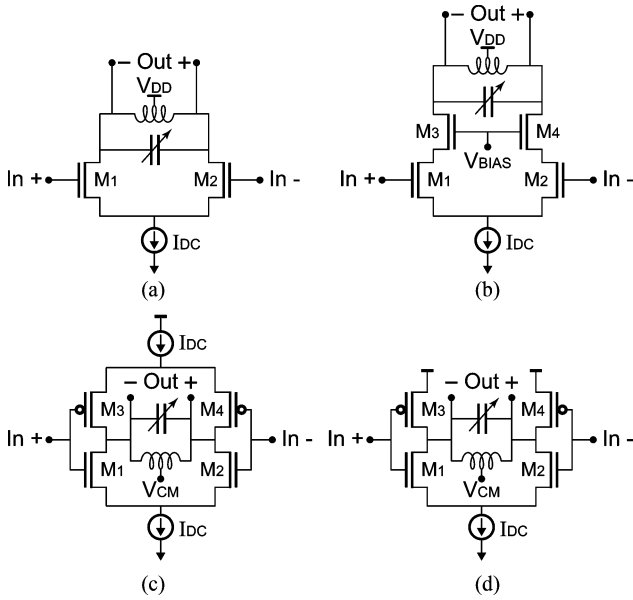
Fig. 4. Four possible implementations of a RF gain stage with a resonant load.
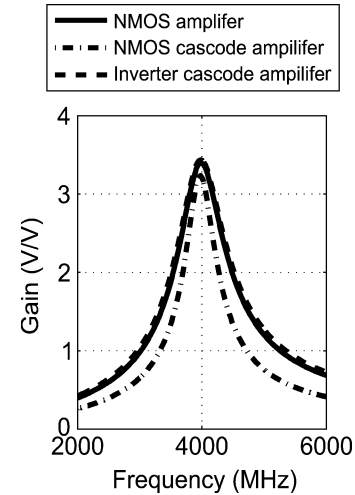

Fig. 5. Gain of an NMOS-based RF amplifier [Fig. 4(a)], an NMOS-based cascode RF amplifier [Fig. 4(b)], and an inverter-based, complementary RF amplifier [Fig. 4(d)].
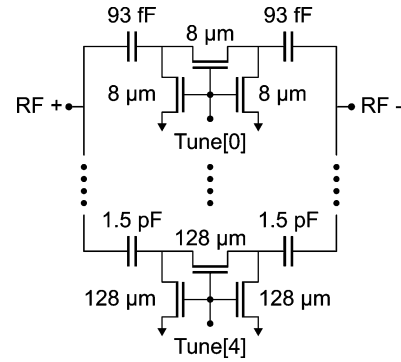

Fig. 6. Digitally tunable load capacitor of the RF amplifier. All nMOS devices are minimum length and their width is shown.
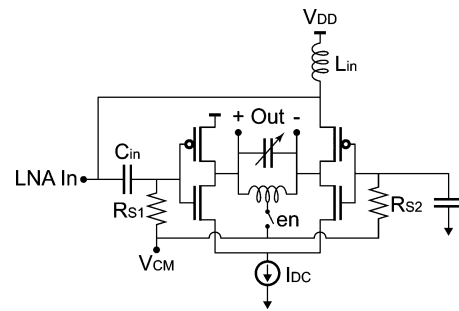

Fig. 7. Schematic of low noise amplifier.

amplifier topology that is energy efficient at a higher supply voltage.

Two popular approaches for RF amplifiers to take advantage of increased voltage headroom are by cascoding [15] and current reuse [16]. Fig. 4(b) shows an example of a RF gain stage with cascoding, and Fig. 4(c) shows an example of current reuse by using pMOS input devices in tandem with nMOS input devices. In Fig. 4(c), two current sources are used to regulate the current as well as cancel common-mode components, whereas in Fig. 4(d) only one current source is used to regulate current. When only a single current source is used, the power supply can be reduced resulting in improved energy efficiency; however, this comes at the cost of degraded common-mode and power supply rejection.

The circuits presented in Fig. 4(a), (b), and (d) were simulated to determine which topology can achieve the maximum gain at a given power consumption, and the simulated results are presented in Fig. 5. To normalize power consumption, the circuit of Fig. 4(a) is supplied a voltage of 0.57 V and a current of 5.26 mA, whereas the other two circuits are supplied a voltage of 1 V and a current of 3 mA. All three topologies achieve similar performance, except that the cascode amplifier achieves slightly less peak gain and has a narrower bandwidth.

As the inverter-based RF amplifier shown in Fig. 4(d) achieves comparable performance at the same power consumption as the nMOS amplifier shown in Fig. 4(a), but operates off a 1 V supply rather than a 0.57 V supply, this topology is chosen as the core RF amplifier. To achieve a sufficiently large tuning range, the load capacitor is implemented with metal-oxide-metal (MOM) capacitors with 5 bits of tuning as shown in Fig. 6.

2) Low Noise Amplifier: The core RF amplifier described and motivated in the preceding subsections serves as the basis of the LNA, shown in Fig. 7. The LNA is an inverter-based RF amplifier that performs single-ended to differential conversion. The LNA is essentially a common-gate, common-source (CG-CS)

amplifier [17], with wideband matching to the 50 Ω antenna achieved by the pMOS common-gate amplifier.

When the LNA is enabled, the switch en is closed, connecting the dc output of the differential inverters with the dc input of the inverters. Through negative feedback, the dc voltages at all of the nodes normalize to the same value, V_{CM}. To allow the LNA to turn on rapidly, switches are placed in parallel with R_{S1} and R_{S2} and these switches are briefly enabled while the LNA turns on. In normal operation, R_{S1} and R_{S2} are sufficiently large that the negative feedback does not degrade gain. When the LNA is disabled, the switch en is opened, I_{DC} is set to 0 A, and
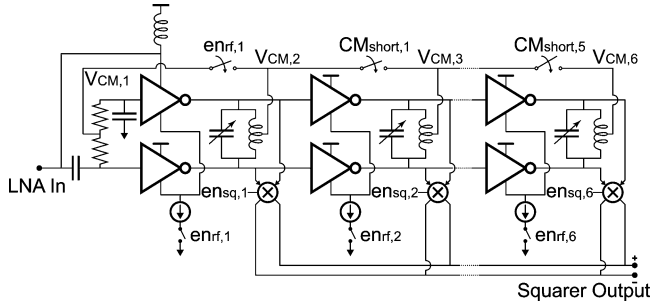
Fig. 8. Schematic of 6-stage RF amplifier, including the LNA. A variable number of stages can be enabled depending on the gain required.
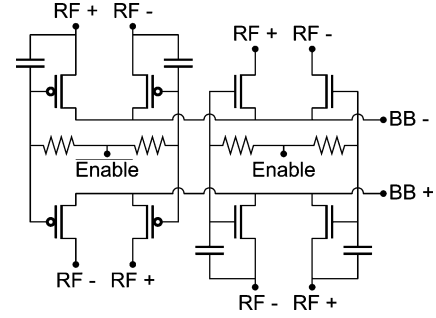

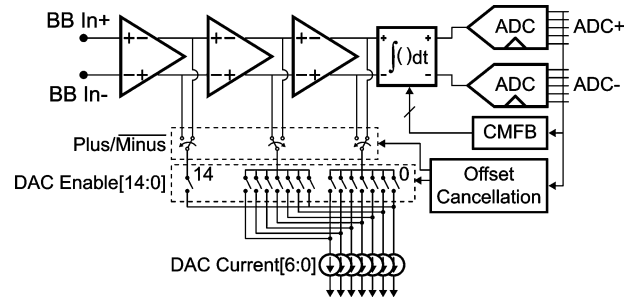Fig. 9. Schematic of differential, passive squarer.

Fig. 10. Baseband signal chain, consisting of a baseband amplifier, an integrator, an ADC, a current-mode DAC that is used to cancel baseband amplifier offsets, and digital calibration logic.

V_{CM} is actively driven to V_{DD}. This allows the output dc voltage to freely float, which is necessary for proper calibration of the receiver.

3) Multi-Stage RF Amplifier: Following the LNA are five stages of RF gain. Fig. 8 presents the schematic of the multi-stage RF amplifier, including the LNA. To dc bias the RF gain stages, the center tap of each stage's inductor is connected to the center taps of adjacent stages' inductors. Due to the differential voltage across each inductor, these center tap nodes are virtual grounds. Moreover, as all RF amplifiers are biased with the same current density, these nodes are nominally at the same dc voltage. By connecting these nodes together with a low impedance connection, the common-mode rejection ratio (CMRR) is superior to what is achieved with more traditional common-mode feedback (CMFB) techniques like resistive feedback. The Monte Carlo simulated common-mode gain of the five stages of RF gain after the LNA has a mean of 7.7 dB and a standard deviation of 7.5 dB at the RF resonant frequency and a mean of 2 dB and a standard deviation of 0.1 dB at low frequencies.

Each gain stage has a squarer at its output, although at any time only one squarer is enabled. Depending on how much RF gain is needed, a variable number of RF gain stages are enabled, as well as the appropriate squarer.

C. Squarer

A squarer serves two functions in the receiver: to frequency shift (or mix) the received RF signal to baseband and to square its amplitude. It is possible to design an entirely passive squarer that consumes no dc bias current; however, these passive squaring circuits are traditionally single ended [14] or pseudo-differential [18]. In this work, a passive, differential squarer is employed that uses transistors biased in the triode region (Fig. 9). The differential squarer is made possible by the inverter-based RF amplifier, as the output voltage of the RF amplifier is nominally midrange, thereby allowing both nMOS and pMOS devices to have sufficient gate overdrive. The squarer consumes no static bias currents or active power and has near zero dc output voltage offsets. A key advantage of this structure is that fairly well matched differential outputs are generated. Due to its nonlinear transfer function, the squarer requires RF inputs with amplitudes above approximately 10 mV. At a 10 mV RF input, the single-ended output voltage amplitude is ∼ 0.7 mV.

D. Baseband Amplifier

Following the squarer is a baseband signal chain consisting of a three-stage amplifier followed by an integrator and ADC (Fig. 10). The baseband amplifiers are simple differential pairs with resistive loads. The cumulative differential gain of the baseband amplifier chain is simulated to be 83 V/V and the 3 dB bandwidth is 230 MHz. The large baseband gain is required to amplify the squarer output from amplitudes as low as 0.5 mV. Each differential pair operates off a 1 V supply, is supplied 320 μA of current, and has resistive and capacitive loads of 2.5 kΩ and 150 fF, respectively. A multi-stage amplifier is used rather than an op amp due to the wide signal bandwidths and because a high Q filter is not required.

Due to the small input levels and high gain, offset compensation is a critical component of the baseband amplifier. An input referred offset of merely 10 mV would saturate the baseband amplifier. Traditionally, the goal of offset compensation is to establish a 0 V differential output voltage given a 0 V differential input voltage; however, in this system a fixed offset at the output needs to be established to maximize dynamic range. This fixed output offset is required because the baseband signal generated by the squarer is monopolar, meaning that the positive squarer output only increases from its "zero-input" level and the negative squarer output only decreases. Thus, the positive baseband amplifier output should nominally be biased near the bottom of the amplifier's dynamic range.

Offset compensation is implemented digitally with a current-mode digital-to-analog converter (DAC) in a discrete time process. Rather than a traditional architecture of a binary-weighted DAC connected to the output of the first baseband amplifier stage, the DAC consists of current sources that can connect to any of the three baseband amplifier stages. This allows for fine offset control without requiring very small

current sources. To ensure monotonicity as the DAC code increases, the current sources transition from being unconnected, to being connected to the final amplifier stage, to eventually being connected to earlier amplifier stages. Depending on whether a positive or negative offset needs to be cancelled, the current sources can connect to the positive or negative output nodes.

During calibration, the LNA is disabled and the baseband inputs are shorted to the same dc value. Next, the integrator and ADC convert the baseband output to a digital value. The ADC output code is processed by a slope tracking state machine to adjust the DAC until the ADC output code approaches the desired ADC value.

E. Integrator and ADC

Following the baseband amplifier is an integrator and ADC. Both the integrator and ADC are clocked at 32 MHz, resulting in an integration period of 31.25 ns. The output of the ADC is a digital representation of the total RF energy received within the 31.25 ns integration period. This absolute measurement of energy is preferred to a relative measurement of energy, because it allows for demodulation of both PPM and OOK data.

The ADC consists of two single ended ADCs, operating on the positive and negative integrator outputs and each generating 5 bits of information. The difference between these ADC values generates a 6 bit output code, although if perfect matching is assumed, only 5 bits of useful information is generated. Despite this limitation, the pseudo-differential structure offers improved power supply rejection and common-mode rejection compared to a single ended 5 bit structure, while also allowing for a simpler implementation than a fully differential structure.

Having the integration output quantized to multiple bits is useful for gain control and for accurate timing synchronization. Due to the 5 bits of ADC information combined with coding on the transmitter, the receiver is able to synchronize with an accuracy of ± 1 ns while being clocked with a period of 31.25 ns [12].

The integrator and ADC are jointly designed to not require any high frequency clocks, as well as to allow for a simple integrator that does not need op amps, loads with high output impedance, or positive feedback. A detailed block diagram of the integrator and ADC are shown in Fig. 11. Together, the integrator and ADC are similar to a single-slope integrating ADC, but with some key differences. The differential inputs are first passed through a differential transconductor to convert the input voltage to a current. This current discharges up to six stages from V_{DD} in succession, similar to that of a dynamic inverter. The differential rate of discharge between the positive and negative ADCs is based on the differential input voltage, and thus an integration function is realized. Based on the number of stages that are discharged in the integration period, 2 bits of coarse quantization are generated. Only 2 bits of information are generated from the six stages because the first two stages are not considered in the coarse quantization. The first two stages should ideally always be discharged by the end of an integration period and thus do not contribute information. These first two stages serve to cancel out the static, zero-input dc current of the differential transconductor that is required to appropriately bias the transconductor in a linear region. Additionally, the time while these first two stages are being discharged is leveraged by the final four stages to evaluate the previous integration value.
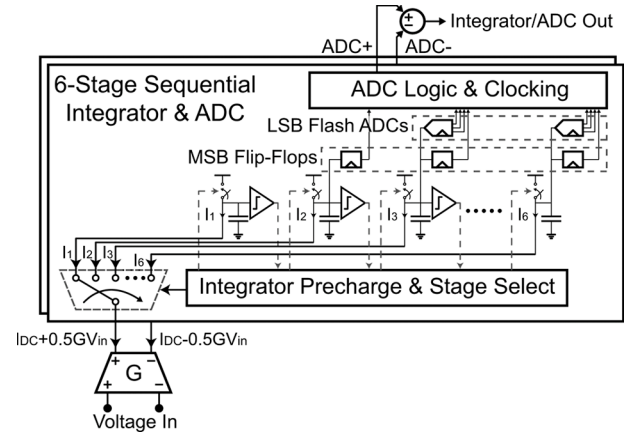

Fig. 11. Six-stage sequential integrator and ADC.

The ADC generates an additional 3 bits of fine quantization that are combined with the 2 bits of coarse quantization. These 3 bits are generated by quantizing the capacitor voltage of the stage that was being discharged at the end of the integration period with a flash ADC. The capacitor voltages on stages three through six are temporarily held constant while the appropriate flash ADC resolves. During this time period, the next integration period has already begun by discharging stage one. A simple flash ADC with a resistive ladder DAC is used to generate these 3 bits. Thus, 5 bits of data are generated by the integrator and ADC. Both positive and negative outputs of the transconductor are independently processed by this integrator and ADC structure, and thus a pseudo-differential output is generated. The integrator and ADC architecture would only need slight modifications to allow for the use of a differential ADC.

F. Clocking

The SoC is designed to be clocked off a fixed 32 MHz oscillator that is always enabled. Due to the noncoherent signaling, clock frequency and timing synchronization accuracy requirements between transmitter and receiver are dramatically reduced. Through the use of a Pierce oscillator stabilized with a quartz crystal, it is possible to achieve frequency accuracies on the order of ± 20 ppm [19], allowing the transmitter and receiver to require only one synchronization per packet, without any phase tracking during the packet payload.

For the receiver to successfully decode data, the integrator and ADC must be phase aligned with the received data. This phase alignment is achieved with a digital synchronization algorithm and a DLL. Based on the result of the digital synchronization, an appropriate phase from the DLL is used to clock the integrator and ADC. During synchronization, the DLL is bypassed and the integrator and ADC are provided the same clock phase as the rest of the digital logic. As the DLL is not being used, the DLL can be calibrated during this time by a successive approximation register (SAR) state machine.

The digital baseband achieves synchronization accuracy of ± 1 ns in an integration window of 31.25 ns, and the DLL is designed to match these specifications. The DLL has 16 outputs, each nominally spaced 1.95 ns apart from one another. Due to the noncoherent signaling, the DLL does not need to have good linearity, and thus it is possible to use very simple delay elements and simple calibration logic. Fig. 12 presents a simplified schematic of the DLL. The core delay element consists of
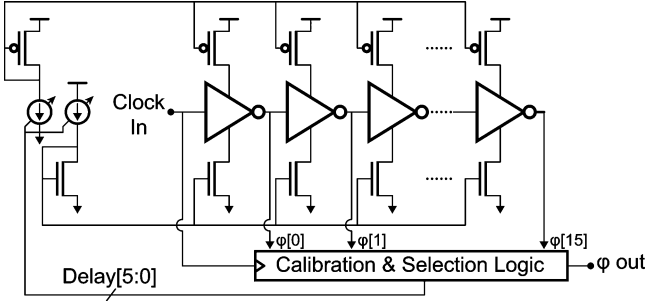
Fig. 12.   Delay-locked loop.

Fig. 13.   Block diagram of stimulation logic included in the UWB receiver SoC.

Fig. 14.   Die photograph of pulsed UWB receiver SoC.

a current starved inverter, and a DAC is used to control the bias current of the inverter. All outputs of the DLL are passed to a digital, synchronous state machine.

As the integrator and ADC operate off a different clock phase than the rest of the digital logic, there is a potential for timing violations or clock offsets at the interface. To address this problem, retiming registers connect to the ADC outputs. These retiming registers can be either positive or negative-edge triggered to ensure sufficient setup and hold time.

G. Digital State Machine and Duty Cycling

As the receiver peak data rate of 16 Mb/s is much larger than the required data rate in the system, the receiver is designed to be duty cycled. Duty cycling is implemented through the use of a programmable digital state machine. Between packets, the radio and modem are disabled and all digital logic is clock gated except for a sleep counter. This low power sleep mode continues until the sleep counter reaches a programmable count value. At this point, the receiver state machine is triggered, and the receiver attempts to receive a packet.

To receive a packet, the digital state machine first enables the RF and analog circuits, which turn on within one clock cycle. Before the receiver modem performs packet detection, the receiver state machine performs calibration of the DLL, baseband amplifier and integrator. This calibration only takes a few microseconds, and is performed before every packet reception to account for any change in temperature or supply voltage since the last packet reception attempt.

H. Stimulation Logic

A key circuit block on the receiver SoC is the stimulator logic which drives the stimulator electrodes (Fig. 13). The stimulator logic consists of a frequency divider, a pulsewidth modulation (PWM) generator and output logic. The clock divider divides the 32 MHz system clock to a stimulator clock of approximately 1 kHz. This low frequency clock serves as the master clock for the PWM generator, which generates a pulse burst with programmable on time, frequency, and number of pulses in a burst. The receiver offers support for up to 8 output channels, and each output channel can be individually set to ground, to the pulse signal, or to a high impedance state. Level converters convert the output signals to 2.5 V, as 1 V is not sufficient to elicit an abdominal movement response from the moth. The stimulation logic is programmed based on received packet data.

IV. UWB RECEIVER SoC: MEASUREMENT RESULTS

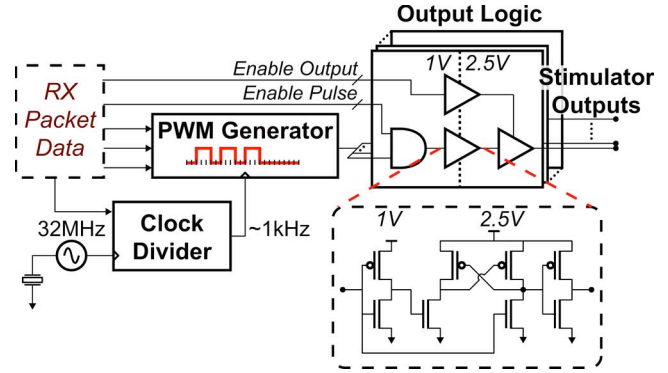The receiver is implemented in a 90 nm CMOS process and a die photo of the chip is shown in Fig. 14. The die area is 2.6 mm by 2.1 mm, and the area is dominated by digital logic, which occupies the right side of the die. Due to the significant amount of digital logic integrated on the same die as the RF front end, there is significant potential for digital supply and substrate noise to result in degraded analog and RF performance. This motivated the use of a differential receiver architecture. Additionally, substrate contact rings are used to isolate the digital and analog blocks, as well as reduce the potential for feedback coupling in the high gain RF front end. The receiver is packaged in a 40-lead (QFN) package and mounted on an FR4 PCB.
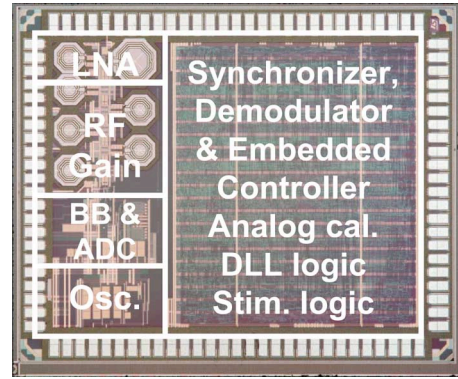
A. Sub-Block Measurements

The differential voltage gain of the RF front end scales from 6 dB to 45 dB depending on the gain setting. Noise figure measurements are made with an Agilent N4002A noise source connected to an Agilent MXA N9020 Signal Analyzer. The minimum noise figure in the 3.5, 4.0, and 4.5 GHz bands is measured to be 7.7, 9.0, and 9.1 dB, respectively. The receiver achieves an s_{11} of -10.5 dB, -9.8 dB, and -7.8 dB in the 3.5, 4.0, and 4.5 GHz bands, respectively.

The squarer is characterized by applying RF input signals to the LNA and directly measuring the outputs of the differential squarers. Ideally, the output voltage amplitude should linearly increase with power and the positive and negative outputs should be identical. The measured results, shown in Fig. 15, achieve very good power-voltage linearity and matching.

To test the integrator and ADC, off-chip signals are applied to the input of the differential transconductor. ADC static and
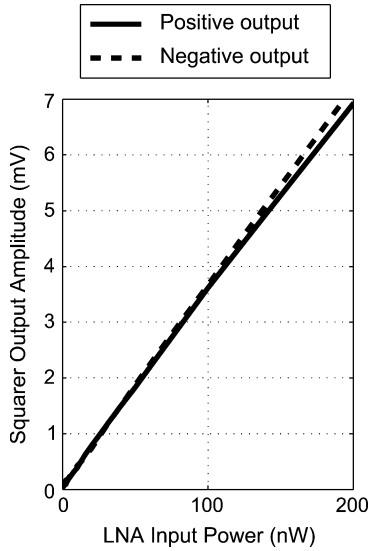
Fig. 15. Positive and negative output amplitudes of the squarer versus LNA input power at its third of six RF gain settings ($f_c = 4.0$ GHz).
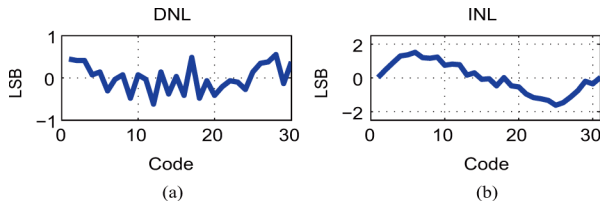

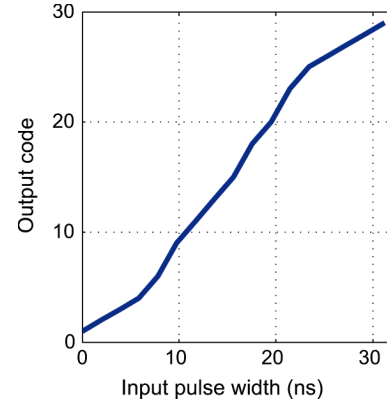Fig. 16. (a) DNL and (b) INL of integrator and ADC.

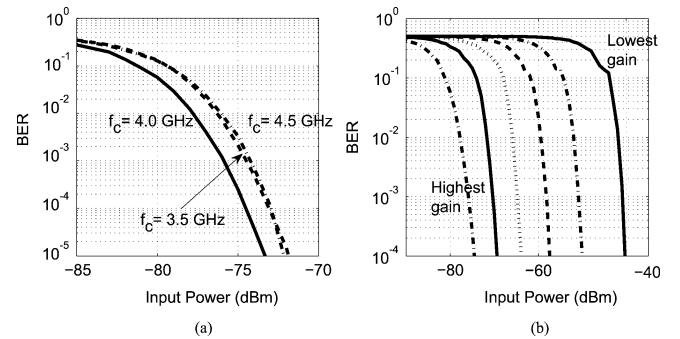Fig. 17. Linearity of ADC when provided a pulse input of varying duration.

Fig. 18. BER of receiver (a) at its highest gain setting at the three center frequencies, and (b) at the different gain settings with $f_c = 4.0$ GHz.

dynamic measurements are complicated by the fact that the integrator cannot be de-embedded from the ADC and that there is no sampling switch. Thus, inputs are effectively time averaged, making it difficult to measure ADC performance by applying sinusoidal inputs. Instead, to measure linearity, dc inputs need to be applied. Fig. 16 presents the differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC. The measured DNL is less than 1 least significant bit (LSB) and the INL is less than 2 LSB. The symmetric, nonlinear nature of the INL is due to the differential transconductor.

Dynamic performance of the integrator and ADC is measured by applying pulses of varying width, simulating the receiver in normal operation (Fig. 17). By applying pulse inputs rather than dc inputs, the bandwidth of the integrator is tested. The measurement results indicate a monotonic response and fairly good linearity, with the linearity likely limited by the differential transconductor.

B. Bit Error Rate and Interference Measurements

The test setup employed to measure the receiver bit error rate (BER) consists of the UWB receiver, power supplies, a laptop, a spectrum analyzer, and an ideal UWB transmitter consisting of an arbitrary waveform generator (AWG), a vector signal generator (VSG), and a RF interference generator. Fig. 18 presents the BER of the receiver in different frequency bands at its highest gain setting and at different gain settings with $f_c = 4.0$ GHz. The receiver achieves a maximum sensitivity of -76 dBm at a

data rate of 16 Mbps and a BER of 10^{-3}. The sensitivity scales by 35 dB from the lowest to highest gain setting, allowing for a trade-off of power consumption for sensitivity.

The BER of the receiver has been characterized in the presence of varying supply voltages, to determine the resilience of the receiver to power supply variation. A variation in the core supply voltage of ± 50 mV results in only a 2 dB degradation in sensitivity. Throughout these measurements, none of the receiver components are recalibrated from the nominal values, including the baseband offset compensation DAC, the RF front end capacitor tuning, and the differential transconductor current.

In a practical wireless system, the receiver must reject interfering signals, both in-band and out-of-band. Key potential sources for out-of-band interferers include 802.11 at 2.45 GHz and 5.25 GHz, as well as Bluetooth at 2.45 GHz. Table I presents the maximum tolerable out-of-band interferer power at 2.45 GHz and 5.25 GHz. In these measurements, the receiver is first set to its maximum gain setting and the UWB input power is set such that the BER of the receiver is 10^{-6}. When $f_c = 4.0$ GHz, this corresponds to an input power level of -73 dBm. Next, the interferer tone is generated and combined with the UWB signal. The maximum tolerable out-of-band power level corresponds to the maximum interferer power level when the BER is less than 10^{-3}. Similar measurements have been taken with in-band interferers, and the maximum tolerable in-band interferer has power -1 dB to 3 dB relative to the UWB signal power, depending on the RF channel frequency.

TABLE I
OUT-OF-BAND INTERFERENCE ROBUSTNESS

Interferer Freq.	Maximum Interferer Power (dBm)		
	f_c = 3.5 GHz	f_c = 4.0 GHz	f_c = 4.5 GHz
2.45 GHz	−22 dBm	−19 dBm	−23 dBm
5.25 GHz	−30 dBm	−30 dBm	−41 dBm

TABLE II
RECEIVER INSTANTANEOUS POWER CONSUMPTION BREAKDOWN

| Receiver component	Power Consumption
Leakage	0.64 mW
Crystal oscillator	0.15 mW
Clock tree (idle)	0.13 mW
Delay locked loop	0.05 mW
Baseband amplifier & ADC	1.51 mW
LNA	5.90 mW
RF Amplifier	0 mW to 14.30 mW
Total idle power	*0.92 mW*
Total active power	*8.38 mW to 22.69 mW*

Fig. 19. Two comparison plots of receiver with previously published work: (a) energy/bit versus data rate, and (b) normalized sensitivity versus energy/bit. In both plots, a point is shown for the receiver at its highest and its lowest gain setting. Data for these plots are found in Table III.

C. Power Consumption and Energy/Bit

As the receiver SoC is targeted for low power, highly energy constrained applications, significant effort was spent to minimize overall power consumption and energy/bit. A breakdown of power consumption is shown in Table II. Due to the extensive digital logic and the absence of power gating switches, the total leakage power is 0.64 mW. The always-on crystal oscillator consumes 0.15 mW. When the receiver is in idle mode, the clock tree is extensively gated; however, an additional 0.13 mW of power is still consumed. The overall receiver power consumption is dominated by the LNA and the RF amplifiers that follow the LNA. Each individual RF amplifier consumes approximately 2.85 mW of power consumption, and the five-stage RF amplifier consumes a total of 14.30 mW of power when all five stages are enabled. At a data rate of 16 Mb/s at the lowest gain setting, the entire receiver consumes 8.38 mW of power and at the highest gain setting, the receiver consumes 22.69 mW of power. When the receiver is duty cycled to low, kb/s data rates, the average power consumption is reduced to the order of a few milliwatts, ultimately limited by leakage power. By adding power gating switches, the average receiver power consumption could approach the microwatt level at kb/s data rates. The receiver power consumption is constant regardless of the RF center frequency and includes the power of the digital backend when decoding data; however, these power measurements do not account for the energy required for synchronization at the start of a packet.

As the receiver operates at an instantaneous data rate of 16 Mb/s, the energy/bit of the receiver is 0.5-to-1.4 nJ/bit depending on the gain setting. Table III and Fig. 19(a) present the energy/bit of the receiver compared to previously published receivers, both narrowband and wideband as well as coherent and noncoherent. The receiver achieves one of the lowest energy/bit values; however, the energy/bit metric has limited utility as it does not account for receiver sensitivity, front end linearity, die area, etc. For example, many radios that achieve a low energy/bit achieve a very poor sensitivity and range, and thus have limited utility in practical systems. As an attempt to better compare receivers of different energy/bit, data rates, and sensitivities, it is possible to normalize receiver sensitivity to a
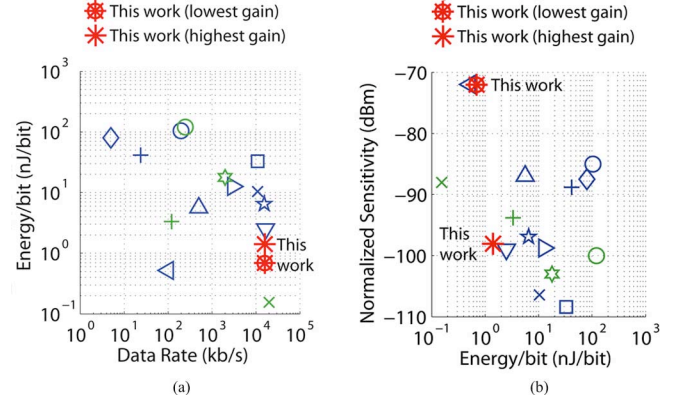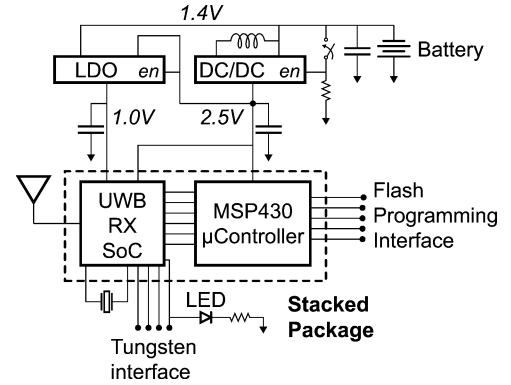

Fig. 20. Block diagram of electronics mounted on a flexible PCB and attached to a moth.

constant data rate. This normalized sensitivity is similar to noise figure, but offers a measure of the entire receiver performance rather than just the noise performance of the RF front end. The following tenet forms the basis of the normalized value.

A 10 dB improvement in receiver sensitivity is equivalent to a decrease in data rate by 10× at a constant energy/bit.

This tenet is based on the fact that for a given modulation scheme and a fixed noise figure, data rate scales linearly with bandwidth, and a 10× decrease in bandwidth results in a 10 dB improvement in sensitivity based on the following equation:

$$P_{r,\min} = -174\,\mathrm{dBc/Hz} + 10\log(\mathrm{BW_{Hz}}) + \mathrm{SNR_{min}} + \mathrm{NF}. \tag{1}$$

In (1), $P_{r,\min}$ represents the sensitivity, BW represents the noise bandwidth, $\mathrm{SNR_{min}}$ represents the minimum signal-to-noise ratio (SNR) required at the output of the receiver, and NF represents the noise figure of the receiver. If NF and $\mathrm{SNR_{min}}$ remain constant, then a 10× decrease in bandwidth results in a 10 dB improvement in sensitivity.

The tenet is also based on the approximation that noise bandwidth should ideally scale linearly with power consumption, resulting in a constant energy/bit. While this approximation is not fundamental, the following two examples provide some justification. For example, if ten identical narrowband radios are operated simultaneously, each in a different frequency band, the av-

TABLE III
COMPARISON OF RECEIVER WITH PREVIOUSLY PUBLISHED WORK

| Author	Data Rate (kbps)	Power (mW)	E/bit (nJ/bit)	Sens. at data rate (dBm)	Sens. scaled to 100kbps (dBm)
Porret [21]	24	1	41.6	−95	−89
Choi [22]	200	21	105	−82	−85
Emira [23]	11000	114	10.3	−86	−106
Otis [24]	5	0.4	80	−101	−88
Darabi [25]	11000	360	32.7	−88	−108
Chen [26]	500	2.8	5.6	−80	−87
Lee [14]	16700	42	2.5	−77	−99
Marholev [27]	3000	38	12.7	−84	−99
Pletcher [28]	100	0.052	0.5	−72	−72
Zheng [29]	15600	102	6.51	−75	−97
Weber [30]	2000	36	17.8	−90	−103
Bohorquez [31]	120	0.4	3.3	−93	−94
Retz [32]	250	30.25	121	−96	−100
Verhelst [33]	20000	3.1	0.159	−65	−88
This work	16000	22.5	1.4	−76	−98
		11	0.7	−50	−72
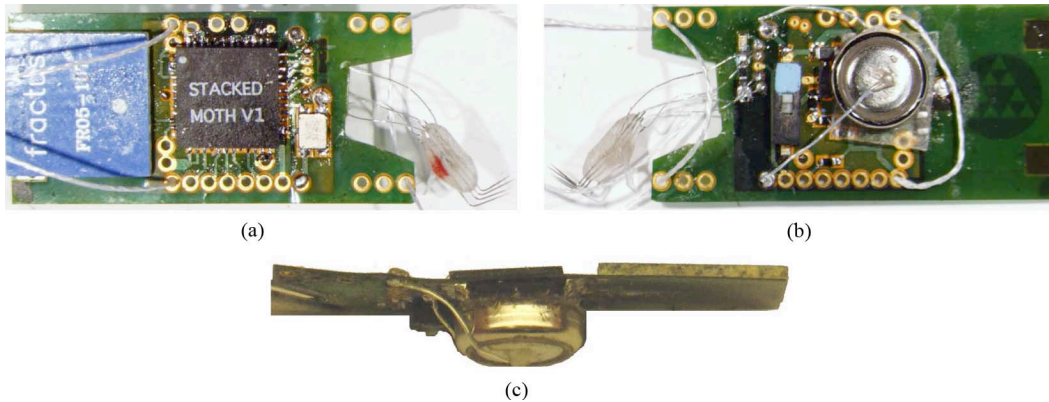
Fig. 21. Flexible PCB: (a) top, (b) bottom, and (c) side.

erage data rate increases by 10× and the average received power increases by 10 dB, but the energy/bit remains constant. Alternatively, if a radio is duty cycled by 10×, both the average data rate decreases by 10× and average received power decreases by 10 dB, but the energy/bit remains constant.[1] In practice, increasing data rates usually results in a sub-linear increase in power consumption, resulting in high data rate radios achieving a better energy/bit at the same scaled sensitivity as low data rate radios. Moreover, leakage power consumption often degrades the energy/bit of radios when they are highly duty cycled. Despite these limitations, the scaled sensitivity metric serves as an effective number (like noise figure) to compare the performance of a wide variety of receivers, both coherent and noncoherent and of varying data rates.

Normalized sensitivity is included as a column in Table III and Fig. 19(b) plots normalized sensitivity versus energy/bit for previously published receivers and this work. Ideally a receiver is positioned at the lower-left corner of this plot, achieving a good normalized sensitivity and a minimum energy/bit. The receiver presented in this paper compares favorably with previously published work. From the plot, there is a definite trade-off between energy/bit and normalized sensitivity.

[1]It is important to note that while duty cycling or through parallelism, the *instantaneous* sensitivity (or minimum detectable signal) does not change, and thus the sensitivity of the receiver has neither improved nor worsened.

V. SYSTEM INTEGRATION AND MEASUREMENT RESULTS

Although the receiver is highly integrated, in the hybrid-insect system, additional electronic components are required. Fig. 20 shows a block diagram of the electronics that are used. The key components include the receiver SoC, a microcontroller, 2.5 V dc-dc converter, 1 V low drop-out (LDO) regulator, miniature coin cell battery, on-off switch, crystal resonator, LED, antenna, and discrete inductors, resistors and capacitors. The electronic components are soldered to a flexible, 4-layer PCB. A flexible PCB allows for a 60–70% reduction in weight and thickness compared to a rigid PCB. Photos of the PCB are shown in Fig. 21. The entire system consumes an average power of 2.5 mW when the receiver attempts to receive a 68 bit synchronization packet every 1 ms.

The electronics are powered by a 1.4-to-1.6 V silver oxide, size 362 coin cell battery that is capable of sourcing the 2.5 mW consumed by the electronics. The battery has a typical capacity of 27 mAh, weighs 0.32 g, and has a impedance at 40 Hz of 10-to-20 Ω. As the receiver SoC requires 1.0 V and 2.5 V supply voltages, dc-dc converters are used to generate the required voltages from the battery. To further reduce form factor and weight, only a single decoupling capacitor is used for each supply voltage. A miniature on-off power switch is used to enable the dc-dc converters, so that the receiver does not consume any static current when turned off.

TABLE IV
WEIGHT BREAKDOWN OF COMPONENTS ATTACHED TO THE MOTH

System Component	Weight
Packaged RX SoC & Microcontroller	161 mg
$1.5 \times 2.6 \times 0.002$ cm PCB	100 mg
Antenna	164 mg
Silver Oxide Battery	320 mg
Harness	85 mg
Other Components	170 mg
Total	*1000 mg*

A key limitation of the receiver SoC is that it has no embedded flash memory and that on power-up it must be programmed to an appropriate state through its digital shift register. A Texas Instruments MSP430 microcontroller with embedded flash memory is included in the system and serves as a power-up programmer. To reduce the form factor and weight, the MSP430 microcontroller is combined in a single QFN package with the receiver SoC by stacking the receiver bare die on top of the microcontroller bare die.

As the receiver cannot send an acknowledgement when a packet has been received, it is not possible for the operator to determine that the receiver is successfully receiving packets and stimulating the moth. As a workaround, a miniature red LED is attached to the PCB and is connected to one of the four stimulation channels. Thus, when the moth is being stimulated, the LED rapidly turns on and off and is visible to the naked eye. A red LED is used because moths cannot see the color and it does not influence their flight.

Table IV presents a weight breakdown of the components attached to the moth. The total weight of all components is 1 g, including the tungsten probe and a harness that is used to attach the PCB to the moth. The Silver-Oxide battery consumes nearly one-third of the total weight. Although lighter batteries exist, none were found that could provide the average current levels required by the receiver SoC.

A. Attaching PCB to Moth

As the average adult moth weighs only 2.5 g, it is a challenge for them to carry the 1 g of hardware. In fact, previous literature has only demonstrated a carrying capacity of 0.7 g [6]. For maximal carrying capacity, any weight attached to the moth must be located near the moth's center of mass. Two alternatives for attaching electronics to the moth are dorsal mounting by attaching the PCB to the moth like a dorsal fin, or ventral mounting by attaching the PCB with a harness. For ventral mounting, a harness is used that is designed to stabilize and position the hardware at the moth's center of gravity. Based on multiple tests, dorsal mounting allows for a maximum carrying capacity of 0.5 g whereas ventral mounting with a four-point harness allows for a maximum carrying capacity of 1 g, and thus ventral mounting was used.

B. Flight Tests

Moth flight tests were conducted in a wind tunnel, and a photo of the wind tunnel test setup is shown in Fig. 22. Multiple video cameras, both high speed and regular speed, were used to capture moth movement. The UWB transmitter [20] was placed on the top of the wind tunnel, and a reference receiver was placed
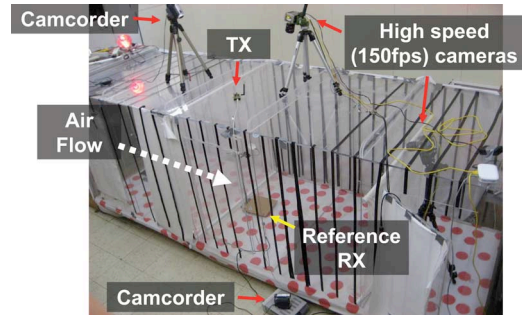

Fig. 22. Photograph of wind tunnel where moth flight tests were conducted.
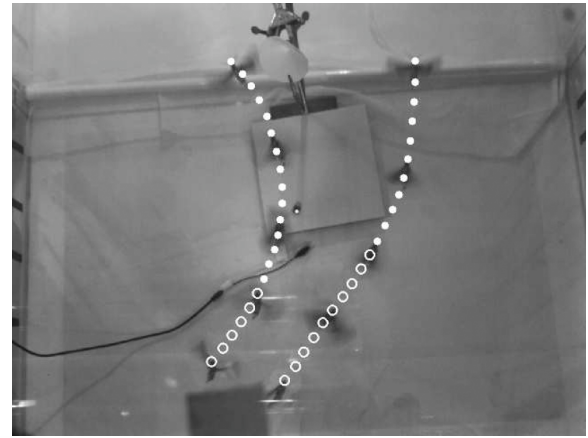

Fig. 23. Two runs of the same moth in a wind tunnel responding to identical pulse stimuli. Stimuli were generated by the receiver SoC after the receiver successfully decoded a transmitted packet. Images of the moth are shown approximately every 130 ms, with markers showing the position of the moth's head approximately every 33 ms (open symbols represent time points before stimulation, closed symbols represent time points during stimulation). In response to the stimulation pulses, the moth's flight path turns to the left.

on the bottom of the wind tunnel in view of the cameras. The reference receiver serves as a secondary LED indicator, to indicate when the moth is being stimulated with pulses. To encourage flight, the wind tunnel was set up with a 30 cm/s wind flow, and all tests were conducted in the dark, as moths typically fly at dusk in an upwind direction. In addition, a sex-pheromone lure was placed upwind from the moth, so that the moth would be encouraged to fly to it.

In a preliminary flight control experiment, a moth was able to fly while carrying the electronics, and the moth's flight direction changed in response to a pulse stimulus. The photo shown in Fig. 23 presents a time-lapsed view of two consecutive flight trajectories of the same moth while being stimulated. In both trajectories, the moth responds to a pulse stimulus with a leftward turn, with a change of bearing of 195° during 500 ms of stimulation in the trajectory on the left and a change of 162° during 350 ms of stimulation in a trajectory on the right. The same pulse stimulus pattern is applied in both trajectories.

The flight control results presented here are preliminary, in that only a single moth has been tested with the receiver with only a single stimulation pattern; however, the results do demonstrate successful operation of the receiver electronics and successful flight of the moth. In addition, in separate experiments, CNS stimulus of a loosely-tethered moth has also been shown to

influence flight direction [11]. Regardless, significant advances in understanding the neural control of flight in the moth are required before robust, multi-directional flight control can be achieved.

VI. CONCLUSION

This paper describes a hybrid-insect flight control system wherein electronics are placed on a *Manduca sexta* moth and the flight direction of the moth is controlled wirelessly. In the system, a highly integrated UWB receiver SoC is mounted on a miniature, flexible PCB and attached to a moth with a harness. The receiver leverages noncoherent, UWB signaling to relax frequency tolerances and to allow for the use of wideband, highly digital architectures. To improve energy efficiency while operating at a fixed 1 V supply, the RF front end uses a multi-stage differential inverter based amplifier with resonant *LC* load. Extensive digital calibration is used in the baseband amplifier, ADC and DLL to rapidly cancel analog voltage and timing offsets. As adult moths have a maximum carrying capacity of 1 g, several steps were taken to reduce overall system weight, including 3-D stacking and using a flexible PCB. The weight of the system is dominated by the battery, which is sized to achieve sufficient battery lifetime and to supply the average, milliwatt power levels required by the radio. Preliminary flight control of a moth was demonstrated, with a battery powered UWB receiver successfully receiving a packet and stimulating the moth, thereby changing the moth's direction of flight.

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