bq34110

Technical Reference Manual

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Contents

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Read This First

About This Manual

This technical reference manual (TRM) discusses the modules and peripherals of the bq34110 battery gas gauge, and how each is used to build a complete battery fuel gauge and end-of-service monitor. Content in this TRM complements, not supersedes, information in the *bq34110 Multi-Chemistry CEDV Battery Gas Gauge for Rarely Discharged Applications Data Sheet* (SLUSCI1).

Notational Conventions

This document uses the following conventions:

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device,
    - Reserved for future device expansion,
    - Reserved for TI testing,
    - Reserved configurations of the device that are not supported.
  - Writing non-default values to the Reserved bits could cause unexpected behavior and should be avoided.

Formatting in This Document

The following formatting convention is used in this document:

- SBS Commands: *italic* with parenthesis and no breaking spaces; for example, *RemainingCapacity()*
- Data Flash: *italic*, **bold**, and breaking spaces; for example, ***Design Capacity***
- Data Flash Bits: *italic* and **bold**; for example, ***[LED1]***
- Register Bits and Flags: *italic* and brackets; for example, *[TDA]*
- Modes and States: ALL CAPITALS; for example, UNSEALED

Glossary

TI Glossary **—** This glossary lists and explains terms, acronyms, and definitions.

Related Documentation from Texas Instruments

See the *bq34110 Multi-Chemistry CEDV Battery Gas Gauge for Rarely Discharged Applications Data Sheet* (SLUSCI1).

For product information, visit the Texas Instruments website at http://www.ti.com/product/bq34110.

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General Description

The bq34110 device incorporates gas gauging and an End-Of-Service (EOS) Determination function for use in single-cell and multi-cell battery packs, with support for multiple battery chemistries, including Li-Ion, LiFePO4, lead-acid (PbA), Nickel Metal Hydride (NiMH), and Nickel Cadmium (NiCd). The gas gauging function uses Compensated End-of-Discharge Voltage (CEDV) technology to accurately predict the battery capacity and other operational characteristics of the battery, and can be interrogated by a host processor to provide cell information, such as remaining capacity, full charge capacity, and average current.

The integrated EOS Determination function is specifically intended for applications where the battery is rarely discharged, such as in uninterruptible power supplies (UPS), enterprise server backup systems, and telecommunications backup modules. In such systems, the battery may remain in a fully (or near-fully) charged state for much of its lifetime, with it rarely or never undergoing a significant discharge. If the health of the battery in such a system is not monitored regularly, then it may degrade beyond the level required for a system backup/discharge event, and thus fail precisely at the time when it is needed most.

The EOS Determination function monitors the health of the battery through the use of infrequent learning phases, which involve a controlled discharge of ~1% capacity, and provides an alert to the system when the battery is approaching the end of its usable service. By coordinating battery charging with the learning phases, the battery capacity available to the system can be maintained above a preselected level to avoid compromising the ability for the battery to support a system discharge event.

The bq34110 device can support multi-cell battery configurations with maximum voltage up to 65 V, through the use of external and internal resistive divider networks, to reduce the voltage to an acceptable range for the device's integrated ADC. These resistive dividers are actively controlled to avoid unnecessary power dissipation when not needed. The device integrates an internal temperature sensor as well as support for an external NTC thermistor, such as a Semitec 103AT or Mitsubishi BN35–3H103FB–50.

The battery current is monitored by measuring the voltage across a series resistor, R_{SENSE}, which is placed in series with the battery pack and has a typical value of 5 mΩ to 20 mΩ. The bq34110 device integrates two ADCs, one of which is dedicated to current measurement, and the second is used for measuring several other parameters, including temperature and voltage.

Communication with the device is provided through an I^2C interface, supporting rates up to 400 kHz. Dual ALERT pins are provided with programmable configuration, which enables them to be used for such functions as a host interrupt/alert or controlling the battery charger.

To minimize power consumption, the bq34110 device has several power modes: NORMAL, SNOOZE, and SLEEP, which are under register or algorithm control. In addition, a separate chip enable (CE) pin is provided to control the internal LDO that powers the bq34110 internal circuitry, and can put the device into SHUTDOWN mode.

Information is accessed through a series of commands called Data Commands (see *Data Commands*), which are indicated by the general format *Command()*. These commands are used to read and write information contained within the bq34110 control and status registers, as well as its data flash locations.

Commands are sent from the host to the bq34110 device via I^2C and can be executed during application development, pack manufacture, or end-equipment operation. Cell information is stored in the bq34110 device in non-volatile flash memory. Many of the data flash locations are accessible during application development and pack manufacture. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by using the bq34110 companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a specific data flash location, the correct data flash subclass and offset must be known.

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The bq34110 device provides 32 bytes of user-programmable data flash memory. This data space is accessed through a data flash interface. For specifics on accessing the data flash, refer to *Accessing Data Flash*.

A SHA-1/HMAC-based battery pack authentication feature is also implemented on the bq34110 device. When the device is in UNSEALED mode, authentication keys can be (re)assigned. A scratch pad area is used to receive challenge information from a host and to export SHA-1/HMAC encrypted responses. See the *Authentication* section for further details.

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Functional Description

2.1 Device Configuration

The bq34110 device has many features that can be enabled, disabled, or modified through settings in the ***Operation Config A*** data flash. These registers are programmed/read via the methods described in *Accessing Data Flash*.

2.1.1 Operation Config A

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Registers	Operation Config A	hex	2	—	—	—	—

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	TEMPS	RSVD	RSVD	RSVD	RSVD	SCALED	SLEEP	SLPWAKE CHG
Low Byte	JEITA	GNDSEL	NiMH_ CHG_EN	Ni_DT	Ni_DV	IWAKE	RSNS1	RSNS0

Legend = **RSVD**: Reserved. Do not use.

TEMPS: Selects external thermistor for *Temperature()* measurements.
True when set. Uses internal temp when clear. The default is 1.

RSVD: Reserved. Do not use.

SCALED: Scaled Capacity and/or Current bit
When set, this bit flags the system that the mA, mAh, and mWh settings and reports will take on a value that is artificially scaled. This setting has no actual effect within the gauge. It is the responsibility of the host to reinterpret the reported values. Scaled current measurement is achieved by calibrating the current measurement to a value lower than actual. The default is 0.

SLEEP: When this bit is set, the bq34110 device can enter sleep if operating conditions allow. The default is 1.

SLPWAKECHG: When this bit is set, the gauge will accumulate estimated charge that has passed during sleep upon wake from sleep when *Current()* > ***Sleep Current,*** but not enough to trigger wake event. If not set, the estimated charge during sleep is not accumulated. The default is 0.

JEITA: When this bit is set, the device performs charging voltage and current selection based on parameters specified in ***Charger Control:JEITA Temperature***. See *Charging and Charge Termination*. The default is 0.

GNDSEL: The ADC ground select control
The VSS pin is selected as ground reference when the bit is clear. SRN is selected when the bit is set. The default is 0.

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NIMH_CHG_EN: When set, the device performs primary charge termination using one of the NiXX algorithms, which may be the ΔT/Δt algorithm or the –ΔV algorithm. See *Charging and Charge Termination*. If ***[NIMH_CHG_EN]*** is set and both ***[Ni_DT]*** and ***[Ni_DV]*** are cleared, the gauge will use the –ΔV algorithm. If ***[NIMH_CHG_EN]*** is cleared, the device will use either JEITA-based charging or WHr Charging, depending on their settings. The default is 0.

Ni_DT: When set, the device performs primary charge termination using the ΔT/Δt algorithm. See *Charging and Charge Termination*. The default is 0.

Ni_DV: When set, the device performs primary charge termination using the –ΔV algorithm. See *Charging and Charge Termination*. The default is 0.

IWAKE/RSNS1/ RSNS0: These bits configure the current wake function (see *Wake-Up Comparator*). The default is ***[IWAKE]***=1, ***[RSNS1]***=0, ***[RSNS0]***=0.

2.1.2 Manufacturer Testing

To improve the manufacturer testing flow, the bq34110 device allows certain features to be toggled on or off through *Control()* commands: for example, the Lifetime Data Collection status is toggled using the *LIFETIME_EN()* subcommand. Enabling only the feature under test can simplify the test flow in production by avoiding any feature interference. These toggling commands will only set the RAM data, which means the conditions set by these commands will be cleared if a reset or seal is issued to the gauge. The *ManufacturingStatus()* keeps track of the status (enabled or disabled) of each feature.

The data flash ***Manufacturing Status Init*** provides the option to enable or disable individual features for normal operation. Upon a reset or a seal command, the *ManufacturingStatus()* will be reloaded from data flash ***Manufacturing Status Init***. This also means if an update is made to *ManufacturingStatus()* to enable or disable a feature, the gauge will only take the new setting if a reset or seal command is sent.

2.1.3 Manufacturing Status Init

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Manufacturing	Manufacturing Status Init	hex	2	—	—	—	—

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
LSB	RSVD	WHR_EN	LF_EN	PCTL_EN	EOS_EN	IGNORE_SD_EN	ACCHG_EN	ACDSG_EN

Legend = **RSVD**: Reserved. Do not use.

WHR_EN: ***WHr Charge Termination*** Enable

1 = ***WHr Charge Termination*** enabled

0 = ***WHr Charge Termination*** disabled (default)

LF_EN: Lifetime Data Collection Enable

1 = Enabled

0 = Disabled (default)

PCTL_EN: Pin Control Enable

This bit allows the host to manually control the state of the pins ALERT1, ALERT2, VEN, and LEN through the *ManufacturerAccessControl()* subcommands *PIN_ALERT1_SET()*, *PIN_ALERT1_RESET()*, *PIN_ALERT2_SET()*, *PIN_ALERT2_RESET()*, *PIN_VEN_SET()*, *PIN_VEN_RESET()*, *PIN_LEN_SET()*, and *PIN_LEN_RESET()*.
NOTE: If ALERT1 or ALERT2 pins are under manual pin control, they should not also be used for alert/interrupt purposes.

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1 = Manual pin control is enabled.

0 = Manual pin control is disabled (default).

EOS_EN: End-Of-Service Determination Enable

Note that if ***[EOS_EN]*** is changed directly in data flash, then the device should be reset for the change to take effect.

1 = End-Of-Service Determination is enabled.

0 = End-Of-Service Determination is disabled (default).

IGNORE_SD_EN: Ignore Self-Discharge Control

1 = Accumulated charge integration ignores self-discharge and only integrates real current.

0 = Accumulated charge integration includes both real and self-discharge current (default).

ACCHG_EN: Accumulated Charge Enable for Charging Current Integration

1 = Positive (charging) values of *Current()* are integrated (default).

0 = Positive (charging) values of *Current()* are not integrated.

ACDSG_EN: Accumulated Charge Enable for Discharging Current Integration

1 = Negative (discharging) values of *Current()* are integrated (default).

0 = Negative (discharging) values of *Current()* are not integrated.

2.2 Pin Controls

The bq34110 device includes multiple pins that can be used for different purposes based on the system configuration, including two ALERT pins (ALERT1 and ALERT2), and can be used as interrupts to a host processor. The device provides a variety of status flags that can be configured to combine together into a single alert signal to generate a single interrupt (for example, using the ALERT1 pin), or flags can be separated to trigger two separate interrupts (using both the ALERT1 and ALERT2 pins). The alert settings are controlled by the ***Pin Control Config*** data flash value.

2.2.1 Pin Control Config

Class	Subclass	Name	Format	Size	Min Value	Max Value	Default Value	Unit
Settings	Configuration	Pin Control Config	hex	1	0x00	0xFF	0x00	—

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	VEN_EN	ALERT2_POL	ALERT2_EN	ALERT1_POL	ALERT1_EN

Legend = **RSVD**: Reserved. Do not use.

VEN_EN: VEN pin control for external voltage divider operation

When set, the VEN pin is used to control an external voltage divider, which provides the divided down voltage to the BAT pin. Setting this pin also disables the use of the internal battery voltage divider within the device. When this bit is cleared, the internal battery divider will be activated whenever a battery voltage measurement is activated.

ALERT1_EN and **ALERT2_EN**: ALERT1 and ALERT2 pin control

These bits are used to control the function of the ALERT1 and ALERT2 pins. When set, the corresponding ALERT pin is used as an interrupt.

ALERT1_POL and **ALERT2_POL**: ALERT1 and ALERT2 interrupt polarity control

These bits are used to control the polarity of the corresponding ALERT pin when used as an interrupt. When set, the pin will have a high output level when the interrupt is set.

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The ***Alert1_0 Config*** to ***Alert1_6 Config*** and ***Alert2_0 Config*** to ***Alert2_6 Config*** data flash values are used to determine which of many internal flags and condition bits can trigger the ALERT1 and ALERT2 interrupt signals. These configuration flash are identical, allowing any combination of flags to be combined to generate the two alert signals.

For example, when Bit 0 (***[DSG]***) in ***Alert1_0 Config*** is set AND the corresponding bit in *BatteryAlert()* (that is, *[DSG]*) is set, then the ALERT1 interrupt will be generated.

The ***Alert1_0..6 Config*** and ***Alert2_0..6 Config*** signals are cleared upon a read of *ALERT1STATUS()* or *ALERT2STATUS()*, respectively.

Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Settings	Configuration	Alert1_0 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_1 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_2 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_3 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_4 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_5 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert1_6 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_0 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_1 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_2 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_3 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_4 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_5 Config	Hex	1	—	—	—	—
Settings	Configuration	Alert2_6 Config	Hex	1	—	—	—	—

The bits in ***ALERT1_0 Config*** and ***ALERT2_0 Config*** match the bits in *BatteryStatus()* lower byte.

7	6	5	4	3	2	1	0
SLEEP	CHGINH	FD	FC	TCA	TDA	CHG	DSG

The bits in ***Alert1_1 Config*** and ***Alert2_1 Config*** match the bits in *BatteryStatus()* upper byte with an exception in Bit 7.

7	6	5	4	3	2	1	0
RSVD	SOCLOW	UTC	UTD	OTC	OTD	BATHIGH	BATLOW

The bits in ***Alert1_2 Config*** and ***Alert2_2 Config*** match the bits in *EOSLearnStatus()* lower byte.

7	6	5	4	3	2	1	0
LCTO	LFAULT	LABRT	LCMD	LPER	LRLX	LCHG	LDSG

The bits in ***Alert1_3 Config*** and ***Alert2_3 Config*** match the bits in *EOSLearnStatus()* upper byte.

7	6	5	4	3	2	1	0
LDONE	LRES	LRSTOR	LCTLEDGE	LUCD	LDPAM	LDPAT	LDPAI

The bits in ***Alert1_4 Config*** and ***Alert2_4 Config*** match the bits in *EOSStatus()*.

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7	6	5	4	3	2	1	0
SRRL	SRCL	RSVD	LTI	RSDLI	RCELLR	IRRCOMP	IRCOMP

The bits in ***Alert1_5 Config*** and ***Alert2_5 Config*** match the bits in *EOSSafetyStatus()*, compressed into a single byte.

7	6	5	4	3	2	1	0
RSVD	RSDLWARN	RSDWARN	DRDWARN	RSVD	RSDLALERT	RSDALERT	DRDALERT

The bits in ***Alert1_6 Config*** and ***Alert2_6 Config*** include the following bits.

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	ACTHR	BLT

Legend = **RSVD:** Reserved. Do not use.

BATLOW: Battery voltage low condition
- 1 = ALERT is triggered when BATLOW becomes set.
- 0 = ALERT is not triggered when BATHIGH becomes set (default).

BATHIGH: Battery voltage high condition
- 1 = ALERT is triggered when BATHIGH becomes set.
- 0 = ALERT is not triggered when BATHIGH becomes set (default).

SOCLOW: Low SOC State is detected.
- 1 = ALERT is triggered when SOCLOW becomes set.
- 0 = ALERT is not triggered when SOCLOW becomes set (default).

ACTHR: Accumulated Charge Threshold Flag
- 1 = The ***Accumulated Charge*** was detected passing a threshold.
- 0 = The ***Accumulated Charge*** has not been detected passing a threshold.

OTC: Overtemperature in Charge condition detected
- 1 = ALERT is triggered when OTC becomes set.
- 0 = ALERT is not triggered when OTC becomes set (default).

OTD: Overtemperature in Discharge condition is detected.
- 1 = ALERT is triggered when OTD becomes set.
- 0 = ALERT is not triggered when OTD becomes set (default).

UTC: Undertemperature in Charge condition detected
- 1 = ALERT is triggered when UTC becomes set.
- 0 = ALERT is not triggered when UTC becomes set (default).

UTD: Undertemperature in Discharge condition is detected.
- 1 = ALERT is triggered when UTD becomes set.
- 0 = ALERT is not triggered when UTD becomes set (default).

CHGINH: Charge Inhibit. Unable to begin charging.

Refer to the data flash ***[Charge Inhibit Temp Low, Charge Inhibit Temp High]*** parameters.
- 1 = ALERT is triggered when CHGINH becomes set.
- 0 = ALERT is not triggered when CHGINH becomes set (default).

FC: Full charge is detected.

This bit is controlled by settings in ***SOC Flag Config A*** and ***SOC Flag Config B***.
- 1 = ALERT is triggered when FC becomes set.

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0 = ALERT is not triggered when FC becomes set (default).

FD: Full discharge is detected. This bit is controlled by settings in ***SOC Flag Config B***.

1 = ALERT is triggered when FD becomes set.

0 = ALERT is not triggered when FD becomes set (default).

DSG: Discharging is detected.

1 = ALERT is triggered when DSG becomes set.

0 = ALERT is not triggered when DSG becomes set (default).

CHG: Charging is detected.

1 = ALERT is triggered when CHG becomes set.

0 = ALERT is not triggered when CHG becomes set (default).

DRDALERT: EOS Direct Resistance Detection Alert becomes set.

1 = ALERT is triggered when DRDALERT becomes set.

0 = ALERT is not triggered when DRDALERT becomes set (default).

DRDWARN: EOS Direct Resistance Detection Warning becomes set.

1 = ALERT is triggered when DRDWARN becomes set.

0 = ALERT is not triggered when DRDWARN becomes set (default).

RSDALERT: EOS Resistance Slope Detection Alert becomes set.

1 = ALERT is triggered when RSDALERT becomes set.

0 = ALERT is not triggered when RSDALERT becomes set (default).

RSDWARN: EOS Resistance Slope Detection Warning becomes set.

1 = ALERT is triggered when RSDWARN becomes set.

0 = ALERT is not triggered when RSDWARN becomes set (default).

RSDLALERT: EOS Resistance Slope Detection Long-Term Alert becomes set.

1 = ALERT is triggered when RSDLALERT becomes set.

0 = ALERT is not triggered when RSDLALERT becomes set (default).

RSDLWARN: EOS Resistance Slope Detection Long-Term Warning becomes set.

1 = ALERT is triggered when RSDLWARN becomes set.

0 = ALERT is not triggered when RSDLWARN becomes set (default).

LCTLEDGE: Learning Discharge (*[LDSG]*) changes state

1 = ALERT is triggered when *[LDSG]* changes state (this is only applicable when LENCTL=0).

0 = ALERT is not triggered when *[LDSG]* changes state (default).

LCTO: Learn Charge Time Out becomes set.

1 = ALERT is triggered when LCTO becomes set.

0 = ALERT is not triggered when LCTO becomes set (default).

LDPAI: Learning Discharge Phase Abort on Current becomes set.

1 = ALERT is triggered when LDPAI becomes set.

0 = ALERT is not triggered when LDPAI becomes set (default).

LDPAT: Learning Discharge Phase Abort on Temperature becomes set.

1 = ALERT is triggered when LDPAT becomes set.

0 = ALERT is not triggered when LDPAT becomes set (default).

LDPAM: Learning Discharge Phase Abort on Timer becomes set.

1 = ALERT is triggered when LDPAM becomes set.

0 = ALERT is not triggered when LDPAM becomes set (default).

RSDLI: Resistance Slope Decisioning Long-Term Invalid

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This bit is set = 1 if the bq34110 EOS Determination function detects that the timer has been interrupted since the ***Initial RRate*** was calculated. In this case, the RSDL algorithm will no longer trigger an alert or warning.

1 = A timer interruption was detected.

0 = A timer interruption has not been detected.

LTI: Learn Timer Invalid

This bit is set = 1 if the bq34110 EOS Determination function detects the timer has been interrupted since the most recent ***Rcell*** was calculated. In this case, the RSD algorithm must capture two new ***Rcell*** values separated in time in order to calculate a new value of ***RRate*** and evaluate this for corresponding alerts and warnings.

1 = A timer interruption was detected.

0 = A timer interruption has not been detected.

RCELLR: ***Rcell*** Reduction Alert

This bit is set = 1 if the bq34110 EOS Determination function detects a value of ***Rcell***, which is more than 2% below the previous value of ***Rcell***. This signal is cleared when the register is read or if a new learning phase begins.

1 = A reduction in ***Rcell*** was detected.

0 = A reduction in ***Rcell*** has not been detected.

IRCOMP: ***Initial Rcell*** Calculation Complete

This bit is set = 1 if the bq34110 EOS Determination function has completed the required learning phases to calculate a value of ***Initial Rcell***. This bit is reset when a new ***Initial Rcell*** calculation is triggered, until the new calculation is complete. This bit can be written by the host through loading data flash, if the host wishes to initialize the device with previously calculated ***Initial Rcell*** data and not trigger a new ***Initial Rcell*** calculation.

1 = ***Initial Rcell*** was obtained.

0 = ***Initial Rcell*** has not been obtained.

IRRCOMP: ***Initial RRate*** Calculation Complete

This bit is set = 1 if the bq34110 EOS Determination function has completed the required learning phases to calculate a value of ***Initial RRate***. This bit is reset when a new ***Initial RRate*** calculation is triggered, until the new calculation is complete. This bit can be written by the host through loading data flash if the host wants to initialize the device with previously calculated ***Initial RRate*** data and not trigger a new ***Initial RRate*** calculation.

1 = ***Initial RRate*** was obtained.

0 = ***Initial RRate*** has not been obtained.

BLT: Battery Level Threshold becomes set.

1 = ALERT is triggered when BLT becomes set.

0 = ALERT is not triggered when BLT becomes set (default).

2.3 Voltage Measurement and Calibration

The bq34110 device is shipped with a factory configuration for the default case of the 1-series Li-Ion cell. This can be changed by setting the ***[VEN_EN]*** bit and by setting the number of series cells in the data flash configuration section.

Multi-cell applications, with voltages up to 65535 mV, may be gauged by using the appropriate input scaling resistors such that the maximum battery voltage, under all conditions, appears at the BAT input as approximately 900 mV. The actual gain function is determined by a calibration process and the resulting voltage calibration factor is stored in the data flash location ***Voltage Divider***.

For single-cell applications, an external divider network is not required. Inside the IC and behind the BAT pin is a nominal 5:1 voltage divider with 88 kΩ in the top leg and 22 kΩ in the bottom leg. This internal divider network is enabled when a battery voltage measurement is activated if the ***[VEN_EN]*** bit is not set. This ratio is optimum for directly measuring a single Li-Ion cell where charge voltage is limited to 4.5 V.

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For higher voltage applications, an external resistor divider network should be implemented as per the reference designs in this document. The quality of the divider resistors is very important to avoid gauging errors over time and temperature. It is recommended to use 0.1% resistors with 25-ppm temperature coefficient. Alternately, a matched network could be used that tracks its dividing ratio with temperature and age due to the similar geometry of each element.

Calculation of the series resistor can be made per the equation below.

NOTE: Exceeding ***Vin max mV*** results in a measurement with degraded linearity.

The bottom leg of the divider resistor should be in the range of 15 kΩ to 25 kΩ, using 16.5 kΩ:

Rseries = 16500 Ω (Vin max mV – 900 mV) / 900 mV (1)

For all applications, the ***Voltage Divider*** value in data flash will be used by the firmware to calibrate the total divider ratio. The nominal value for this parameter is the maximum expected value for the stack voltage. The calibration routine adjusts the value to force the reported voltage to equal the actual applied voltage.

Table 2-1. Voltage Divider

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Calibration	Data	Voltage Divider	Unsigned Integer	2	0	65535	5000	mV

2.3.1 1S Example

For stack voltages under 4.5 V max, it is not necessary to provide an external voltage divider network. The internal 5:1 divider should be selected by clearing the ***[VEN_EN]*** bit. The default value for ***Voltage Divider*** is 5000 (representing the internal 5000:1000 mV divider) when no external divider resistor is used, and the default number of series cells = 1. In the 1-S case, there is usually no requirement to calibrate the voltage measurement, because the internal divider is calibrated during factory test to within 2 mV.

2.3.2 7S Example

In the multi-cell case, the hardware configuration is different. An external voltage divider network is calculated using the Rseries formula above. The bottom leg of the divider should be in the range of 15 kΩ to 25 kΩ.

2.3.3 Hardware Considerations for High Voltage Packs

For an application exceeding ~60 V, the external voltage divider should be selected to reduce the maximum pack voltage to a level of approximately 900 mV at the device BAT pin. Figure 2-1 shows the BAT resistor divider. For example, if an 18S Li-Ion pack is used, then the maximum pack voltage should be set to the recommended single-cell maximum voltage (for example, 5 V) times the actual number of series cells (for example 18) which is 90 V.

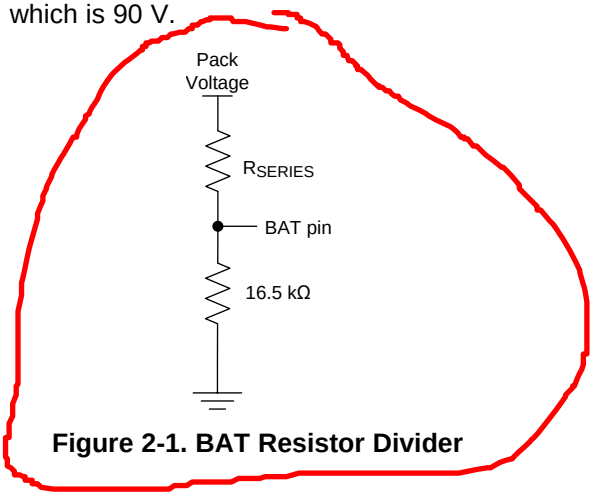

Figure 2-1. BAT Resistor Divider

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Use Equation 2 to setup the voltage divider to support a 90-V pack voltage.

$$R_{SERIES} = 16\,500\ \Omega \times \frac{(\text{Maximum Pack Voltage mV} - 900\ \text{mV})}{900\ \text{mV}} \quad (2)$$

The second resistor in the resistor divider network should have a value between 15 kΩ and 25 kΩ. For this example, use 16.5 kΩ and Equation 3 to calculate the series resistance.

$$R_{SERIES} = 16\,500\ \Omega \times \frac{(90\,000\ \text{mV} - 900\ \text{mV})}{900\ \text{mV}} = 1.631\ \text{M}\Omega \quad (3)$$

A standard value 1.62-MΩ resistor will support an 89-V pack voltage and provide adequate cell-voltage measurement margin for a Li-Ion cell.

2.3.4 Parameter Configuration Considerations for High Voltage Applications

The data flash configuration must scale the pack voltage to ensure that the maximum reported voltage does not exceed 65 535 mV.

This additional scaling is created by scaling the value stored in number of series cells, together with the value used for the external voltage divider ratio. Use Equation 4 to calculate the maximum pack voltage with the example values.

$$\frac{\text{Maximum Pack Voltage}}{\text{Maximum Reportable Value}} = \frac{90\,000\ \text{mV}}{65\,535\ \text{mV}} = 1.38 \quad (4)$$

The number of series cells is an integer unit so the scaling factor should be rounded up. For this example, use a 2x scaling factor.

$$\text{Stored Number of Cells} = \frac{\text{Actual Number of Cells}}{\text{Scaling Factor}} \rightarrow \frac{18}{2} = 9 \quad (5)$$

Therefore, the ***Number of Series Cells*** is set to 9. The voltage must be divided by 2 when calibrating the voltage. For example, if the applied pack voltage is 80 V, then the designer should enter 40 000 mV in the program. This will result in the ***Voltage Divider*** being calibrated to a value near 44500 mV (representing 1/2 of the 89:1 divider ratio).

In this configuration, the host device that is reading the reported voltage value must also know that the voltage is scaled so that it can rescale the voltage to the true pack voltage.

Due to the maximum ***Voltage Divider*** setting of 65535 (which represents a resistive divide ratio of 65.536:1), which may need to be slightly higher due to calibration for resistor tolerances, it is recommended to use a maximum divider ratio of 60:1 when scaling is not being used

NOTE: The actual number of series cells that can be scaled is limited. The result of the equation must be an integer. The result cannot be rounded up or down because this would cause the gauge to calculate the wrong cell voltage. As an example, if the actual number of series cells was 17, then the number of series cells must be set to 17 and the voltage will be reported as a single cell. The ***[VEN_EN]*** bit must be set in the pack configuration register.

2.3.5 Considerations for High-Current Systems (> ±32 767 mA)

The gauge can support charge and discharge currents up to 32 767 mA. Current scaling is required to support higher currents. High-current packs are typically high-capacity packs as well, so both the current and capacity may need to be considered when scaling the pack. The scale factor is calculated for both parameters and the largest scale factor is used for both parameters.

2.3.5.1 Hardware Considerations

To ensure accurate current measurement, the input voltage generated across the current-sense resistor should not exceed ±125 mV. The value of the sense resistor must be set to ensure that this voltage is not exceeded at the maximum charge and discharge current.

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2.3.5.2 Parameter Configuration Considerations

The data flash configuration must scale the current to ensure that the maximum current does not exceed 32 767 mA. As an example, if the maximum discharge current is 64 A, then the scale factor is set to 64 000 mA / 32 767 mA = 1.95x or is rounded up to 2x. All current and capacity parameters in the data flash should be divided by 2.

2.3.5.3 How to Calibrate for Current Scaling

The current must be scaled during the calibration phase. If 2x scaling is used, then the current is divided by 2. If a 4-A discharge current is used to calibrate the pack, then –2000 mA is entered as the actual current. All current and capacity parameters are reported at half the actual value and the host must to multiply these parameters by the scale factor to find the true value.

2.3.6 Considerations for High-Capacity Systems (> 29 Ah)

The gauge can support pack capacities up to 29 Ah. Current scaling is required to support higher capacities. High-capacity packs are typically high current packs as well, so both the current and capacity may need to be considered when scaling the pack. The scale factor is calculated for both parameters and the largest scale factor is used for both parameters.

2.3.6.1 Parameter Configuration Considerations

The data flash configuration must scale the capacity to ensure that the maximum capacity does not exceed 29 000 mAh. As an example, if the maximum pack capacity is 100 Ah, then the scale factor is set to 100 000 mAh / 29 000 mAh = 3.45x or rounded up to 4x. All current and capacity parameters in the data flash (such as ***Sleep Current***, ***Quit Current***, ***Design Capacity***, ***Accumulated Charge Positive Threshold***, and so on) are divided by 4x, and current calibration must also follow the scaling, as described in Section 2.3.5.3.

2.3.7 Autocalibration

The bq34110 device provides an autocalibration feature that will measure the voltage offset error across SRP and SRN as operating conditions change. It subtracts the resulting offset error from normal sense resistor voltage, V_{SR}, for maximum measurement accuracy.

The device performs a single offset calibration at entry to SLEEP mode, except if *Temperature()* is ≤ ***Offset Cal Inhibit Temp Low*** or *Temperature()* is ≥ ***Offset Cal Inhibit Temp High***.

The gas gauge also performs a single offset when:

1. Voltage change since last offset calibration ≥ 256 mV for 30 s OR
2. Temperature change since last offset calibration is greater than 8°C for ≥ 30 s OR
3. *AverageCurrent()* < 100 mA for 30 s.

Capacity and current measurements should continue at the last measured rate during the offset calibration when these measurements cannot be performed. If the battery voltage drops more than 256 mV during the offset calibration, the load current has likely increased; thus, the offset calibration is aborted. The *CONTROL_STATUS()[CCA]* bit is set during coulomb counter autocalibration.

Automatic offset calibration will not be initiated during a learning phase when the EOS Determination function is enabled.

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The bq34110 device defines the coulomb counter deadband voltage for the measured voltage between the SRP and SRN pins used for capacity accumulation in units of 294 nV. Any voltages within ***±CC Deadband*** do not contribute to capacity accumulation.

The device also uses the ***Deadband*** parameter, such that any current within ± ***Deadband*** will be reported as 0 mA by the *Current()* function. This parameter does not affect capacity accumulation.

2.3.7.1 Deadband

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Calibration	Current	Deadband	Unsigned Integer	1	0	255	5	mA

2.3.7.2 CC Deadband

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Calibration	Current	CC Deadband	Unsigned Integer	1	0	255	17	294 nV

2.3.7.3 Offset Cal Inhibit Temp Low

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Power	Offset Cal Inhibit Temp Low	Signed Integer	2	–400	1200	50	0.1°C

2.3.7.4 Offset Cal Inhibit Temp High

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Power	Offset Cal Inhibit Temp High	Signed Integer	2	–400	1200	450	0.1°C

2.4 Temperature Measurement

The bq34110 device can measure temperature through an integrated temperature sensor or an external NTC thermistor. Only one source can be used, and the selection is made by setting ***Operation Config A [TEMPS]*** appropriately. Temperature measurements are made by calling the *Temperature()* function (see *Data Commands* for specific information).

TEMPS: *Temperature()* source selection

1 = External temperature sensor is used (default).

0 = Internal temperature sensor is used.

When an external thermistor is selected, REG25 (pin 7) is used to bias the thermistor and TS (pin 11) is used to measure the thermistor voltage (a pull-down circuit is implemented inside the device). The device then correlates the voltage to temperature, assuming the thermistor is a Semitec 103AT or similar device.

The bq34110 device includes a temperature model for the internal as well as external temperature measurements. The external temperature model default values model a Semitec 103AT NTC thermistor.

NOTE: Do not modify these values without consulting with TI.

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Table 2-2. Internal Temperature Measurement Model

Subclass Name	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Units
Temp Model	Int Coeff 1	Signed integer	2	–32768	32767	0	Num
Temp Model	Int Coeff 2	Signed integer	2	–32768	32767	0	Num
Temp Model	Int Coeff 3	Signed integer	2	–32768	32767	–12324	Num
Temp Model	Int Coeff 4	Signed integer	2	–32768	32767	6131	0.1°K
Temp Model	Int Min AD	Signed integer	2	–32768	32767	0	Num
Temp Model	Int Max Temp	Signed integer	2	–32768	32767	6131	0.1°K

Table 2-3. External Temperature Measurement Model

Subclass Name	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Units
Temp Model	Ext Coeff 1	Signed integer	2	–32768	32767	20982	Num
Temp Model	Ext Coeff 2	Signed integer	2	–32768	32767	–13836	Num
Temp Model	Ext Coeff 3	Signed integer	2	–32768	32767	5202	Num
Temp Model	Ext Coeff 4	Signed integer	2	–32768	32767	2337	0.1°K
Temp Model	Ext Min AD	Signed integer	2	–32768	32767	12909	Num

The bq34110 device also includes temperature compensation for the internal voltage reference when used for voltage measurement.

Table 2-4. Internal Voltage Reference Temperature Compensation Model

Subclass Name	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Units
Temp Model	Vcomp Coeff 1	Signed integer	2	–32768	32767	0	Num
Temp Model	Vcomp Coeff 2	Signed integer	2	–32768	32767	14902	Num
Temp Model	Vcomp Coeff 3	Signed integer	2	–32768	32767	–623	Num
Temp Model	Vcomp Coeff 4	Signed integer	2	–32768	32767	37	Num
Temp Model	Vcomp Input Multiplier	Unsigned integer	1	0	255	48	Num
Temp Model	Vcomp Output Divisor	Signed integer	2	–32768	32767	256	Num

2.4.1 Overtemperature: Charge

If during charging, *Temperature()* reaches the threshold of ***OT Chg*** for a period of ***OT Chg Time*** and *AverageCurrent()* > ***Charge Detection Threshold***, then the *[OTC]* bit of *BatteryStatus()* is set.

NOTE: If ***OT Chg Time*** = 0, then the feature is completely disabled.

2.4.1.1 OT Chg

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTC	OT Chg	Unsigned Integer	2	0	1200	550	0.1°C

2.4.1.2 Charge Detection Threshold

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Current Thresholds	Chg Detection Threshold	Unsigned Integer	2	0	2000	75	mA

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2.4.1.3 OT Chg Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTC	OT Chg Time	Unsigned Integer	1	0	60	2	s

2.4.1.4 OT Chg Recovery

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTC	OT Chg Recovery	Unsigned Integer	2	0	1200	500	0.1°C

2.4.2 Overtemperature: Discharge

If during discharging or relaxation, *Temperature()* reaches the threshold of ***OT Dsg*** for a period of ***OT Dsg Time***, and *AverageCurrent()* ≤ –***Discharge Detection Threshold***, then the *[OTD]* bit of *BatteryStatus()* is set. If ***OT Dsg Time*** = 0, then the feature is completely disabled.

When *Temperature()* falls to ***OT Dsg Recovery***, the *[OTD]* bit of *BatteryStatus()* is reset.

2.4.2.1 OT Dsg

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTD	OT Dsg	Unsigned Integer	2	0	1200	600	0.1°C

2.4.2.2 OT Dsg Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTD	OT Dsg Time	Unsigned Integer	1	0	60	2	s

2.4.2.3 Discharge Detection Threshold

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Current Thresholds	Discharge Detection Threshold	Unsigned Integer	2	0	2000	60	mA

2.4.2.4 OT Dsg Recovery

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	OTD	OT Dsg Recovery	Unsigned Integer	2	0	1200	550	0.1°C

2.4.3 Undertemperature: Charge

If during charging, *Temperature()* reaches the threshold of ***UT Chg*** for a period of ***UT Chg Time*** and *AverageCurrent()* > ***Charge Detection Threshold***, then the *[UTC]* bit of *BatteryStatus()* is set.

NOTE: If ***UT Chg Time*** = 0, then the feature is completely disabled.

When *Temperature()* rises to ***UT Chg Recovery***, the *[UTC]* of *BatteryStatus()* is reset.

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2.4.3.1 UT Chg

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTC	UT Chg	Signed Integer	2	–1200	1200	–100	0.1°C

2.4.3.2 UT Chg Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTC	UT Chg Time	Unsigned Integer	1	0	60	2	s

2.4.3.3 UT Chg Recovery

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTC	UT Chg Recovery	Signed Integer	2	–1200	1200	0	0.1°C

2.4.4 Undertemperature: Discharge

If during discharging or relaxation, *Temperature()* reaches the threshold of ***UT Dsg*** for a period of ***UT Dsg Time***, and *AverageCurrent()* ≤ –***Discharge Detection Threshold***, then the *[UTD]* bit of *BatteryStatus()* is set. If ***UT Dsg Time*** = 0, then the feature is completely disabled.

When *Temperature()* rises to ***UT Dsg Recovery***, the *[UTD]* bit of *BatteryStatus()* is reset.

2.4.4.1 UT Dsg

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTD	UT Dsg	Signed Integer	2	–1200	1200	–150	0.1°C

2.4.4.2 UT Dsg Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTD	UT Dsg Time	Unsigned Integer	1	0	60	2	s

2.4.4.3 UT Dsg Recovery

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Safety	UTD	UT Dsg Recovery	Signed Integer	2	–1200	1200	–50	0.1°C

2.5 SCALED Mode

The bq34110 device supports high-current and high-capacity batteries above 32.76 A and 29 Ah indirectly by scaling the actual sense resistor value compared with the calibrated value stored in the device. The need for this is due to the standardization of a 2-byte data command having a maximum representation of +/–32767. When the ***[SCALED]*** bit is set, this indicates that the current and capacity data is scaled.

It is important to know that setting the ***[SCALED]*** flag does not actually change anything in the operation of the device. It serves as a notice to the host that the various reported values should be reinterpreted based on the scale used. Because the flag has no actual effect, it can be used to represent other scaling values.

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NOTE: It is recommended to only scale by a value between 1 and 10 to optimize resolution and accuracy while still extending the data range.

2.6 Accumulated Charge Measurement

The bq34110 device integrates an ***Accumulated Charge*** function that measures the integrated charge passed in or out of the cell since the integration is reset. This function can be used to generate an alert to the host when a programmable threshold of ***Accumulated Charge*** is achieved.

The device also integrates the elapsed time since the integration began, assuming the timer has not been interrupted by a power cycle or put into SHUTDOWN mode. This time is read using the command *AccumulatedTime()*. If an event has occurred that interrupted the timer, the value of *AccumulatedTime()* will be fixed unchanging at 0 until the integration is reset.

The charge and time integration is reset at full charge termination or upon issue of the *AccumulationReset()* command. While the battery is discharging (that is, the measured *Current()* is negative), then the charge integration counter increases. If the battery starts charging (that is, the measured *Current()* is positive), then the charge integration counter decreases. The integrated charge value in mAh can be read by the host using the command *AccumulatedCharge()*. The elapsed time (which does not decrease in value) is read by issuing the *AccumulatedTime()* command.

The ***Accumulated Charge*** calculation uses the current measured across the sense resistor and, similar to the coulomb counter integration, ignores currents below a programmed level controlled by ***CC Deadband***. In periods when the bq34110 device is in SNOOZE or SLEEP mode, the ***Accumulated Charge*** integration includes an estimate of the charge integrated based on analysis of the periodic measured current.

If the user prefers to include cell self-discharge in the integration, this capability can be enabled or disabled using the ***[IGNORE_SD_EN]*** configuration bit.

The charge integration can also be limited to only include positive (charging) currents, only negative (discharging) currents, or both, through setting the ***[ACCHG_EN]*** and ***[ACDSG_EN]*** configuration bits. If ***both [ACCHG_EN]*** and ***[ACDSG_EN]*** are reset, then the timer is halted. These bits can be set using the *ACCUM_CHG_EN()* and *ACCUM_DSG_EN()* commands.

When the cell is fully charged and the FC bit is set due to normal charge termination, then the integration counter is again reset. At this point, the values of ***Accumulated Charge*** and time just before reset are stored and can be read using *LastAccumulatedCharge()* and *LastAccumulatedTime()*. The values stored in *LastAccumulatedCharge()* and *LastAccumulatedTime()* are cleared each time the command is issued and the respective value read. They are also overwritten whenever the integration counter is reset again. The user can set thresholds to alert the host when *AccumulatedCharge()* reaches a particular level in both the charge (positive) and discharge (negative) directions. These thresholds are set by ***Accumulated Charge Positive Threshold*** and ***Accumulated Charge Negative Threshold***.

NOTE: *AccumulatedCharge()* does not reset when a threshold is reached, the reset should be initiated by the host using *AccumulationReset()*. When a threshold is passed, a flag is set in *OperationStatus()[ACTHR]*.

It is possible for the integration counter to be reset at normal charge termination, but the charger to continue charging the battery for additional time until the charger ceases charging. In this case, the integration counter would reset, then proceed to integrate this additional charge. The user should be aware of this possibility and if it is a concern to plan for a workaround, such as programming the integration to only accumulate discharging currents or to detect when the charger stops charging, and then issue an *AccumulationReset()* command to clear any residual charging integration.

Due to the charge integration and timer information being stored in RAM, any power cycle of the device or putting the device into SHUTDOWN will result in the loss of *AccumulatedCharge()*, *AccumulatedTime()*, *LastAccumulatedCharge()*, and *LastAccumulatedTime()* data.

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Command	R/W	Type	Min	Max	Default	Units
AccumulatedCharge	R	Signed integer, 2-bytes	–32767	32767	0	mAh
LastAccumulatedCharge	R	Signed integer, 2-bytes	–32767	32767	0	mAh
AccumulatedTime	R	Unsigned integer, 2-bytes	0	65535	0	5 min
LastAccumulatedTime	R	Unsigned integer, 2-bytes	0	65535	0	5 min
AccumulationReset	W	Boolean	NA	NA	NA	

2.6.1 Accumulated Charge Positive Threshold

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Accumulated Charge	Accumulated Charge Positive Threshold	Signed Integer	2	0	32767	1000	mAh

2.6.2 Accumulated Charge Negative Threshold

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Accumulated Charge	Accumulated Charge Negative Threshold	Signed Integer	2	0	32767	1000	mAh

2.7 Gas Gauging

The bq34110 device implements a Compensated End of Discharge Voltage (CEDV) gauging algorithm, which accurately predicts the battery capacity and other operational characteristics of a rechargeable cell or pack. It can be interrogated by a system processor through the I^2C communication interface to provide cell information, such as time-to-empty (TTE), state-of-charge (SOC), and state-of-health (SOH). Changes in flag values associated with configurable thresholds or settings within the algorithm can also be provided to the host as an interrupt using one of the two ALERT pins on this device. The data from the gas gauge function is provided in units of mAh, and the device is capable of gauging a maximum capacity of 32 Ah. The operational overview in Figure 2-2 illustrates the gas gauge operation of the bq34110 device.

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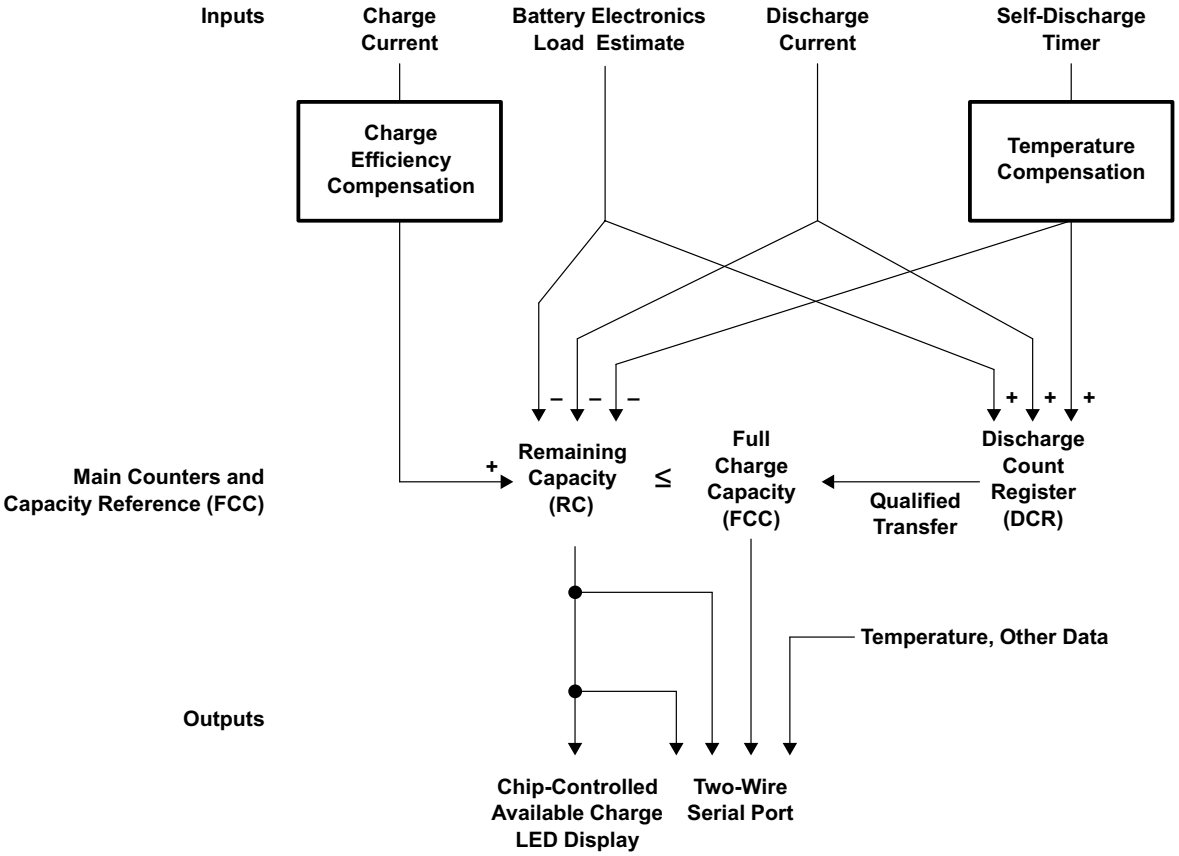

Figure 2-2. bq34110 Gas Gauging Overview

2.7.1 CEDV Gas Gauging Operational Overview

The bq34110 device accumulates the measured quantities of charge and discharge and estimates self-discharge of the battery. The bq34110 device compensates the charge current measurement for temperature and state-of-charge of the battery. The bq34110 device also adjusts the self-discharge estimation based on temperature. The initial battery state-of-charge estimation on first insertion of the battery pack in the system may display a factor of the true value. The system must go through a full charge and then a full discharge cycle before the correct *FullChargeCapacity()* (FCC) is estimated.

The main charge counter, *RemainingCapacity()* (RC), represents the available charge or energy capacity in the battery at any given time. The bq34110 device adjusts RC for charge, self-discharge, and other compensation factors. The information in the RC register is accessible through the I^2C interface. The *FullChargeCapacity()* (FCC) register represents the initial or last measured full discharge of the battery. It is used as the battery full-charge reference for relative capacity indication. The bq34110 device updates FCC after the battery undergoes a qualified discharge from nearly full to a low battery level. FCC is accessible through the I^2C interface.

The Discharge Count Register (DCR) is an internal register that tracks discharge of the battery. The bq34110 device uses the DCR to update the FCC register if the battery undergoes a qualified discharge from nearly full to a low battery level. In this way, the bq34110 device learns the true discharge capacity of the battery under-system use conditions.

2.7.2 Main Gas Gauge Registers

Remaining Capacity (RC)—Remaining capacity in the battery

RC represents the remaining capacity in the battery. The bq34110 device computes *RC* in units of mAh.

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RC counts up during charge to a maximum value of *FCC* and down during discharge and self-discharge to a minimum of 0. In addition to charge and self-discharge compensation, the bq34110 device calibrates *RC* at three low-battery-voltage thresholds—EDV2, EDV1, and EDV0. This provides a voltage-based calibration to the RC counter.

Design Capacity (DC)—User-specified battery full capacity

DC is the user-specified battery full charge capacity in units of mAh and is calculated from ***Design Capacity***. *DC* also represents the full-battery reference for the absolute display mode.

Table 2-5. Design Capacity

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Profile	Design Capacity	Signed Integer	2	0	32767	2200	mAh

Full Charge Capacity (FCC)—Last measured discharge capacity of the battery

FCC is the last measured discharge capacity of the battery. It is represented in units of mAh. On initialization, the bq34110 device sets *FullChargeCapacity()* to the data flash value stored in ***Learned Full Charge Capacity*** (FCC), which should be initialized using the same units. During subsequent discharges, the bq34110 device updates *FullChargeCapacity()* with the last measured discharge capacity of the battery. The last measured discharge of the battery is based on the value in the DCR after a qualified discharge occurs. Once updated, the bq34110 device writes the new *FullChargeCapacity()* value to data flash to ***Learned Full Charge Capacity***. *FullChargeCapacity()* represents the full battery reference for the state-of-charge calculations.

Discharge Count Register (DCR)—The DCR counts up during discharge, independent of RC. The DCR counts discharge activity, battery load estimation, and self-discharge increment.

The bq34110 device initializes the *DCR* at the beginning of a discharge to *FCC* – *RC* when *RC* is within the programmed value in ***Near Full***. The DCR initial value of *FCC* – *RC* is reduced by *FCC/128* if ***[SC]*** = 1 in ***CEDV Gauging Configuration*** and is not reduced if ***[SC]*** = 0. The DCR stops counting when the battery voltage reaches the EDV2 threshold on discharge. The *DCR* uses the same units as *FCC* and *RC*.

Cycle Count —The number of cycles the battery has experienced is calculated and tracked by the bq34110 device.

One cycle occurs when the accumulated discharge ≥ cycle threshold. The cycle threshold is calculated as ***Cycle Count Percentage*** times either *FullChargeCapacity()* (when ***CEDV Gauging Configuration[CCT]*** = 1) or *DesignCapacity()* (when ***CEDV Gauging Configuration[CCT]*** = 0). The device saves the cycle count value to ***Cycle Count***, which is read using the command *CycleCount()*.

NOTE: A minimum of 10% of a *DesignCapacity()* change of the accumulated discharge is required for a cycle count increment. This prevents an erroneous cycle count increment due to extremely low *FullChargeCapacity()*.

Table 2-6. Cycle Count

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	State Profile	Cycle Count	Unsigned Integer	2	0	65535	0	count

Table 2-7. Cycle Count Percentage

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	Cycle	Cycle Count Percentage	Unsigned Integer	1	0	100	90	%

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2.7.3 Capacity Learning (FCC Update) and Qualified Discharge

The bq34110 device updates *FCC* with an amount based on the value in *DCR* if a qualified discharge occurs. The new value for *FCC* equals the *DCR* value plus the programmable ***Near Full*** and low battery levels per the following equation:

FCC (new) = DCR (final) = DCR (initial) + Measured Discharge to EDV2 + (FCC × ***Battery_Low%***) (6)

Where ***Battery_Low%*** = (***Battery Low***% value in data flash) ÷ 100

A qualified discharge occurs if the battery discharges from *RC* ≥ *FCC* – ***Near Full*** to the EDV2 voltage threshold with the following conditions:

- No valid charge activity occurs during the discharge period. A valid charge is defined as a charge of 10 mAh into the battery.
- No more than 256 mAh of self-discharge or battery load estimation occurs during the discharge period.
- The temperature does not drop below the low temperature thresholds programmed in ***Low Temp*** during the discharge period.
- The battery voltage reaches the EDV2 threshold during the discharge period and the voltage is greater than or equal to the EDV2 threshold – 256 mV when the bq34110 device detected EDV2.
- Current remains ≥3C/32 when EDV2 is reached.
- No overload condition exists when the EDV2 threshold is reached or if RC has dropped to ***Battery_Low %*** × *FCC.*

The bq34110 device sets *[VDQ]* = 1 in *OperationStatus()* when a qualified discharge begins. The bq34110 device sets *[VDQ]* = 0 if any disqualifying condition occurs. One complication may arise regarding the state of *[VDQ]* if ***[CSYNC]*** is set in ***CEDV Gauging Configuration***. When ***[CSYNC]*** is enabled, *RemainingCapacity()* is written to equal *FullChargeCapacity()* on valid primary charge termination. This capacity synchronization is done even if the condition *RC* ≥ *FCC* – ***Near Full*** is not satisfied at charge termination.

FCC cannot be reduced by more than ***FCC Learn Down*** or increased by more than ***FCC Learn Up*** during any single update cycle. If ***[FCC_LIMIT]*** is set in ***CEDV Gauging Configuration***, then *FCC* cannot learn above the ***Design Capacity***. The bq34110 device saves the new *FCC* value to the data flash within 4 s of being updated.

2.7.4 End-of-Discharge Thresholds and Capacity Correction

The bq34110 device monitors the battery for three low-voltage thresholds: EDV0, EDV1, and EDV2.

If the ***[EDV_CMP]*** bit in ***CEDV Gauging Configuration*** is clear, fixed EDV thresholds may be programmed in ***Fixed EDV0***, ***Fixed EDV1***, and ***Fixed EDV2*** in mV.

If the ***[EDV_CMP]*** bit in ***CEDV Gauging Configuration*** is set, automatic EDV compensation is enabled and the bq34110 device computes the EDV0, EDV1, and EDV2 thresholds based on values stored in the selected CEDV profile in data flash and the battery's current discharge rate and temperature. If the ***[FIXED_EDV0]*** bit in ***CEDV Gauging Configuration*** is also set, then the EDV0 threshold will be set to the programmed ***Fixed EDV0***, and the EDV1 and EDV2 compensated thresholds will not go below the programmed ***Fixed EDV0***.

The bq34110 device disables EDV detection if current exceeds the ***Overload Current*** threshold. The bq34110 device resumes EDV threshold detection after current drops below the ***Overload Current*** threshold. Any EDV threshold detected is reset after charge is applied, and *[VDQ]* is cleared after 10 mAh of charge.

Class	Subclass	Name	Format	Size in Bytes	Min	Max	Default	Unit
Gas Gauging	CEDV Cfg	Overload Current	Signed Integer	2	0	32767	5000	mA

The bq34110 device uses the EDV thresholds to apply voltage-based corrections to the RC register per to the content in Table 2-8.

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Table 2-8. State-of-Charge Based on Low Battery Voltage

Threshold	Relative State-of-Charge (RSOC)
EDV0	0%
EDV1	3%
EDV2	***Battery Low%***

The bq34110 device performs EDV-based RC adjustments with *Current()* ≥ 3C/32. No EDVs are set if *Current()* < C/32. The bq34110 device adjusts RC as it detects each threshold. If the voltage threshold is reached before the corresponding capacity on discharge, the bq34110 device reduces RC to the appropriate amount, as shown in Table 2-8.

If an RC % level is reached on discharge before the voltage reaches the corresponding threshold, then RC is held at that % level until the threshold is reached. RC is only held if *[VDQ]* = 1, indicating a valid learning cycle is in progress. If ***Battery_Low%*** is set to zero, EDV1 and EDV0 corrections are disabled.

2.7.5 EDV Discharge Rate and Temperature Compensation

If EDV compensation is enabled, the bq34110 device calculates battery voltage to determine EDV0, EDV1, and EDV2 thresholds as a function of battery capacity, temperature, and discharge load. The general equation for EDV0, EDV1, and EDV2 calculation is as follows:

$$EDV0,1,2 = n (EMF \times FBL - |I_{LOAD}| \times R0 \times FTZ) \quad (7)$$

- EMF is a no-load cell voltage higher than the highest cell EDV threshold computed. EMF is programmed in mV in ***EMF***.
- I_{LOAD} is the current discharge load magnitude.
- n = the number of series cells.
- FBL is the factor that adjusts the EDV voltage for battery capacity and temperature to match the no-load characteristics of the battery.

$$FBL = f (C0, C + C1, T) \quad (8)$$

- C (either 0%, 3% or Battery Low% for EDV0, EDV1, and EDV2, respectively) and C0 are the capacity related EDV adjustment factors. C0 is programmed in the CEDV profile ***C0***. C1 is the needed residual battery capacity remaining at EDV0 (RC = 0). The C1 factor is stored in the CEDV profile ***C1***.
- T is the current temperature in °K.
- R0•FTZ represents the resistance of a cell as a function of temperature and capacity.

$$FTZ = f (R1, T0, C + C1, TC) \quad (9)$$

- R0 is the first order rate dependency factor stored in the CEDV profile ***R0***.
- T is the current temperature. C is the battery capacity relating to EDV0, EDV1, and EDV2.
- R1 adjusts the variation of impedance with battery capacity. R1 is programmed in the CEDV profile ***R1***.
- T0 adjusts the variation of impedance with battery temperature. T0 is programmed in the CEDV profile ***T0***.
- TC adjusts the variation of impedance for cold temperatures (T < 23°C) TC is programmed in the CEDV profile ***TC***.

The graphs below show the calculated EDV0, EDV1, and EDV2 thresholds versus capacity using the typical compensation values for different temperatures and loads for a Li-Ion 18650 cell. The compensation values vary widely for different cell types and manufacturers and must be matched exactly to the unique characteristics for optimal performance.

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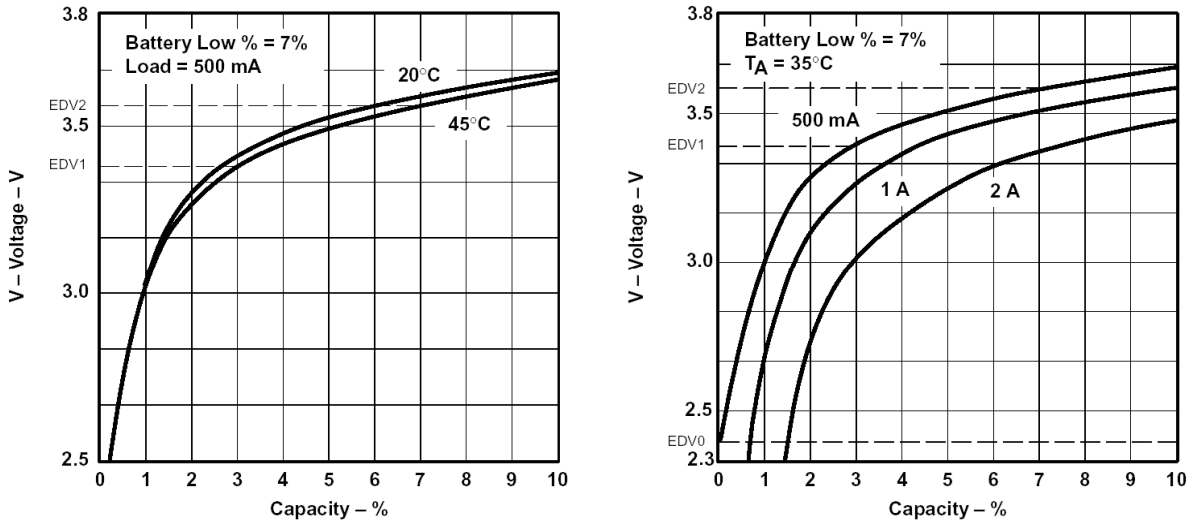

Figure 2-3. (a) EDV Calculations vs Capacity for Various Temperatures, (b) EDV Calculations vs Capacity for Various Loads

2.7.6 EDV Age Factor

The EDV ***Age Factor*** allows the bq34110 device to correct the EDV detection algorithm to compensate for cell aging. This parameter scales cell impedances as the cycle count increases. This new factor is used to accommodate for much higher impedances observed in larger capacity and/or aged cells. For most applications, the default value of zero is sufficient. However, for some very specific applications, this new aging factor may be required. In those cases, experimental data must be taken at the 0, 100, 200, and 300 cycle read points using a typical discharge rate while at ambient temperature. Entering this data into a TI provided MathCAD™ program will yield the appropriate EDV ***Age Factor*** value. Contact TI Applications Support @ http://www-k.ext.ti.com/sc/technical-support/email-tech-support.asp?AAP for more detailed information.

2.7.7 Self-Discharge

The bq34110 device estimates the self-discharge of the battery to maintain an accurate measure of the battery capacity during periods of inactivity. The bq34110 device makes self-discharge adjustments to RC every 1/4 second when awake and periodically when in SLEEP mode. The period is determined by ***Sleep Current Time***.

The self-discharge estimation rate is a continuous function that doubles for every increase of 10 degrees, and halves for each decrease of 10 degrees. Table 2-9 shows the relation of the self-discharge estimation at a given temperature to the programmed rate.

Table 2-9. Self-Discharge for Rate Programmed

TEMPERATURE (°C)	SELF-DISCHARGE RATE
Temp = 0C	1/4 Y% per day
Temp = 10C	½ Y% per day
Temp = 20C	Y% per day
Temp = 30C	2Y% per day
Temp = 40C	4Y% per day
Temp = 50C	8Y% per day
Temp = 60C	16Y% per day
Temp = 70C	32Y% per day

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The nominal self-discharge rate, %PERDAY (% per day), is programmed in an 8-bit value ***Self-Discharge Rate*** by the following relation:

Self-Discharge Rate = %PERDAY / 0.01

Table 2-10. Self-Discharge Rate

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Cfg	Self-Discharge Rate	Unsigned Integer	1	0	255	20 (corresponds to 0.2% per day)	0.01% per day

2.7.8 Battery Electronic Load Compensation

The bq34110 device can be configured to compensate for a constant load (as from battery electronics) present in the battery pack at all times. The bq34110 device applies the compensation continuously when the charge or discharge is below the digital filter. The bq34110 device applies the compensation in addition to self-discharge. The compensation occurs at a rate determined by the value stored in ***Electronics Load***. The compensation range is 0 μA–765 μA in steps of approximately 3 μA.

The amount of internal battery electronics load estimate in μA, BEL, is stored as follows:

Electronics Load = BEL/3

2.7.9 CEDV Configuration

Various gas gauging features can be configured by the ***CEDV Gauging Configuration*** data flash.

Table 2-11. CEDV Gauging Configuration

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Configuration	CEDV Gauging Configuration	Hex	2	0x0000	0xFFFF	0x102A	—

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RSVD	RSVD	RESTORE_REMCAP	SME0	RSVD	FCC_FOR_VDQ	RSVD	FCC_LIMIT
Low Byte	RSVD	RSVD	FIXED_EDV0	SC	EDV_CMP	RSVD	CSYNC	CCT

Legend = **RSVD:** Reserved. Do not use.

RESTORE_REMCAP: Restore *RemainingCapacity()*

- 1 = Upon reset or power-up, the device restores the previous value of *RemainingCapacity()*, which was stored before going into shutdown.
- 0 = The device does not restore the previous value of *RemainingCapacity()* after reset or power-up, but instead recalculates it.

SME0: Smoothing Configuration (See *CEDV Smoothing* for more information.)

- 1 = SOC smooths directly to EDV0.
- 0 = SOC smooths to EDV2, then to EDV1, then and EDV0.

FCC_FOR_VDQ: Capacity Learning during Qualified Discharge

- 1 = The device only updates FCC when full charge termination is detected.
- 0 = The device updates FCC per capacity learning criteria.

FCC_LIMIT: The ***FCC_LIMIT*** bit selects whether FCC limit can go above ***Design Capacity***.

- 1 = FCC is limited to ***Design Capacity***.
- 0 = FCC can learn above ***Design Capacity***.

FIXED_EDV0: The ***FIXED_EDV0*** bit selects whether EDV0 is always fixed.

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1 = EDV0 will always use ***Fixed EDV0***. EDV1 and EDV2 compensation will not go below ***Fixed EDV0***.

0 = EDV0 is determined based on the ***[EDV_CMP]*** bit.

SC: The ***SC*** bit enables learning cycle optimization for a Smart Charger or independent charge.

1 = Learning cycle is optimized for independent charger.

0 = Learning cycle is optimized for Smart Charger.

EDV_CMP: The ***EDV_CMP*** bit determines whether the bq34110 device implements automatic EDV compensation to calculate the EDV0, EDV1, and EDV2 thresholds based on rate, temperature, and capacity.

If the bit is cleared, the bq34110 device uses the fixed values programmed in data flash for EDV0, EDV1, and EDV2. If the bit is set, the bq34110 device calculates EDV0, EDV1, and EDV2.

1 = EDV compensation is enabled.

0 = EDV compensation is disabled.

CSYNC: The CSYNC bit selects whether RC is set to FCC at charge termination.

1 = RC will be set to FCC when charge termination is reached.

0 = RC is not changed when charge termination is reached.

CCT: Cycle Count Threshold

1 = The device evaluates a percentage of *FullChargeCapacity()* when determining if a cycle is counted.

0 = The device evaluates a percentage of *DesignCapacity()* when determining if a cycle is counted (default).

The *GaugingStatus() ManufacturerAccessControl()* subcommand returns flags associated with the CEDV gas gauging function.

Table 2-12. *GaugingStatus()*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	VDQ	EDV2	EDV1	RSVD	RSVD	FCCX	RSVD	REST
Low Byte	CF	DSG	EDV	RSVD	TC	TD	FC	FD

Legend = **RSVD:** Reserved. Do not use.

VDQ: Discharge Qualified for Learning

1 = Detected

0 = Not Detected

EDV2: End-of-Discharge Voltage Level 2

1 = EDV2 voltage is reached during discharge.

0 = EDV2 voltage is not reached or not in DISCHARGE mode.

EDV1: Discharge Qualified for Learning

1 = Detected

0 = Not Detected

FCCX: *FullChargeCapacity()* is updated.

This bit changes state each time *FullChargeCapacity()* updates.

REST: This bit indicates whether the device is in RELAX mode.

1 = The device has reached relaxation.

0 = The device has not reached relaxation.

CF: Condition Flag

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1 = This bit is set if the device determines that the error in gauging has reached a level where a condition cycle is needed (discharging to EDV2 and charging to full).

0 = Gauging error has not reached the level where a condition cycle is needed.

DSG: Discharge/Relax

This bit is set whenever the cell is detected in a RELAX state or discharging, but not when charging. Note that this bit differs from the DSG bit in *BatteryStatus()*, which is set only when a discharge current is present, but not during relaxation.

1 = Charging is not detected.

0 = Charging is detected.

EDV0: End-of-Discharge Voltage Level 0 (Termination)

1 = Termination voltage is reached during DISCHARGE.

0 = Termination voltage is not reached or not in DISCHARGE mode.

TC: Terminate Charge

1 = Detected

0 = Not Detected

TD: Terminate Discharge

1 = Detected

0 = Not Detected

FC: Fully Charged

1 = Detected

0 = Not Detected

FD: Fully Discharged

1 = Detected

0 = Not Detected

2.7.10 Initial Battery Capacity at Device Reset

The bq34110 device estimates the initial capacity of a battery pack at device reset, which is the case when battery cells are first attached to the application circuit. The initial *FullChargeCapacity() (FCC)* is a direct copy of the data flash parameter ***Learned Full Charge Capacity***. The initial RC is estimated using the voltage characteristics of the programmed battery voltage table (see ***Voltage 0% DOD*** through ***Voltage 100% DOD***) and ***Learned Full Charge Capacity***. Upon the update of RC based on the battery voltage table data, the *GaugingStatus() [CF]* flag will be cleared. This gives a reasonably accurate RC; however, battery capacity learning is required in order to find the accurate FCC and RC.

The determined value of remaining capacity can be further scaled, if needed, through the value of ***RemCap Init Percent.*** Upon a reset, the final value of *RemainingCapacity()* is initialized from the ***RemCap Init Percent*** value of the initial value correlated to the battery voltage table.

Table 2-13. Rem Cap Init Percent

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Cfg	Rem Cap Init Percent	Unsigned Integer	1	0	110	100	%

The data flash parameter ***Learned Full Charge Capacity*** should be programmed to the ***Design Capacity*** at initial device setup.

Table 2-14. Voltage % DOD

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Profile	Voltage 0% DOD	Signed Integer	2	–32768	32767	4173	mV
Gas Gauging	CEDV Profile	Voltage 10% DOD	Signed Integer	2	–32768	32767	4043	mV

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Table 2-14. Voltage % DOD (continued)

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Profile	Voltage 20% DOD	Signed Integer	2	–32768	32767	3925	mV
Gas Gauging	CEDV Profile	Voltage 30% DOD	Signed Integer	2	–32768	32767	3821	mV
Gas Gauging	CEDV Profile	Voltage 40% DOD	Signed Integer	2	–32768	32767	3725	mV
Gas Gauging	CEDV Profile	Voltage 50% DOD	Signed Integer	2	–32768	32767	3656	mV
Gas Gauging	CEDV Profile	Voltage 60% DOD	Signed Integer	2	–32768	32767	3619	mV
Gas Gauging	CEDV Profile	Voltage 70% DOD	Signed Integer	2	–32768	32767	3582	mV
Gas Gauging	CEDV Profile	Voltage 80% DOD	Signed Integer	2	–32768	32767	3515	mV
Gas Gauging	CEDV Profile	Voltage 90% DOD	Signed Integer	2	–32768	32767	3439	mV
Gas Gauging	CEDV Profile	Voltage 100% DOD	Signed Integer	2	–32768	32767	2713	mV

2.7.11 Gas Gauge Operating Modes

Entry and exit of each mode is controlled by data flash parameters in the ***Current Thresholds*** subclass. The *[DSG]* flag referenced below is from the MAC *GaugingStatus()* subcommand and is set in both RELAX and DISCHARGING modes. The *[DSG]* flag in *BatteryStatus()* is slightly different—it sets only in DISCHARGING mode and not in RELAX mode.

CHARGE mode is exited and RELAX mode is entered when *Current()* goes below ***Quit Current*** for a period of ***Charge Relax Time***. DISCHARGE mode is entered when *Current()* goes below ***(–)Dsg Current Threshold***. DISCHARGE mode is exited and RELAX mode is entered when *Current()* goes above ***(–)Quit Current*** threshold for a period of ***Discharge Relax Time***. CHARGE mode is entered when *Current()* goes above ***Chg Current Threshold***.

Table 2-15. Charge Relax Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Current Thresholds	Charge Relax Time	Unsigned Integer	1	0	255	60	s

Table 2-16. Discharge Relax Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Current Thresholds	Discharge Relax Time	Unsigned Integer	2	0	8191	60	s

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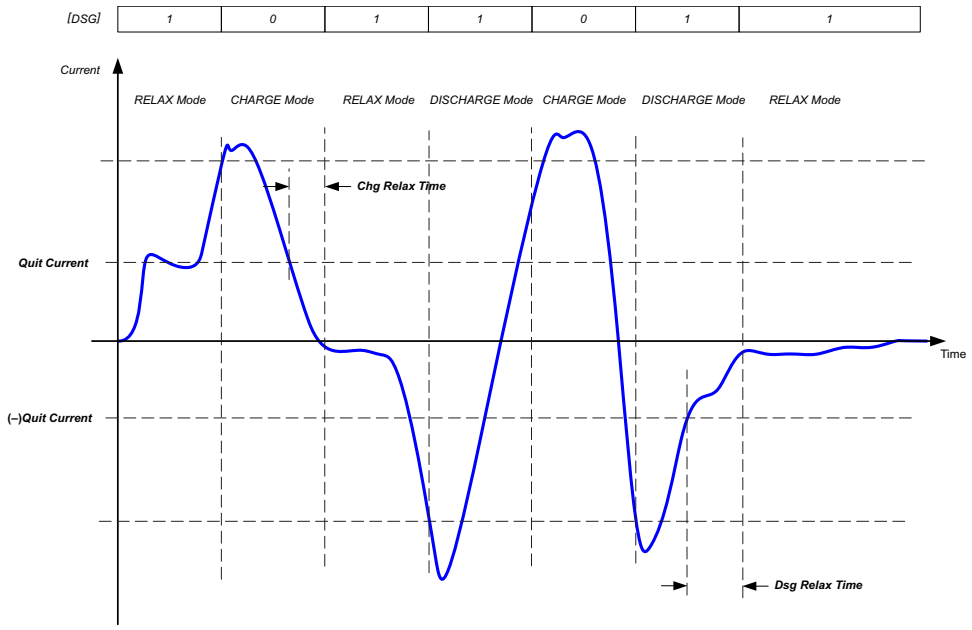

Figure 2-4. Fuel Gauge Operating Mode Example

2.7.12 CEDV Smoothing

The bq34110 device has the ability to smooth the *RemainingCapacity()* during discharge in order to avoid a drop in *RelativeStateOfCharge()* when the EDV thresholds are reached. This feature is enabled by setting the ***Smoothing Config [SMEN]*** = 1 and configuring the ***Smoothing Start Voltage*** and ***Smoothing Delta Voltage***.

The smoothing will activate only when all of the following conditions are true:

- *Current()* < 0
- *Voltage()* < ***Smoothing Start Voltage***
- EDV2 was reached (*[EDV2]* = 1) OR (*Voltage()* – present EDV2 threshold) < ***Smoothing Delta Voltage***.
- *Maximum Voltage()* during the previous one minute is greater than the maximum *Voltage()* during the current minute (that is, "drop rate" is greater than zero).
- *RemainingCapacity()* is greater than the capacity at the next EDV point.

While smoothing is active, the "drop rate" is used to estimate the time to the EDV point under the assumption that the rate is constant (linear). This information is then used to estimate how much current would need to be applied in order to have *RemainingCapacity()* reach the expected capacity at the EDV point. The actual *Current()* is then scaled by the "smoothing current." This will either speed up or slow down the *RemainingCapacity()* accumulation to reach the EDV threshold at the correct time.

Whenever the *RemainingCapacity()* accumulation is actively scaled, the *OperationStatus()[SMTH]* bit will be set.

The smoothing will deactivate whenever an EDV threshold is reached until the rate to the next EDV threshold can be calculated. However, smoothing past the EDV2 point will only occur if the ***Smoothing Config [SMEXT]*** is set to 1.

To improve smoothing at the end of discharge, the SME0 configuration bit provides additional flexibility. This is particularly useful when ***FIXED_EDV0*** is set and the calculated EDV2/EDV1 is lower than EDV0. In this scenario, the SOC smooths to EDV2, then to EDV1, and then to EDV0, leading to SOC jumps. If the SME0 bit is set, then the SOC smooths directly to EDV0, leading to a smooth transition to empty.

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Table 2-17. Smoothing Configurations

SMEN	SMEXT	SME0	Description
0	0	0	No Smoothing
0	0	1	No Smoothing
0	1	0	No Smoothing
0	1	1	No Smoothing
1	0	0	Smoothing to EDV2
1	0	1	Smoothing to EDV0 if calculated EDV2/EDV1 is less than EDV0.
1	1	0	Smoothing to EDV2 ≥ EDV1 ≥ EDV0
1	1	1	Smoothing to EDV0 if calculated EDV2/EDV1 is less than EDV0.

Table 2-18. Smoothing Start Voltage

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Smoothing Config	Smoothing Start Voltage	Signed Integer	2	0	4300	3700	mV

Table 2-19. Smoothing Delta Voltage

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gas Gauging	CEDV Smoothing Config	Smoothing Delta Voltage	Signed Integer	2	0	4200	100	mV

Table 2-20. Smoothing Config

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Gauging	CEDV Smoothing Config	Smoothing Config	Hex	1	0x00	0xff	0x08	—

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	SMOOTH EOC_EN	SMEXT	VAVG	SMEN

Legend = **RSVD:** Reserved. Do not use.

SMOOTHEOC_EN: In situations when the FCC is not updated during a discharge cycle or on a subsequent charge cycle, if the valid charge termination is reached, RSOC is synced to 100% regardless of the true RSOC.

When enabled, the RSOC value is gradually increased to 100% instead of a sudden jump in selected situations. The default is 1 (enabled).

SMEXT: When set to 1, smoothing will continue to EDV1 and EDV0 points.

When set to 0, smoothing will stop at EDV2. The default is 0.

VAVG: When set to 1, smoothing uses average voltage.

When set to 0 smoothing will use measured voltage. The default is 0.

SMEN: When set to 1 the smoothing result will be reported on *RemainingCapacity()*.

When set to 0 the normal CEDV remaining capacity will be reported. The default is 0.

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2.8 Battery Condition Warnings

2.8.1 Battery Low Warning

The bq34110 device can indicate, and optionally trigger an alert signal, when the battery voltage falls below a programmable threshold. This feature is disabled if ***Battery Low Time*** is set to 0.

NOTE: If ***Battery Low Time*** is set to 30 seconds or higher, the device may initiate an automatic offset calibration during the time window, resulting in the BATLOW signal being delayed approximately an additional 15–20 seconds beyond the ***Battery Low Time*** setting.

Status	Condition	Action
Normal	*Voltage()* > ***BATLOW: Battery Low Set Threshold***	*BatteryStatus()[BATLOW]* = 0
Trip	*Voltage()* ≤ ***BATLOW: Battery Low Set Threshold*** For ***BATLOW:Battery Low Time***	*BatteryStatus()[BATLOW]*= 1
Recovery	*Voltage()* > ***BATLOW:Battery Low Clear Threshold***	*BatteryStatus()[BATLOW]* = 0

Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Safety	BATLOW	Battery Low Set Threshold	Integer	2	0	5000	3150	mV
Safety	BATLOW	Battery Low Time	Integer	1	0	255	2	s
Safety	BATLOW	Battery Low Clear Threshold	Integer	2	0	5000	3400	mV

2.8.2 Battery High Warning

The bq34110 device can indicate and optionally trigger an alert signal when the battery voltage falls below a programmable threshold. This feature is disabled if ***Battery High Time*** is set to 0.

Status	Condition	Action
Normal	*Voltage()* > ***BATHIGH: Battery High Set Threshold***	*BatteryStatus()[BATHIGH]* = 0
Trip	*Voltage()* ≤ ***BATHIGH: Battery High Set Threshold*** For ***BATHIGH:Battery High Time*** duration	*BatteryStatus()[BATHIGH]*= 1
Recovery	*Voltage()* > ***BATHIGH:Battery High Clear Threshold***	*BatteryStatus()[BATHIGH]* = 0

Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Safety	BATHIGH	Battery High Set Threshold	Integer	2	0	5000	4200	mV
Safety	BATHIGH	Battery High Time	Integer	1	0	255	2	s
Safety	BATHIGH	Battery High Clear Threshold	Integer	2	0	5000	4100	mV

2.8.3 Battery Low SOC Warning

The bq34110 device can indicate, and optionally trigger an alert signal, when the battery state-of-charge (SOC) falls below a programmable threshold. This feature is disabled by setting ***SOC Low Threshold*** and ***SOC Low Recovery*** to 0.

Status	Condition	Action
Normal	*RelativeStateOfCharge()* > ***SOC Low Threshold***	*BatteryStatus()[SOCLOW]* = 0
Trip	*RelativeStateOfCharge()* ≤ ***SOC Low Threshold***	*BatteryStatus()[SOCLOW]* = 1
Recovery	*RelativeStateOfCharge()* > ***SOC Low Recovery***	*BatteryStatus()[SOCLOW]* = 0

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Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Safety	SOCLOW	SOC Low Threshold	Signed Integer	1	0	100	10	%
Safety	SOCLOW	SOC Low Recovery	Integer	1	0	100	30	%

2.9 Charging and Charge Termination

For proper bq34110 operation, the battery per cell charging voltage should be specified by the user in the 3 ***Charge Voltage T#-T#*** registers. These parameters should be set to the recommended charging voltage for the entire battery stack divided by the number of series cells.

The bq34110 device includes multiple algorithms for charging and charge termination, including JEITA-based charging, temperature-based charging, negative delta voltage based charging, and WHr charging.

The *ChargingVoltage()* and *ChargingCurrent()* will be selected by the bq34110 device following the *JEITA* method depending on the [JEITA] bit setting. If this bit is set, the voltage and current is selected based on the settings in ***Charge Voltage T#-T#***, ***Charge Current T#-T#***, and ***JEITA T# Temp***. The ***JEITA T# Temp*** provides temperature boundaries for the temperature category.

If *Temperature()* < ***JEITA T1 Temp***, then charging is inhibited,
ChargingVoltage() = 0,
ChargingCurrent() = 0.

If ***JEITA T1 Temp*** ≤ *Temperature()* ≤ ***JEITA T2 Temp***, then
ChargingVoltage() = ***Charge Voltage T1 – T2***,
ChargingCurrent() = ***Charge Current T1 – T2***.

If ***JEITA T2 Temp*** < *Temperature()* ≤ ***JEITA T3 Temp***, then
ChargingVoltage() = ***Charge Voltage T2 – T3***,
ChargingCurrent() = ***Charge Current T2 – T3***.

If ***JEITA T3 Temp*** < *Temperature()* ≤ ***JEITA T4 Temp***, then
ChargingVoltage() = ***Charge Voltage T3 – T4***,
ChargingCurrent()= ***Charge Current T3 – T4***.

If ***JEITA T4 Temp*** < *Temperature()*, then charging is inhibited,
ChargingVoltage() = 0,
ChargingCurrent() = 0.

If the *[JEITA]* bit is reset (and WHr Charging is not enabled), then operation is as follows:

If *Temperature()* < ***JEITA T1 Temp***, then charging is inhibited,
ChargingVoltage() = 0,
ChargingCurrent() = 0.

If ***JEITA T1 Temp*** ≤ *Temperature()* ≤ ***JEITA T4 Temp***, then
ChargingVoltage() = ***Charge Voltage T2 – T3***,
ChargingCurrent() = ***Charge Current T2 – T3***.

If ***JEITA T4 Temp*** < *Temperature()*, then charging is inhibited,
ChargingVoltage() = 0,
ChargingCurrent() = 0.

The device detects valid charge termination in one of three ways:

1. Current Taper method:
    1. During two consecutive periods of ***Current Taper Window***, the *AverageCurrent()* is less than ***Taper Current*** AND
    2. During the same periods, the accumulated change in capacity > ***Minimum Taper Capacity*** AND
    3. *Voltage()* is > *ChargingVoltage()* – ***Taper Voltage***. When this occurs, the *[CHG]* bit of *BatteryStatus()* is cleared. Also, if the ***[CSYNC]*** bit of ***CEDV_Gauging_Configuration*** is set, and *RemainingCapacity()* is set equal to *FullChargeCapacity()*.

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Table 2-21. Charger Control Class

Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Charger Control	Charge Inhibit Cfg	Chg Inhibit Temp Low	Signed integer	2	–400	1200	0	0.1°C
Charger Control	Charge Inhibit Cfg	Chg Inhibit Temp High	Signed integer	2	–400	1200	450	0.1°C
Charger Control	Charge Inhibit Cfg	Temp Hys	Signed integer	2	0	100	50	0.1°C
Charger Control	JEITA Temperature	T1 Temp	Signed integer	2	–400	1200	0	0.1°C
Charger Control	JEITA Temperature	T2 Temp	Signed integer	2	–400	1200	100	0.1°C
Charger Control	JEITA Temperature	T3 Temp	Signed integer	2	–400	1200	450	0.1°C
Charger Control	JEITA Temperature	T4 Temp	Signed integer	2	–400	1200	550	0.1°C
Charger Control	JEITA Temperature	Charge Current T1-T2	Signed integer	2	0	32767	300	mA
Charger Control	JEITA Temperature	Charge Current T2-T3	Signed integer	2	0	32767	660	mA
Charger Control	JEITA Temperature	Charge Current T3-T4	Signed integer	2	0	32767	1100	mA
Charger Control	JEITA Temperature	Charge Voltage T1-T2	Signed integer	2	0	32767	4100	mV
Charger Control	JEITA Temperature	Charge Voltage T2-T3	Signed integer	2	0	32767	4200	mV
Charger Control	JEITA Temperature	Charge Voltage T3-T4	Signed integer	2	0	32767	4100	mA
Charger Control	Charge Termination	Maintenance Current	Signed integer	2	0	1000	200	mA
Charger Control	Charge Termination	Taper Current	Signed integer	2	0	1000	100	mA
Charger Control	Charge Termination	Minimum Taper Capacity	Signed integer	2	0	1000	25	mAh/256
Charger Control	Charge Termination	Taper Voltage	Signed integer	2	0	1000	100	mV
Charger Control	Charge Termination	Current Taper Window	Unsigned integer	1	0	60	40	s
Charger Control	WHr Charge Termination	Max Charge Voltage	Signed integer	2	0	32767	4200	mV
Charger Control	WHr Charge Termination	WHr CV Step	Signed integer	2	0	32767	50	mV
Charger Control	WHr Charge Termination	WHr Termination Capacity	Signed integer	2	0	32767	2200	mAh
Charger Control	WHr Charge Termination	FC WHr Clear	Signed integer	2	0	32767	2090	mAh
Charger Control	NiMH Charge Termination	Delta Temperature	Signed integer	2	–400	1200	30	0.1°C
Charger Control	NiMH Charge Termination	Delta Temperature Time	Unsigned integer	2	0	255	100	s
Charger Control	NiMH Charge Termination	Holdoff Time	Unsigned integer	2	0	255	180	s
Charger Control	NiMH Charge Termination	Holdoff Current	Signed integer	2	0	32767	240	mA

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Table 2-21. Charger Control Class (continued)

Class	Subclass	Name	Type	Size	Min Value	Max Value	Default Value	Unit
Charger Control	NiMH Charge Termination	Holdoff Temperature	Signed integer	2	–400	1200	250	0.1°C
Charger Control	NiMH Charge Termination	Cell Negative Delta Voltage	Signed integer	2	0	32767	17	mV
Charger Control	NiMH Charge Termination	Cell Negative Delta Time	Unsigned integer	1	0	255	16	s
Charger Control	NiMH Charge Termination	Cell Negative Delta Qual Voltage	Signed integer	2	0	32767	4200	mV

2. ***Delta Temperature*** (ΔT/Δt) method—For ΔT/Δt, the bq34110 device detects an increase in temperature over many seconds. The ΔT/Δt setting is programmable in the temperature step, ***Delta Temperature*** (0°C – 25.5°C), and the time step, ***Delta Temperature Time*** (0 s–1000 s). Typical settings for 1°C/minute include 2°C/120 s and 3°C/180 s (default). Longer times may be used for increased slope resolution.

   In addition to the ΔT/Δt timer, a holdoff timer starts (using ***Holdoff Time***) when the battery is charged at more than ***Holdoff Current*** (default is 240 mA), and the temperature is above ***Holdoff Temperature***. Until this timer expires, ΔT/Δt detection is suspended. If *Current()* drops below ***Holdoff Current*** or *Temperature()* below ***Holdoff Temperature***, the holdoff timer resets and restarts only when the current and temperature conditions are met again.
3. Negative Delta Voltage (–ΔV) method—For negative delta voltage, the bq34110 device detects a charge termination when the pack voltage drops during charging by ***Cell Negative Delta Voltage*** for a period of ***Cell Negative Delta Time*** during which time *Voltage()* must be greater than ***Cell Negative Delta Qual Voltage***. If there is difficulty in the system to detect charge termination using this technique, then an alternative option is provided based only on voltage and time. Charge termination can be achieved by setting ***Cell Negative Delta Voltage*** to 0. In this case, the gauge monitors when the pack voltage exceeds ***Cell Negative Delta Qual Voltage*** for ***Cell Negative Delta Time***, and if *Current()* > 0 during this time, then charge termination will be detected.

When either condition occurs, the *GaugingStatus()[FC]* bit is set. Also, if the ***[CSYNC]*** bit of ***CEDV_Gauging_Configuration*** is set, and *RemainingCapacity()* is set equal to *FullChargeCapacity()*.

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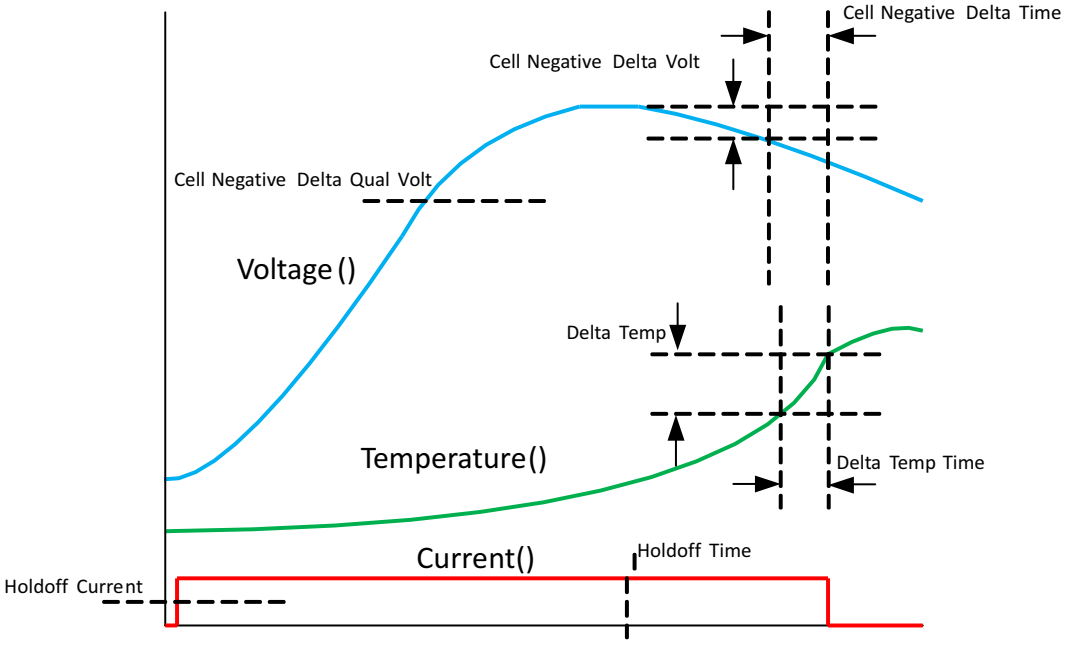

Figure 2-5. NiXX Termination

2.9.1 Charge Inhibit

The gas gauge can indicate when battery temperature has fallen below or risen above predefined thresholds ***Charge Inhibit Temp Low*** or ***Charge Inhibit Temp High***, respectively. In this mode, the *BatteryStatus()[CHGINH]* bit is set to indicate this condition. The *[CHGINH]* bit is cleared once the battery temperature returns to the range ***[Charge Inhibit Temp Low + Temp Hys***, ***Charge Inhibit Temp High*** – ***Temp Hys]***.

The charging should not start when the temperature is below the ***Charge Inhibit Temp Low*** or above the ***Charge Inhibit Temp High***. The charging can continue if the charging starts inside the window ***[Charge Inhibit Temp Low, Charge Inhibit Temp High]***.

2.9.2 Charge Control

The bq34110 device integrates two battery charge control architectures: discrete control and smart control. In a discrete charge control implementation, selected pins (some or all of ALERT1, ALERT2, VEN, and LEN) can be used to enable/disable charging and to adjust the charging voltage of an external supply, if they are not already being used for other another purpose.

In the simplest level of control, a pin can be used to directly control an external charger enable. This is controlled using ***Direct Charge Pin Control***.

NOTE: If none of the pins is selected for use, then the function is not enabled.

If ***Direct Charge Pin Control*** is enabled in normal operation (outside the EOS Determination function's learning phase), it is set while *Voltage()* is below ***FC Clear Voltage Threshold***, and it is cleared when charge terminates and *[FC]* is set. It also will be cleared if a fault occurs that would interrupt charging, such as a *[BATHIGH]*, *[OTC]*, or *[UTC]* event.

During the EOS Determination function's learning phase, this pin is only allowed to set whenever LCHG is set, then it is deasserted when LCHG mode ends.

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Table 2-22. Direct Charge Pin Control

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Configuration	Direct Charge Pin Control	Hex	1	0x00	0xff	0x00	—

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	DCHGPOL	DCP2	DCP1	DCP0

Legend = **RSVD:** Reserved. Do not use.

DCHGPOL (Bit 3): Direct Charge Control Pin Polarity

If set, the pin selected for direct charger control will generate a 1 output when charging is to be enabled, and a 0 output when charging is to be disabled.

Conversely, if not set, the pin selected for direct charger control will generate a 0 output when charging is to be enabled, and a 1 output when charging is to be disabled.

DCP2–DCP0 (Bits 2–0): Direct Charge Pin Control

These bits determine which, if any, of the ALERT1, ALERT2, VEN, or LEN pins is used for direct charge control.

0xx = None of the pins is used for direct charger control.
100 = The ALERT1 pin is used for direct charger control.
101 = The ALERT2 pin is used for direct charger control.
110 = The VEN pin is used for direct charger control.
111 = The LEN pin is used for direct charger control.

Discrete control of the charging voltage can be implemented using up to 3 additional pins, whereby the combination of the pin levels determines the charging voltage. The pins used for this purpose are selected based on the settings in ***Charge Level Pin Control***.

NOTE: If ALERT1 or ALERT2 pins are used for direct charger control, they should not also be used for alert/interrupt purposes.

Table 2-23. Charge Level Pin Control

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	Configuration	Charge Level Pin Control	Hex	1	0x00	0x3f	0x00	—

7	6	5	4	3	2	1	0
RSVD	RSVD	VEN_PUP	LEN_PUP	CHGL_ALRT1	CHGL_ALRT2	CHGL_VEN	CHGL_LEN

Legend = **RSVD:** Reserved. Do not use.

VEN_PUP: Pull-Up Control for VEN Pin

This bit controls how the VEN pin drives a high level when in GPIO and in discrete pin control mode. If set, the device will use a strong logic 1 output drive; otherwise, it will use a high impedance state.

LEN_PUP: Pull-Up Control for LEN Pin

This bit controls how the LEN pin drives a high level when in GPIO and in discrete pin control mode. If set, the device will use a strong logic 1 output drive; otherwise, it will use a high impedance state.

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CHGL_ALRT1: Charge Level Control for ALERT1 Pin

If set, this bit directs the device to use ALERT1 for discrete charge level control.

Note that since ALERT1 is an open-drain pin, it will require a pull-up resistor to generate a high voltage.

CHGL_ALRT2: Charge Level Control for ALERT2 Pin

If set, this bit directs the device to use ALERT2 for discrete charge level control.

Note that since ALERT2 is an open-drain pin, it will require a pull-up resistor to generate a high voltage.

CHGL_VEN: Charge Level Control for VEN Pin

If set, this bit directs the device to use VEN for discrete charge level control.

CHGL_LEN: Charge Level Control for LEN Pin

If set, this bit directs the device to use LEN for discrete charge level control.

NOTE: A maximum of three pins should be selected for use in charge level control. If all four bits (CHGLA1, CHGLA2, CHGLVEN, CHGLLEN) are set, this will be interpreted as if all bits were not set.

Additionally, the pin selected under ***Direct Charge Pin Control*** cannot also be used for charge level control.

The pins selected for discrete charge level control are automatically arranged MSB to LSB in the following order:

ALERT1, ALERT2, VEN, LEN

This is based on which pins are or are not selected. For example, if ALERT2 and LEN are selected for discrete charge level control, then ALERT2 will be the MSB, and LEN will be the LSB.

The charge voltage levels that map to the discrete charge control bits are programmed in ***Charge Voltage Level A*** to ***Charge Voltage Level H***.

Table 2-24. Charge Voltage Levels

Data Flash	Charge Level Control Bits (MSB/Middle Bit/LSB)	Default (mV)
Charge Voltage Level A	000	3900
Charge Voltage Level B	001	3950
Charge Voltage Level C	010	4000
Charge Voltage Level D	011	4050
Charge Voltage Level E	100	4100
Charge Voltage Level F	101	4150
Charge Voltage Level G	110	4200
Charge Voltage Level H	111	4250

NOTE: It is important to make all values increase monotonically, with the lowest voltage in ***Charge Voltage Level A***, and the highest voltage in ***Charge Voltage Level H***. If fewer than 8 levels are used, program all unused levels to the same value as the highest charge voltage setting that is in use.

The number of levels used will always start from ***Charge Voltage Level A***, as shown in the table below:

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Number of Levels Used	Data Flash Settings Used
1	Charge Voltage Level A
2	Charge Voltage Level A ~ B
4	Charge Voltage Level A ~ D
8	Charge Voltage Level A ~ H

For example, if ALERT2 is selected for direct charge control, and VEN and LEN are selected for discrete charge levels, the Charge Voltage Levels would be set as:

Data Flash	Charge Voltage Level
Charge Voltage Level A	3900
Charge Voltage Level B	4000
Charge Voltage Level C	4100
Charge Voltage Level D	4200
Charge Voltage Level E	4200
Charge Voltage Level F	4200
Charge Voltage Level G	4200
Charge Voltage Level H	4200

Table 2-25. Charge Voltage Level A–H

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Configuration	Charge Level Control	Charge Voltage Level A	Signed integer	2	0	32767	3900	mV
Charger Configuration	Charge Level Control	Charge Voltage Level B	Signed integer	2	0	32767	3950	mV
Charger Configuration	Charge Level Control	Charge Voltage Level C	Signed integer	2	0	32767	4000	mV
Charger Configuration	Charge Level Control	Charge Voltage Level D	Signed integer	2	0	32767	4050	mV
Charger Configuration	Charge Level Control	Charge Voltage Level E	Signed integer	2	0	32767	4100	mV
Charger Configuration	Charge Level Control	Charge Voltage Level F	Signed integer	2	0	32767	4150	mV
Charger Configuration	Charge Level Control	Charge Voltage Level G	Signed integer	2	0	32767	4200	mV
Charger Configuration	Charge Level Control	Charge Voltage Level H	Signed integer	2	0	32767	4250	mV

The levels of the ALERT1, ALERT2, VEN, and LEN pins can be manually controlled by the host using the *[PCTL_EN]* and the *ManufacturerAccessControl()* subcommands of *PIN_ALERT1_SET*, *PIN_ALERT1_RESET*, *PIN_ALERT2_SET*, *PIN_ALERT2_RESET*, *PIN_VEN_SET*, *PIN_VEN_RESET*, *PIN_LEN_SET*, and *PIN_LEN_RESET*.

The bq34110 device also supports smart charge control, whereby the device makes the appropriate decisions for maximum charging current and voltage per the integrated charge algorithm. This enables a smart charger to manage the charging of the battery pack through reading these values, using the *ChargingCurrent()* and *ChargingVoltage()* commands. The bq34110 device does not broadcast the charger values; they must be read by the host or charger.

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2.9.3 WHr Charging

The bq34110 device incorporates an innovative charge termination procedure specifically for use in systems that strive to extend battery life by charging the battery only as much as required to achieve a target level of capacity. The ***WHr Charge Termination*** function is excellent for applications where a particular level of battery capacity is required, such as battery backup modules or uninterruptible power supplies. As the battery ages, the charging voltage required to maintain the target level of capacity increases, which in a fixed charge voltage system would require overcharging the battery in the early stages of its lifetime to ensure sufficient capacity in its later stages of life.

The ***WHr Charge Termination*** function provides an adaptive charge voltage control that dynamically determines the *ChargingVoltage()* required to achieve a programmable target level of battery capacity. To take advantage of this function, the system must have a smart charger or some ability to adjust charging voltage.

NOTE: The ***WHr Charge Termination*** function is not applicable to NiMH battery chemistries.

2.9.3.1 Detailed Description

When enabled, the ***WHr Charge Termination*** function initially sets *ChargingVoltage()* to the number of cells × ***Cell Charge Voltage T2 – T3*** if [JEITA] is not set, or the appropriate voltage based on *Temperature()* if *[JEITA]* is set. This value is also loaded into ***Last Charge Voltage T2 – T3*** if *[JEITA]* is not set, or the appropriate voltage based on *Temperature()* if *[JEITA]* is set at this initial step. The battery is charged using this voltage, with termination complete when the following charge-complete criteria are met:

- *Voltage()* > *ChargingVoltage()* – ***Charging Taper Voltage*** AND
- *Current()* < ***Taper Current*** for two ***Current Taper Window*** AND
- *RemainingCapacity()* > ***WHr Termination Capacity*** OR *ChargingVoltage()* = ***Max Charge Voltage***.

If the first two conditions are satisfied, but *RemainingCapacity()* ≤ ***WHr Termination Capacity***, then:

- *ChargingVoltage()* is set to ***Last Charge Voltage T2 – T3 + WHr CV Step***: for example, 3.9 V + 0.05 V × the number of series cells.
- Charging continues incrementing the CV mode voltage until the charge-complete criteria are met. The ceiling on allowable values of *ChargingVoltage()* is set by ***Max Charge Voltage***. If the incrementing procedure attempts to increase *ChargingVoltage()* to a level above ***Max Charge Voltage***, then *ChargingVoltage()* will be set to ***Max Charge Voltage***.
- When charge completes, the appropriate ***Last Charge Voltage Tx - Ty*** is updated to the last *ChargingVoltage()* used for charging.

After charging terminates, charging can be restarted when *RemainingCapacity()* < ***FC WHr Clear***.

NOTE: If the discrete charge level control is enabled, then the bq34110 device uses the *ChargingVoltage()* data to set the discrete charge level, using the charge level control pins. In this case, the device selects which discrete level to use, based on the ***Charge Voltage Level A-H*** values, to provide the highest voltage less than or equal to *ChargingVoltage()*.

Table 2-26. WHr Termination Capacity

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Control	WHr Charge Termination	WHr Termination Capacity	Signed Integer	2	0	32767	2200	mAh

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Table 2-27. Last Charge Voltage Tx - Ty

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Control	Learned Charge Voltage	Last Charge Voltage T1 – T2	Signed Integer	2	0	32767	4100	mV
Charger Control	Learned Charge Voltage	Last Charge Voltage T2 – T3	Signed Integer	2	0	32767	4200	mV
Charger Control	Learned Charge Voltage	Last Charge Voltage T3 – T4	Signed Integer	2	0	32767	4100	mV

Last Charge Voltage Tx - Ty is updated to the most recent value of *ChargingVoltage()* used during normal and ***WHr Charge Termination*** charging.

NOTE: During EOS Determination Learning Charge Phases, ***Last Charge Voltage Tx - Ty*** is not incremented due to the charging voltage being increased by ***Learn Charge Voltage Delta***.

Table 2-28. Max Charge Voltage

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Control	WHr Charge Termination	Max Charge Voltage	Signed Integer	2	0	32767	4200	mV

Table 2-29. WHr CV Step

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Control	WHr Charge Termination	WHr CV Step	Signed Integer	2	0	32767	50	mV

Table 2-30. FC WHr Clear

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Charger Control	WHr Charge Termination	FC WHr Clear	Signed Integer	2	0	32767	2090	mAh

2.10 Power Modes and Control

The bq34110 device has four power modes associated with the gas gauging function, as well as with the EOS Determination function. In addition, it provides a hardware-controlled powerdown using the CE pin.

The power consumption of the bq34110 device can change significantly based on host commands it receives and the operation it is conducting at the time. Some operations are initiated based on host commands, such as commands that trigger measurements of temperature, voltage, or current, or to write data flash, and so are under the direct control of the host. However, other operations are dependent on automatic timers or external system events.

An example of this is when no charge or discharge current is flowing, the gas gauge remains in a low power state, monitoring for any current that may begin flowing through the sense resistor. If a current is detected, the device transitions into a higher power operation as it enables the coulomb counter and other gas gauge circuitry, as long as current continues flowing. Similarly, the EOS Determination function will be in a very low power state between learning phases, with only the timer operating. However, when a learning phase begins, the device will draw higher power as it continuously monitors the battery *Voltage()*, *Current()*, and other parameters while the learning phase is in progress.

The four bq34110 power modes are NORMAL, SNOOZE, SLEEP, and SHUTDOWN.

- In NORMAL mode, the device is fully powered and can execute any allowable task.

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- In SNOOZE mode, the device periodically wakes to take data measurements and updates the data set. Both the low-frequency and high-frequency oscillators are active in this reduced-power mode.
- In SLEEP mode, the device maintains the low-frequency oscillator but turns off the high-frequency oscillator and exists in a even further reduced-power state, periodically taking measurements and performing calculations.
- In SHUTDOWN mode, the device is fully powered down and can only be awakened using the chip enable (CE) pin.

Because the gas gauging and EOS Determination functions each have decisioning included, which may require them to change states, the bq34110 device generally resides in the state that accommodates both functions operating as required.

2.10.1 NORMAL Mode

The bq34110 device is in NORMAL mode when not in any other power mode. During this mode, *Current()*, *Voltage()*, and *Temperature()* measurements are taken, and the interface data set is updated. Decisions to change states are also made. This mode is exited by activating a different power mode.

Because the device consumes the most power in the NORMAL mode, the gas gauging and EOS Determination algorithms minimize the time the device remains in this mode.

2.10.2 SNOOZE Mode

SNOOZE mode is entered automatically if the feature is enabled (*CONTROL_STATUS()[SNOOZE]* bit = 1 and ***Operation Config A [SLEEP]*** bit = 1) and *Current()* is below the programmable level ***Sleep Current***. If the *[SNOOZE]* bit is set, this prevents the device from entering SLEEP mode. This mode maintains the high-frequency oscillator active, which then allows the device to respond to communication without the added delay that may be needed in SLEEP mode.

During SNOOZE mode, the gas gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition.

The bq34110 device exits SNOOZE mode if any entry condition is broken, specifically when:

- Any communication activity occurs with the device.
- *Current()* rises above ***Sleep Current***.
- A current in excess of I_{WAKE} through R_{SENSE} is detected.
- The EOS Determination function timer counting the ***Auto Learn Time***, ***Auto Learn Retry Time***, or ***Alert-Warn Learn Time*** expires, whereupon a new learning phase is initiated.

2.10.3 SLEEP Mode

SLEEP mode is entered automatically if the feature is enabled (***Operation Config A [SLEEP]*** bit = 1 and *CONTROL_STATUS()[SNOOZE]* bit = 0) and *Current()* is below the programmable level ***Sleep Current***. Once entry into SLEEP mode is qualified, but prior to entering it, the gas gauge performs a coulomb counter autocalibration to minimize offset.

During SLEEP mode, the gas gauge periodically takes data measurements and updates its data set. However, a majority of its time is spent in an idle condition. The interval at which the device wakes to take measurements is set by the data flash values of ***Sleep Current Time*** and ***Sleep Voltage Time***.

The gas gauge exits the SLEEP mode if any entry condition is broken, specifically when either:

- *Current()* rises above ***Sleep Current***.
- A current in excess of I_{WAKE} through R_{SENSE} is detected.
- The EOS Determination function timer counting the ***Auto Learn Time***, ***Auto Learn Time Retry***, or ***Alert-Warn Learn Time*** expires, whereupon a new learning phase is initiated.

While in the SLEEP mode, the fuel gauge can suspend serial communications as much as 4 ms by holding the communication line(s) low. This delay is necessary to correctly process host communication since the fuel gauge processor is mostly halted.

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Table 2-31. Sleep Current

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Power	Sleep Current	Signed Integer	2	0	100	10	mA

Table 2-32. Sleep Current Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Power	Sleep Current Time	Unsigned Integer	1	0	255	20	s

Table 2-33. Sleep Voltage Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Configuration	Power	Sleep Voltage Time	Unsigned Integer	1	0	100	20	s

2.10.4 SHUTDOWN Mode

The SHUTDOWN mode is controlled by the state of the chip enable (CE) pin, with the bq34110 device powered if the CE pin is driven high, and the device in a full powerdown state while the CE pin is held low. The internal LDO within the bq34110 device is powered down whenever the CE pin is driven low, and all data within the device that has not been written into data flash will be lost. The only manner for the device to exit the SHUTDOWN mode is for the CE pin to be driven high.

2.10.5 Wake-Up Comparator

The wake-up comparator is used to indicate a change in cell current while the device is in SNOOZE or SLEEP mode. The bits [RSNS1–RSNS0] in ***Operation Config A*** are used to set the sense resistor selection. The *[IWAKE]* bit in the same register is used to select one of two possible voltage threshold ranges for the given sense resistor selection. An internal interrupt is generated when the threshold is breached in either charge or discharge directions. A setting of 0x00 of [RSNS1, RSNS0] disables this feature.

RSNS1	RSNS0	I_{WAKE}	Vth (SRP – SNR)
0	0	0	Disabled
0	0	1	Disabled
0	1	0	+1.25 mV or –1.25 mV
0	1	1	+2.5 mV or –2.5 mV
1	0	0	+2.5 mV or –2.5 mV
1	0	1	+5 mV or –5 mV
1	1	0	+5 mV or –5 mV
1	1	1	+10 mV or –10 mV

2.11 End-Of-Service Determination

The bq34110 device incorporates the End-Of-Service (EOS) Determination function to determine the end of useful service of the battery and provide alerts based on this detection. Learning phases are used to gather information about the present state of the battery through its cell resistance. The EOS Determination function is enabled when *[EOS_EN]* in *ManufacturingStatus()* = 1. This bit can be toggled using the *EOS_EN()* subcommand. If the *[EOS_EN]* bit or other data flash values related to this function are changed directly in data flash, they will not take effect until a device reset is issued.

For best results, it is recommended that JEITA-based charging and ***WHr Charge Termination*** are not enabled when the EOS Determination feature is used.

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There are two ways to initiate a learning phase:

a. To have it automatically controlled by the device (recommended) based on when the internal ***Auto Learn Time*** timer has expired since the last successful learning phase OR

b. To have it triggered by the host by writing a *ManufacturerAccessControl() EOS_START_LEARN()* subcommand to the device.

Automatic learning is disabled if ***Auto Learn Time*** = 0. There is also a special test mode, which is entered using the *[LTEST]* bit and sets several timers to short time durations.

The learning phase can be implemented in two ways, which are controlled by the *[LSM]* bit:

a. **CHARGE-BEFORE-DISCHARGE**: The device begins a Learn Charge Phase where it enables charging to a voltage given by the charging voltage determined by the selected algorithm (JEITA, for example) incremented by ***Learn Charge Voltage Delta***. This increases charging from the level used when not in a learning phase.

NOTE: The data flash value of ***Last Charge Voltage Tx - Ty*** is not increased due to this Learn Charge Phase.

After this charging is completed through normal charge termination, the device waits for the cell to relax. It then initiates a ***Learn Discharge Phase***, whereby an intended ***Learn Discharge Current*** is enabled for a length of time given by ***Learn Discharge Time***. When this time has expired, the device disables the ***Learn Discharge Current***. The bq34110 device analyzes the response of the battery to this discharge current to estimate the status of the battery regarding its end of usable service.

If needed, the device can then be configured to continue discharging the battery until *Voltage()* reaches the appropriate voltage as determined by the charging algorithm selected, OR

b. **DISCHARGE-BEFORE-CHARGE**: The device begins by ensuring it is in a RELAXED state (typically fully or near-fully charged).

The device begins a ***Learn Discharge Phase*** by enabling ***Learn Discharge Current*** for a length of time given by ***Learn Discharge Time***. When this time has expired, the device disables the ***Learn Discharge Current***.

The device can now be recharged to the appropriate voltage as determined by the charging algorithm selected, if needed.

NOTE: The learning discharge current value is set by external components and is not directly controlled by the bq34110 device. However, this current is monitored throughout the ***Learn Discharge Phase*** and evaluated to ensure it is close to the intended value.

The **CHARGE-BEFORE-DISCHARGE** approach described above in (a) is appealing in that the battery voltage is not discharged below the appropriate charging voltage level by the learning phase. However, it requires the use of a charger with programmable charging voltage, which may be a limitation in some systems. For those cases, the **DISCHARGE-BEFORE-CHARGE** approach in (b) is provided, whereby a charger with a fixed output voltage can be used with the tradeoff that the battery voltage will be discharged below this level during the ***Learn Discharge Phase***. However, the amount of this reduction in battery voltage, and thus capacity, can be controlled and limited to acceptable levels through appropriate device settings.

The response of the battery to the learning discharge current is analyzed and used to estimate the cell resistance, ***Rcell***, and this resistance estimate is used in two different methods to evaluate the cell EOS status:

a. **Direct Resistance Decisioning**: This method uses the newly measured value of ***Rcell*** and computes the ratio of ***Rcell*** with that of an ***Initial Rcell*** captured when the battery was first put into service. The ratios are compared to thresholds to generate an alert and a warning.

Alert if $\frac{Rcell}{Initial\ Rcell} >$ ***AlertThreshold,***

Warning if $\frac{Rcell}{Initial\ Rcell} >$ ***WarningThreshold***

b. **Resistance Slope Decisioning**: This method uses the changes with respect to time of ***Rcell***,

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comparing this to programmable thresholds to generate an alert and a warning.

Use of **Resistance Slope Decisioning** requires an accurate measurement of the time between consecutive learning phases for calculation of the slope of ***Rcell*** change with respect to time. This will not be possible if the device is powered off between learning phases, in which case, **Direct Resistance Decisioning** can still be used. If the device is programmed to use **Resistance Slope Decisioning** and a power cycle is detected (or anything which could impact the validity of the time measurement between learning phases), then the device defaults to only using **Direct Resistance Decisioning** until the device is continuously powered long enough to complete multiple learning phases and accurately evaluate the ***Rcell*** change over time.

2.11.1 End-Of-Service Determination—Detailed Description

The ***EOS Configuration*** data flash is used to configure certain settings associated with the EOS Determination function.

Table 2-34. EOS Configuration

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	LTEST	LVR	LSM	LENCTL

Legend = **RSVD:** Reserved. Do not use.

LTEST: Learn Test Mode Control

This bit is used to put the device into a test mode for reduced timing testing of the EOS Determination function.

1 = When this bit is set = 1, the following values are set:

Auto Learn Time = 10 min

Auto Learn Retry Time = 5 min

Alert-Warn Learn Time = 10 min

Minimum Learn Time = 10 min

0 = The device uses the values programmed in data flash for the above parameters (default).

LVR: Learn Voltage Restore Control

This bit determines whether the device continues discharging during ***Learn Discharge Phase*** until *Voltage()* reaches the appropriate ***Last Charge Voltage Tx - Ty*** (when set = 1), or to simply stop discharge when the timer reaches ***Learn Discharge Time*** (when set = 0).

1 = The device continues ***Learn Discharge Phase*** until *Voltage()* reaches the appropriate ***Last Charge Voltage Tx - Ty.***

0 = The device stops ***Learn Discharge Phase*** when the timer reaches ***Learn Discharge Time*** (default).

LSM: Learn Sequence Mode Control

This bit determines whether the EOS algorithm uses CHARGE-BEFORE-DISCHARGE or DISCHARGE-BEFORE-CHARGE mode.

1 = DISCHARGE-BEFORE-CHARGE mode is used.

0 = CHARGE-BEFORE-DISCHARGE mode is used (default).

LENCTL: Learning Pin (LEN) Control Enable

This bit determines whether the LEN pin on the bq34110 device is used to directly control the external FET implementing the ***Learn Discharge Phase***, or whether the host will control the external FET. In the case when the host controls the FET, it is expected that the *[LCTLEDGE]* bit in *EOSLearnStatus()* will be set to trigger an ALERT interrupt to the host whenever *[LDSG]* changes state (that is, transitions from 0 to 1, or from 1 to 0).

1 = The LEN pin is used to control ***Learn Discharge Current***.

0 = The LEN pin is not used to control ***Learn Discharge Current*** (default).

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The device includes a variety of flags to provide visibility into the operation of the EOS Determination Learning process. These are found in *EOSLearnStatus()*:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	LCTO	LFAULT	LABRT	LCMD	LPER	LRLX	LCHG	LDSG
MSB	LDONE	LRES	LRSTOR	LCTLEDGE	LUCD	LDPAM	LDPAT	LDPAI

The sequence of steps involved in a learning phase differs depending on the setting of *[LSM]*. These are depicted in the following figures.

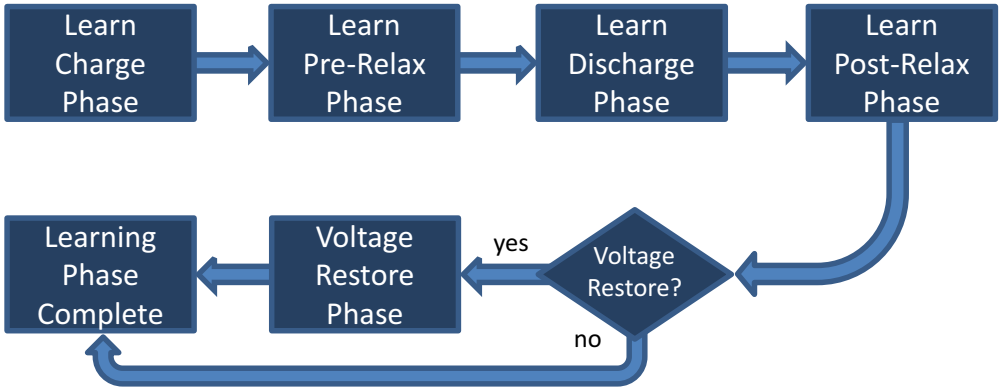

Figure 2-6. State Diagram for LSM=0

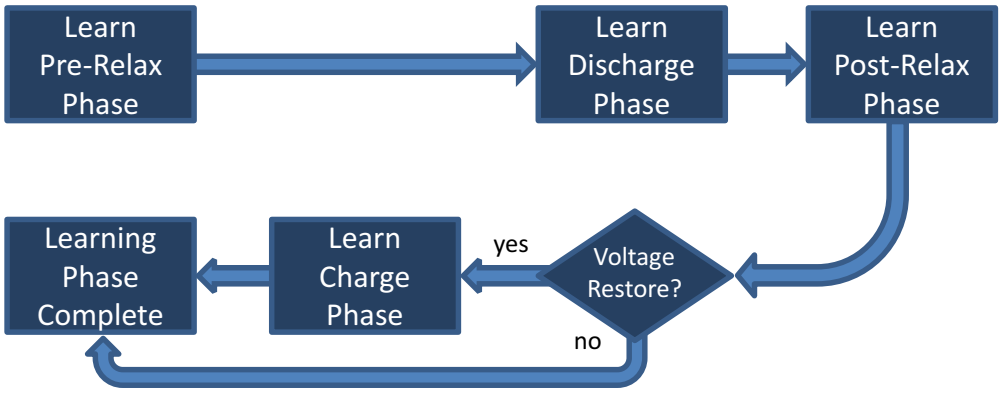

Figure 2-7. State Diagram for LSM=1

2.11.1.1 Periodic and Manual Learn Command

For manual control of learning phases, the *ManufacturerAccessControl()* subcommand *EOS_START_LEARN()* is used. When the device receives this command, it sets the *[LCMD]* flag and initiates the learning phase if conditions permit: for example, charger present, no charging or safety faults, and the temperature is within acceptable limits. The *[LDPAT]* and *[LFAULT]* flags will be set if the Learning Discharge Phase is attempted but temperature conditions do not permit it.

If the device is in periodic (automatic) learning mode, then the *[LPER]* bit will be set while the device is in a learning phase.

EOS_ABORT_LEARN(): This *ManufacturerAccessControl()* subcommand is used to abort a learning phase that is in progress. Use of this command during a learning phase results in a failed learning phase and setting the [LABRT] flag, whereupon the device will retry another learning phase after a time period of ***Auto Learn Retry Time***.

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When the device attempts to initiate a learning phase, but conditions do not permit this, then the device will wait for ***Auto Learn Retry Time*** to again attempt a learning phase. Note that this will occur whether the device is configured in periodic learning or learning is initiated through a host command.

If the case occurs where an alert or warning is detected, either through **Direct Resistance Decisioning** or **Resistance Slope Decisioning**, the ***Alert-Warn Learn Time*** is used to schedule a new learning phase. If multiple fault events must be detected before the alert or warning flags are set, and an aborted learning phase occurs after the first alert or warning is detected, then ***Alert-Warn Learn Time*** is used to schedule future ***Rcell*** measurements rather than ***Auto Learn Retry Time***.

NOTE: If *[LTEST]* is set, special values override the selected timer values to facilitate device operation testing in a shorter time scale.

To avoid interruption to the EOS Determination measurements and calculations, automatic offset calibration is not initiated during a learning phase. While it is possible for the host to manually initiate a calibration event during a learning phase, it is recommended that the host avoid this.

Table 2-35. Auto Learn Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Auto Learn Time	Unsigned Integer	2	0	65535	1500	Hours

Table 2-36. Auto Learn Retry Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Auto Learn Retry Time	Unsigned Integer	1	0	255	1	Hours

Table 2-37. Alert-Warn Learn Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Alert-Warn Learn Time	Unsigned Integer	2	0	65535	1	Hours

NOTE: ***Alert-Warn Learn Time*** has priority over ***Auto Learn Retry Time***, so if multiple occurrences must be detected before an alert or warning is triggered, and after the first occurrence is detected that a fault occurred that invalidated a following attempted learning phase, the ***Alert-Warn Learn Time*** will be used to determine the time to the next learning phase attempt. It should also be noted that if ***Alert-Warn Learn Time*** is set to be lower than ***Minimum Learn Time***, then ***Minimum Learn Time*** will be used to determine the time to the next learning phase attempt.

2.11.1.2 Learn Charge Phase

The operation of the device is first described for the case of *[LSM]* = 0, in which the device uses CHARGE-BEFORE-DISCHARGE mode. In this mode, the device first enters Learn Charge Phase by setting *ChargingVoltage()* to the appropriate charging voltage determined by the selected charging algorithm (JEITA, for example) incremented by ***Learn Charge Voltage Delta***. The *[LCHG]* flag is set and charge terminates using standard charge termination criteria. Upon termination of charge, then *[LCHG]* is cleared. Note that the data flash value of ***Last Charge Voltage Tx - Ty*** is not incremented due to this Learn Charge Phase.

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The time while *[LCHG]* is set is measured and compared against a threshold given by ***Learn Charge Time Limit*** to identify an excessive charging time, which may indicate an issue in the system. When the learn charging time exceeds this limit, the *[LCTO]* flag is set, learning is terminated, and the *[LFAULT]* flag is set to indicate a fault has occurred. The *[LCHG]* flag is reset whenever the device exits from CHARGING mode. If a learning fault occurs, the status flag (*[LCHG]* in this case) remains set to enable the host to understand what mode the system was in when the fault occurred.

Table 2-38. Learn Charge Time Limit

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Charge Time Limit	Unsigned Integer	2	0	65535	3600	s

NOTE: The standard charge termination criteria voltage condition is relative to *ChargingVoltage(),* so the same settings are used for *Normal* and *Learn* charging phases.

Table 2-39. Learn Charge Voltage Delta

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Charge Voltage Delta	Unsigned Integer	2	0	32767	100	mV

2.11.1.3 Learn Pre-Relax Phase

If *[LSM]* = 0, then the device next waits for relaxation of the cell, during which *Voltage()* is monitored for 100-s time windows. While in this phase, the device sets the *[LRLX]* flag. If the change in the consecutive 100-s averages of *Voltage()* is less than 4 µV, then relaxation is deemed achieved. If not, the device continues monitoring for another 100-s time window. It is important that the cell be fully relaxed before the algorithm can continue onto the ***Learn Discharge Phase***. The status of relaxation can be seen by the *[REST]* bit in the *Gauging Status* register, after which the algorithm can move onto the ***Learn Discharge Phase***. If a learning fault occurs while in the ***Learn Pre-Relax Phase*** or the ***Learn Post-Relax Phase***, the status flag (*[LRLX]* in this case) will remain set to allow the host to understand what mode the system was in when the fault occurred.

When the device is in learning mode (but not in the ***Learn Discharge Phase***), and a current is detected differently than what is expected, the *[LUCD]* bit will be set. It is set if the device is attempting to charge or relax, and a discharge current in excess of ***Discharge Detection Threshold*** is detected. It is also set if the device is in a RELAX mode and a charging current in excess of ***Charge Detection Threshold*** is detected. This detection also terminates the learning phase, and this flag will remain set so the host can recognize why the learning phase was aborted. This bit will be reset to 0 when charging is terminated or the register is read.

2.11.1.4 Learn Discharge Phase

After achieving relaxation, the bq34110 device next enters the ***Learn Discharge Phase***, whereby the device enables the ***Learn Discharge Current*** (depending on the *[LENCTL]* setting), sets the *[LDSG]* flag, and begins the timer.

External circuitry is required to actively discharge the battery at a constant current rate where the discharge current flows through the sense resistor connected across SRP – SRN. This will be implemented by the device controlling the LEN pin on the device, or the host directly controlling the current (depending on the *[LENCTL]* setting). To provide sufficient resolution in the associated calculations, it is important that the level of this ***Learn Discharge Current*** be large enough so that it generates a cell voltage change of approximately 5 mV or greater. A current level of C/20 or higher is generally recommended.

[LDSG] remains enabled until the timer reaches ***Learn Discharge Time***, at which point (if *[LVR]* = 0), the *[LDSG]* flag is reset and ***Learn Discharge Current*** is disabled. The device then transitions into the ***Learn Post-Relax Phase***.

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The *[LVR]* (Learn Voltage Restore) bit is used to tell the device to resume discharging using the learning load after completion of the voltage determined by the charging algorithm selected until *Voltage()* reaches the appropriate voltage determined by the charging algorithm selected (when *[LVR]* is set = 1). When this is finished (or when the ***Learn Post-Relax Phase*** is complete, if *[LVR]* is set = 0), the entire learning phase is complete, at which point the device sets the *[LDONE]* flag.

During the time period while the timer is active for the ***Learn Discharge Time*** period, the average current and average temperature over this time period will be calculated by the device and saved, at the conclusion of the ***Learn Discharge Phase***. These values are used in later calculations to provide better accuracy.

While the device is in ***Learn Discharge Phase***, it is also monitoring *Current()* and ensuring it is within an acceptable range around the intended discharge current. The algorithm knows the intended current based on the ***Learn Discharge Current***, which is the intended ***Learn Discharge Current*** implemented using the external circuitry. This current should generally be designed greater than C/20. The boundary the algorithm uses for the acceptable range is determined using the ***Learn Discharge Current Boundary***. If the current exceeds the ***Learn Discharge Current Boundary***, the *[LDPAI]* and *[LFAULT]* flags are set, and the learning phase is aborted. If a learning fault does occur, the status flag (*[LDSG]* in this case) will remain set to allow the host to understand what mode the system was in when the fault occurred.

The value of ***Learn Discharge Current*** should be selected large enough to accept variations in the current with temperature and system noise, but low enough to ensure identification of other events, such as an unintended charging session starting or a system load discharge event beginning. The ***Learn Discharge Current*** should also be chosen well above the ***Discharge Detection Threshold*** and ***Quit Current*** to ensure proper operation.

Table 2-40. Learn Discharge Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Discharge Time	Unsigned Integer	2	0	65535	500	s

Table 2-41. Learn Discharge Current

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Discharge Current	Signed Integer	2	1	32767	100	mA

Table 2-42. Learn Discharge Current Boundary

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Discharge Current Boundary	Unsigned Integer	2	0	100	25	% of Learn Discharge Current

NOTE: If *[LENCTL]* is set such that the bq34110 device does not directly control the ***Learn Discharge Current*** using the LEN pin. Then after setting *[LDSG]*, the device will monitor *Current()* for up to ***Learn Request Timeout*** seconds and start the timer only when the current has entered the acceptable range around ***Learn Discharge Current***. This will accommodate delay in the host responding to the ALERT interrupt to see the *[LCTLEDGE]* signal and enable the ***Learn Discharge Current***.

If the bq34110 device does not detect a valid current within a time period of ***Learn Request Timeout*** after setting *[LDSG]*, then the device will set *[LFAULT]*, delay a time given by ***Auto Learn Retry Time***, and then initiate a new learning phase. The *[LDSG]* flag will remain set so the host can read and determine the phase in which the fault occurred. The ***Learn Request Timeout*** timer is similarly used after the *[LCTLEDGE]* signal asserts when the host should disable the learning load.

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Table 2-43. Learn Request Timeout

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Request Timeout	Unsigned Integer	1	0	255	4	s

The ***Learn Discharge Phase*** can be terminated for other criteria (beyond its intended, valid termination by persisting for the ***Learn Discharge Time*** period), including *Current()* exiting the acceptable range, safety fault detected, or temperature exceeding allowed learning temperature limits. If the ***Learn Discharge Phase*** is terminated for any reason other than valid termination, then *[LFAULT]* is set, indicating that the learning phase was not completed. *[LFAULT]* is cleared when the learning process is initiated again.

The ***Learn Discharge Phase*** is only allowed when the temperature is within an allowed range, which is given by the ***Learn Min Temperature*** and ***Learn Max Temperature***. If a ***Learn Discharge Phase*** is attempted when the temperature is outside this allowed range, the *[LDPAT]* and *[LFAULT]* flags are set.

Table 2-44. Learn Min Temperature

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Min Temperature	Signed Integer	2	–400	1500	50	0.1°C

Table 2-45. Learn Max Temperature

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Max Temperature	Signed Integer	2	–400	1500	400	0.1°C

If the *[LSM]* is set = 1, then DISCHARGE-BEFORE-CHARGE mode is used, in which the operation sequence is described below:

1. Check for relaxation by monitoring *Voltage()* as described above, delay until relaxation is achieved.
2. Enable *[LDSG]*, enable the ***Learn Discharge Current***, and reset the timer to begin ***Learn Discharge Phase***.
3. When the timer reaches ***Learn Discharge Time***, then disable *[LDSG]* and ***Learn Discharge Current***.

2.11.1.5 Learn Post-Relax Phase

After the ***Learn Discharge Phase*** completes, the bq34110 device will disable the learning current and enter the ***Learn Post-Relax Phase***, whereby the device again waits for relaxation of the cell, during which *Voltage()* is monitored for 100-s time windows. While in this phase, the device sets the *[LRLX]* flag. If the change in the consecutive 100-s averages of *Voltage()* is less than 4 µV, then relaxation is deemed achieved. If not, the device continues monitoring for another 100-s time window. It is important that the cell be fully relaxed before the algorithm can continue. The status of relaxation can be seen by the *[REST]* bit in the Gauging Status register. If a learning fault occurs while in the ***Learn Post-Relax Phase***, the status flag (*[LRLX]* in this case) will remain set to allow the host to understand what mode the system was in when the fault occurred.

As in the ***Learn Pre-Relax Phase***, if a discharge current in excess of ***Discharge Detection Threshold*** or a charging current in excess of ***Charge Detection Threshold*** is detected, then the *[LUCD]* flag is set. This detection also terminates the learning phase, and this flag will remain set so the host can recognize why the learning phase was aborted. This bit will be reset to 0 when charging is terminated or the register is read.

At the completion of the ***Learn Post-Relax Phase***, if in CHARGE-BEFORE-DISCHARGE mode and *Voltage()* > the charging voltage determined by the selected charging algorithm and *[LVR]* = 1, then the device will set *[LDSG]* and enable the ***Learn Discharge Current*** until *Voltage()* ≤ the calculated charging voltage. At which point, *[LDSG]* is reset and the ***Learn Discharge Current*** is disabled. The *[LRSTOR]* bit will be set while the device is continuing discharge to reach the calculated charging voltage.

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If in DISCHARGE-BEFORE-CHARGE mode and *[LVR]* = 0, then the device will set *[LDONE]* and complete learning. If *[LVR]* = 1, then the device will initiate a new charging session to charge the battery back to the appropriate charging voltage determined by the selected charging algorithm using a similar sequence as described above. In this case, the device sets the *[LCHG]* and *[LRSTOR]* flags to indicate to the host that charging can begin. If charging does not terminate within ***Learn Charge Time Limit***, then *[LCTO]* and *[LFAULT]* is set. If a learning fault does occur, the status flag (*[LCHG]* in this case) will remain set to allow the host to understand what mode the system was in when the fault occurred.

NOTE: It is possible that a ***Learn Discharge Phase*** has completed, and a new ***Rcell*** value has been calculated and stored, but during a Voltage Restore phase, a fault could occur. This would cause *[LFAULT]* to be set, and the device would retry a new learning phase after ***Auto Learn Retry Time***.

2.11.1.6 Cell Resistance Calculation

The device uses the values obtained during each learning phase to estimate a value of ***Rcell*** for the battery. Note the actual value of this ***Rcell*** estimate is not critical here, rather its change as the battery ages is what is important. The *[LRES]* bit indicates when a new ***Rcell*** value has been acquired and stored by the device.

The change in value of ***Rcell*** must be normalized relative to differences in temperature when they are captured. Therefore, the bq34110 device uses resistance temperature parameters in ***Rcell High & Low Temperature Coefficients*** to calculate an expected value of resistance at the ***Learn Target Temperature***.

The ***Rcell High & Low Temperature Coefficients*** are obtained during a pre-production test whereby the customer initiates ***Initial Rcell*** calculations at temperatures of 5°C, 25°C, and 40°C. These ***Initial Rcell*** values are put into a spreadsheet provided by TI, which then calculates the values of ***Rcell High Temperature Coefficient*** and ***Rcell Low Temperature Coefficient***. These values are then loaded into data flash and used by the device to normalize effective ***Rcell*** measurements back to an equivalent value at the ***Learn Target Temperature***.

NOTE: The ***Rcell*** and ***Initial Rcell*** values read by the device are normalized to ***Learn Target Temperature***. During the pre-production testing to capture the ***Initial Rcell*** values as described above, it is important to keep the ***Rcell High & Low Temperature Coefficients*** set = 0, so the ***Initial Rcell*** values captured there are not further normalized.

It is important that the temperature remain stable during the learning phase. If the temperature is detected to vary more than 10°C during certain portions of the learning phase, the learning phase will be aborted, and the *[LDPAT]* and *[LFAULT]* flags will be set.

Table 2-46. Rcell High Temperature Coefficient

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Rcell High Temperature Coefficient	Signed Integer	2	–32767	32768	0	2^{-16}/ 0.1°C

Table 2-47. Rcell Low Temperature Coefficient

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Rcell Low Temperature Coefficient	Signed Integer	2	–32767	32767	0	2^{-16}/ 0.1°C

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Table 2-48. Learn Target Temperature

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Learn Target Temperature	Signed Integer	2	–400	1500	250	0.1°C

Learn Target Temperature should be the typical or nominal temperature for intended cell operation.

2.11.1.7 End-Of-Service Evaluation

2.11.1.7.1 Direct Resistance Decisioning

The device uses the change in ***Rcell*** relative to the value of ***Initial Rcell*** as one method to estimate EOS. The ratio of ***Rcell*** / ***Initial Rcell*** is compared to two thresholds to generate *[DRDALERT]* and *[DRDWARN]* flags by:

$$[DRDALERT] \text{ is set if } \frac{Rcell}{Initial\ Rcell} > \left(1+\frac{DRD\ Alert\ Level}{100}\right)$$

$$[DRDWARN] \text{ is set if } \frac{Rcell}{Initial\ Rcell} > \left(1+\frac{DRD\ Warning\ Level}{100}\right)$$

The EOS alerts and warnings are read using the command *EOSSafetyStatus()*, which will clear the alert bits in this register. There is also a *ManufacturerAccessControl()* subcommand *EOS_SAFETY_STATUS()*, which can be read and does not clear the alert bits.

The following data flash values are set to provide levels at which the bq34110 device will generate an alert or a warning, based on the DRD algorithm.

Table 2-49. DRD Alert Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	DRD Alert Level	Unsigned Integer	2	0	65535	15	%

Table 2-50. DRD Warning Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	DRD Warning Level	Unsigned Integer	2	0	65535	30	%

In normal situations, the value of ***Rcell*** is expected to increase over time. If the value of ***Rcell*** is detected to decrease from the previous measurement, this is unexpected and may indicate an abnormal situation, such as a cell having been replaced. The bq34110 device will set the *[RCELLR]* flag if a reduction in the value of ***Rcell*** of more than 2% is detected.

To offer improved robustness, there is the option to enable a filter to help ensure that the condition has been detected for a number of consecutive learning phases through programming ***DRD Alert Counts*** and ***DRD Warning Counts***.

If the DRD Alert calculation is positive for ***DRD Alert Counts***, then *[DRDALERT]* is set. If ***DRD Alert Counts*** is set = 0, then this test is disabled.

If the DRD Warning calculation is positive for ***DRD Warning Counts***, then *[DRDWARN]* is set. If ***DRD Warning Counts*** is set = 0, then this test is disabled.

Additionally, once the first instance of the either a DRD Alert or DRD Warning condition is detected then the time between automatic learns can be adjusted and is based on ***Alert-Warn Learn Time***. If ***Alert-Warn Learn Time*** = 0, then the value in ***Auto Learn Time*** continues to be used.

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After ***DRD Alert Counts*** number of alert conditions have occurred and a *[DRDALERT]* has been triggered, then the timing to the next learning phase returns to ***Auto Learn Time***.

Table 2-51. DRD Alert Counts

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	DRD Alert Counts	Unsigned Integer	1	0	255	3	Counts

Table 2-52. DRD Warning Counts

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	DRD Warning Counts	Unsigned Integer	1	0	255	3	Counts

When the *[DRDALERT]* flag is set, it will be cleared after being read by the host. However, if the *[DRDWARN]* flag is set, it is NOT cleared after being read by the host, but can only be cleared by the host using the *ManufacturerAccessControl()* subcommand *EOS_WARNCLR()*.

2.11.1.7.2 Resistance Slope Decisioning

This second method used by the device for evaluating EOS is based on the slope of the change in ***Rcell*** versus time. The preferred approach is to use both ***Direct Resistance Decisioning*** with ***Resistance Slope Decisioning***, whereby an even more robust solution is obtained.

Resistance Slope Decisioning requires an accurate measurement of the time between consecutive learning phases, which it uses to calculate the slope of the ***Rcell*** change with respect to time. For best results, this mode should be used with automatic learning mode enabled and the device experiences no (or few) power cycles during its lifetime.

Here, the device collects ***Rcell*** information using periodic learning phases, which may be in either CHARGE-BEFORE-DISCHARGE or DISCHARGE-BEFORE-CHARGE mode. The device measures accurately the time between learning phases, and this is then used to calculate the rate of change in ***Rcell*** with respect to time, which is termed ***RRate***. The value of ***RRate*** is stored in units of µΩ/day as a two-byte signed value, which can store values up to a maximum of 32767 µΩ/day. If a value of ***RRate*** is calculated exceeding this level, the value stored will be limited at 32767. If this value is read back by the host, it should serve as an indication that the ***RRate*** value has saturated the range allotted for storing it.

During operation, the algorithm uses the newly measured value of ***RRate*** and computes the ratio of ***RRate*** with that of an ***Initial RRate*** captured when the battery was first put into service. The ratios are compared to thresholds to generate an alert and a warning:

$$\textit{[RSDAlert]} \text{ is set if } \frac{RRate}{Initial\ RRate} > 1 + \left(\frac{RRate\ Alert\ Level}{100}\right)$$

$$\textit{[RSDWarn]} \text{ is set if } \frac{RRate}{Initial\ RRate} > 1 + \left(\frac{R\,Rate\ Warning\ Level}{100}\right)$$

Table 2-53. RSD Alert Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSD Alert Level	Unsigned Integer	2	0	65535	15	%

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Table 2-54. RSD Warning Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSD Warning Level	Unsigned Integer	2	0	65535	30	%

The device also maintains a long-term timer value, which counts the time from the completion of the ***Initial RRate*** learning phases to the present time. This value will only be valid if no power cycles or interruptions to device operation have been encountered since the ***Initial RRate*** learning phases were completed. If there is a power cycle such that the timer has been interrupted, then the *[RDSLI]* flag will be set, which indicates that no alerts or warnings based on the long-term RSD value (described below) will ever be triggered.

A long-term value for the resistance slope (given by $\boldsymbol{RRate}_{longterm}$) is calculated as the change in ***RRate*** from the ***Initial RRate*** value to the most recent ***RRate*** measurement.

The ratio of ***RRate*** to $\boldsymbol{RRate}_{longterm}$ is compared against thresholds to provide further information as:

[RSDLAlert] is set if $\frac{\boldsymbol{RRate}}{\boldsymbol{RRate}_{\text{longterm}}} > (1+ \frac{\boldsymbol{RSDL\ Alert\ Level}}{100})$

[RSDLWarn] is set if $\frac{\boldsymbol{RRate}}{\boldsymbol{RRate}_{\text{longterm}}} > (1+ \frac{\boldsymbol{RSDL\ Warning\ Level}}{100})$

NOTE: It is important that the delay between successive ***Rcell*** calculations be long enough such that the slope of resistance change can be accurately calculated. If the triggering of learning phases is being performed manually (rather than automatically using the ***Auto Learn Time***), then it is possible for the host to request successive learning phases with too short of a time delay between them. The minimum time required for successive learning phases is set by ***Minimum Learn Time***, If the host manually requests a new learning phase without waiting for ***Minimum Learn Time***, then the *[LDPAM]* flag will be set and the request for a new learning phase will be declined. The *[LFAULT]* flag is not set here because the learning phase was never started.

It is important that ***Auto Learn Time*** be set larger than ***Minimum Learn Time***; otherwise, ***Minimum Learn Time*** will be used in place of ***Auto Learn Time***. It is also recommended that, if Resistance Slope Decisioning is used, the value of ***RRate*** be ~>10 in practice, to enable appropriate resolution during mathematical computation within the device.

NOTE: Note that ***Minimum Learn Time*** will also limit the time between successive ***Rcell*** measurements even when DRD Decisioning is used and RSD/RSDL Decisioning is not used. In the case where RSD/RSDL Decisioning is not being used, the user can set the ***Minimum Learn Time*** to zero if frequent ***Rcell*** measurements are needed.

Table 2-55. RSDL Alert Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSDL Alert Level	Unsigned Integer	1	0	255	15	%

Table 2-56. RSDL Warning Level

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSDL Warning Level	Unsigned Integer	1	0	255	30	%

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Table 2-57. Minimum Learn Time

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Minimum Learn Time	Unsigned Integer	2	0	65535	1	hours

Table 2-58. Warning Status

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Safety Status	Warning Status	Hex	1	0x00	0xff	0x00	—

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSDLWARN	RSDWARN	DRDWARN

To offer improved robustness, there is the option to enable a filter to help ensure that the condition has been detected for a number of consecutive learning phases through programming ***RSD Alert Counts*** and ***RSD Warning Counts***.

If the RSD Alert calculation is positive for ***RSD Alert Counts*** then *[RSDALERT]* is set. Similarly, if the RSDL Alert calculation is positive for ***RSD Alert Counts***, then *[RSDLALERT]* is set. If ***RSD Alert Counts*** is set = 0, then these tests will not be enabled.

If the RSD Warning calculation is positive for ***RSD Warning Counts***, then *[RSDWARN]* is set. Similarly, if the RSDL Warning calculation is positive for ***RSD Warning Counts*** then *[RSDLWARN]* is set. If ***RSD Warning Counts*** is set = 0, then these tests will not be enabled.

Additionally, once the first instance of the either a RSD Alert, RSDL Alert, RSD Warning, or RSDL Warning condition is detected then the time between automatic learns can be adjusted and is based on ***Alert-Warn Learn Time***. If ***Alert-Warn Learn Time*** = 0 then the value in ***Auto Learn Time*** continues to be used.

Table 2-59. RSD Alert Counts

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSD Alert Counts	Unsigned Integer	1	0	255	3	Counts

Table 2-60. RSD Warning Counts

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	RSD Warning Counts	Unsigned Integer	1	0	255	3	Counts

Table 2-61. Initial RRate

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Slope Decision	Initial RRate	Unsigned Integer	2	0	65535	0	µΩ/day

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When the bq34110 device is operating in Resistance Slope Decisioning mode and a power cycle is detected, such that the timer is stopped and restarted, then newly calculated values of ***RRate*** will no longer be compared against the long-term value of the resistance slope. Thus, the *[RSDLAlert]* and *[RSDLWarn]* flags will never be set. The *[RSDLI]* flag is set to indicate an interruption has occurred.

In addition, a new value of ***RRate*** cannot be calculated until two learning phases are completed with the device maintaining power between them, so a valid time is available for the calculation.

If the system designer is concerned about the power drawn by the bq34110 timer, another option is for the system to power up the bq34110 device, maintain power long enough for the device to complete two learning phases and calculate a valid ***RRate*** value for evaluation. The device can then be powered down until another evaluation is needed, in which case the sequence can be repeated.

2.11.1.8 Initial Rcell and RRate Learning Process

When the cell is first put into service, ***Initial Learn Pulse Number*** learning phases will be initiated, each resulting in a calculated ***Rcell*** value. These ***Rcell*** values will be averaged and stored as ***Initial Rcell***.

The *EOS_RCELL_RRATE_LEARN()* command is available for the host to initiate the measurement of an ***Initial Rcell*** value. This command will also reset the timer measuring the time since completion of the ***Initial Rcell*** measurement.

NOTE: The ***Initial Rcell*** measurement can be done while in test mode, but the ***Initial RRate*** measurement cannot practically be done in test mode with an actual cell, due to the minimal change expected in the values of ***Rcell*** when using the short time durations of the test mode.

If any fault is detected during the ***Initial Rcell*** or ***Initial RRate*** measurement process, all learned data associated with the Rcell measurement in progress is discarded, and the device will initiate a new learning phase after ***Auto Learn Retry Time***. If the ***Initial RRate*** value measured by the device is zero or negative, this result is ignored, and the device will still consider ***Initial RRate*** not yet learned. In this case, the host should initiate a new ***Initial RRate*** using *EOS_RCELL_RRATE_LEARN()*.

Table 2-62. Initial Learn Pulse Number

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Resistance Learning	Initial Learn Pulse Number	Unsigned Integer	1	0	255	1	counts

Table 2-63. Initial Rcell

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	Initial Rcell	Unsigned Integer	2	0	65535	0	mΩ

Table 2-64. Initial Rcell Learned

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
End Of Service	Direct Resistance Decision	Initial Rcell Learned	Boolean	1	0	1	0	—

The time since the last successful calculation of ***Rcell*** is provided via the *EOSSTATUS2()* command. If timing were disrupted since the last ***Rcell*** calculation, such as caused by a power cycle on the device, then this register will read zero until a new ***Rcell*** is calculated.

Similarly, the time since the successful calculation of ***Initial Rcell*** is also provided via the *EOSSTATUS2()* command. If timing was disrupted since the ***Initial Rcell*** calculation, this register will read zero, and the *[RSDLI]* flag will be set.

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When the cell is first put into service, the first learning phases that are initiated are used to calculate multiple values for ***RRate***. These multiple values are averaged and stored as ***Initial RRate***. For the ***Initial RRate*** procedure to operate, the ***Auto Learn Time*** cannot be set = 0.

NOTE: For the EOS Determination function to provide best results, it is important that the values of ***Rcell*** be measured at a consistent level of charge. This means it cannot directly be used together with JEITA charging or ***WHr Charge Termination*** without additional steps.

If the ***Initial Learn Pulse Number*** is set greater than 1, ***Learn Voltage Restore*** is set = 1, and ***Learn Sequence Mode*** is set = 1 (DISCHARGE-BEFORE-CHARGE mode), the bq34110 device will wait for the cell to be charged after each ***Learn Post-Relax Phase*** is complete before it completes the learning cycle for a single initial learn pulse. It then initiates the next learning cycle for the next initial learn pulse.

However, if the ***Learn Voltage Restore*** is set = 0, then the bq34110 device will wait for the cell to be charged back after the ***Learn Post-Relax Phase*** is complete, but will immediately complete the learning cycle and initiate a new learning cycle for the next initial learn pulse. This will result in each of the multiple initial learn pulses being captured at slightly different depth-of-discharge, which can introduce an additional error into the measurement, depending on the battery chemistry used. To avoid this error, it is recommended that either the ***Learn Voltage Restore*** be set = 1 or the ***Initial Learn Pulse Number*** be set = 1.

Because the Learn Discharge Pulses only discharge the battery a small amount, recharging to compensate for this small discharge may create difficulty in achieving proper charge termination, depending on the battery chemistry used. This case should be evaluated during development, and if necessary, the pertinent charge termination settings can be adjusted to address this issue. For example, the ***Current Taper Window*** and ***Minimum Taper Capacity*** may need to be reduced to facilitate proper charge termination.

A possible issue can arise if the bq34110 gauge is configured for CHARGE-BEFORE-DISCHARGE mode, and a fault occurs after charging, but before the ***Learn Discharge Phase*** has completed. Then when the device attempts a new learning phase, it may have difficulty achieving proper charge termination, since the battery was already charged to the required level. In this case, a possible workaround is to enable the learning load and discharge the battery back to the original level before the next learning phase occurs.

2.12 Battery Level Threshold

The battery level threshold (BLT) feature indicates when the SOC of a battery pack has depleted to a certain value set in a DF register. This feature allows a host to program two capacity-based thresholds that govern the triggering of the BLT flag and the setting or clearing of the *OperationStatus()[BLT]* on the basis of *RemainingCapacity()*. The interrupt on pins ALERT1 and/or ALERT2 is enabled or disabled via ***Alert1_6[BLT]*** and ***Alert2_6[BLT]***, respectively.

- *OperationStatus()[BLT]* is set when:
  - Current > 0 and *RemainingCapacity()* > *BLTChargeSet()*. This threshold is initialized at reset from ***Init Charge Set***.
  - Current ≤ 0 and *RemainingCapacity()* < *BLTDischargeSet()*. This threshold is initialized at reset from ***Init Discharge Set***.
- When either *BLTDischargeSet()* or *BLTChargeSet()* commands are received, *OperationStatus()[BLT]* will clear and the flag will be deasserted. The new threshold is written to either *BLTDischargeSet()* or *BLTChargeSet()*.
- At reset, the flag is set to the deasserted state.

Table 2-65. BLTDischargeSet()

Name	Access			Protocol	Type	Min	Max	Default	Unit
	SE	US	FA						
BLT Discharge Set	R/W	R/W	R/W	Word	S2	—	65535	150	mAh

This read/write word command updates the BLT set threshold for DISCHARGE mode for the next BLT flag assertion, deasserts the present BLT flag, and clears the *OperationStatus()[BLT]* bit.

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Table 2-66. BLTChargeSet()

Name	Access			Protocol	Type	Min	Max	Default	Unit
	SE	US	FA						
BLT Charge Set	R/W	R/W	R/W	Word	S2	—	65535	175	mAh

The read/write word command updates the BLT set threshold for CHARGE mode for the next BLT flag assertion, deasserts the present BLT flag, and clears the *OperationStatus()[BLT]* bit.

Table 2-67. Init Discharge Set

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	BLT	Init Discharge Set	I2	2	0	32767	150	mAh

Description: Initial value for *BLTDischargeSet()*

Table 2-68. Init Charge Set

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Settings	BLT	Init Charge Set	I2	2	0	32767	175	mAh

Description: Initial value for *BLTChargeSet()*

2.13 Lifetime Data Collection

The bq34110 Lifetime Data Collection function can be enabled by setting *ManufacturingStatus()[LF_EN]* to gather data regarding the battery and store it to data flash.

The device logs the lifetime data for temperature, voltage, and current with programmable frequency and resolution. The data log recordings are controlled by settings in the ***Lifetime Resolution*** data flash subclass. The Lifetime Data Collection can be started by setting the *[LF_EN]* bit. Data available for collection include maximum charge and discharge currents, maximum pack voltage, number of data flash updates, and minimum and maximum temperature.

Once the Lifetime Data Collection function is enabled, the measured values are compared to what is already stored in the data flash. If the measured value is higher than the maximum or lower than the minimum value stored in the data flash by more than the "Resolution" set for at least one parameter, the entire Data Flash Lifetime Registers are updated after at least 60 seconds.

There is a 60-s minimum update time between DF writes. When a new maximum or minimum is detected, a 60-s timer is enabled, and the DF writes occur at the end of this window. Any additional max/min value detected within this window will also be updated. The first new max/min value detected after this window will trigger the next 60-s timer window.

Internal to the bq34110 device, there exists a RAM maximum/minimum table in addition to the DF maximum/minimum table. The RAM table is updated independent of the resolution parameters. The DF table is updated only if at least one of the RAM parameters exceeds the DF value by more than the resolution associated with it. When DF is updated, the entire RAM table is written to DF. Consequently, it is possible to see a new maximum or minimum value for a certain parameter even if the value of this parameter never exceeds the maximum or minimum value stored in the data flash for this parameter value by the resolution amount.

The Lifetime Data Collection of one or more parameters can be reset or restarted by writing new default (or starting) values to the corresponding data flash registers through sealed or unsealed access as described below. However, when using unsealed access, new values will only take effect after device reset.

The logged data can be accessed as RW in UNSEALED mode from the ***Lifetime*** class of data flash. Lifetime data may be accessed read-only when sealed using the *LT_DATA()* subcommand, which returns data on *MACData()*.

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The logging settings such as ***Temperature Resolution***, ***Voltage Resolution***, and ***Current Resolution*** can be configured only in UNSEALED mode by writing to the ***Lifetime Resolution*** subclass of the data flash.

The ***Lifetime Resolution*** data flash contains the parameters that set the limits related to how much a data parameter must exceed the previously logged maximum/minimum value to be updated in the lifetime log. For example, voltage must exceed ***Max Pack Voltage*** by more than ***Voltage Resolution*** to update ***Max Pack Voltage*** in the data flash.

Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Lifetimes	Temperature	Max Temperature	Unsigned Integer	2	–400	1200	300	0.1°C
Lifetimes	Temperature	Min Temperature	Signed Integer	2	–400	1200	200	0.1°C
Lifetimes	Current	Max Charge Current	Signed Integer	2	0	32767	0	mA
Lifetimes	Current	Max Discharge Current	Signed Integer	2	0	32767	0	mA
Lifetimes	Voltage	Max Pack Voltage	Signed Integer	2	0	32767	160	20 mV
Lifetimes	Voltage	Min Pack Voltage	Signed Integer	2	0	32767	175	20 mV
Lifetimes	Lifetime Resolution	Temperature Resolution	Unsigned Integer	1	0	255	10	0.1°C
Lifetimes	Lifetime Resolution	Current Resolution	Unsigned Integer	1	0	255	100	mA
Lifetimes	Lifetime Resolution	Voltage Resolution	Unsigned Integer	1	0	255	1	20 mV

2.14 Authentication

2.14.1 Overview

The bq34110 device can act as a SHA-1/HMAC authentication slave by using its internal engine. Sending a 160-bit SHA-1 challenge message to the device causes the device to return a 160-bit digest, based on the challenge message and hidden plain-text authentication keys. When this digest matches an identical one generated by a host or dedicated authentication master (operating on the same challenge message and using the same plain text keys), the authentication process is successful.

The device contains a default plain-text authentication key of 0x0123456789ABCDEFFEDCBA987654321. If using the device's internal authentication engine, the default key can be used for development purposes, but should be changed to a secret key and the part immediately sealed before putting a pack into operation.

2.14.2 Key Programming

When the device's SHA-1/HMAC internal engine is used, authentication keys are stored as plain text in memory. The *Authentication_Key()* command is the *ManufacturerAccessControl()* 0x0037 command and enables the update of the authentication key into the device. The device must be in FULL ACCESS mode for the authentication key to update.

To update a new authentication key, send the *Authentication_Key()* + the new 128-bit authentication key to *MACData()*.

There is no direct read access to the authentication key. After writing the new authentication to the gauge, the gauge will generate an all-zero challenge and provide the corresponding response for verification.

2.14.3 Authentication Challenge

To initiate an authentication challenge while in SEALED mode:

- Write 0x00 to *ManufacturerAccessControl()* at 0x3F.
- Write the 20-byte challenge to *MACData()* at addresses 0x40 through 0x53.
- Write the checksum to *MACDataSum()* at address 0x60.

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At the last write to *MACDataSum()*, the bq34110 device will check the checksum and, if correct, begin an authentication computation. This procedure takes approximately 200 ms, after which the resulting digest will be written to *MACData()*, overwriting the pre-existing challenge.

To initiate an authentication challenge while in UNSEALED mode:

- Write 0x01 to *MACDataLen()* at 0x61.
- Write the 20-byte challenge to *MACData()* at addresses 0x40 through 0x53.
- Write the checksum to *MACDataSum()* at address 0x60.

At the last write to *MACDataSum()*, the bq34110 device will check the checksum and, if correct, begin an authentication computation. This procedure takes approximately 200 ms, after which the resulting digest will be written to *MACData()*, overwriting the pre-existing challenge.

NOTE: If there is an error detected in the checksum or the *MACData()* was read before the authentication computation was completed, then *MACData()* will still hold the original challenge data.

2.15 Communications

Communication with the bq34110 device is primarily via its I²C bus. The device supports the standard I²C read, incremental read, one-byte write quick read, and functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively.

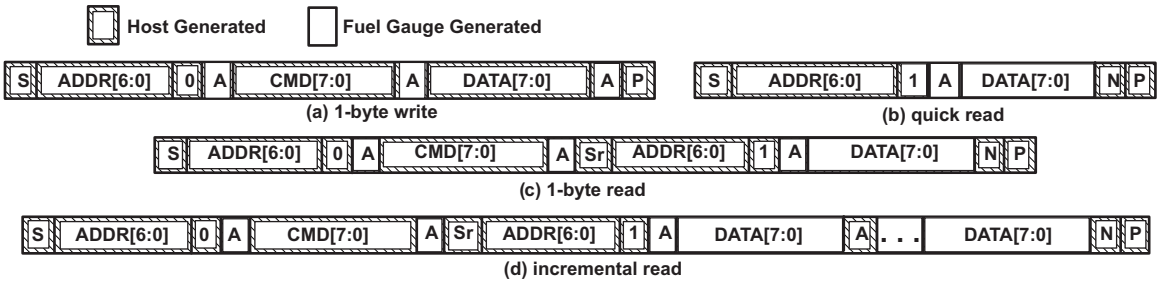

Figure 2-8. Supported I²C formats: (a) 1-byte write, (b) quick read, (c) 1 byte-read, and (d) incremental read (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The “quick read” returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the device or the I²C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as 2-byte commands that require two bytes of data).

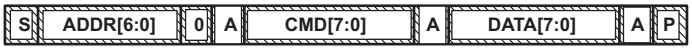

Figure 2-9. Attempt to Write a Read-Only Address (Nack After Data Sent By Master)

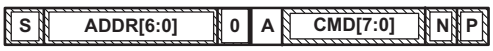

Figure 2-10. Attempt to Read an Address Above 0x7F (NACK Command)

Figure 2-11. Attempt at Incremental Writes (Nack All Extra Data Bytes Sent)

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Figure 2-12. Incremental Read at the Maximum Allowed Read Address

The I²C engine releases both SDA and SCL if the I²C bus is held low for ***Bus Low Time***. If the device were holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power SLEEP mode.

Detailed examples of I²C transactions accessing gauge data can be found in the *Using I²C Communication with the bq275xx Series of Fuel Gauges Application Report* (SLUA467).

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Data Commands

The bq34110 device uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each command has an associated command-code pair, as indicated in Table 3-1. Because each command consists of two bytes of data, two consecutive I^2C transmissions must be executed to initiate the command function and to read or write the corresponding two bytes of data. Additional options for transferring data are described under the *Control()* command section below. Read and write permissions depend on the active access mode, SEALED or UNSEALED. See *Communications* for I^2C details.

3.1 Command Summary

Table 3-1. Command Summary

Name	Acronym	COMMAND CODE	UNIT	SEALED ACCESS
Control()/CONTROL_STATUS()	CNTL	0x00 and 0x01	NA	R/W
Temperature()	TEMP	0x06 and 0x07	0.1°K	R
Voltage()	VOLT	0x08 and 0x09	mV	R
BatteryStatus()	BSTAT	0x0A and 0x0B	NA	R
Current()	Current()	0x0C and 0x0D	mA	R
RemainingCapacity()	RC	0x10 and 0x11	mAh	R
FullChargeCapacity()	FCC	0x12 and 0x13	mAh	R
AverageCurrent()	AI	0x14 and 0x15	mA	R
TimeToEmpty()	TTE	0x16 and 0x17	Minutes	R
TimeToFull()	TTF	0x18 and 0x19	Minutes	R
AccumulatedCharge		0x1A and 0x1B	mAh	R
AccumulatedTime		0x1C and 0x1D	5 min	R
LastAccumulatedCharge		0x1E and 0x1F	mAh	R
LastAccumulatedTime		0x20 and 0x21	5 min	R
AveragePower()	AP	0x24 and 0x25	mW	R
InternalTemperature()	INTTEMP	0x28 and 0x29	0.1°K	R
CycleCount()	CC	0x2A and 0x2B	Number	R
RelativeStateOfCharge()	RSOC	0x2C and 0x2D	%	R
StateOfHealth()	SOH	0x2E and 0x2F	%	R
ChargingVoltage()	CV	0x30 and 0x31	mV	R
ChargingCurrent()	CC	0x32 and 0x33	mA	R
BLTDischargeSet		0x34 and 0x35	mAh	RW
BLTChargeSet		0x36 and 0x37	mAh	RW
OperationStatus()		0x3A and 0x3B	NA	R
DesignCapacity()	Design Capacity	0x3C and 0x3D	mAh	R
ManufacturerAccessControl()	MAC	0x3E and 0x3F		RW
MACData()		0x40 through 0x5F		RW
MACDataSum()		0x60		RW
MACDataLen()		0x61		RW
EOSLearnStatus		0x64 and 0x65		R

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Table 3-1. Command Summary (continued)

Name	Acronym	COMMAND CODE	UNIT	SEALED ACCESS
EOSSafetyStatus		0x66 and 0x67		R
EOSStatus		0x68		R
AnalogCount()		0x79		R
RawCurrent()		0x7A and 0x7B		R
RawVoltage()		0x7C and 0x7D	mV	R
RawIntTemp()		0x7E and 0x7F	0.1°K	R
RawExtTemp()		0x80 and 0x81	0.1°K	R

3.2 Control(): 0x00/0x01

Issuing a *Control()* (or Manufacturer Access Control or MAC) command requires a 2-byte subcommand. The subcommand specifies the particular MAC function needed. The *Control()* command allows the system to control specific features of the gas gauge during normal operation and additional features when the device is in different access modes, as described below. On this device, *Control()* commands may also be sent to *ManufacturerAccessControl()*. Any subcommand that has a data response will be read back on *MACData()*. The readback of *CONTROL_STATUS()* is an exception in that this data is not read back on *MACData()*, but is read back directly.

Reading the *Control()* registers will always report the *CONTROL_STATUS()* data field except after the *DEVICE_TYPE()* and *FW_VERSION()* subcommands. After these subcommands, *CONTROL_STATUS()* will report the value 0xFFA5 one time before reverting to the normal data response. This is a flag to indicate that the data response has been moved to *MACData()*. Writing a 0x0000 to *Control()* is no longer necessary to read the *CONTROL_STATUS()*; however, doing so is acceptable.

When executing commands that require data (such as data flash writes), the subcommand can be written to either *Control()* or *ManufacturerAccessControl()* registers; however, it is recommended to write using the *ManufacturerAccessControl()* registers as this allows performing the full command in a single I^2C transaction.

Table 3-2. *Control()* MAC Subcommands

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of key features. This command should be read back on 0x00; it will not read back on *MACData()*.
DEVICE_TYPE	0x0001	Yes	Reports the device type of 0x0110 (indicating the bq34110 device)
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type
HW_VERSION	0x0003	Yes	Reports the hardware version of the device type
IF_SUM	0x0004	Yes	Reports Instruction flash checksum
STATIC_DF_SUM	0x0005	Yes	Reports the static data flash checksum
PREV_MACWRITE	0x0007	Yes	This MAC subcommand returns previous *Control()* subcommand code.
BOARD_OFFSET	0x0009	Yes	Invokes the board offset correction
CC_OFFSET	0x000A	Yes	Invokes the CC offset correction
CC_OFFSET_SAVE	0x000B	Yes	Saves the results of the offset calibration process
ALL_DF_SUM	0x0010	Yes	This MAC subcommand returns the checksum of the entire data flash except for calibration data.
SET_SNOOZE	0x0013	Yes	This MAC subcommand forces the *CONTROL_STATUS()[SNOOZE]* bit to 1.
CLEAR_SNOOZE	0x0014	Yes	This MAC subcommand forces the *CONTROL_STATUS()[SNOOZE]* bit to 0.
ACCUM_DSG_EN	0x001E	No	This MAC subcommand toggles the value of *ManufacturingStatus()[ACDSG_EN].*

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Table 3-2. *Control()* **MAC Subcommands (continued)**

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
ACCUM_CHG_EN	0x001F	No	This MAC subcommand toggles the value of *ManufacturingStatus()[ACCHG_EN].*
IGNORE_SELFDSG_EN	0x0020	No	This MAC subcommand toggles the value of *ManufacturingStatus()[IGNORE_SD_EN].*
EOS_EN	0x0021	No	This MAC subcommand toggles the value of *ManufacturingStatus()[EOS_EN].*
PIN_CONTROL_EN	0x0022	No	This MAC subcommand toggles the value of *ManufacturingStatus()[PCTL_EN].*
LIFETIME_EN	0x0023	No	This MAC subcommand toggles the value of *ManufacturingStatus()[LF_EN].*
WHR_EN	0x0024	No	This MAC subcommand toggles the value of *ManufacturingStatus()[WHR_EN].*
CAL_TOGGLE	0x002D	No	This MAC subcommand toggles the value of *OperationStatus()[CALMD].*
SEAL	0x0030	No	Places the device in SEALED access mode
ENTER_ROM	0x0033	No	Places the device into ROM mode (same function as 0x0F00).
SECURITY_KEYS	0x0035	No	Reads and writes Security Keys
AUTHENTICATION_KEY	0x0037	No	Writes the authentication key into data flash
EOS_START_LEARN	0x0039	Yes	Initiates an EOS learning phase
EOS_ABORT_LEARN	0x003A	Yes	Aborts an EOS learning phase
EOS_RCELL_RRATE_LEARN	0x003B	No	Initiates the ***Initial Rcell*** and ***Initial RRate*** learning procedures
EOS_WARNCLR	0x003C	Yes	Clears the EOS Warning flags
EOS_INITIAL_RCELL	0x003E	Yes	Used to read and write the EOS ***Initial Rcell*** value
EOS_INITIAL_RRATE	0x003F	Yes	Used to read and write the EOS ***Initial RRate*** value
RESET	0x0041	No	Resets device
EOS_LOAD_ON	0x0044	No	Turns on the learning load
EOS_LOAD_OFF	0x0045	No	Turns off the learning load
DEVICE_NAME	0x004A	Yes	This MAC subcommand returns the device name.
ACCUM_RESET	0x004B	Yes	Resets the Accumulated Charge integration counter
EOS_SAFETY_STATUS	0x0051	Yes	This returns the same value as the *EOSSafetyStatus()* command, but does not clear the bits after reading.
OPERATION_STATUS	0x0054	Yes	This returns the same value as the *OperationStatus()* command.
GaugingStatus	0x0056	Yes	This MAC subcommand returns the information in the CEDV gauging status register.
ManufacturingStatus	0x0057	Yes	This MAC subcommand returns the values of various functional modes of the device.
ALERT1STATUS	0x005E	Yes	This MAC subcommand returns the value of flags as given by ***Alert1_0..6 Config***.
ALERT2STATUS	0x005F	Yes	This MAC subcommand returns the value of flags as given by ***Alert2_0..6 Config***.
LT_DATA_1	0x0060	Yes	This MAC subcommand returns lifetime data.
PIN_ALERT1_SET	0x0068	Yes	Sets the ALERT1 pin to high
PIN_ALERT1_RESET	0x0069	Yes	Resets the ALERT1 pin to low
PIN_ALERT2_SET	0x006A	Yes	Sets the ALERT2 pin to high
PIN_ALERT2_RESET	0x006B	Yes	Resets the ALERT2 pin to low
PIN_VEN_SET	0x006C	Yes	Sets the VEN pin to high
PIN_VEN_RESET	0x006D	Yes	Resets the VEN pin to low
PIN_LEN_SET	0x006E	Yes	Sets the LEN pin to high
PIN_LEN_RESET	0x006F	Yes	Resets the LEN pin to low

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Table 3-2. *Control()* **MAC Subcommands (continued)**

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
MANU_DATA	0x0070	Yes	This MAC subcommand returns the Manufacturer Information Block. This can be written directly when unsealed.
EOSSTATUS1	0x007A	Yes	This MAC subcommand returns status information associated with the EOS Determination function.
EOSSTATUS2	0x007B	Yes	This MAC subcommand returns status information associated with the EOS Determination function.
ENTER_ROM	0x0F00	No	Places the device into ROM mode (same function as 0x0033)
STORE_REMCAP_A	0x22C1	Yes	Used to initiate storing the present value of *RemainingCapacity* for post-reset restore
STORE_REMCAP_B	0x28A0	Yes	Used to initiate storing the present value of *RemainingCapacity* for post-reset restore

3.2.1 CONTROL_STATUS: 0x0000

A read of this command should be done by reading 0x00, which directly returns the data below. This command is an exception in that it does not read back on *MACData()*. The status word includes the following information:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Low Byte	RSVD	RSVD	CCA	BCA	SNOOZE	RSVD	RSVD	RSVD

RSVD: Reserved. Do not use.

CCA (Bit 5): Indicates the device Coulomb Counter Calibration routine is active. Active when set.

BCA (Bit 4): Indicates the device Board Calibration routine is active. Active when set.

SNOOZE (Bit 3): Status bit indicating a request for entry into SNOOZE mode. True when set. Default is 0.

3.2.2 DEVICE_TYPE: 0x0001

This MAC subcommand instructs the bq34110 device to return the device type to addresses 0x40/0x41.

3.2.3 FW_VERSION: 0x0002

This MAC subcommand instructs the bq34110 device to return the device number (0110 for the bq34110 device), followed by the firmware version (single byte), and the firmware build number (single byte) in big-endian format.

3.2.4 HW_VERSION: 0x0003

This MAC subcommand instructs the bq34110 device to return the hardware version to addresses 0x40/0x41.

3.2.5 IF_SUM: 0x0004

This MAC subcommand instructs the bq34110 device to report the instruction flash checksum.

3.2.6 STATIC_DF_SUM: 0x0005

This MAC subcommand instructs the bq34110 device to report the static data flash checksum.

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3.2.7 PREV_MACWRITE: 0x0007

This MAC subcommand instructs the bq34110 device to return the previous command written to addresses 0x40/0x41. The value returned is limited to less than 0x0020. The data returned by this command is provided in little-endian format.

3.2.8 BOARD_OFFSET: 0x0009

This MAC subcommand instructs the bq34110 device to calibrate board offset. During board offset calibration, the *[BCA]* bit is set.

3.2.9 CC_OFFSET: 0x000A

This MAC subcommand instructs the bq34110 device to calibrate the coulomb counter offset. During calibration, the *[CCA]* bit is set.

3.2.10 CC_OFFSET_SAVE: 0x000B

This MAC subcommand instructs the bq34110 device to save the coulomb counter offset after calibration.

3.2.11 ALL_DF_SUM: 0x0010

This MAC subcommand instructs the bq34110 device to report the checksum of the entire data flash except for calibration data.

3.2.12 SET_SNOOZE: 0x0013

This MAC subcommand forces the *CONTROL_STATUS()[SNOOZE]* bit to 1.

3.2.13 CLEAR_SNOOZE: 0x0014

This MAC subcommand forces the *CONTROL_STATUS()[SNOOZE]* bit to 0.

3.2.14 ACCUM_DSG_EN: 0x001E

This MAC subcommand toggles the value of *ManufacturingStatus()[ACDSG_EN]*.

3.2.15 ACCUM_CHG_EN: 0x001F

This MAC subcommand toggles the value of *ManufacturingStatus()[ACCHG_EN]*.

3.2.16 IGNORE_SELFDSG_EN: 0x0020

This MAC subcommand toggles the value of *ManufacturingStatus()[IGNORE_SD_EN]*.

3.2.17 EOS_EN: 0x0021

This MAC subcommand toggles the value of *ManufacturingStatus()[EOS_EN]*.

NOTE: If *[EOS_EN]* is changed directly in data flash, then the device should be reset for the change to take effect.

3.2.18 PIN_CONTROL_EN: 0x0022

This MAC subcommand toggles the value of *ManufacturingStatus()[PCTL_EN]*.

3.2.19 LIFETIME_EN: 0x0023

This MAC subcommand toggles the value of *ManufacturingStatus()[LT_EN]*.

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3.2.20 WHR_EN: 0x0024

This MAC subcommand toggles the value of *ManufacturingStatus()[WHR_EN]*.

3.2.21 CAL_TOGGLE: 0x002D

This MAC subcommand toggles the value of *OperationStatus()[CALMD]*.

3.2.22 SEAL: 0x0030

This MAC subcommand instructs the bq34110 device to transition from UNSEALED state to SEALED state. The fuel gauge should always be set to SEALED state for use in customers' end equipment.

3.2.23 ENTER_ROM: 0x0033

This MAC subcommand instructs the bq34110 device to enter ROM mode. This has the same function as the subcommand 0x0F00.

3.2.24 SECURITY_KEYS: 0x0035

This is a read/write command that changes the Unseal and Full Access Keys.

To read the keys, do the following:

1. Send the *Securitykeys()* subcommand to the *Control()* or *ManufacturerAccessControl()*.
2. Write 0x35 0x00 to either *Control(0x00, 0x01)* or *ManufacturerAccessControl(0x3E, 0x3F)*.
3. Read back 8 bytes at *MACData(0x40–0x47)*.

To write the keys, do the following:

1. Write 0x35 0x00 to either *Control(0x00, 0x01)* or *ManufacturerAccessControl(0x3E, 0x3F)*.
2. Write the data in big endian format to *MACData(0x40–0x47)*.
3. Write the checksum to *MACDataSum(0x60)*. The checksum is the complement of the sum of the data and command bytes.
4. Write the length of 0x08 to *MACDataLen(0x61)*. The length includes the command, data, checksum, and length bytes.

3.2.25 AUTHENTICATION_KEY: 0x0037

This MAC subcommand writes the authentication key into the device. See Authentication for more details.

3.2.26 EOS_START_LEARN: 0x0039

This MAC subcommand instructs the bq34110 device to begin a learning phase.

3.2.27 EOS_ABORT_LEARN: 0x003A

This MAC subcommand instructs the bq34110 device to stop a learning phase.

3.2.28 EOS_RCELL_RRATE_LEARN: 0x003B

This MAC subcommand instructs the bq34110 device to initiate an ***Initial Rcell*** and ***Initial RRate*** measurement.

3.2.29 EOS_WARNCLR: 0x003C

This MAC subcommand instructs the bq34110 device to clear the EOS warning bits (this includes *[DRDWARN]*, *[RSDWARN]*, and *[RSDLWARN]*).

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3.2.30 EOS_INITIAL_RCELL: 0x003E

This MAC subcommand is used to read the stored ***Initial_Rcell*** measurement or to overwrite the value with a previously measured value.

3.2.31 EOS_INITIAL_RRATE: 0x003F

This MAC subcommand is used to read the ***Initial_RRate*** measurement or to overwrite the value with a previously measured value.

3.2.32 RESET: 0x0041

This MAC subcommand instructs the bq34110 device to perform a full reset. This command is only available when the device is UNSEALED.

3.2.33 EOS_LOAD_ON: 0x0044

This MAC subcommand instructs the bq34110 device to enable the EOS learning load.

3.2.34 EOS_LOAD_OFF: 0x0045

This MAC subcommand instructs the bq34110 device to disable the EOS learning load.

3.2.35 DEVICE_NAME: 0x004A

This MAC subcommand returns the device name on *MACData()* in ASCII characters (0x62 0x71 0x33 0x34 0x31 0x31 0c30 for the bq34110 device).

3.2.36 ACCUM_RESET: 0x004B

This MAC subcommand resets the ***Accumulated Charge*** integration counter.

3.2.37 EOS_SAFETY_STATUS: 0x0051

This MAC subcommand returns the same values as the *EOSSafetyStatus()* command, but does not clear the bits after reading.

3.2.38 OPERATION_STATUS: 0x0054

This MAC subcommand returns the same values as the *OperationStatus()* command.

3.2.39 GaugingStatus: 0x0056

This MAC subcommand returns various flags associated with the CEDV gas gauging function.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High byte	VDQ	EDV2	EDV1	RSVD	RSVD	FCCX	RSVD	REST
Low byte	CF	DSG	EDV	RSVD	TC	TD	FC	FD

Legend = **RSVD:** Reserved. Do not use.

VDQ: Discharge Qualified for Learning

1 = Detected

0 = Not Detected

EDV2: End-of-Discharge Voltage Level 2

1 = EDV2 voltage is reached during discharge.

0 = EDV2 voltage is not reached, or is not in DISCHARGE mode.

EDV1: Discharge Qualified for Learning

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1 = Detected
0 = Not Detected

FCCX: *FullChargeCapacity()* has been updated.
This bit changes state each time *FullChargeCapacity()* updates.

REST: This bit indicates whether the device is in RELAX mode.
1 = The device has reached relaxation.
0 = The device has not reached relaxation.

CF: Condition Flag
1 = This bit is set if the device determines that the error in gauging has reached a level where a condition cycle is needed (discharging to EDV2 and charging to full).
0 = The gauging error has not reached the level where a condition cycle is needed.

DSG: Discharge/Relax
This bit is set when the cell is detected in a RELAX state or discharging, just not charging.
Note that this bit differs from the DSG bit in *BatteryStatus()*, which is set only when a discharge current is present, not during RELAX.
1 = Charging Not Detected
0 = Charging Detected

EDV0: End-of-Discharge Voltage Level 0 (Termination)
1 = Termination voltage is reached during discharge.
0 = Termination voltage is not reached or is not in DISCHARGE mode.

TC: Terminate Charge
1 = Detected
0 = Not Detected

TD: Terminate Discharge
1 = Detected
0 = Not Detected

FC: Fully Charged
1 = Detected
0 = Not Detected

FD: Fully Discharged
1 = Detected
0 = Not Detected

3.2.40 ManufacturingStatus: 0x0057

This MAC subcommand instructs the bq34110 device to provide the status of various functional modes, reflecting their state in the ***Manufacturing Status Init*** data flash. These bits are described in detail in Section 2.1.2.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High byte	CAL_EN	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
Low byte	RSVD	WHR_EN	LF_EN	PCTL_EN	EOS_EN	IGNORE_SD_EN	ACCHG_EN	ACDSG_EN

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Legend = **RSVD**: Reserved. Do not use.

CAL_EN: Calibration Enabled

1 = Indicates the device is in CALIBRATION mode.

0 = Indicates the device is not in CALIBRATION mode.

WHR_EN: ***WHr Charge Termination*** Enable

1 = ***WHr Charge Termination*** is enabled.

0 = ***WHr Charge Termination*** is disabled (default).

LF_EN: Lifetime Data Collection Enable

1 = Enabled

0 = Disabled (default)

PCTL_EN: Pin Control Enable

This bit allows the host to manually control the state of the pins ALERT1, ALERT2, VEN, and LEN through the *ManufacturerAccessControl()* subcommands *PIN_ALERT1_SET()*, *PIN_ALERT1_RESET()*, *PIN_ALERT2_SET()*, *PIN_ALERT2_RESET()*, *PIN_VEN_SET()*, *PIN_VEN_RESET()*, *PIN_LEN_SET()*, and *PIN_LEN_RESET()*.

1 = Manual pin control is enabled.

0 = Manual pin control is disabled (default).

EOS_EN: End-Of-Service Determination Enable

Note that if ***[EOS_EN]*** is changed directly in data flash, then the device should be reset for the change to take effect.

1 = End-Of-Service Determination is enabled.

0 = End-Of-Service Determination is disabled (default).

IGNORE_SD_EN: Ignore Self-Discharge Control

1 = Accumulated charge integration ignores self-discharge, only integrates real current.

0 = Accumulated charge integration includes both real and self-discharge current (default).

ACCHG_EN: Accumulated Charge Enable for Charging Current Integration

1 = Positive (charging) values of *Current()* are integrated (default).

0 = Positive (charging) values of *Current()* are not integrated.

ACDSG_EN: Accumulated Charge Enable for Discharging Current Integration

1 = Negative (discharging) values of *Current()* are integrated (default).

0 = Negative (discharging) values of *Current()* are not integrated.

3.2.41 ALERT1STATUS: 0x005E

This MAC subcommand returns the value of flags as given by ***Alert1_0 Config*** to ***Alert1_6 Config***.

3.2.42 ALERT2STATUS: 0x005F

This MAC subcommand returns the value of flags as given by ***Alert2_0 Config*** to ***Alert2_6 Config***.

3.2.43 LT_DATA: 0x0060

This MAC subcommand returns the lifetime operation data. For more information, see *Lifetime Data Collection*.

3.2.44 PIN_ALERT1_SET: 0x0068

This MAC subcommand directs the bq34110 device to assert the ALERT1 pin.

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3.2.45 PIN_ALERT1_RESET: 0x0069

This MAC subcommand directs the bq34110 device to deassert the ALERT1 pin.

3.2.46 PIN_ALERT2_SET: 0x006A

This MAC subcommand directs the bq34110 device to assert the ALERT2 pin.

3.2.47 PIN_ALERT2_RESET: 0x006B

This MAC subcommand directs the bq34110 device to deassert the ALERT2 pin.

3.2.48 PIN_VEN_SET: 0x006C

This MAC subcommand directs the bq34110 device to assert the VEN pin.

3.2.49 PIN_VEN_RESET: 0x006D

This MAC subcommand directs the bq34110 device to deassert the VEN pin.

3.2.50 PIN_LEN_SET: 0x006E

This MAC subcommand directs the bq34110 device to assert the LEN pin.

3.2.51 PIN_LEN_RESET: 0x006F

This MAC subcommand directs the bq34110 device to deassert the LEN pin.

3.2.52 MANU_DATA: 0x0070

This MAC subcommand is used to read/write the 32-byte Manufacturer Information Block. See *Manufacturer Information Block* for more details.

3.2.53 EOSSTATUS1: 0x007A

This MAC subcommand returns 22-bytes of read-only information on *MACData()*. All numerical information that spans multiple bytes is represented in little-endian format.

Byte	Name	Description
0–3	EOS Auto Learn Time	This 4-byte number is a countdown timer in seconds, which counts down from the programmed value of ***Auto Learn Time*** to zero for a new learning phase to occur.
4	Learn Request Timeout	This is a single-byte countdown timer in seconds, which counts down from the programmed value of ***Learn Request Timeout*** to zero for the host to control the learning load.
5	Learning State	This is a single-byte number that shows in which state is the ***learning phase***. See below for further details.
6–7	Learning Start Voltage	This two-byte number contains the voltage in mV that the EOS algorithm measured just before the ***Learn Discharge Phase*** begins.
8–9	Learning End Voltage	This two-byte number contains the voltage in mV that the EOS algorithm measured just before the ***Learn Discharge Phase*** ended.
10–11	Learning Charge Timer	This two-byte number is a countdown timer in seconds, which counts down from the programmed value of ***Learn Charge Timeout*** to zero.
12–13	Learning Discharge Timer	This two-byte number is a countdown timer in seconds, which counts down the duration of the learning discharge pulse.
14–17	Minimum Learn Time	This 3-byte number is a countdown timer in seconds, which counts down from the programmed value of ***Minimum Learn Time*** to zero.
18–19	EOS Avg Dsg Current	This is the calculated 100-s average discharge current measured over the last ***Learn Discharge Phase*** in mA.
20–21	EOS Avg Dsg Temp	This is the calculated average temperature measured over the last ***Learn Discharge Phase*** in 0.1°C.

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Table 3-3. Byte 5: Learning State

Integer Value	State
Note that these bits reflect the present status at the time and are not sticky.	
0	IDLE
1	START
2	CHARGE
3	PRE-RELAX
4	DISCHARGE
5	POST-RELAX
6	CALC_RES
7	RESTORE VOLTAGE (CHG before DSG cycle)
8	RESTORE VOLTAGE (DSG before CHG cycle)
8	FAULT

3.2.54 EOSSTATUS2: 0x007B

This MAC subcommand returns 25-bytes of read-only information on *MACData()*. All numerical information that spans multiple bytes is represented in little-endian format.

Byte	Name	Description
0–1	EOS Learned Resistance	This two-byte number provides the most recently calculated value of ***Rcell.***
2–3	EOS Learned Res Time Hours	This two-byte number provides the hour value of the EOS timer since the most recent ***Rcell*** value was captured.
4–5	EOS Learned Res Time Seconds	This two-byte number provides the seconds value of the EOS timer since the most recent ***Rcell*** value was captured.
6–7	EOS Last Learned Resistance	This two-byte number provides the previous calculated value of ***Rcell***. Note that this does not include ***Initial Rcell*** calculations.
8–9	EOS Last Learned Res Time Hours	This two-byte number provides the hour value of the EOS timer since the last ***Rcell*** value was captured.
10–11	EOS Last Learned Res Time Seconds	This two-byte number provides the seconds value of the EOS timer since the last ***Rcell*** value was captured.
12–13	EOS Initial RRate Age Hours	This two-byte number provides the hour value of the EOS timer since the ***Initial RRate*** value was captured.
14–15	EOS Initial RRate Age Seconds	This two-byte number provides the seconds value of the EOS timer since the ***Initial RRate*** value was captured.
16–17	EOS RRate	This two-byte number provides the most recently calculated value of ***RRate.***
18–19	EOS RRate Long	This two-byte number provides the most recently calculated value of $\boldsymbol{RRate}_{longterm}$.
20–23	InitialRcell/RRate Learn Res	This 4-byte value is a sum of the individual ***Rcell*** or ***RRate*** measurements captured thus far for averaging multiple values during the ***Initial Rcell*** and ***Initial RRate*** computation procedure. The number of measurements averaged is dictated by the value of ***Initial Learn Pulse Number***.
24	InitialRcell/RRate Learn Count	This single-byte number provides the number of Learning Discharge Pulses used thus far during computation of the ***Initial Rcell*** and ***Initial RRate*** values. The final number of measurements averaged is dictated by the value of ***Initial Learn Pulse Number***.

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3.2.55 ENTER_ROM: 0x0F00

This MAC subcommand instructs the bq34110 device to enter ROM mode. This has the same function as the subcommand 0x0033.

3.2.56 STORE_REMCAP_A: 0x22C1

When this MAC subcommand is written within 4 seconds of when the *STORE_REMCAP_B()* MAC subcommand is written, the present value of *RemainingCapacity()* is stored to data flash. When the bq34110 device is reset, the value of *RemainingCapacity()* is initialized to the stored value.

3.2.57 STORE_REMCAP_B: 0x28A0

When this MAC subcommand is written within 4 seconds of when the *STORE_REMCAP_A()* MAC subcommand is written, the present value of *RemainingCapacity()* is stored to data flash. When the bq34110 device is reset, the value of *RemainingCapacity()* is initialized to the stored value.

3.3 Temperature(): 0x06/0x07

This read-only command pair returns an unsigned integer value of the temperature, in units of 0.1°K, measured by the device and has a range of 0 to 6553.5°K. The source of the measured temperature is configured by the ***[TEMPS]*** bit in the ***Operation Config A*** register.

TEMPS: *Temperature()* source selection

1 = External temperature sensor is used (default).

0 = Internal temperature sensor is used.

Table 3-4. Temperature()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
Temperature	R	R	R	Word	U2	0	65535	0.1°K

3.4 Voltage(): 0x08/0x09

This read-word command pair returns an unsigned integer value of the measured battery voltage in mV with a range of 0 V to 65535 mV.

Table 3-5. Voltage()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
Voltage	R	R	R	Word	U2	0	65535	mV

3.5 BatteryStatus(): 0x0A/0x0B

This read only register provides indications on the status of the battery.

Table 3-6. BatteryStatus()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
BatteryStatus	R	R	R	Word	Hex	0x00	0xff	—

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MSB	RSVD	SOCLOW	UTC	UTD	OTC	OTD	BATHIGH	BATLOW
LSB	SLEEP	CHGINH	FD	FC	TCA	TDA	CHG	DSG

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Legend = **RSVD:** Reserved. Do not use.

SOCLOW: State-Of-Charge low detection

1 = Low SOC state is detected.

0 = Low SOC state is not detected.

UTC: Undertemperature in Charge condition is detected.

1 = Undertemperature in Charge is detected.

0 = Undertemperature in Charge is not detected.

UTD: Undertemperature in Discharge condition is detected.

1 = Undertemperature in Discharge is detected.

0 = Undertemperature in Discharge is not detected.

OTC: Overtemperature in Charge condition is detected.

1 = Overtemperature in Charge is detected.

0 = Overtemperature in Charge is not detected.

.

OTD: Overtemperature in Discharge condition is detected.

1 = Overtemperature in Discharge is detected.

0 = Overtemperature in Discharge is not detected.

BATHIGH: Battery High Voltage Alarm.

This flag is set and cleared based on the selected thresholds in ***Safety.BATHIGH*** data flash settings.

BATLOW: Battery Low Voltage Alarm

This flag is set and cleared based on the selected thresholds in ***Safety.BATLOW*** data flash settings.

SLEEP: The device is in SLEEP mode when set.

1 = The device is in SLEEP mode.

0 = The device is not in SLEEP mode.

CHGINH: Charge inhibit.

If set, this indicates charging should not begin because *Temperature()* is outside the acceptable range.

1 = Charging is inhibited, indicating charging should not begin.

0 = Charging is not inhibited.

FD: Full discharge is detected.

This flag is set and cleared based on the selected ***SOC Flag Config B*** options.

FC: Full charge is detected.

This bit is controlled by settings in ***SOC Flag Config A*** and ***SOC Flag Config B***.

TCA: Terminate Charge Alarm.

This flag is set and cleared based on the selected ***SOC Flag Config A*** options.

TDA: Terminate Discharge Alarm.

This flag is set and cleared based on the selected ***SOC Flag Config A*** options.

CHG: Charge current detection

1 = Charge current is detected.

0 = No charge is detected.

DSG: Discharge current detection

1 = Discharge is current detected.

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0 = No discharge is detected.

3.6 Current(): 0x0C/0x0D

This read-only command pair returns a signed integer value that is the average current flowing through the sense resistor. It is updated every 1 second with units of 1 mA per LSB.

Table 3-7. Current()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
Current	R	R	R	Word	I2	–32768	32767	mA

3.7 RemainingCapacity(): 0x10/0x11

This read-only command pair returns the compensated battery capacity remaining. Unit is 1 mAh per LSB.

Table 3-8. RemainingCapacity()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
RemainingCapacity	R	R	R	Word	U2	0	65535	mAh

3.8 FullChargeCapacity(): 0x12/0x13

This read-only command pair returns the learned full battery capacity. Unit is 1 mAh per LSB.

Table 3-9. FullChargeCapacity()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
FullChargeCapacity	R	R	R	Word	U2	0	65535	mAh

3.9 AverageCurrent(): 0x14/0x15

This read-word function returns a signed integer value that approximates a one-minute rolling average of the current being supplied (or accepted) through the battery terminals in mA with a range of –32,768 to 32,767.

AverageCurrent() is calculated by a rolling IIR filtered average of *Current()* function data with a period of 14.5 s. During the time after a reset or when switching between charge and discharge currents and before 14.5 s has elapsed, the reported *AverageCurrent()* = *Current()* function value.

Table 3-10. AverageCurrent()

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
AverageCurrent	R	R	R	Word	I2	–32767	32767	mA

The data flash value ***Filter*** determines the time constant of the filter operation used in the calculation of *AverageCurrent()* as follows:

AverageCurrent() = a × *AverageCurrent()* old + (1-a) × *Current()* with:

a = ***Filter***/256; time constant = (1 s) / ln(1/a) (default = 14.5 s)

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Class	Subclass	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
Calibration	Current	Filter	Unsigned integer	1	0	255	239	—

3.10 TimeToEmpty(): 0x16/0x17

This read-word function returns the predicted remaining battery capacity based on the present rate of discharge.

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
TimeToEmpty	R	R	R	Word	U2	0	65535	min

3.11 TimeToFull(): 0x18/0x19

This read-word function returns the predicted time to full charge based on *Current()*.

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
TimeToFull	R	R	R	Word	U2	0	65535	min

3.12 AveragePower(): 0x24/0x25

This read-word function returns a signed integer value that approximates a one-minute rolling average of the power being supplied (or accepted) through the battery terminals in units of 10 mW with a range of –32,768 to 32,767.

AveragePower() is calculated by a rolling IIR filtered average of *Current()* and *Voltage()* function data with a period of 14.5 s. During the time after a reset or when switching between charge and discharge currents and before 14.5 s has elapsed, the reported *AveragePower()* = *Current()* × *Voltage()*.

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
AveragePower	R	R	R	Word	I2	–32767	32767	10 mW

3.13 InternalTemperature(): 0x28/0x29

This read-only function returns an unsigned integer value of the internal temperature sensor in units of 0.1°K measured by the gas gauge. This function can be useful as an additional system-level temperature monitor if the main *Temperature()* function is configured for external or host-reported temperature.

3.14 CycleCount(): 0x2A/0x2B

This read-only function returns an unsigned integer value of the number of cycles that the active cell has experienced with a range of 0 to 65535. One cycle occurs when accumulated discharge ≥ cycle threshold. The cycle threshold is calculated as ***Cycle Count Percentage*** times either *FullChargeCapacity()* (when ***CEDV Gauging Configuration [CCT]*** = 1) or *DesignCapacity()* (when ***[CCT]*** = 0).

3.15 RelativeStateOfCharge(): 0x2C/0x2D

This read-only command returns an unsigned integer value of the predicted remaining battery capacity expressed as a percentage of *FullChargeCapacity()* with a range of 0 to 100%.

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3.16 StateofHealth(): 0x2E/0x2F

This command returns the state-of-health (SOH) information of the battery. *StateOfHealth()* is calculated as a percentage of *FullChargeCapacity()* relative to ***Design Capacity***. It is a read-only command.

Byte 0: LSB of SOH in capacity

Byte 1: MSB of SOH in capacity

Byte 2: LSB of SOH in energy

Byte 3: MSB of SOH in energy

3.17 ChargingVoltage(): 0x30/0x31

This read-only function returns an unsigned integer value of the needed charging voltage of the battery. A value of 65,535 indicates that the battery is requesting the maximum voltage from the battery charger.

3.18 ChargingCurrent(): 0x32/0x33

This function returns the needed charging current determined by the device.

Name	Access			Protocol	Type	Min	Max	Unit
	SE	US	FA					
ChargingCurrent()	R	R	R	Word	U2	0	65535	10 mA

3.19 BLTDischargeSet(): 0x34/0x35

This read/write word command updates the BLT set threshold for DISCHARGE mode for the next BLT flag assertion, deasserts the present BLT flag, and clears the *OperationStatus()[BLT]* bit.

Name	Access			Protocol	Type	Min	Max	Default	Unit
	SE	US	FA						
BLT Discharge Set	R/W	R/W	R/W	Word	S2	—	65535	150	mAh

3.20 BLTChargeSet(): 0x36/0x37

This read/write word command updates the BLT set threshold for CHARGE mode for the next BLT flag assertion, deasserts the present BLT flag, and clears the *OperationStatus()[BLT]* bit.

Name	Access			Protocol	Type	Min	Max	Default	Unit
	SE	US	FA						
BLT Charge Set	R/W	R/W	R/W	Word	S2	—	65535	175	mAh

3.21 OperationStatus(): 0x3A/0x3B

This read-only command returns the value of various flags. When read, this data is returned in little-endian format.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	INITCOMP	AUTH
Low Byte	BLT	SMTH	ACTHR	VDQ	EDV2	SEC1	SEC0	CALMD

Legend = **RSVD:** Reserved. Do not use.

AUTH: Authentication status

1 = Authentication is in progress.

0 = Authentication is not in progress.

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INITCOMP: Initialization Complete

1 = Device initialization (after reset or initial power up) is complete.

0 = Device initialization is not complete.

BLT: Battery Level Threshold Flag.

Setting and clearing this flag depends upon various conditions. See *Battery Level Threshold* for details.

SMTH: Smoothing Flag

This flag indicates whether the *RemainingCapacity()* accumulation is currently scaled by the smoothing engine.

1 = Smoothing engine is enabled.

0 = Smoothing engine is not enabled.

ACTHR: Accumulated Charge Threshold Flag

1 = The accumulated charge has been detected passing a threshold.

0 = The accumulated charge has not been detected passing a threshold.

VDQ: Discharge Qualified flag

This flag indicates whether the present discharge cycle is qualified for an FCC update.

1 = Discharge cycle is qualified.

0 = Discharge cycle is not qualified.

EDV2: EDV2 flag

This flag indicates whether the measured cell voltage is below the EDV2 threshold.

1 = Cell voltage is below the EDV2 threshold.

0 = Cell voltage is not below the EDV2 threshold.

SEC1, SEC0: Security Status bits

1, 1 = Sealed status

1, 0 = Unsealed status

0, 1 = Full access status

0, 0 = Invalid. This indicates the state has not yet been loaded.

CALMD: CALIBRATION mode

This flag indicates whether the device is in CALIBRATION mode or not. It is controlled by the *CAL_TOGGLE()* subcommand, which toggles its state.

1 = Calibration is enabled; *ManufacturingData()* is enabled to output ADC and coulomb counter raw data.

0 = Calibration is disabled.

3.22 DesignCapacity(): 0x3C/0x3D

This read-only function returns the value stored in ***Design Capacity***. This is intended to be the theoretical or nominal capacity of a new pack in units of 1 mAh per LSB, and is used for the calculation of *StateOfHealth()*.

3.23 ManufacturerAccessControl(): 0x3E/0x3F

This read-write word function returns the subcommand that is currently active for reads on *MACData()*.

Word writes to this function will set a subcommand. Commands that do not require data will execute immediately (identical to writes to *Control()*).

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3.24 MACData(): 0x40 through 0x5F

This read-write block returns the result data for the currently active subcommand. It is recommended to start the read at *ManufacturerAccessControl()* to verify the active subcommand.

Writes to this block are used to provide data to a subcommand when required.

3.25 MACDataSum(): 0x60

This read-write function returns the checksum of the current subcommand and data block.

Writes to this register provide the checksum necessary in order to execute subcommands that require data. The checksum is calculated as the complement of the sum of the *ManufacturerAccessControl()* and the *MACData()* bytes. *MACDataLen()* determines the number of bytes of *MACData()* that are included in the checksum.

3.26 MACDataLen(): 0x61

This read-write function returns the number of bytes of *MACData()* that are part of the response and included in *MACDataSum()*.

Writes to this register provide the number of bytes in *MACData()* that should be processed as part of the subcommand. Subcommands that require block data are not executed until *MACDataSum()* and *MACDataLen()* are written together as a word.

3.27 EOSLearnStatus(): 0x64/0x65

This command returns various flags providing information on the EOS Determination function.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	LCTO	LFAULT	LABRT	LCMD	LPER	LRLX	LCHG	LDSG
MSB	LDONE	LRES	LRSTOR	LCTLEDGE	LUCD	LDPAM	LDPAT	LDPAI

RSVD: Reserved. Do not use.

LCTO: Learn Charge Time Out

This bit is set = 1 if the bq34110 device is in LEARN CHARGE mode and detects the charging time has exceeded ***Learn Charge Time Limit***. This bit is reset to 0 when a new learning phase begins.

1 = A Learn Excessive Charge Time has been detected.

0 = A Learn Excessive Charge Time has not been detected.

LFAULT: Learn Fault Flag

This bit is set = 1 whenever a learning phase is terminated for any reason other than a valid termination, and also if any other fault (such as in *GaugingStatus()* or *BatteryStatus()*) occurred during the learning phase. The bit will be reset to 0 when a new learning phase begins.

1 = A learning phase has been aborted.

0 = A learning phase has not been aborted.

LABRT: Learn Abort on Command

This bit is set = 1 whenever a learning phase was aborted by the host. A bit that has been set = 1 will be reset to 0 when a new learning phase begins.

1 = A requested learning phase has been aborted.

0 = A requested learning phase has not been aborted.

LCMD: Learn Command

This bit is set = 1 if learning is activated and a learning phase has been started by a command. The bit will remain high until the learning phase is complete (including charging, learning, discharging, and related calculations).

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1 = The device is in a command-initiated learning phase.

0 = The device is not in a command-initiated learning phase.

LPER: Learn Periodic Mode

This bit is set = 1 if learning is activated and the bq34110 device is in PERIODIC LEARN mode. This bit is only set while the device is in a learning phase.

1 = The device is in periodic learn mode.

0 = The device is not in periodic learn mode.

LRLX: Learn RELAX mode

This bit is set = 1 if learning is activated and the bq34110 device is in a RELAX mode during learning. This means the cell is waiting to detect a relaxed condition; it may not have achieved relaxation yet.

1 = The device is in RELAX mode during learning.

0 = The device is not in RELAX mode during learning.

LCHG: Learn CHARGE mode

This bit is set = 1 if the bq34110 device is in learn CHARGE mode. If the device is controlling a charger directly through a device pin, then the value of this signal will be reflected on the selected pin. If instead the host is controlling the charger, then this bit can be used to signal the host to initiate charging.

1 = A LEARN CHARGE mode is in progress.

0 = A LEARN CHARGE mode is not in progress.

LDSG: Learn DISCHARGE Mode

This bit is set = 1 if the bq34110 device is in automatic END-OF-SERVICE DETERMINATION mode and the device intends to begin a ***Learn Discharge Phase***. It is set = 0 when the device intends the ***Learn Discharge Phase*** to end. If the device is controlling the discharge directly using the LEN pin, then the LEN pin will reflect the value of LDSG. If instead the host is controlling the ***Learn Discharge Current***, this bit will signal the host to enable the ***Learn Discharge Current***.

1 = A ***Learn Discharge Phase*** has been requested or is in progress.

0 = A ***Learn Discharge Phase*** is requested to stop or has been stopped.

LDONE: Learn Done

This bit is set = 1 when a valid learning phase has completed.

1 = A valid learning phase was completed.

0 = A valid learning phase was not completed.

LRES: Learned ***Rcell***

This bit is set = 1 when the bq34110 device has completed the computation of a new ***Rcell*** value during the present learning phase. This bit is cleared when the learning phase is complete.

1 = A new value of ***Rcell*** was acquired.

0 = A new value of ***Rcell*** has not yet been acquired.

LRSTOR: Learn Voltage Restore

This bit is set = 1 if whenever the ***Learn Discharge Phase*** is complete and the voltage can be restored back to its original level. This bit is cleared when the learning phase is complete.

1 = A Learning Discharge Phase has completed, and the voltage can be restored.

0 = The device has completed the learning phase.

LCTLEDGE: Learn Discharge Flag Edge Detected

This bit is set = 1 if whenever LDSG changes state. This can be used by the host as an interrupt to recognize when a learning load should be activated and when it should be disabled. This bit clears when the register is read.

1 = A change in LDSG was detected (this is only applicable when LENCTL=0).

0 = A change in LDSG was not detected.

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LUCD: Learn Unexpected Current Detected

This bit is set when the device is in LEARNING mode (but not in the ***Learn Discharge Phase***), and a current is detected differently than what is expected. It is set if the device is attempting to charge or relax, and a discharge current in excess of ***Discharge Detection Threshold*** is detected. It is also set if the device is in a RELAX mode and a charging current in excess of ***Charge Detection Threshold*** is detected. This detection also terminates the learning phase, and this bit will remain set as a flag to the host as to why the learning phase was aborted. This bit will be reset to 0 when a new learning phase begins.

1 = An unexpected system-related current was detected during a learning charge or learning relax period.

0 = An unexpected system-related current was not detected.

LDPAM: ***Learn Discharge Phase*** Abort on Timer

This bit is set = 1 when a ***Learn Discharge Phase*** was requested by the host but was declined due to the time since the last ***Learn Discharge Phase*** was less than the interval specified in ***Minimum Learn Time***. A bit that was set = 1 will be reset to 0 when ***Minimum Learn Time*** has passed.

1 = A requested ***Learn Discharge Phase*** was declined.

0 = A requested ***Learn Discharge Phase*** has not been declined.

LDPAT: ***Learn Discharge Phase*** Abort on Temperature

This bit is set = 1 when a ***Learn Discharge Phase*** was initiated but was aborted due to *Temperature()* measured outside the range allowed by ***Learn Min Temperature*** and ***Learn Max Temperature***. A bit that was set = 1 will be reset to 0 when a new ***Learn Discharge Phase*** begins.

1 = A ***Learn Discharge Phase*** was aborted.

0 = A ***Learn Discharge Phase*** has not been aborted.

LDPAI: ***Learn Discharge Phase*** Abort on Current

This bit is set = 1 when a ***Learn Discharge Phase*** was initiated but was aborted due to *Current()* measured outside the range allowed by ***Learn Discharge Current*** and ***Learn Discharge Current Boundary***. A bit that was set = 1 will be reset to 0 when a new ***Learn Discharge Phase*** begins.

1 = A ***Learn Discharge Phase*** was aborted.

0 = A ***Learn Discharge Phase*** has not been aborted.

3.28 EOSSafetyStatus(): 0x66/0x67

This command returns flags generated by the EOS Determination function.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LSB	RSVD	RSVD	RSVD	RSVD	RSVD	RSDL ALERT	RSDALERT	DRDALERT
MSB	RSVD	RSVD	RSVD	RSVD	RSVD	RSDLWARN	RSDWARN	DRDWARN

Legend = **RSVD:** Reserved. Do not use.

RSDLALERT: Resistance Slope Decisioning Long-Term Alert

This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the *[RSDLALERT]* signal. This signal is cleared when the register is read or if a new learning phase begins.

1 = An RSDLALERT was detected.

0 = An RSDLALERT has not been detected.

RSDALERT: Resistance Slope Decisioning Alert

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This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the [RSDALERT] signal. This signal is cleared when the register is read or if a new learning phase begins.

1 = An RSDALERT was detected.

0 = An RSDALERT has not been detected.

DRDALERT: Direct Resistance Decisioning Alert

This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the *[DRDALERT]* signal. This signal is cleared when the register is read or if a new learning phase begins.

1 = A DRDALERT was detected.

0 = A DRDALERT has not been detected.

RSDLWARN: Resistance Slope Decisioning Long-Term Warning

This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the *[RSDLWARN]* signal. This signal is NOT cleared when the register is read. It can only be cleared using the command *EOS_WARNCLR()*.

1 = An RSDLWARN was detected.

0 = An RSDLWARN has not been detected.

RSDWARN: Resistance Slope Decisioning Warning

This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the *[RSDWARN]* signal. This signal is NOT cleared when the register is read. It can only be cleared using the command *EOS_WARNCLR()*.

1 = An RSDWARN was detected.

0 = An RSDWARN has not been detected.

DRDWARN: Direct Resistance Decisioning Warning

This bit is set = 1 if the bq34110 EOS Determination function detects the condition described above to trigger the *[DRDWARN]* signal. This signal is NOT cleared when the register is read. It can only be cleared using the command *EOS_WARNCLR()*.

1 = A DRDWARN was detected.

0 = A DRDWARN has not been detected.

3.29 EOSStatus(): 0x68

This command returns additional flags that provide information related to the EOS Determination function.

7	6	5	4	3	2	1	0
SRRL	SRCL	RSVD	LTI	RSDLI	RCELLR	IRRCOMP	IRCOMP

Legend = **RSVD:** Reserved. Do not use.

SRRL: ***Initial RRate*** Learning in Progress

This bit is set = 1 if the bq34110 EOS Determination function begins the required learning phases to calculate a value of ***Initial RRate***, generally after an *EOS_RCELL_RRATE_LEARN()* command has been issued. The bit will clear when the ***Initial RRate*** learning and computation is complete.

SRCL: ***Initial Rcell*** Learning in Progress

This bit is set = 1 if the bq34110 EOS Determination function begins the required learning phases to calculate a value of ***Initial Rcell***, generally after an *EOS_RCELL_RRATE_LEARN()* command has been issued. The bit will clear when the Initial Rcell learning and computation is complete.

LTI: Learn Timer Invalid

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This bit is set = 1 if the bq34110 EOS Determination function detects that the timer has been interrupted since the most recent ***Rcell*** was calculated. In this case, the RSD algorithm must capture two new ***Rcell*** values separated in time to calculate a new value of ***RRate*** and evaluate this for corresponding alerts and warnings.

1 = A timer interruption was detected.

0 = A timer interruption has not been detected.

RSDLI: Resistance Slope Decisioning Long-Term Invalid

This bit is set = 1 if the bq34110 EOS Determination function detects that the timer has been interrupted since the ***Initial RRate*** was calculated. In this case, the RSDL algorithm will no longer trigger an alert or warning.

1 = A timer interruption was detected.

0 = A timer interruption has not been detected.

RCELLR: ***Rcell*** Reduction Alert

This bit is set = 1 if the bq34110 EOS Determination function detects a value of Rcell that is more than 2% below the previous value of ***Rcell***. This signal is cleared when the register is read or if a new learning phase begins.

1 = A reduction in ***Rcell*** was detected.

0 = A reduction in ***Rcell*** has not been detected.

IRRCOMP: ***Initial RRate*** Calculation Complete

This bit is set = 1 if the bq34110 EOS Determination function has completed the required learning phases to calculate a value of ***Initial RRate***. This bit is reset when a new ***Initial RRate*** calculation is triggered until the new calculation is complete. This bit can be written by the host through loading data flash if the host wishes to initialize the device with previously calculated ***Initial RRate*** data and not trigger a new ***Initial RRate*** calculation.

1 = ***Initial RRate*** was obtained.

0 = ***Initial RRate*** has not been obtained.

IRCOMP: ***Initial Rcell*** Calculation Complete

This bit is set = 1 if the bq34110 EOS Determination function has completed the required learning phases to calculate a value of Initial Rcell. This bit is reset when a new ***Initial Rcell*** calculation is triggered until the new calculation is complete. This bit can be written by the host through loading data flash if the host wishes to initialize the device with previously calculated ***Initial Rcell*** data and not trigger a new ***Initial Rcell*** calculation.

1 = ***Initial Rcell*** was obtained.

0 = ***Initial Rcell*** has not been obtained.

3.30 AnalogCount(): 0x79

This read-only function returns the analog calibration counter. The value is incremented every time the analog calibration data is updated.

3.31 RawCurrent(): 0x7A/0x7B

This read-only function returns the raw data from the coulomb counter, which is indirectly related to the current being measured.

3.32 RawVoltage(): 0x7C/0x7D

This read-only function returns the raw data from the cell voltage reading.

3.33 RawIntTemp(): 0x7E/0x7F

This read-only function returns the raw data from the internal temperature measurement.

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3.34 RawExtTemp(): 0x80/0x81

This read-only function returns the raw data from the external temperature measurement.

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Data Flash

Data flash (DF) can only be updated if *Voltage()* ≥ ***Flash Update OK Voltage***, except while the device is in CALIBRATION mode. Flash programming current can cause an increase in LDO dropout. The value of ***Flash Update OK Voltage*** should be selected such that the device V_{CC} voltage does not fall below its minimum of 2.4 V during flash write operations.

4.1 Accessing Data Flash

Accessing data flash is supported by accessing the actual physical memory in the address range 0x4000–0x43FF. This provides up to 1k of directly addressable DF. In this mode, the subcommand represents the actual base address in DF to access. Reads provide a 32-byte block (except if it runs off the end of DF). The length will identify if it is at the end (less than 32 bytes). Writes can have anywhere from 1 to 32 bytes, which provide the ability to write a single DF parameter without having to read a row first.

4.1.1 Write to DF Example

Assume data1 is located at address 0x4000 and data2 is located at address 0x4002 and both data1 and data2 are U2 type. To update data1 and data2 to 0x1234 and 0x5678, respectively, do the following:

- Write 0x00 0x40 (DF address in little endian format) to *ManufacturerAccessControl(0x3E, 0x3F)*.
- Write 0x12 0x34 0x56 0x78 (data in big endian format) to *MACData(0x40–0x43)*. The writes to *ManufacturerAccessControl()* and *MACData()* can be performed in a single transaction.
- Write 0xAB (complement of the sum of the *ManufacturerAccessControl()* and *MACData()* bytes) to *MACDataSum(0x60)*.
- Write 0x08 (4 + length of *MACData()* bytes) to *MACDataLen(0x61)*.
- The data flash write will execute when the *MACDataSum()* and *MACDataLen()* are written in order (word write) and are verified to be correct.

4.1.2 Read from DF Example

- Write 0x00 0x40 (DF address in little endian format) to *ManufacturerAccessControl(0x3E, 0x3F)*.
- Read *ManufacturerAccessControl(0x3E, 0x3F)* to verify.
- Read data from *MACData(0x40–0x5F)*.
- Read checksum and length from *MACDataSum(0x60)*, *MACDataLen()*.
- Verify checksum. All data above can be read in a single transaction by reading 36 bytes starting at *ManufacturerAccessControl()*.

4.1.3 Auto-Increment Reading

To support faster data flash dumps, the 0x4000–0x43FF commands will auto-increment after a successful read. This enables the host to skip the write word step, which increases throughput by at least 2x. After a word read is detected of the *MACDataSum()* and *MACDataLen()* registers, the gauge will add the current block size to the command (32 bytes). There is no auto-increment for the last block of DF.

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4.2 Access Modes

The bq34110 device provides three security modes that control data flash access permissions (see Table 4-1). Public Access refers to data flash locations specified in *Data Flash Summary* that are accessible to the user. Private Access refers to reserved data flash locations used by the device system. Following the procedure outlined in *Accessing Data Flash*, care should be taken to avoid writing to Private data flash locations when performing block writes in FULL ACCESS mode.

Table 4-1. Data Flash Access

SECURITY MODE	DF—PUBLIC ACCESS	DF—PRIVATE ACCESS
BOOTROM	N/A	N/A
FULL ACCESS	R/W	R/W
UNSEALED	R/W	R/W
SEALED	R	N/A

Although FULL ACCESS and UNSEALED modes appear identical, FULL ACCESS mode allows the device to directly transition to BOOTROM mode and also write access keys. UNSEALED mode does not have these abilities.

4.3 Sealing/Unsealing Data Flash Access

The bq34110 device implements a key-access scheme to transition between SEALED, UNSEALED, and FULL ACCESS modes. Each transition requires that a unique set of two keys are sent to the device via the *Control()* command (these keys are unrelated to the keys used for SHA-1/HMAC authentication). The keys must be sent consecutively, with no other data written to the *Control()* register in between. Do not set the two keys to identical values.

When in the SEALED mode, the *OperationStatus()[SEC1, SEC0]* bits are set to [1, 1]. When the UNSEAL keys are correctly received by the gas gauge, the bits will be set to [1, 0]. When the FULL ACCESS keys are correctly received, then the bits will change to [0, 1]. The state [0, 0] is not valid, and only indicates that the state has not yet been loaded.

The access keys are changed using the *SECURITY_KEYS()* subcommand. This command enables a read/write of the 4 key words (8 bytes). Each word is in big endian order, with the first two words being the unseal code and the remaining two words being the full access codes.

When writing the codes to *Control()* or *ManufacturerAccessControl()*, they must be sent in little endian order; therefore, if 0x1234 and 0x5678 are written as the unseal codes to *SECURITY_KEYS()*, then to unseal requires writing 0x34 0x12 followed by writing 0x78 0x56. The two codes must be written within 4 s of each other to succeed.

The read/write subcommand *SECURITY_KEYS()* can be sent to *Control()* or *ManufacturerAccessControl()* to read/write the keys.

To read the keys:

- Write 0x35 0x00 to either *Control(0x00, 0x01)* or *ManufacturerAccessControl(0x3E, 0x3F)*.
- Read back 8 bytes at *MACData(0x40–0x47)*.

To write the keys:

- Write 0x35 0x00 to either *Control(0x00, 0x01)* or *ManufacturerAccessControl(0x3E, 0x3F)*.
- Write the data in big endian format to *MACData(0x40–0x47)*.
- Write the checksum to *MACDataSum(0x60)*. The checksum is the complement of the sum of the data and command bytes.
- Write the length of 0x08 to *MACDataLen(0x61)*. The length includes the command, data, checksum, and length bytes.

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4.4 SOC Flag Configuration A (SOC Flag Config A) Register

The settings in ***SOC Flag Config A*** configure how the *[TC]*, *[FC]*, and *[TD]* flags in *GaugingStatus()* set and clear. These flags are also used to set the *[TCA]*, *[TDA]*, and *[FC]* flags in *BatteryStatus()*.

Table 4-2. SOC Configuration Flag A Register Bit Definitions

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
High Byte	RSVD	RSVD	RSVD	RSVD	TCSETVCT	FCSETVCT	RSVD	RSVD
Default	0	0	0	0	1	1	0	0
	0x0C							
Low Byte	TCCLEAR RSOC	TCSET RSOC	TCCLEARV	TCSETV	TDCLEAR RSOC	TDSET RSOC	TDCLEARV	TDSETV
Default	1	0	0	0	1	1	0	0
	0x8C							

RSVD = Reserved

TCSETVCT= Enables *BatteryStatus()[TCA]* flag set on primary charge termination
0 = Disabled
1 = Enabled (default)

FCSETVCT= Enables *BatteryStatus()[FC]* flag set on primary charge termination
0 = Disabled
1 = Enabled (default)

TCCLEARRSOC = Enables *BatteryStatus()[TCA]* flag clear when *RelativeStateOfCharge()* ≤ ***TC:Clear % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

TCSETRSOC = Enables *BatteryStatus()[TCA]* flag set when *RelativeStateOfCharge()* ≥ ***TC:Set % RSOC Threshold***
0 = Disabled (default)
1 = Enabled

TCCLEARV = Enables *BatteryStatus()[TCA]* flag clear when *Voltage()* ≤ ***TC:Clear Voltage Threshold***
0 = Disabled (default)
1 = Enabled

TCSETV = Enables *BatteryStatus()[TCA]* flag set when *Voltage()* ≥ ***TC:Set Voltage Threshold***
0 = Disabled (default)
1 = Enabled

TDCLEARRSOC = Enables *BatteryStatus()[TDA]* flag clear when *RelativeStateOfCharge()* ≥ ***TD:Clear % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

TDSETRSOC = Enables *BatteryStatus()[TDA]* flag set when *RelativeStateOfCharge()* ≤ ***TD:Set % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

TDCLEARV = Enables *BatteryStatus()[TDA]* flag clear when *Voltage()* ≥ ***TD:Clear Voltage Threshold***
0 = Disabled (default)
1 = Enabled

TDSETV = Enables *BatteryStatus()[TDA]* flag set when *Voltage()* ≤ ***TD:Set Voltage Threshold***
0 = Disabled (default)
1 = Enabled

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4.5 SOC Flag Configuration B (SOC Flag Config B) Register

Table 4-3. SOC Configuration Flag B Register Bit Definitions

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	FCCCLEAR RSOC	FCSET RSOC	FCCLEARV	FCSETV	FDCLEAR RSOC	FDSET RSOC	FDCLEARV	FDSETV
Default	1	0	0	0	1	1	0	0
	0x8C							

FCCLEARRSOC = Enables *BatteryStatus()[FC]* flag clear when *RelativeStateOfCharge()* ≤ ***FC:Clear % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

FCSETRSOC = Enables *BatteryStatus()[FC]* flag set when *RelativeStateOfCharge()* ≥ ***FC:Set % RSOC Threshold***
0= Disabled (default)
1 = Enabled

FCCLEARV = Enables *BatteryStatus()[FC]* flag clear when *Voltage()* ≤ ***FC:Clear Voltage Threshold***
0 = Disabled (default)
1 = Enabled

FCSETV = Enables *BatteryStatus()[FC]* flag set when *Voltage()* ≥ ***FC:Set Voltage Threshold***
0 = Disabled (default)
1 = Enabled

FDCLEARRSOC = Enables *BatteryStatus()[FD]* flag clear when *RelativeStateOfCharge()* ≥ ***FD:Clear % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

FDSETRSOC = Enables *BatteryStatus()[FD]* flag set when *RelativeStateOfCharge()* ≤ ***FD:Set % RSOC Threshold***
0 = Disabled
1 = Enabled (default)

FDCLEARV = Enables *BatteryStatus()[FD]* flag clear when *Voltage()* ≥ ***FD:Clear Voltage Threshold***
0 = Disabled (default)
1 = Enabled

FDSETV = Enables *BatteryStatus()[FD]* flag set when *Voltage()* ≤ ***FD:Set Voltage Threshold***
0 = Disabled (default)
1 = Enabled

4.6 Manufacturer Information Block

The gas gauge contains 32 bytes of user-programmable data flash storage called the ***Manufacturer Info Block***. This block is accessible using the *MANU_DATA()* subcommand. The *MANU_DATA()* command is read/write when UNSEALED and read-only when SEALED.

To read the block in any mode, write 70 00 (*MANU_DATA()*) to *ManufacturerAccessControl()* or *Control()*, then read the *MACData()* block.

To write the block, send 70 00 to *ManufacturerAccessControl()*, write the 32 byte data block to *MACData()*, and then write the checksum and length to *MACDataSum()* and *MACDataLen()*. The write will not proceed until the checksum and length are verified.

It is also possible to write the ***Manufacturer Info Block*** using the data flash interface by writing to the DF address where the block is stored.

NOTE: The ***Manufacturer Info Block*** is read-only when in SEALED mode.

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Table 4-4. Manufacturer Info Block

Class	Subclass	Address	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
System Data	Manufacturer Data	0x4042	Manufacturer Info Block A01	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4043	Manufacturer Info Block A02	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4044	Manufacturer Info Block A03	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4045	Manufacturer Info Block A04	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4046	Manufacturer Info Block A05	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4047	Manufacturer Info Block A06	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4048	Manufacturer Info Block A07	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4049	Manufacturer Info Block A08	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404A	Manufacturer Info Block A09	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404B	Manufacturer Info Block A10	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404C	Manufacturer Info Block A11	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404D	Manufacturer Info Block A12	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404E	Manufacturer Info Block A13	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x404F	Manufacturer Info Block A14	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4050	Manufacturer Info Block A15	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4051	Manufacturer Info Block A16	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4052	Manufacturer Info Block A17	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4053	Manufacturer Info Block A18	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4054	Manufacturer Info Block A19	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4055	Manufacturer Info Block A20	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4056	Manufacturer Info Block A21	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4057	Manufacturer Info Block A22	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4058	Manufacturer Info Block A23	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4059	Manufacturer Info Block A24	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405A	Manufacturer Info Block A25	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405B	Manufacturer Info Block A26	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405C	Manufacturer Info Block A27	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405D	Manufacturer Info Block A28	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405E	Manufacturer Info Block A29	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x405F	Manufacturer Info Block A30	Hex	1	0x00	0xFF	0x00	—
System Data	Manufacturer Data	0x4060	Manufacturer Info Block A31	Hex	1	0x00	0xFF	0x00	—

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Table 4-4. Manufacturer Info Block (continued)

Class	Subclass	Address	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
System Data	Manufacturer Data	0x4061	Manufacturer Info Block A32	Hex	1	0x00	0xFF	0x00	—

4.7 Data Flash Summary

The data types used in this section are described below.

Type	Min Value	Max Value
F4	$\pm 9.8603 \times 10^{-39}$	$\pm 5.707267 \times 10^{37}$
H1	0x00	0xFF
H2	0x00	0xFFFF
H4	0x00	0xFFFF FFFF
I1	–128	127
I2	–32768	32767
I4	–2,147,483,648	2,147,483,647
Sx	1-byte string	x-byte string
U1	0	255
U2	0	65535
U4	0	4,294,967,295

Table 4-5. Data Flash Table

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	Data	0x4000	CC Gain	F4	1.00E–01	4.00E+00	.47095	—
Calibration	Data	0x4004	CC Delta	F4	2.98262E+04	1.193046E+06	5.677446e5	—
Calibration	Data	0x4008	CC Offset	I2	–32767	32767	–1432	mA
Calibration	Data	0x400C	Board Offset	I1	–128	127	0	µA
Calibration	Data	0x400D	Int Temp Offset	I1	–128	127	0	0.1°C
Calibration	Data	0x400E	Ext Temp Offset	I1	–128	127	0	0.1°C
Calibration	Data	0x400F	Pack V Offset	I1	–128	127	0	mV
Calibration	Data	0x4010	Voltage Divider	U2	0	65535	5000	mV
Calibration	Temp Model	0x41C1	Int Coeff 1	I2	–32768	32767	0	Num
Calibration	Temp Model	0x41C3	Int Coeff 2	I2	–32768	32767	0	Num
Calibration	Temp Model	0x41C5	Int Coeff 3	I2	–32768	32767	–12324	Num
Calibration	Temp Model	0x41C7	Int Coeff 4	I2	–32768	32767	6131	0.1°K
Calibration	Temp Model	0x41C9	Int Min AD	I2	–32768	32767	0	—
Calibration	Temp Model	0x41CB	Int Max Temp	I2	–32768	32767	6131	0.1°K
Calibration	Temp Model	0x41CD	Ext Coeff 1	I2	–32768	32767	20982	Num
Calibration	Temp Model	0x41CF	Ext Coeff 2	I2	–32768	32767	–13836	Num
Calibration	Temp Model	0x41D1	Ext Coeff 3	I2	–32768	32767	5202	Num
Calibration	Temp Model	0x41D3	Ext Coeff 4	I2	–32768	32767	2337	0.1°K
Calibration	Temp Model	0x41D5	Ext Min AD	I2	–32768	32767	12909	—
Calibration	Temp Model	0x41D7	Vcomp Coeff 1	I2	–32768	32767	0	Num
Calibration	Temp Model	0x41D9	Vcomp Coeff 2	I2	–32768	32767	14902	Num
Calibration	Temp Model	0x41DB	Vcomp Coeff 3	I2	–32768	32767	–623	Num
Calibration	Temp Model	0x41DD	Vcomp Coeff 4	I2	–32768	32767	37	Num
Calibration	Temp Model	0x41DF	Vcomp Input Multiplier	U1	0	255	48	Num
Calibration	Temp Model	0x41E0	Vcomp Output Divisor	I2	–32768	32767	256	Num
Calibration	Current	0x41E2	Filter	U1	0	255	239	Num

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	Current	0x41E3	Deadband	U1	0	255	5	mA
Calibration	Current	0x41E4	CC Deadband	U1	0	255	34	149 nV
Charger Control	Charge Inhibit Cfg	0x4100	Chg Inhibit Temp Low	I2	–400	1200	0	0.1°C
Charger Control	Charge Inhibit Cfg	0x4102	Chg Inhibit Temp High	I2	–400	1200	450	0.1°C
Charger Control	Charge Inhibit Cfg	0x4104	Temp Hys	I2	0	100	50	0.1°C
Charger Control	JEITA Temperature	0x4106	T1 Temp	I2	–400	1200	0	0.1°C
Charger Control	JEITA Temperature	0x4108	T2 Temp	I2	–400	1200	100	0.1°C
Charger Control	JEITA Temperature	0x410A	T3 Temp	I2	–400	1200	450	0.1°C
Charger Control	JEITA Temperature	0x410C	T4 Temp	I2	–400	1200	550	0.1°C
Charger Control	JEITA Temperature	0x410E	Charge Current T1-T2	I2	0	32767	300	mA
Charger Control	JEITA Temperature	0x4110	Charge Current T2-T3	I2	0	32767	1100	mA
Charger Control	JEITA Temperature	0x4112	Charge Current T3-T4	I2	0	32767	660	mA
Charger Control	JEITA Temperature	0x4114	Charge Voltage T1-T2	I2	0	32767	4100	mV
Charger Control	JEITA Temperature	0x4116	Charge Voltage T2-T3	I2	0	32767	4200	mV
Charger Control	JEITA Temperature	0x4118	Charge Voltage T3-T4	I2	0	32767	4100	mA
Charger Control	Charge Termination	0x411A	Maintenance Current	I2	0	1000	0	mV
Charger Control	Charge Termination	0x411C	Taper Current	I2	0	1000	100	mA
Charger Control	Charge Termination	0x411E	Minimum Taper Capacity	I2	0	1000	25	0.01 mAh
Charger Control	Charge Termination	0x4120	Taper Voltage	I2	0	1000	100	mV
Charger Control	Charge Termination	0x4122	Current Taper Window	U1	0	60	40	s
Charger Control	WHr Charge Termination	0x4123	Max Charge Voltage	I2	0	32767	4200	mV
Charger Control	WHr Charge Termination	0x4125	WHr CV Step	I2	0	32767	50	mV
Charger Control	WHr Charge Termination	0x4127	WHr Termination Capacity	I2	0	32767	1100	mAh
Charger Control	WHr Charge Termination	0x4129	FC WHr Clear	I2	0	32767	1000	mAh
Charger Control	NiMH Charge Termination	0x412B	Delta Temperature	I2	–400	1200	30	0.1°C
Charger Control	NiMH Charge Termination	0x412D	Delta Temperature Time	U2	0	255	100	s
Charger Control	NiMH Charge Termination	0x412F	Holdoff Time	U2	0	255	180	s
Charger Control	NiMH Charge Termination	0x4131	Holdoff Current	I2	0	32767	240	mA
Charger Control	NiMH Charge Termination	0x4133	Holdoff Temperature	I2	–400	1200	250	0.1°C
Charger Control	NiMH Charge Termination	0x4135	Cell Negative Delta Voltage	I2	0	32767	17	mV
Charger Control	NiMH Charge Termination	0x4137	Cell Negative Delta Time	U1	0	255	16	s
Charger Control	NiMH Charge Termination	0x4138	Cell Negative Delta Qual Voltage	I2	0	32767	3600	mV

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Charger Control	Learned Charge Voltage	0x40C7	Last Charge Voltage T1-T2	I2	0	32767	4100	mV
Charger Control	Learned Charge Voltage	0x40C9	Last Charge Voltage T2-T3	I2	0	32767	4200	mV
Charger Control	Learned Charge Voltage	0x40CB	Last Charge Voltage T3-T4	I2	0	32767	4100	mV
Charger Control	Charge Level Control	0x4197	Charge Voltage Level A	I2	0	32767	3900	mV
Charger Control	Charge Level Control	0x4199	Charge Voltage Level B	I2	0	32767	3950	mV
Charger Control	Charge Level Control	0x419B	Charge Voltage Level C	I2	0	32767	4000	mV
Charger Control	Charge Level Control	0x419D	Charge Voltage Level D	I2	0	32767	4050	mV
Charger Control	Charge Level Control	0x419F	Charge Voltage Level E	I2	0	32767	4100	mV
Charger Control	Charge Level Control	0x41A1	Charge Voltage Level F	I2	0	32767	4150	mV
Charger Control	Charge Level Control	0x41A3	Charge Voltage Level G	I2	0	32767	4200	mV
Charger Control	Charge Level Control	0x41A5	Charge Voltage Level H	I2	0	32767	4250	mV
Settings	Configuration	0x413D	Pin Control Config	H1	0x0	0x1F	0x00	Hex
Settings	Configuration	0x413E	Alert1_0 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x413F	Alert1_1 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4140	Alert1_2 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4141	Alert1_3 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4142	Alert1_4 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4143	Alert1_5 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4144	Alert1_6 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4145	Alert2_0 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4146	Alert2_1 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4147	Alert2_2 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4148	Alert2_3 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4149	Alert2_4 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x414A	Alert2_5 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x414B	Alert2_6 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x4195	Direct Charge Pin Control	H1	0x0	0x0F	0x00	Hex
Settings	Configuration	0x4196	Charge Level Pin Control	H1	0x0	0x3F	0x00	Hex
Settings	Configuration	0x41FD	SOC Flag Config A	H2	0x0	0x0FFF	0x0C8C	Hex
Settings	Configuration	0x41FF	SOC Flag Config B	H1	0x0	0xFF	0x8C	Hex
Settings	Configuration	0x4218	EOS Configuration	H1	0x0	0x0F	0x01	Hex
Settings	Configuration	0x424B	CEDV Gauging Configuration	H2	0x0	0x3FFF	0x102A	Hex
Settings	BLT	0x414D	Init Discharge Set	I2	0	32767	150	mAh
Settings	BLT	0x414F	Init Charge Set	I2	0	32767	175	mAh
Settings	Accumulated Charge	0x416C	Accum Charge Positive Threshold	I2	0	32767	1000	mAh
Settings	Accumulated Charge	0x416E	Accum Charge Negative Threshold	I2	0	32767	1000	mAh
Settings	Manufacturing	0x40D7	Mfg Status Init	H2	0x0	0xFFFF	0x0000	Hex
Safety	OTC	0x4170	OT Chg	I2	0	1200	550	0.1°C
Safety	OTC	0x4172	OT Chg Time	U1	0	60	2	s
Safety	OTC	0x4173	OT Chg Recovery	I2	0	1200	500	0.1°C
Safety	OTD	0x4175	OT Dsg	I2	0	1200	600	0.1°C
Safety	OTD	0x4177	OT Dsg Time	U1	0	60	2	s
Safety	OTD	0x4178	OT Dsg Recovery	I2	0	1200	550	0.1°C

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Safety	UTC	0x417A	UT Chg	I2	–400	1200	0	0.1°C
Safety	UTC	0x417C	UT Chg Time	U1	0	60	2	s
Safety	UTC	0x417D	UT Chg Recovery	I2	–400	1200	50	0.1°C
Safety	UTD	0x417F	UT Dsg	I2	–400	1200	0	0.1°C
Safety	UTD	0x4181	UT Dsg Time	U1	0	60	2	s
Safety	UTD	0x4182	UT Dsg Recovery	I2	–400	1200	50	0.1°C
Safety	BATLOW	0x4184	Battery Low Set Threshold	I2	0	5000	3150	mV
Safety	BATLOW	0x4186	Battery Low Time	U1	0	60	2	s
Safety	BATLOW	0x4187	Battery Low Clear Threshold	I2	0	5000	3400	mV
Safety	BATHIGH	0x4189	Battery High Set Threshold	I2	0	5000	4300	mV
Safety	BATHIGH	0x418B	Battery High Time	U1	0	60	2	s
Safety	BATHIGH	0x418C	Battery High Clear Threshold	I2	0	5000	4200	mV
Safety	SOCLOW	0x418E	SOC Low Threshold	U1	0	100	10	%
Safety	SOCLOW	0x418F	SOC Low Recovery	U1	0	100	30	%
Configuration	Registers	0x413A	Operation Config A	H2	0x0000	0xFFFF	0x8204	Hex
Configuration	Registers	0x4151	Device Type	H2	0x0000	0xFFFF	0x0110	Hex
Configuration	Registers	0x4155	Number of Series Cells	U1	1	100	1	Num
Configuration	Power	0x4157	Flash Update OK Voltage	I2	0	5000	2800	mV
Configuration	Power	0x4159	Sleep Current	I2	0	100	10	mA
Configuration	Power	0x415B	Bus Low Time	U1	0	255	5	s
Configuration	Power	0x415C	Offset Cal Inhibit Temp Low	I2	–400	1200	50	0.1°C
Configuration	Power	0x415E	Offset Cal Inhibit Temp High	I2	–400	1200	450	0.1°C
Configuration	Power	0x4160	Sleep Voltage Time	U1	0	100	20	s
Configuration	Power	0x4161	Sleep Current Time	U1	0	255	20	s
Configuration	Current Thresholds	0x4162	Discharge Detection Threshold	I2	0	2000	60	mA
Configuration	Current Thresholds	0x4164	Charge Detection Threshold	I2	0	2000	75	mA
Configuration	Current Thresholds	0x4166	Quit Current	I2	0	1000	40	mA
Configuration	Current Thresholds	0x4168	Discharge Relax Time	U2	0	8191	60	s
Configuration	Current Thresholds	0x416A	Charge Relax Time	U1	0	255	60	s
Configuration	Current Thresholds	0x416B	Quit Relax Time	U1	0	63	1	s
Configuration	Data	0x406A	Device Name	S9	x	x	bq34110	—
Configuration	Data	0x4073	Data Flash Version	H2	0x0000	0xFFFF	0xFFFF	—
Configuration	Data	0x4075	Serial Number	H2	0x0000	0xFFFF	0x0001	Hex
Configuration	Data	0x4077	Manufacture Date	U2	0	65535	0	Day + Mo*32 + (Yr –1980) *512
Configuration	Data	0x41A7	Default Temperature	I2	2732	3732	2982	0.1°K
Configuration	Integrity Data	0x4062	DF Static Checksum	H2	0x0000	0x7FFF	0x0000	Hex
Configuration	Integrity Data	0x4064	All DF Checksum	H2	0x0000	0x7FFF	0x0000	Hex
Configuration	Integrity Data	0x4066	IF Checksum	H4	0x00000000	0xFFFFFFFF	0xFBD3E090	Hex
Configuration	Integrity Data	0x40D4	Full Reset Counter	U1	0	255	0	Num
Configuration	Integrity Data	0x40D5	Reset Counter WD	U1	0	255	0	Num
System Data	Manufacturer Data	0x4042	Manufacturer Info Block A01	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4043	Manufacturer Info Block A02	H1	0x00	0xFF	0x00	Hex

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
System Data	Manufacturer Data	0x4044	Manufacturer Info Block A03	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4045	Manufacturer Info Block A04	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4046	Manufacturer Info Block A05	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4047	Manufacturer Info Block A06	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4048	Manufacturer Info Block A07	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4049	Manufacturer Info Block A08	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404A	Manufacturer Info Block A09	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404B	Manufacturer Info Block A10	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404C	Manufacturer Info Block A11	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404D	Manufacturer Info Block A12	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404E	Manufacturer Info Block A13	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x404F	Manufacturer Info Block A14	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4050	Manufacturer Info Block A15	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4051	Manufacturer Info Block A16	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4052	Manufacturer Info Block A17	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4053	Manufacturer Info Block A18	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4054	Manufacturer Info Block A19	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4055	Manufacturer Info Block A20	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4056	Manufacturer Info Block A21	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4057	Manufacturer Info Block A22	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4058	Manufacturer Info Block A23	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4059	Manufacturer Info Block A24	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405A	Manufacturer Info Block A25	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405B	Manufacturer Info Block A26	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405C	Manufacturer Info Block A27	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405D	Manufacturer Info Block A28	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405E	Manufacturer Info Block A29	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x405F	Manufacturer Info Block A30	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4060	Manufacturer Info Block A31	H1	0x00	0xFF	0x00	Hex
System Data	Manufacturer Data	0x4061	Manufacturer Info Block A32	H1	0x00	0xFF	0x00	Hex
Lifetimes	Lifetime Resolution	0x4190	Temperature Resolution	U1	0	255	10	0.1°C

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Lifetimes	Lifetime Resolution	0x4191	Current Resolution	U1	0	255	100	mA
Lifetimes	Lifetime Resolution	0x4192	Voltage Resolution	U1	0	255	1	20 mV
Lifetimes	Temperature	0x4080	Max Temperature	I2	–400	1200	300	0.1°C
Lifetimes	Temperature	0x4082	Min Temperature	I2	–400	1200	200	0.1°C
Lifetimes	Current	0x4084	Max Charge Current	I2	0	32767	0	mA
Lifetimes	Current	0x4086	Max Discharge Current	I2	–32768	32767	0	mA
Lifetimes	Voltage	0x4088	Max Pack Voltage	I2	0	32767	160	20 mV
Lifetimes	Voltage	0x408A	Min Pack Voltage	I2	0	32767	175	20 mV
Gas Gauging	CEDV Profile	0x41F5	Design Capacity mAh	I2	0	32767	2200	mAh
Gas Gauging	CEDV Profile	0x424D	EMF	U2	0	65535	3743	—
Gas Gauging	CEDV Profile	0x424F	C0	U2	0	65535	149	—
Gas Gauging	CEDV Profile	0x4251	R0	U2	0	65535	867	—
Gas Gauging	CEDV Profile	0x4253	T0	U2	0	65535	4030	—
Gas Gauging	CEDV Profile	0x4255	R1	U2	0	65535	316	—
Gas Gauging	CEDV Profile	0x4257	TC	U1	0	255	9	—
Gas Gauging	CEDV Profile	0x4258	C1	U1	0	255	0	—
Gas Gauging	CEDV Profile	0x4259	Age Factor	U1	0	255	0	—
Gas Gauging	CEDV Profile	0x425A	Fixed EDV 0	I2	0	32767	3031	—
Gas Gauging	CEDV Profile	0x425C	EDV 0 Hold Time	U1	1	255	1	s
Gas Gauging	CEDV Profile	0x425D	Fixed EDV 1	I2	0	32767	3385	—
Gas Gauging	CEDV Profile	0x425F	EDV 1 Hold Time	U1	1	255	1	s
Gas Gauging	CEDV Profile	0x4260	Fixed EDV 2	I2	0	32767	3501	—
Gas Gauging	CEDV Profile	0x4262	EDV 2 Hold Time	U1	1	255	1	s
Gas Gauging	CEDV Profile	0x4263	Voltage 0% DOD	I2	–32768	32767	4173	mV
Gas Gauging	CEDV Profile	0x4265	Voltage 10% DOD	I2	–32768	32767	4043	mV
Gas Gauging	CEDV Profile	0x4267	Voltage 20% DOD	I2	–32768	32767	3925	mV
Gas Gauging	CEDV Profile	0x4269	Voltage 30% DOD	I2	–32768	32767	3821	mV
Gas Gauging	CEDV Profile	0x426B	Voltage 40% DOD	I2	–32768	32767	3725	mV
Gas Gauging	CEDV Profile	0x426D	Voltage 50% DOD	I2	–32768	32767	3656	mV
Gas Gauging	CEDV Profile	0x426F	Voltage 60% DOD	I2	–32768	32767	3619	mV
Gas Gauging	CEDV Profile	0x4271	Voltage 70% DOD	I2	–32768	32767	3582	mV
Gas Gauging	CEDV Profile	0x4273	Voltage 80% DOD	I2	–32768	32767	3515	mV
Gas Gauging	CEDV Profile	0x4275	Voltage 90% DOD	I2	–32768	32767	3439	mV
Gas Gauging	CEDV Profile	0x4277	Voltage 100% DOD	I2	–32768	32767	2713	mV
Gas Gauging	Design	0x41F9	Design Voltage	I2	0	32767	3700	mV
Gas Gauging	Cycle	0x41FB	Cycle Count Percentage	U1	0	100	90	%
Gas Gauging	FD	0x4200	Set Voltage Threshold	I2	0	5000	3000	mV
Gas Gauging	FD	0x4202	Clear Voltage Threshold	I2	0	5000	3100	mV
Gas Gauging	FD	0x4204	Set % RSOC Threshold	U1	0	100	0	%
Gas Gauging	FD	0x4205	Clear % RSOC Threshold	U1	0	100	5	%
Gas Gauging	FC	0x4206	Set Voltage Threshold	I2	0	5000	4200	mV
Gas Gauging	FC	0x4208	Clear Voltage Threshold	I2	0	5000	4100	mV
Gas Gauging	FC	0x420A	Set % RSOC Threshold	U1	0	100	100	%
Gas Gauging	FC	0x420B	Clear % RSOC Threshold	U1	0	100	95	%
Gas Gauging	TD	0x420C	Set Voltage Threshold	I2	0	5000	3200	mV
Gas Gauging	TD	0x420E	Clear Voltage Threshold	I2	0	5000	3300	mV
Gas Gauging	TD	0x4210	Set % RSOC Threshold	U1	0	100	6	%
Gas Gauging	TD	0x4211	Clear % RSOC Threshold	U1	0	100	8	%
Gas Gauging	TC	0x4212	Set Voltage Threshold	I2	0	5000	4200	mV
Gas Gauging	TC	0x4214	Clear Voltage Threshold	I2	0	5000	4100	mV

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Gas Gauging	TC	0x4216	Set % RSOC Threshold	U1	0	100	100	%
Gas Gauging	TC	0x4217	Clear % RSOC Threshold	U1	0	100	95	%
Gas Gauging	State Profile	0x40C0	Learned Full Charge Capacity	I2	0	32767	2200	mAh
Gas Gauging	State Profile	0x40C2	Stored Remaining Capacity	I2	0	32767	0	mAh
Gas Gauging	State Profile	0x40C5	Cycle Count	U2	0	65535	0	—
Gas Gauging	CEDV Cfg	0x427D	Battery Low %	U2	0	65535	700	.01%
Gas Gauging	CEDV Cfg	0x4288	Learning Low Temp	U1	0	255	119	0.1°C
Gas Gauging	CEDV Cfg	0x4291	OverLoad Current	I2	0	32767	3400	mA
Gas Gauging	CEDV Cfg	0x4295	Self Discharge Rate	U1	0	255	20	0.01%/ day
Gas Gauging	CEDV Cfg	0x4296	Electronics Load	I2	0	255	0	3 μA
Gas Gauging	CEDV Cfg	0x4298	Near Full	I2	0	32767	200	mAh
Gas Gauging	CEDV Cfg	0x429A	Reserve Capacity	I2	0	32767	0	mAh
Gas Gauging	CEDV Cfg	0x429C	Chg Eff	U1	0	100	100	%
Gas Gauging	CEDV Cfg	0x429D	Dsg Eff	U1	0	100	100	%
Gas Gauging	CEDV Cfg	0x429E	RemCap Init Percent	U1	0	110	100	%
Gas Gauging	CEDV Smoothing Config	0x429F	Smoothing Config	H1	0x00	0xFF	0x08	Hex
Gas Gauging	CEDV Smoothing Config	0x42A0	Smoothing Start Voltage	I2	0	5000	3700	mV
Gas Gauging	CEDV Smoothing Config	0x42A2	Smoothing Delta Voltage	I2	0	5000	100	mV
Gas Gauging	CEDV Smoothing Config	0x42A4	Max Smoothing Current	U2	0	65535	8000	mA
Gas Gauging	CEDV Smoothing Config	0x42A9	EOC Smooth Current	U1	0	10	2	0.1%
Gas Gauging	CEDV Smoothing Config	0x42AA	EOC Smooth Current Time	U1	0	255	60	s
End Of Service	Resistance Learning	0x4219	Auto Learn Time	U2	0	65535	1500	Hours
End Of Service	Resistance Learning	0x421B	Auto Learn Retry Time	U1	0	255	1	Hours
End Of Service	Resistance Learning	0x421C	Minimum Learn Time	U2	0	65535	750	Hours
End Of Service	Resistance Learning	0x421E	Alert-Warn Learn Time	U2	0	65535	750	Hours
End Of Service	Resistance Learning	0x4220	Initial Learn Pulse Number	U1	0	255	1	Counts
End Of Service	Resistance Learning	0x4221	Learn Charge Voltage Delta	I2	0	32767	100	mV
End Of Service	Resistance Learning	0x4223	Learn Charge Time Limit	U2	0	65535	3600	s
End Of Service	Resistance Learning	0x4225	Learn Discharge Current	I2	0	32767	220	mA
End Of Service	Resistance Learning	0x4227	Learn Discharge Current Boundary	I2	0	100	25	%
End Of Service	Resistance Learning	0x4229	Learn Discharge Time	U2	0	65535	500	s
End Of Service	Resistance Learning	0x422B	Learn Request Timeout	U1	0	255	4	s
End Of Service	Resistance Learning	0x422C	Learn Min Temperature	I2	–400	1500	100	0.1°C
End Of Service	Resistance Learning	0x422E	Learn Max Temperature	I2	–400	1500	400	0.1°C
End Of Service	Resistance Learning	0x4230	Learn Target Temperature	I2	–400	1500	250	0.1°C
End Of Service	Resistance Learning	0x4232	Rcell High Temp Coefficient	I2	–32768	32767	0	2^{-16} /0.1°C

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Table 4-5. Data Flash Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
End Of Service	Resistance Learning	0x4234	Rcell Low Temp Coefficient	I2	–32768	32767	0	2^{-16} /0.1°C
End Of Service	Direct Resistance Decision	0x40CD	Initial Rcell	I2	0	32767	0	mΩ
End Of Service	Direct Resistance Decision	0x40CF	Initial Rcell Learned	U1	0	1	0	—
End Of Service	Direct Resistance Decision	0x4239	DRD Alert Level	U2	0	65535	45	%
End Of Service	Direct Resistance Decision	0x423B	DRD Alert Counts	U1	0	255	3	Counts
End Of Service	Direct Resistance Decision	0x423C	DRD Warning Level	U2	0	65535	60	%
End Of Service	Direct Resistance Decision	0x423E	DRD Warning Counts	U1	0	255	3	Counts
End Of Service	Resistance Slope Decision	0x40D0	Initial RRate	I2	0	32767	0	—
End Of Service	Resistance Slope Decision	0x40D2	Initial RRate Learned	U1	0	1	0	—
End Of Service	Resistance Slope Decision	0x423F	RSD Alert Level	U2	0	65535	15	%
End Of Service	Resistance Slope Decision	0x4241	RSD Alert Counts	U1	0	255	3	Counts
End Of Service	Resistance Slope Decision	0x4242	RSD Warning Level	U2	0	65535	30	%
End Of Service	Resistance Slope Decision	0x4244	RSD Warning Counts	U1	0	255	3	Counts
End Of Service	Resistance Slope Decision	0x4245	RSDL Alert Level	U2	0	65535	15	%
End Of Service	Resistance Slope Decision	0x4247	RSDL Warning Level	U2	0	65535	30	%
End Of Service	Safety Status	0x40D3	Warning Status	H1	0x0	0xFF	0x0	Hex

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Factory Calibration

The bq34110 device requires factory calibration. The device performs only a limited number of calibration functions, and the rest of the functions must be performed by a host system using commands provided by the gauge for this purpose. The following sections give a detailed description of the various calibration sequences with the help of flowcharts.

5.1 General I²C Command Information

In the following flowcharts, all I²C functions take three arguments.

Write command arguments:

- Address
- Data
- Wait time in ms

Read command arguments:

- Address
- Number of bytes read
- Wait time in ms

5.2 Calibration Overview

5.2.1 Method

The calibration method is broken up into the following sections. The first four sequences are subroutines to be used in the main calibration sequences.

- Section 5.3, *Enter CALIBRATION Mode*
- Section 5.4, *Exit CALIBRATION Mode*
- Section 5.5, *CC Offset*
- Section 5.6, *Board Offset*
- Section 5.7, *Obtain Raw Calibration Data*
- Section 5.8, *Temperature Calibration*
- Section 5.9, *Voltage Calibration*
- Section 5.10, *Current Calibration*
- Section 5.11, *Floating Point Conversion*

5.2.2 Sequence

Perform the following calibration sequence during battery pack manufacturing process:

1. Perform CC Offset.
2. Perform Board Offset.
3. Perform Temperature Calibration.
4. Perform Voltage Calibration.
5. Perform Current Calibration.
6. Write calibration results to data flash.

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5.3 Enter CALIBRATION Mode

The bq34110 device must be enabled (CE pin pulled high), then the following sequence puts the device in CALIBRATION mode. These steps must be performed when the gauge is in UNSEALED mode.

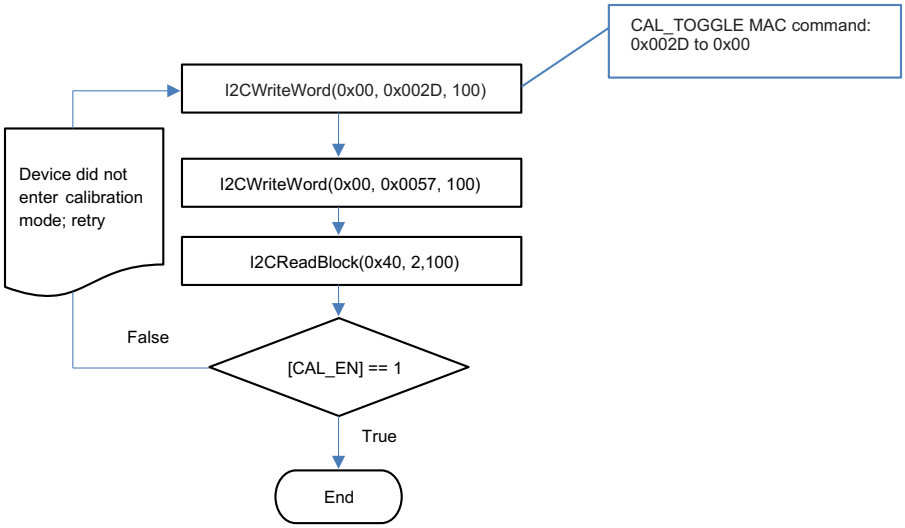

Figure 5-1. Entering Calibration Mode

5.4 Exit CALIBRATION Mode

This sequence takes the gauge out of CALIBRATION mode. These steps must be performed when the gauge is in UNSEALED mode.

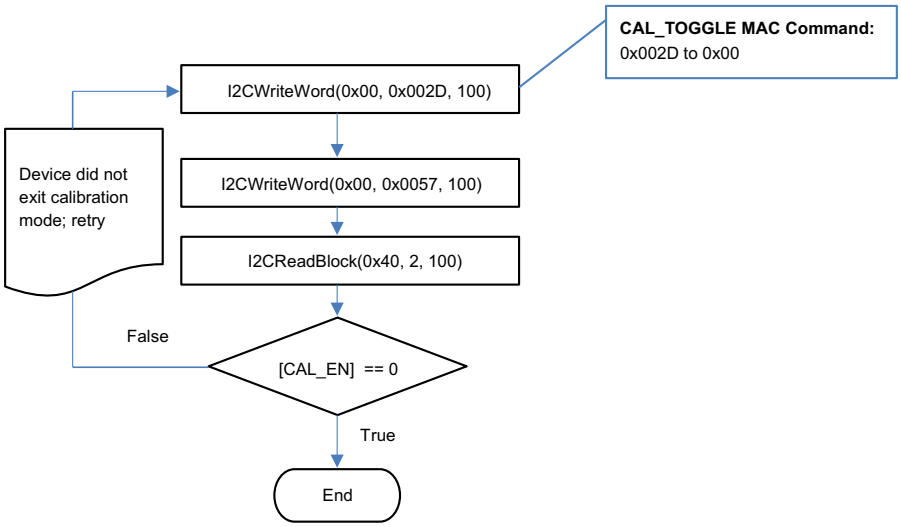

Figure 5-2. Exiting Calibration Mode

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5.5 CC Offset

Use MAC commands for ***CC Offset*** calibration. The host system does not need to write information to the data flash (DF). See *CONTROL_STATUS: 0x0000* for the description of the *CONTROL_STATUS[CCA]* bit. The host system needs to ensure the fuel gauge is UNSEALED.

NOTE: While the device is calibrating ***CC Offset***, the host system must not read the *CONTROL_STATUS* register at a rate greater than once every 0.5 seconds.

The step labeled **Enter CALIBRATION Mode** refers to Section 5.3, *Enter CALIBRATION Mode*.

The step labeled **Exit CALIBRATION Mode** refers to Section 5.4, *Exit CALIBRATION Mode*.

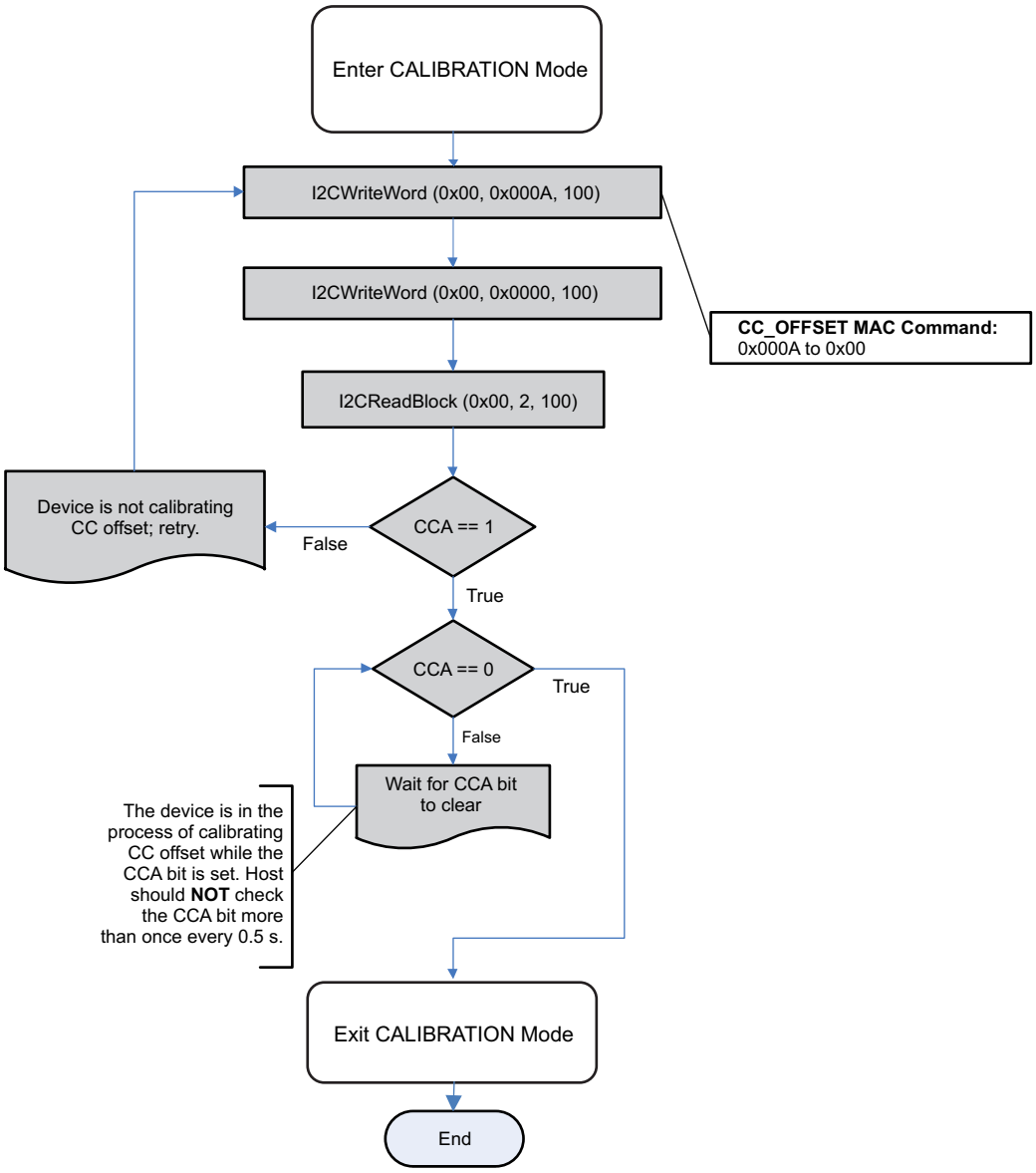

Figure 5-3. CC Offset Flow

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5.6 Board Offset

Use MAC commands for ***Board Offset*** calibration. The host system does not need to write information to the DF. The host system needs to ensure the fuel gauge is UNSEALED. See *CONTROL_STATUS: 0x0000* for the description of the *CONTROL_STATUS[CCA]* and *[BCA]* bits.

Calculating the ***Board Offset*** also calculates the ***CC Offset***; therefore, it is not necessary to go through the ***CC Offset*** calibration process if the ***Board Offset*** calibration process is implemented.

NOTE: While the device is calibrating ***CC Offset***, the host system should not read the *CONTROL_STATUS()* register at a rate greater than once every 0.5 seconds.

The step labeled **Enter CALIBRATION Mode** refers to Section 5.3, *Enter CALIBRATION Mode*.

The step labeled **Exit CALIBRATION Mode** refers to Section 5.4, *Exit CALIBRATION Mode*.

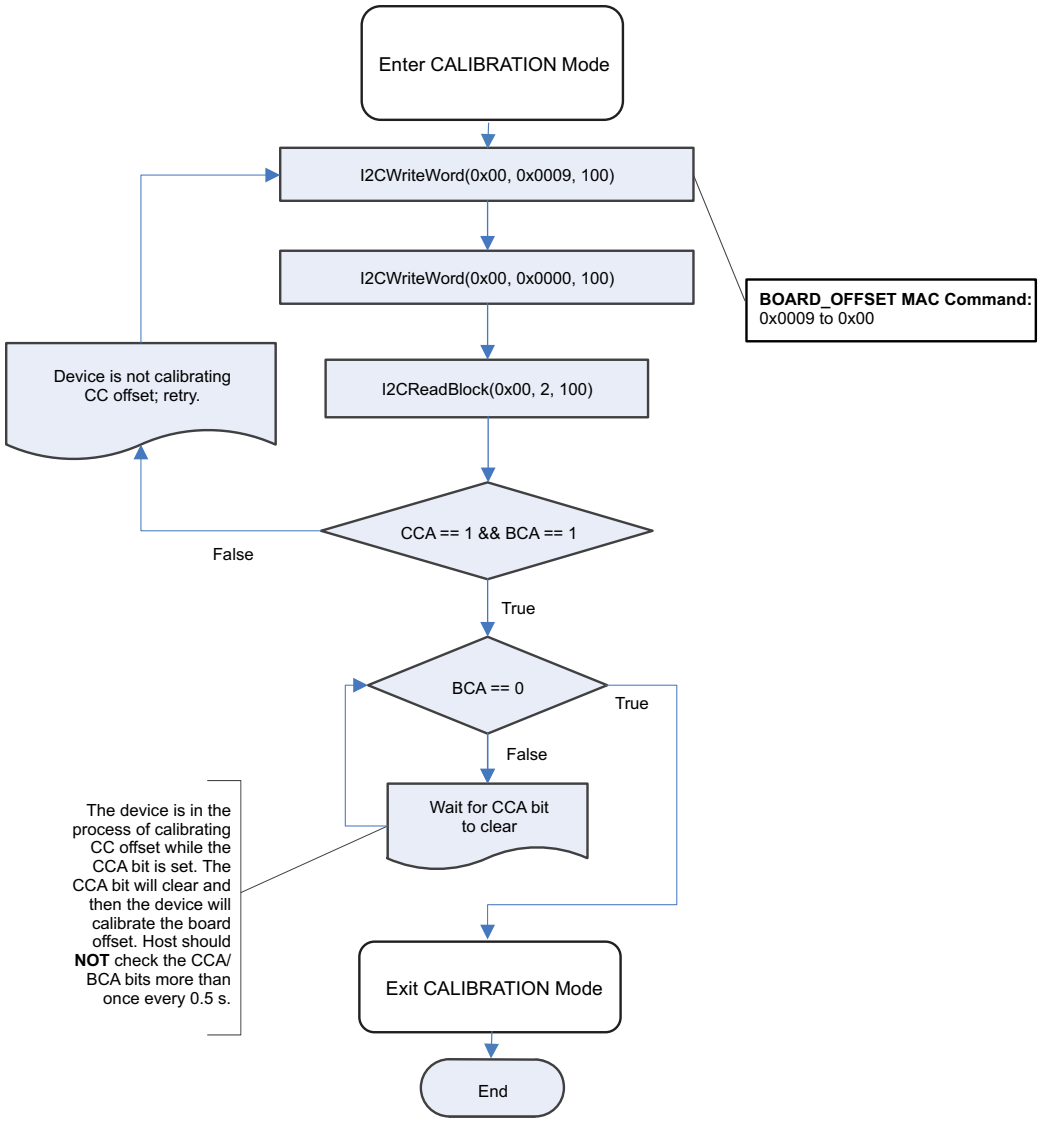

Figure 5-4. Board Offset Flow

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5.7 Obtain Raw Calibration Data

The following flowchart demonstrates how the host system obtains the raw data to calibrate current, voltage, and temperature. The host system uses this flow in conjunction with the current, voltage, and temperature flows described in this chapter. It is recommended that the host system samples the raw data multiple times at a rate of once per second to obtain an average of the raw current, voltage, and temperature. The host system needs to ensure the fuel gauge is UNSEALED.

NOTE: The data provided in *RawCurrent()* at 0x7A/0x7B is indirectly related to the current being measured.

NOTE: The step labeled **Enter CALIBRATION Mode** refers to Section 5.3, *Enter CALIBRATION Mode*.

The step labeled **Exit CALIBRATION Mode** refers to Section 5.4, *Exit CALIBRATION Mode*.

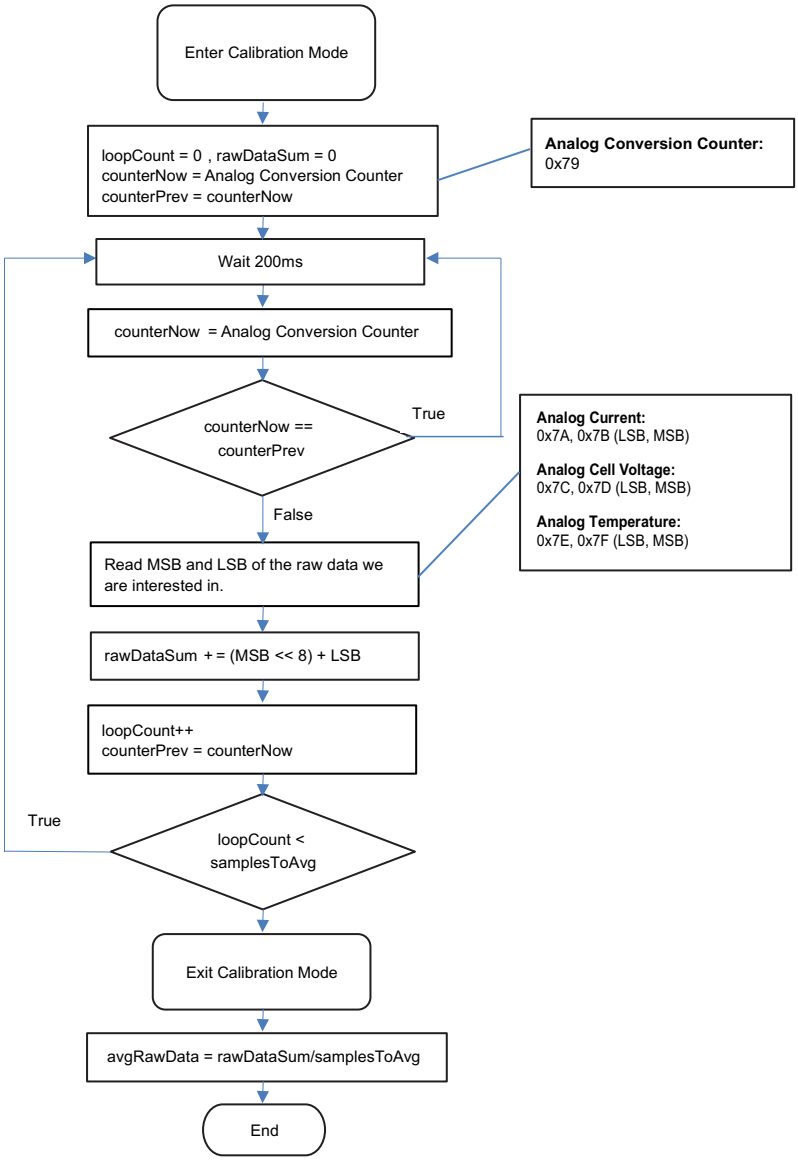

Figure 5-5. Calibration Flow

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5.8 Temperature Calibration

This feature calibrates the temperature source set by ***Operation Config A [TEMPS]***. A known temperature must be applied to the device for temperature calibration. The calculated temperature offset is written to the corresponding location in DF. The temperature offset is represented by an integer that is a single byte in size and can be written to the appropriate location in DF without any intermediate steps. The host system needs to ensure the fuel gauge is UNSEALED.

NOTE: a) The step labeled **Obtain avgRawTemp** refers to *Obtain Raw Calibration Data*.

b) When using bqStudio, ensure that the selected calibration of Internal or External temperature matches the setting on the ***[TEMPS]*** selection.

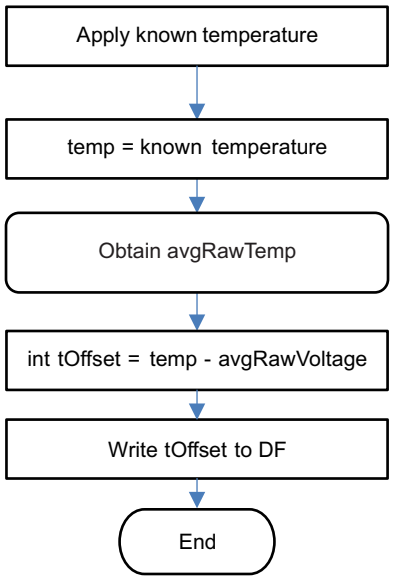

Figure 5-6. Temperature Calibration

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5.9 Voltage Calibration

The bq34110 device has the option to use an external voltage divider circuit to scale the voltage down before it is measured at the BAT pin (see *Voltage Measurement and Calibration* for more details). The gain of this divider network should be calibrated and stored in the ***Voltage Divider*** parameter, as shown in the diagram below. The ***Voltage Divider*** parameter in data flash is represented as an unsigned word with the maximum value 65535, which would represent a divider ratio of 65.536.

Before attempting to write the updated value of ***Voltage Divider***, the bq34110 should be placed into CALIBRATION mode, which disables the restriction of writing to DF when measured *Voltage()* < ***Flash Update OK Voltage***. Otherwise, the device may prevent the update of the new value of ***Voltage Divider***.

NOTE: The step labeled **Obtain avgRawVoltage** refers to *Obtain Raw Calibration Data*.

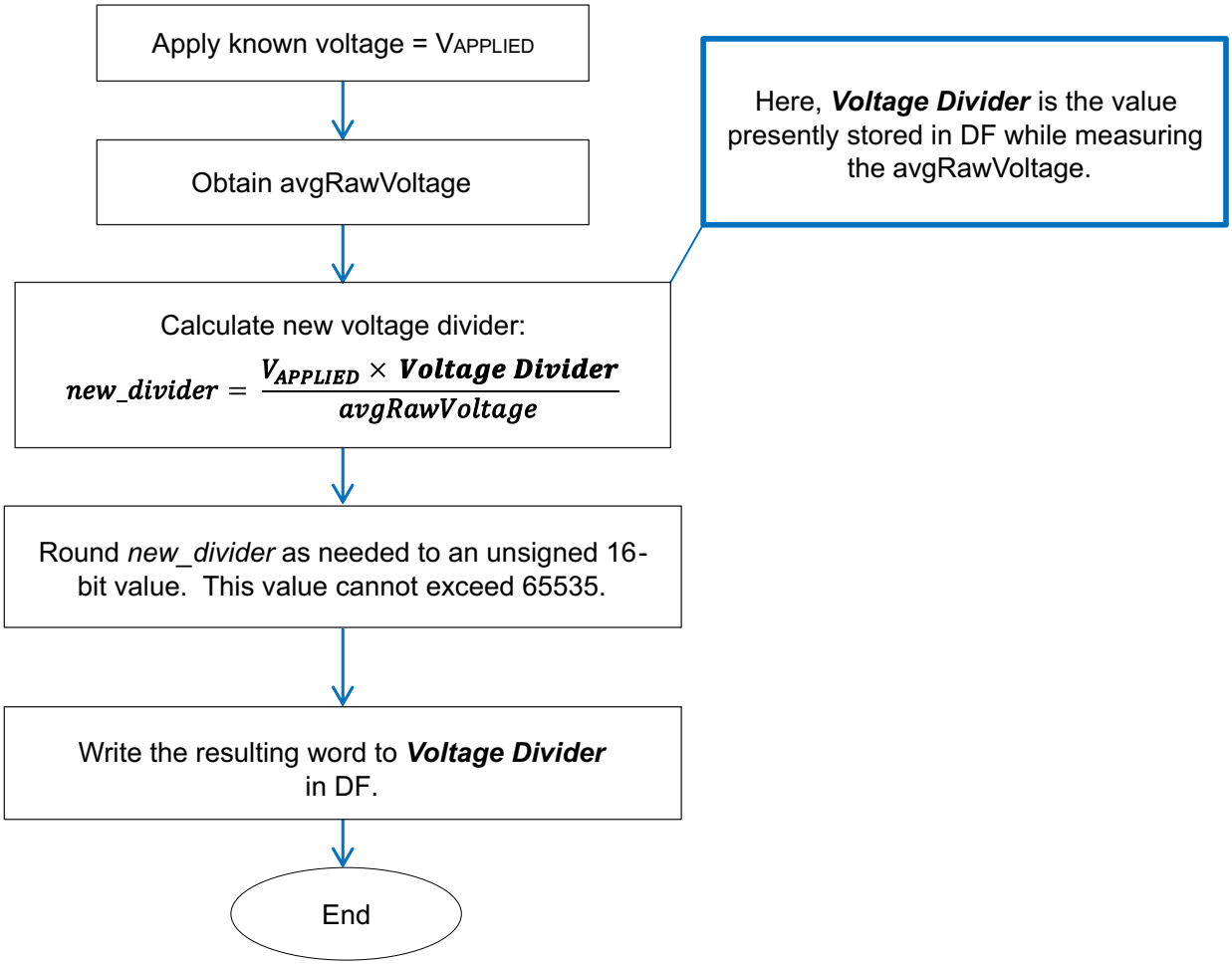

Figure 5-7. Voltage Divider Calibration

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The bq34110 device is default-configured to use the BAT input for voltage measurement, and the data used for calibration is made available through the calibration commands. In this setup, the calculated voltage offset must be written to the corresponding location in DF. The voltage offset is represented by an integer that is a single byte in size and can be written to the DF parameter ***Pack V Offset***. The diagram below shows the steps to calibrate the voltage offset in this case. The host system needs to ensure the fuel gauge is UNSEALED.

NOTE: The step labeled **Obtain avgRawVoltage** refers to *Obtain Raw Calibration Data*.

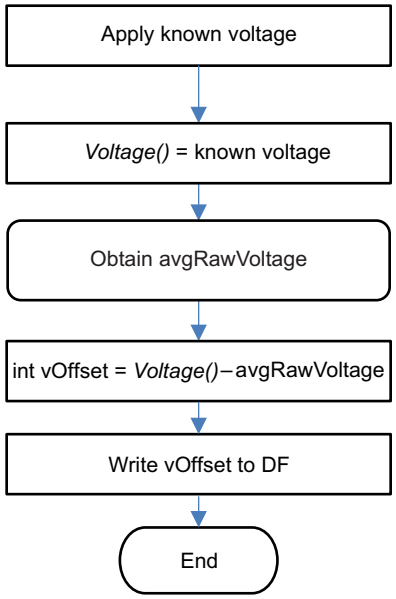

Figure 5-8. Pack Voltage Calibration

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5.10 Current Calibration

CC Gain and ***CC Delta*** are two calibration parameters for current calibration. A known load, typically 1000 mA, is applied to the device during this process. Details on converting the ***CC Gain*** and ***CC Delta*** to floating point format are in *Floating Point Conversion*. The host system needs to ensure the fuel gauge is UNSEALED.

NOTE: The step labeled **Obtain avgRawCurrent** refers to *Obtain Raw Calibration Data*.

The step labeled **Convert ccGain and ccDelta to Gauge's floating point representation and write to DF** refers to *Floating Point Conversion*.

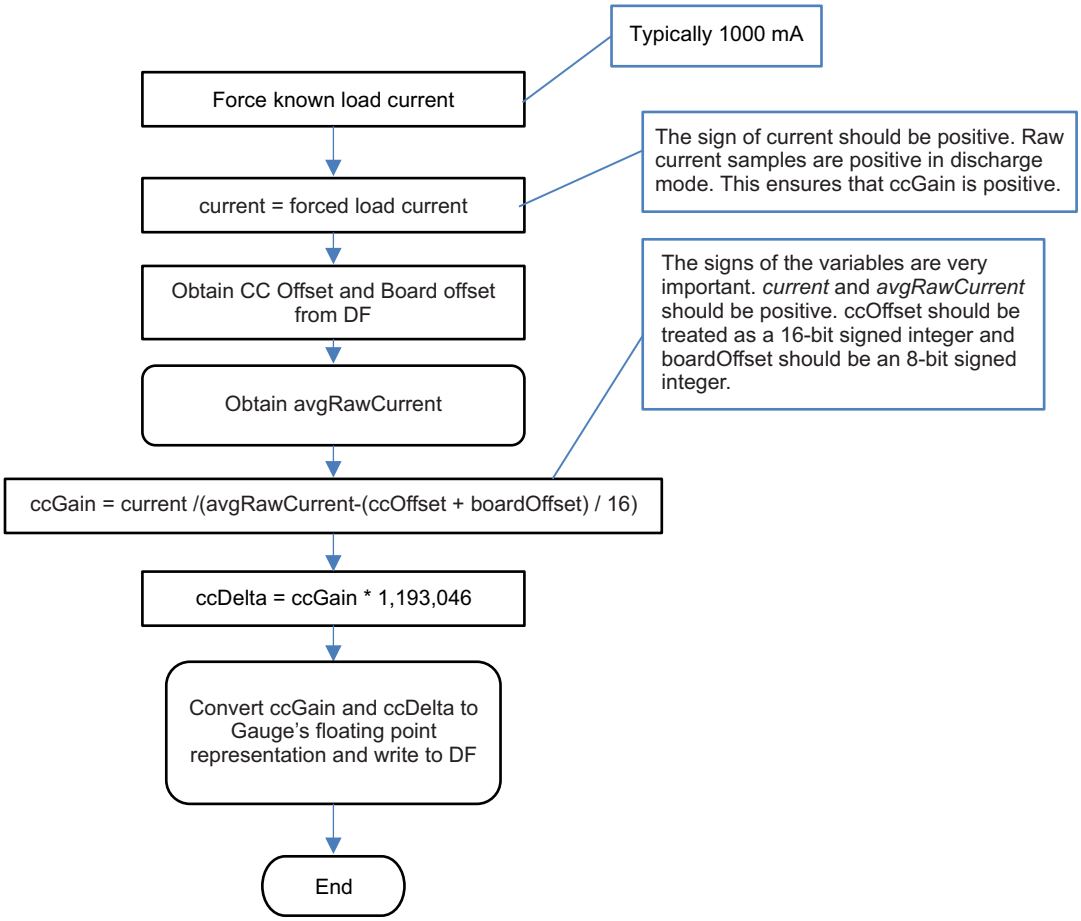

Figure 5-9. Current Calibration

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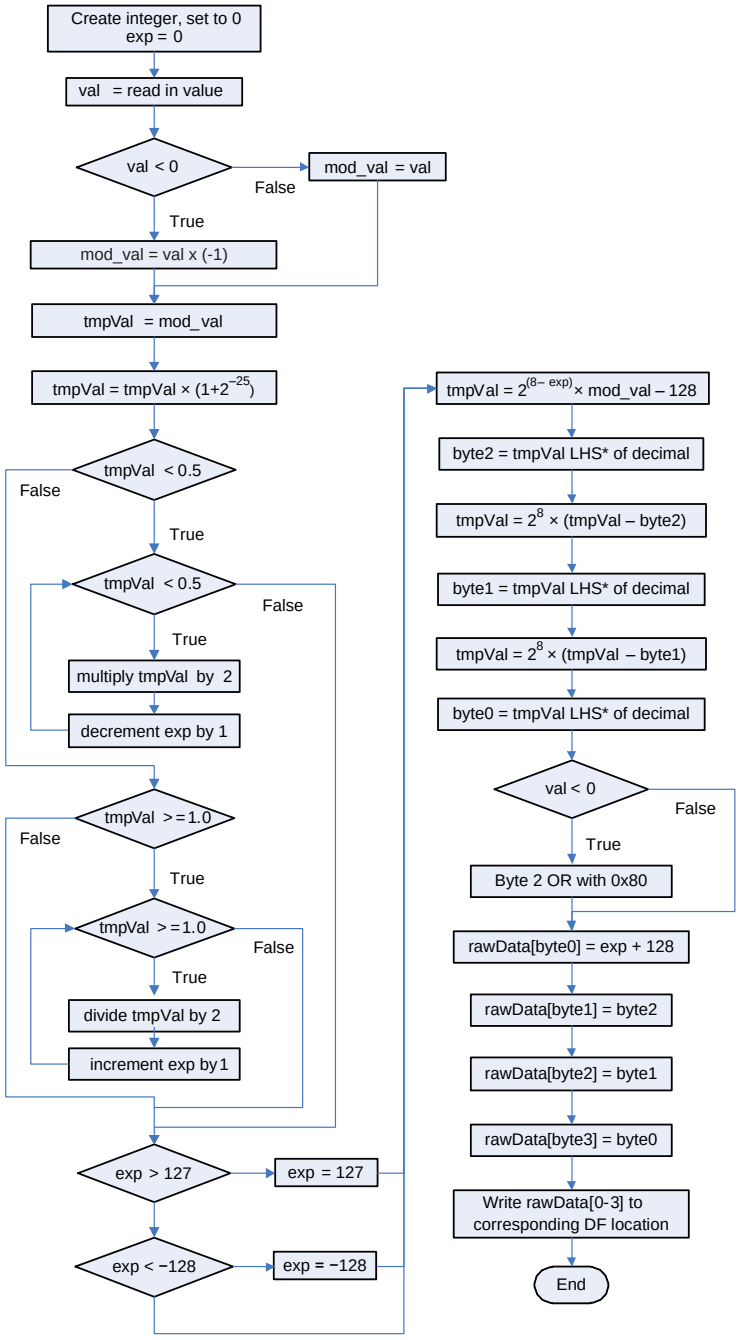
5.11 Floating Point Conversion

Figure 5-10 details how to convert the floating point ***CC Gain*** and ***CC Delta*** values to the format recognized by the gauge.



* LHS is an abbreviation for left-hand side. This refers to truncating the floating point value by removing anything to the right of the decimal point.

Figure 5-10. Floating Point Conversion

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2016) to A Revision **Page**

- Added additional detail on selected bits in ***Operation Config A*** 9
- Added more descriptions regarding voltage divider design and scaling..... 16
- Changed Sleep Time to Sleep Current Time 29
- Changed Bit 5 in high byte from RSVD to RESTORE_REMCAP and added a description 30
- Changed "negative temperature based charging" to "temperature-based charging" 37
- Added description of functionality when ***Cell Negative Delta Voltage*** is set to zero 39
- Changed "pin" to "bit" in some descriptions..... 42
- Changed Bit 1 in *BLTChargSet()* high byte from RSVD to INITCOMP and added a description 81
- Added SOC Flag Config A section, describing additional data flash settings 91
- Added SOC Flag Config B section, describing additional data flash settings 92
- Added captions to figures in Chapter 5..... 102

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