Implementation of an Embedded GPS Receiver Based on FPGA and MicroBlaze

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***Abstract*—A GPS receiver based on FPGA and MicroBlaze was developed. This kind of GPS receiver is made up of a RF Front-End and FPGA, with NemeriX NJ1006A and Xilinx XC2VP30 as its core chips. The RF Front-End chip NJ1006A receives the GPS signal and converts it to IF signal which is transfered to FPGA .The correlators array , C/A code generator,C/A code DCO and carrier DCO were analyzed and designed with Verilog hardware description language on FPGA. The algorithm of acquisition and tracking of GPS signal were discussed and implemented with MicroBlaze soft processor core in XC2VP30 . Meanwhile, the MicroBlaze soft processor core is responsible for communicating with FPGA user logic via the interface named OPB Bus. A parallel correlator using three local replica C/A code was developed and implemented on this FPGA-based GPS receiver, which improved the acquiring efficiency and accuracy of the GPS receiver. The simulation and verification results of the algorithm of GPS receiver are provided. The results demonstrated that the availability and reliability of this kind of design scheme of GPS receiver works well.**

Keywords-Global Positioning System (GPS); FPGA ; MicroBlaze; Parallel correlation; SoC

I. INTRODUCTION

Recently, there are many kinds of design schemes of GPS receivers. Some GPS receivers are designed to be based on GPS chipset solutions provided by some GPS chip corporations. These GPS receivers are implemented by some ways such as using three chips solution[1], two chips solution and single chip solution. For example, the receiver can be composed of ATR0610, ATR0601 and ATR0625,which are produced by Atmel corporation .This is a typical kind of three chips solution. The ATR0610 is a low noise amplifier. The ATR0601 is a down-converter , and the ATR0625 is a base-band processor. Moreover, there are still many solutions using two chips, for example, some system consists of NJ1006A and NJ1030A. The single chip solution can be implemented by NJ1836A .This kind of design scheme is mature and reliable. However ,the developers are not so clearly of the implementation methods of the internal principle and algorithm in the chips. In addition, some GPS receivers also have been designed based on PC[2]. These sorts of GPS receivers are mainly composed of three parts of RF, correlator and PC. The acquisition and tracking software is implemented on PC which works under Windows and C language environments. The RF and correlator parts are mounted on a PCI board that guarantees a link between the PC and the modules. Even though it could track GPS signals and calculate user position in real time successfully, the computational time for the signal acquisition and tracking is still massive for the whole software. In addition to GPS receiver we mentioned above , some GPS receivers have been designed based on FPGA and DSP/ARM. FPGA substitutes the role of the correlator array, C/A generator, carrier DCO and so on. The DSP/ARM controls the C/A code and carrier DCO increment and computes navigation data, then calculates some useful parameters information such as position, velocity, time information and so on. Obviously, it's not very convenient for this kind of design scheme to integrate the whole complicated system onto a single chip. So a design scheme of GPS receiver based on Field Programmable Gate Arrays (FPGA) and MicroBlaze is proposed, which plays both the operation and signal processing role for a full GPS receiver on a single FPGA chip. The design scheme accords with the design method of system on a chip (SoC). Moreover, it is possible to update the GPS algorithm and meet the need of other position systems in the future.

II. SYSTEM DESIGN SCHEME

The hardware devices for the implementation of the GPS receiver based on FPGA and MicroBlaze consists of five parts. A view of the hardware structure of the GPS receiver is shown in Fig.1. The hardware structure includes a RF chip that converts GPS RF signal to one kind of 2-bit digital IF signal The GPS correlation is carried out by Virtex-II^{pro} XC2VP30. MicroBlaze accomplishes the functions including GPS base-band signal processing, C/A code and carrier DCO increment control and computing navigation solutions. MicroBlaze is a soft processor core implemented into XC2VP30. OPB Bus is adapted as an interface protocol between the correlator and MicroBlaze soft processor core. A SRAM with 64Mbytes is used to store temporary data information, while a Flash chip with 32Mbytes is used to store program and almanac data and so on. Some external port modules including serial port and debug port are used to communicate with other devices.

The decision to adapt this kind of FPGA and MicroBlaze is mainly driven by the powerful capability of computational processing, and the capability of signal processing and mathematical computation are offered by MicroBlaze soft processor core implemented in FPGA XC2VP30. Moreover, it is possible to meet both updating GPS signal processing algorithm and maintaining the mostly same hardware except the RF module for different receiver specifications, for

example, designing hybrid GPS/Galileo receiver and dual frequency GPS receiver. Most important of all, it is possible and convenient to implement an ASIC design on the basis of FPGA in the future. In addition, all functions integrated on a single chip is proved to develop the capability of anti-interfere and reduce power consumption of the whole system.

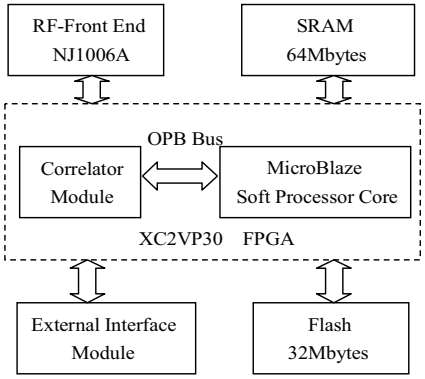


Figure.1 Hardware system structure block diagram

III. RF Front-End Design

The NEMERIX NJ1006A RF chip is adopted as GPS receiver RF Front-End IC[3]. NJ1006A receives GPS RF signal, and converts RF signal to IF signal ,which is sampled. The ADC in NJ1006A converts IF signal to 2-bit digital output: sign and magnitude, that is SGN and MAG. In the design, the chip's frequency plan is suggested that the reference frequency is about 16.367MHz. The IF signal frequency is 4.188MHz,and the sampling frequency for IF signal is about 5.714MHz . According to the design, the output of the NJ1006A: 2-bit digital signal and CP (clock signal) are connected with the base-band processor. The RF chip can be connected to many GPS base-band chips or software GPS processors such as NJ1030A , NJ2020 and so on.

IV. Implementation of GPS Digital Base-band Channel

A typical architecture about each digital base-band channel is shown in Fig.2.As shown in Fig.2, the digital base-band channel mainly consists of local carrier DCO，local C/A code generator, integrate & dump register and correlator array[4][5]. The digital IF signal from RF Front-End module is directly sent to the digital base-band channel, which multiplies them using the local generated sine and cosine signal which replicate the input carrier. The local carrier DCO generates the in-phase and in-quadrature streams. In order to be conveniently described below, subscript 'I' is referred to as an in-phase component, while subscript 'Q' is referred to as an in-quadrature component. The samples on these branches should be correlated with the early code, prompt code and late code generated by local C/A code generator. Then, there are totally six correlation values, and they'll be integrated and dumped every correlation period. Finally, the results are sent to MicroBlaze soft processor core where all operations including discriminator, carrier phase and C/A code phase increment control and computing navigation solutions and so on are implemented.

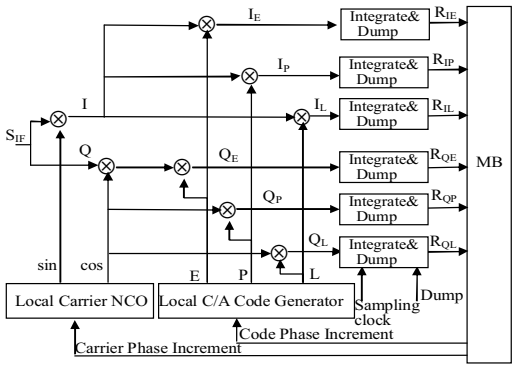


Figure.2 Digital Base-band Structure Block Diagram

A. *Verilog implementation of the correlator*

The base-band processing part is designed onto Xilinx XC2VP30 using Verilog hardware description language. At present, all the correlator chips are required to have the function of acquisition and tracking twelve different satellites simultaneously. In order to verify some key algorithm before implementing the entire GPS receiver and each channel has the same architecture, a single channel GPS receiver has been implemented in this design yet.

One channel correlator was implemented with Verilog language. RTL schematic circuit diagram of the correlator is shown in Fig.3. Fig.4 shows the data simulation result of the accumulator&dump register for the correlator.

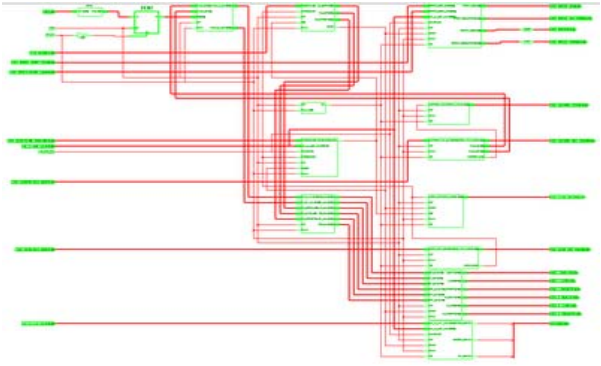


Figure.3 RTL schematic circuit diagram of the correlator

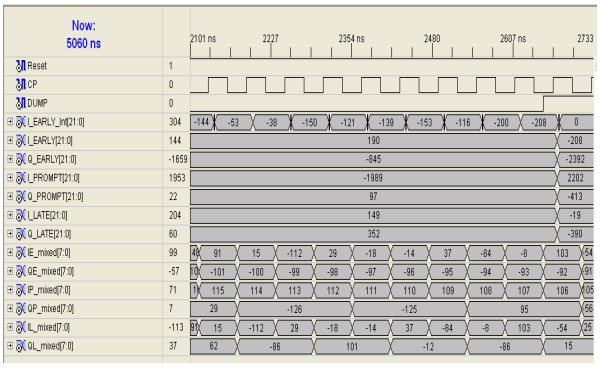


Figure 4. Accumulator&Dump register simulation results

B. Local carrier generator and carrier DCO

The part consists of sine, cosine Look–Up Table(LUT) and Digital controlled oscillator (DCO). The LUT gives four values±1, ±3 and eight phase values, which are used to form the sine and cosine output .The carrier DCO, which is clocked at the CP clock signal frequency, is used to synthesize the local digital oscillator signal which is required to convert the input signal to base-band signal in the carrier mixed block. Moreover, because of the Doppler shift and the reference frequency error，the carrier DCO must be adjusted automatically and continuously to synchronize with the carrier frequency of the input signal . RTL schematic circuit diagram of the carrier DCO is shown in Fig.5, and Fig.6 shows the data simulation result of the carrier DCO for the correlator.

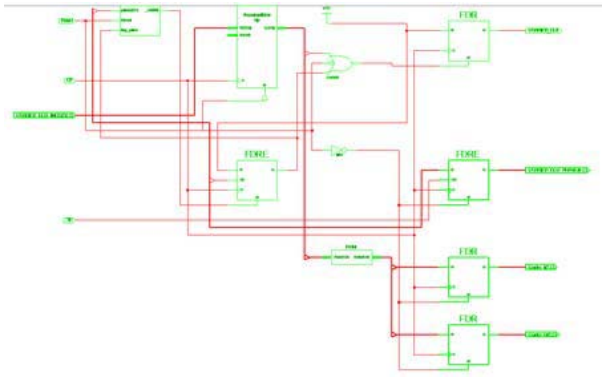


Figure.5 RTL Schematic circuit diagram of carrier DCO

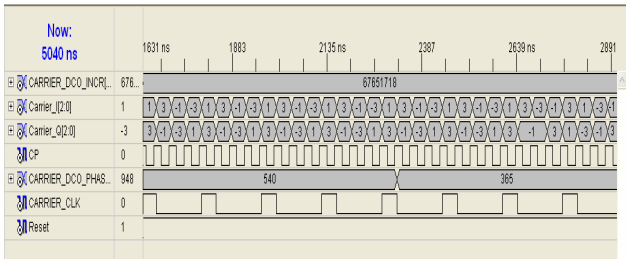


Figure.6 Carrier DCO simulation result

C. GPS Signal Analyse

The received GPS signal can be written as:

$$s(t) = D(t-\tau)C(t-\tau)\sqrt{2P(t-\tau)}\sin[2\pi f_c t + \phi] + n(t) \quad (1)$$

Where D(t) is the data waveform, C(t) is the pseudorandom noise(PRN) code, fc is the carrier frequency, n(t) is the noise interfering signal. P(t) is the signal power. τ is the signal transmitted delay. ϕ is Doppler phase shift.

In order to analyze the signal processing conveniently, the signal transmitted delay (τ) and n(t) are temporarily ignored. Thus, (1) can be expressed as the following formula.

$$s(t) = D(t)C(t)\sqrt{2P(t)}\sin[2\pi f_c t + \phi] \quad (2)$$

The received signal is converted to IF through RF mixer, then is sampled according to the sampling clock. Thus, the digital IF can be described as the following formula[6]. In order to be described conveniently, only continuous signal formula is expressed below.

$$s_{IF}(t) = C(t)\times D(t)\sqrt{2P(t)}\times\sin(\omega_{IF} t + \phi) \quad (3)$$

The local replica carrier signal is as follows:

In-phase phase: $U_{I_L} = \sin(\omega_0 t + \varphi_0)$

Quadrature phase: $U_{Q_L} = \cos(\omega_0 t + \varphi_0)$

Therefore, correlation output is

$$\begin{aligned} U_I &= s_{IF}(t)\times\sin(\omega_0 t + \varphi_0) \\ &= C(t)\times D(t)\times\sqrt{2P(t)}\times\sin(\omega_{IF} t + \varphi)\times\sin(\omega_0 t + \varphi_0) \\ &= -\frac{1}{2}C(t)\times D(t)\times\sqrt{2P(t)}\times[\cos((\omega_{IF}+\omega_0)t + \varphi + \varphi_0) \\ &\quad -\cos((\omega_{IF}-\omega_0)t + \varphi - \varphi_0)] \\ U_Q &= s_{IF}(t)\times\cos(\omega_0 t + \varphi_0) \\ &= C(t)\times D(t)\times\sqrt{2P(t)}\times\sin(\omega_{IF} t + \varphi)\times\cos(\omega_0 t + \varphi_0) \\ &= \frac{1}{2}C/A(t)\times D(t)\times\sqrt{2P(t)}\times[\sin((\omega_{IF}+\omega_0)t + \varphi + \varphi_0) \\ &\quad +\sin((\omega_{IF}-\omega_0)t + \varphi - \varphi_0)] \end{aligned}$$

After the signal U_I and U_Q are filtered by lowpass , then, the output base-band signal can be expressed as follows:

$$U_Q = \frac{\sqrt{2P(t)}}{2}C(t)\times D(t)\times\sin((\omega_{IF}-\omega_0)t + \varphi - \varphi_0)$$

When the U_I and U_Q signal is synchronized through acquisition and carrier tracking ,which includes frequency and phase, ω_{IF} and φ are respectively equal to ω_0 and φ_0 .Therefore, the output signal is described as the following :

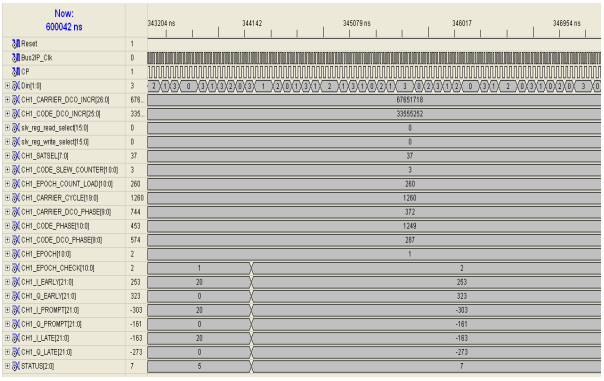
$U_I = \frac{\sqrt{2P(t)}}{2}D(t)$, that is the navigation data.

V. MicroBlaze Soft Processor Core

MicroBlaze is an embedded soft RISC processor with 32-bit data and addresses bus. The processor is optimized for implementation in XILINX FPGAs, and supports both on-chip BlockRAM and external memory. Meanwhile, it supports some peripherals and interface .Because of these advanced features, all the functions related the GPS receivers can be implemented on a single FPGA. In addition, some soft peripheral IP can also be provided by Xilinx .User can use them for designing FPGA-based embedded processor system conveniently. At the same time ,according to the need of the application of the specific system, custom IP can be created and added to the application system by yourself.

The MicroBlaze processor in the GPS receiver performs many different operations and tasks which can be summarized as the following：1) interfacing the custom IP;2)controlling and managing the acquisition and tracking phase increment;3) computing navigation solutions and sending out position, velocity and time information and so on.

In the design, a custom IP for correlator is designed and applied to our system. The custom IP mainly accomplishes all the function of the correlator and data transmission between FPGA user logic and MicroBlaze processor. Fig.7 shows the data transmission simulation result between the FPGA user logic and MB.



Figrue.7 Data transmission between FPGA and MB

Some algorithms including managing the acquiring and tracking and calculating navigation solutions are implemented by MicroBlaze[7][8]. Thus, GPS receiver can accomplish the tasks of acquisition of the satellites and tracking of the acquired code and carrier,and send out the navigation information such as position,velocity,time and so on[9][10]. The software program flow diagram is shown in Fig.8.

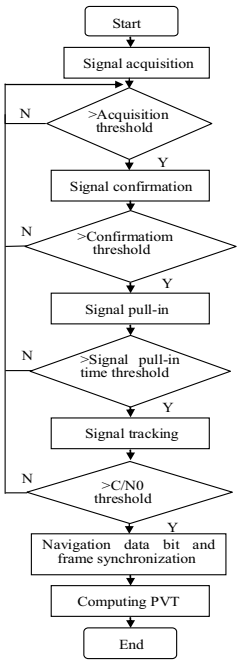


Figure.8 Software flow diagram of acquiring and tracking

VI. Conclusions

In this paper, the status of the design of GPS receiver has been discussed. The design and implementation of a GPS receiver based on FPGA and MicroBlaze have been discussed in detail, and all the modules of the correlator have been studied and simulated. The local C/ A code loop generates three outputs: the early code, the late code, and the prompt code. Using the three output , the parallel correlation has been developed and improved the acquiring performance of efficiency and accuracy of the GPS receiver. The acquisition and tracking algorithms of GPS receiver have been analyzed and data transmission between FPGA user logic and MicroBlaze processor through OPB Bus has been implemented and verified. This kind of design scheme of the GPS receiver based on FPGA and MicroBlaze can meet the need of updating GPS signal processing algorithm and implementing ASIC design on the basis of FPGA in the future. Furthermore, the SoC design can also develop the capability of anti-interfere and the reduction of power consumption.

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