

ECE241 Midterm 2025



Class scores distribution [Show](#)

My score

39.4% (31.5/80)

Q1

9

-|



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[10 marks] 1. Number Representation

[2 marks] (a) Convert the following decimal numbers to 12-bit binary:

i. 197 1100...0101.....

ii. 2049 1100...0000 0001.....

[2 marks] (b) Convert the following binary to hexadecimal

i. 101100101100 82C.....

ii. 010110010111 597.....

[2 marks] (c) Convert the following hexadecimal to 12-bit binary

i. 241 0010 0000 0001

ii. ECF 1110 1100 1111

[2 marks] (d) Convert the following binary to decimal

i. 00101101 45.....

ii. 01000001 65.....

$$\begin{array}{r} 64 \\ \downarrow \\ 1 \end{array}$$

$$\begin{array}{r} 32 \\ \times \\ 8 \\ \hline 24 \end{array}$$

$$\begin{array}{r} 16 \\ \times \\ 4 \\ \hline 4 \end{array}$$

$$\begin{array}{r} 8 \\ \times \\ 4 \\ \hline 4 \end{array}$$

[2 marks] (e) What is the minimum number of bits needed to represent the result from the addition of one 8-bit number and four 6-bit numbers?

$$\begin{array}{r}
 \text{9 bits} \\
 \text{needed} \\
 \hline
 \begin{array}{r}
 \overbrace{}^8 + \overbrace{}^6 \\
 \quad \overbrace{}^6 \\
 \hline
 \quad \overbrace{}^6
 \end{array}
 \end{array}$$

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Q2a

2

[6 marks] 2. Boolean Algebra

[2 marks]

- (a) Minimize the following expression using Boolean algebra. The minimized result should be in the sum-of-products (SOP) form. Show all your work and label the rules/identities used. There is an Aid Sheet at the end of this exam.

$$ab + a\bar{b}c + \bar{a}bc + \bar{a}\bar{b}c$$

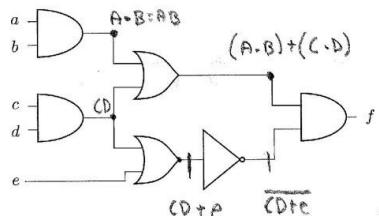
$$\begin{aligned} & ab + a(b+\bar{b}c) + \bar{a}c(b+\bar{b}) \rightarrow \text{Factoring} \\ & = ab + a\bar{b}c + \bar{a}c \rightarrow ab \\ & = ab + ac + \bar{a}c \\ & = ab + c(a+\bar{a}) \rightarrow \text{Factoring} \\ & = ab + c \rightarrow ab. \end{aligned}$$

[4 marks]

- (b) Derive the minimal sum-of-products (SOP) expression for the logic circuit shown below using Boolean algebra. Show all steps and label rules/identities used.

Q2b

2



$$F = (A \cdot B) + (C \cdot D) + (\overline{C} \cdot \overline{D} \cdot e)$$

$$F = (AB + CD) + (\overline{C}D + \overline{e}) \rightarrow 15b.$$

$$F = AB\overline{C}\overline{D} + AB\overline{e} + \overline{C}\overline{D}\overline{e} \quad \text{DeMorgan's use incorrect -1}$$

$$F = AB(\overline{C} + \overline{e}) + \overline{C}\overline{D}\overline{e}$$

Page 3

$$F = AB(\overline{C}\overline{D}\overline{e}) + \overline{C}\overline{D}\overline{e} \rightarrow 15a$$

$$F = AB(CD) + \overline{C}\overline{D} \rightarrow 1$$

$$F = AB(CD) + \overline{C}\overline{D} \rightarrow 1$$

$$F = \overline{C}(e + \overline{e}) \rightarrow 1$$

$$F = \overline{C}\overline{D}\overline{e} + ABCD$$

Final
answer
incor-
rect
(abce +
abde) -1



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Q3a

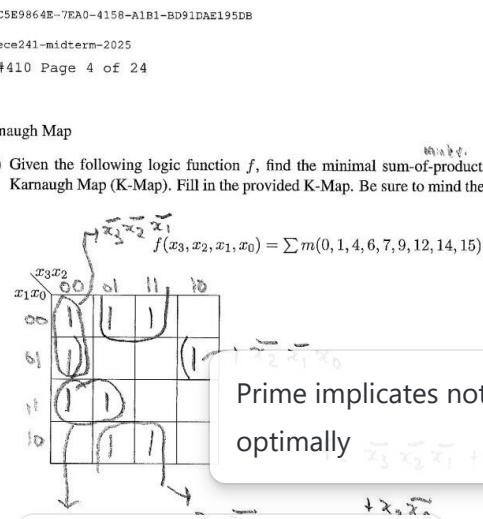
1

[6 marks] 3. Karnaugh Map

[4 marks]

- (a) Given the following logic function f , find the minimal sum-of-products (SOP) form using a Karnaugh Map (K-Map). Fill in the provided K-Map. Be sure to mind the ordering of variables.

x_3x_2	x_2x_1	x_1x_0	$x_3x_2x_1x_0$	f
0 0 0 0	0	1	0 0 0 0	1
0 0 0 1	0	1	0 0 0 1	1
0 0 1 0	0	1	0 0 1 0	1
0 0 1 1	0	1	0 0 1 1	1
0 1 0 0	0	1	0 1 0 0	1
0 1 0 1	0	1	0 1 0 1	1
0 1 1 0	0	1	0 1 1 0	1
0 1 1 1	0	1	0 1 1 1	1
1 0 0 0	1	0	1 0 0 0	1
1 0 0 1	1	0	1 0 0 1	1
1 0 1 0	1	0	1 0 1 0	1
1 0 1 1	1	0	1 0 1 1	1
1 1 0 0	1	1	1 1 0 0	1
1 1 0 1	1	1	1 1 0 1	1
1 1 1 0	1	1	1 1 1 0	1
1 1 1 1	1	1	1 1 1 1	1

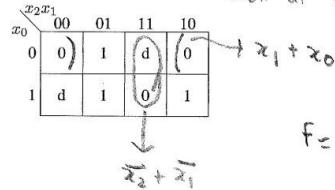


K-map filled in incorrectly -1

Final expression incorrect -1

- (b) Given the following K-Map, find the minimal product-of-sums (POS) form of the logic function $f(x_2, x_1, x_0)$. Note: you are required to provide POS form (not SOP form).

Look at 0's



$$f = (x_1 + x_0)(\bar{x}_2 + \bar{x}_1)$$

Correct 2

Page 4

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[8 marks] 4. Product-of-Sums / NOR Gates

The following truth table is for the majority function. a, b, c are inputs; f is the output. This is the function for C_{out} in a full adder.

c	a	b	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

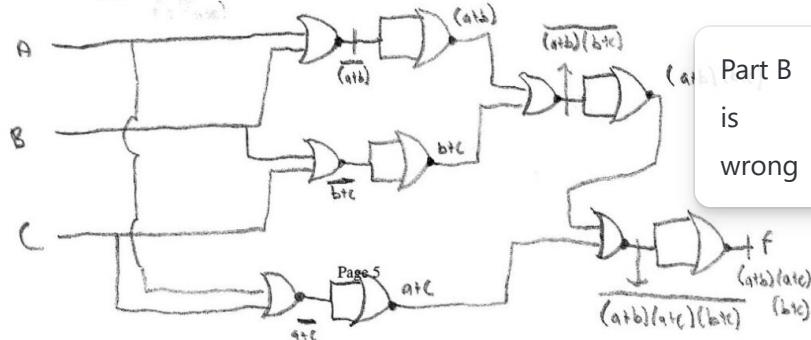
[4 marks]

- (a) Show the function in minimized product-of-sums (POS) form. Use any approach to minimize the function.

$$f = (a+c)(\bar{a}+b)(\bar{b}+c)$$

[4 marks]

- (b) Provide a gate-level schematic for the function using only 2-input NOR gates. Label each wire in your schematic with its corresponding logic function. Unclear schematics will receive reduced marks.



Q4 4



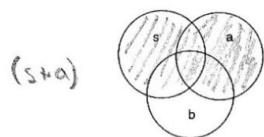
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Q5

1

- [6 marks] 5. Venn Diagram Proof
Use Venn diagrams to prove or disprove that $(s + a)(\bar{s} + b) = \bar{s}a + sb$. Show your work using the figures below for full marks.

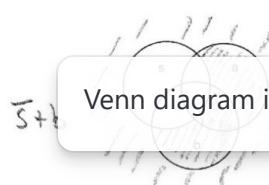
left-hand side



right-hand side



Venn diagram incorrect -1



Venn diagram incorrect -1



Venn diagram incorrect -1

$$(s+a)(\bar{s}+b)$$

Venn diagram incorrect -1

Venn diagram incorrect -1

$$(s+a)(\bar{s}+b) = sa + sb$$

\therefore not true

$$(s+a)(\bar{s}+b)$$

$$= sb + \bar{s}a + ab$$

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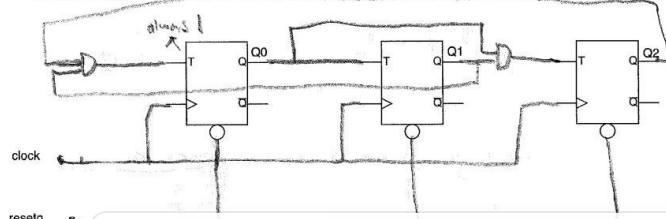
Q6

1

[5 marks] 6. Counter Design Question

Consider the following partial circuit with three T flip-flops. You must complete the circuit by adding additional logic gates and wires so that it implements an up-counter that counts from 0 to 5, i.e. $Q_2Q_1Q_0 = 000, \dots, 101$, and then stops counting (remains at $Q_2Q_1Q_0 = 101$). The *resetn* input is an active-low asynchronous reset that causes $Q_2Q_1Q_0$ to reset to 000.

You may use any logic gates you have learned about in this course. Unclear schematics may receive reduced marks.



101 detection circuitry incorrect /
missing. -2

FF,Q1 input incorrect / missing. -1

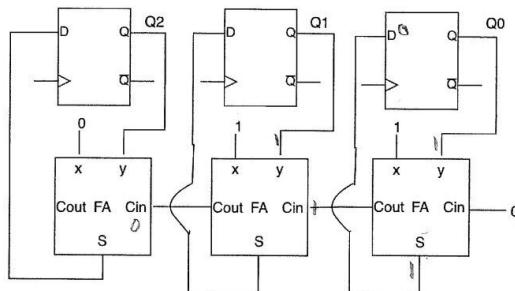
FF,Q2 input incorrect / missing. -1



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[12 marks] 7. Storage Elements

- [5 marks] (a) Consider the following circuit with three D-type flip-flops and three full adders (FAs). Assuming that the flip-flop outputs are initially all zero. Give the values of Q_2, Q_1, Q_0 for the next 8 clock cycles. Just use text for your answer, as in 000, ...,



Q7a/b

0

Answer: 000, 001, 010, 011, 100, 101, 110, 111

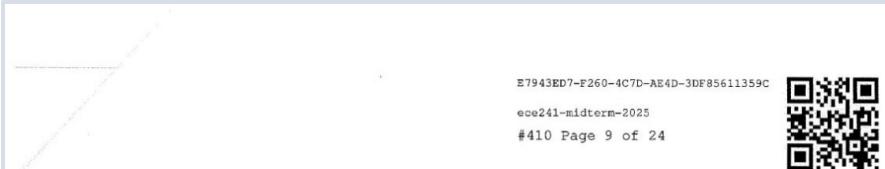
completely incorrect sequence -5

- [1 mark] (b) In one sentence, describe the output sequence produced by the above circuit.

Answer: Shift register

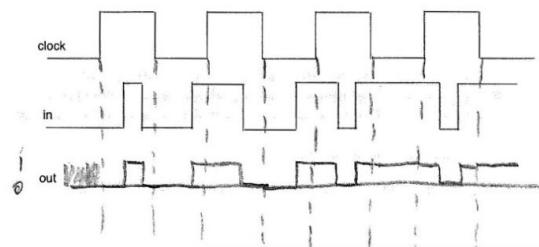
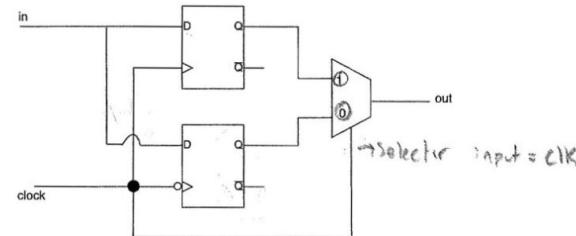
incorrect description -1

Q7c



[6 marks]

(c) Complete the timing diagram for the circuit below. Assume the values stored in both flip-flops are unknown before the first rising clock edge.



6x Incorrect value at rising/ falling edge

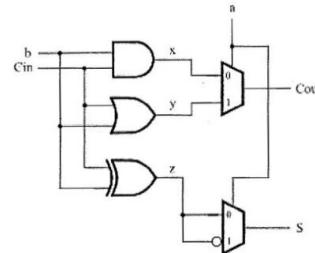
-6



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[12 marks] 8. Adder question

(a) The figure below gives a circuit that implements a full adder using logic gates and multiplexers.



[3 marks]

- i. In the space provided on the following page complete Verilog code for the full adder that corresponds to this circuit structure. The module and signal definitions are given below as a starting point. Use **if-else** statements to specify the multiplexers in your code.

... put your answer on the next page.

Page 10

Q8ai 3

Answer:

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```
module FA (a, b, Cin, s, Cout);
    input a, b, Cin;
    output reg s, Cout;
    wire x, y, z;
    assign x = b & cin;
    assign y = b | cin;
    assign z = b ^ cin;

    always @(*) begin
        if (a == 0)
            Cout = x;
        else
            Cout = y;
        s = z;
    end
endmodule
```

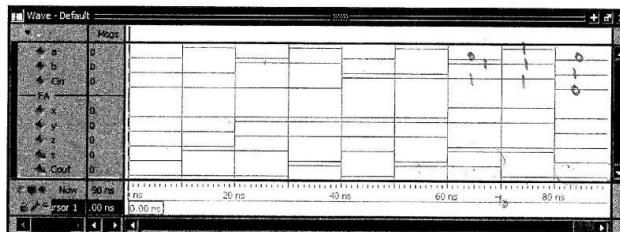
Page 11



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[3 marks]

- ii. If you performed a ModelSim simulation of your Verilog code, it would work perfectly (for sure!). But assume now that this question is part of a lab exercise and your lab partner, who is not as prone to perfection as yourself, has simulated their Verilog code using ModelSim and shared the simulation results with you. Your task is to determine if your partner's Verilog code produces a correct result in all cases. Those simulation results, for your lab partner's Verilog code, are given below.



Q8aii

1

Answer the following two questions.

Does your partner's simulation result show a correct implementation of the full adder circuit for all input valuations? If not, which input valuations are incorrect?

Answer: At 80ns, S is wrong. To ns, Cout=1. At 60ns, S is n

Wron

correctly identified simulation was incorrect

1

Being as specific as possible, what do you think is wrong in your partner's Verilog code?

Answer: Their boolean logic expressions for Cout and S are not correct

Page 12



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- (b) In Lab 2, you implemented a circuit that could add two BCD digits and display the two-digit result on the 7-segment displays HEX1 and HEX0.

For this question you are to solve a similar problem, but for a circuit that can add two BCO digits, where BCO means *Binary Code Octal*. Thus, your circuit produces the result:

$$S = X + Y + C_{in},$$

where S is a two-digit base-8 result, X and Y are base-8 numbers and C_{in} is a carry-in. The maximum size of the result is $S = 7 + 7 + 1 = (17)_8$.

[2 marks]

Q8bi

0

- i. Fill in the table below to show what digits should be shown on HEX1 and HEX0 for each possible result S .

Convert binary to octal

Result	HEX1	HEX0
0000	0	0
0001	0	1
0010	0	2
0011	0	3
0100	0	4
0101	0	5
0110	0	6
0111	0	7
1000	0	8
1001	0	9
1010	1	0
1011	1	1
1100	1	2
1101	1	3
1110	1	4
1111	1	5

0000 0000

0001 0001

HEX1 column incorrect
for some result value(s). **-1**

HEX0 column incorrect
for some result value(s). **-1**



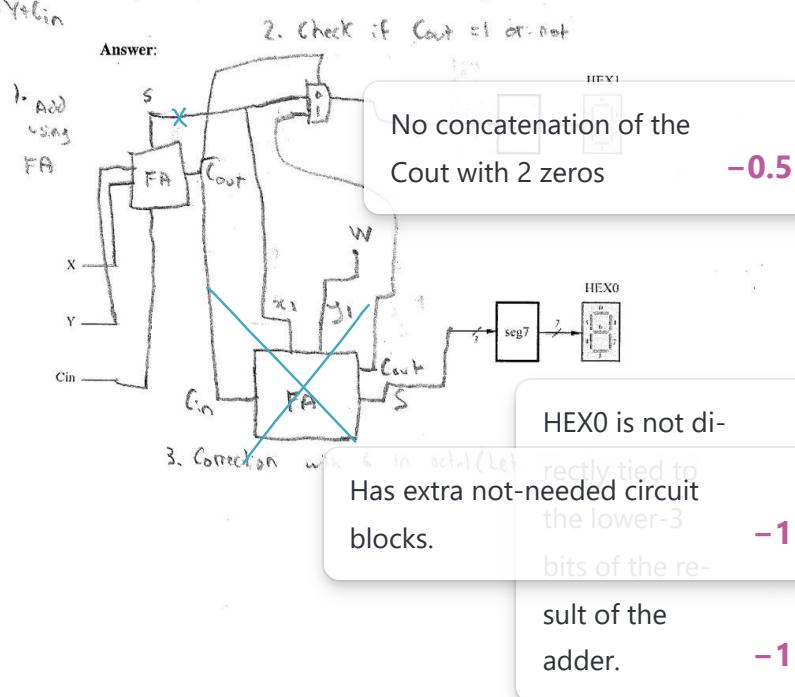
C15D3CFE-D2E4-4E1A-A35E-1EA6FBAA2C2B
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[4 marks]

- ii. In the space below complete the design of your circuit that produces the 2-digit octal sum $S = X + Y + C_{in}$. You can use any needed logic gates or multiplexers, an n -bit adder module (you do not need to show the design of the adder; just draw it as a symbol with inputs and outputs). You do not need to design the 7-segment decoder that is shown in the partial circuit diagram below. In your solution, draw all lines and symbols clearly, and label all key features; marks will be deducted for unclear drawings.

Q8bii

1.5



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[15 marks] 9. Verilog question

[2 marks]

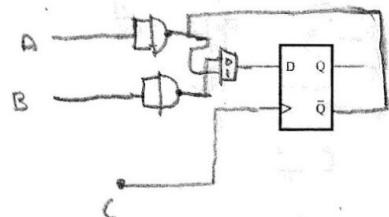
- (a) Consider the Verilog module given below. Complete the logic circuit below so that it correctly implements this Verilog code. You should make use of 2-to-1 multiplexers where appropriate, and can also include other logic gates as needed. Marks will deducted for messy circuits, so keep your circuits as simple as possible and draw carefully.

```
module TFF (A, B, C, Q);
    input A, B, C;
    output reg Q;
    always @(posedge C)
        if (B == 0)
            Q <= 1'b0;
        else if (A == 1)
            Q <= ~Q;
endmodule
```

Answer:

Q9a

0



B sync. reset logic incorrect / missing. -1
A toggle logic incorrect / missing. -1



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[4 marks]

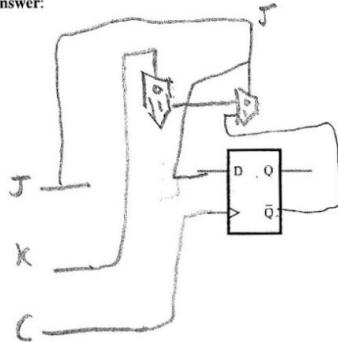
- (b) Consider the Verilog module given below. Complete the logic circuit below so that it correctly implements this Verilog code. You should make use of 2-to-1 multiplexers where appropriate, and can also include other logic gates as needed. Marks will deducted for messy circuits, so keep your circuits as simple as possible and draw carefully.

```
module JKFF (J, K, C, Q);
    input J, K, C;
    output reg Q;
    always @ (posedge C)
        if (K)
            if (J)
                Q <= ~Q;
            else
                Q <= 1'b0;
        else
            if (J)
                Q <= 1'b1;
endmodule
```

Answer:

Q9b

4



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[4 marks]

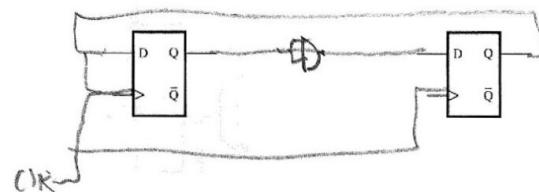
- (c) Consider the Verilog module given below. Complete the logic circuit below so that it correctly implements this Verilog code. You should make use of 2-to-1 multiplexers where appropriate, and can also include other logic gates as needed. Marks will deducted for messy circuits, so keep your circuits as simple as possible and draw carefully.

```
module SR (W, X, Y, Z, R, C, Q);
    input W, X, Y, Z, C;
    input [1:0] R;
    output reg [1:0] Q;

    always @ (posedge C)
        if (!Z)
            Q <= 2'b0;
        else if (Y)
            if (X)
                Q <= R;
            else
                Q <= {W, Q[1]};
endmodule
```

Answer:

Q9c 0

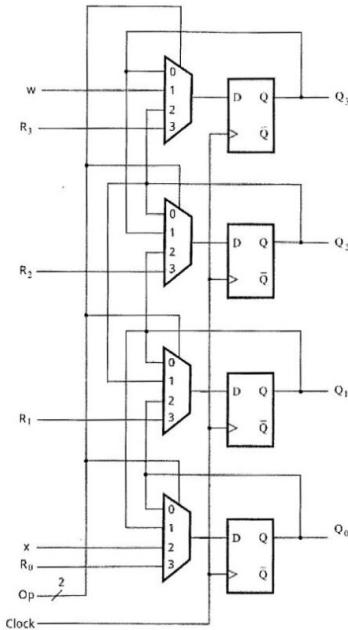


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- (d) Consider the logic circuit shown below. In this circuit any two wires that cross each other are connected together only if there is a **dot** at their intersection.



Answer the questions about this circuit on the following page.

Page 18



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Q9di

0 [2 marks]

- i. Discuss briefly what this circuit "does", by describing what happens in the circuit during each clock cycle for the different possible valuations of the 2-bit *Op* input.

Answer:

Shift register when enable = 1, it loads and
when op = 0, it shifts

[3 marks]

- ii. In the space below write complete Verilog code that can be used to specify this circuit. The module definition is provided for you as a starting point.

Answer:

```
module Univ (w, x, R, Op, Clock, Q);
    input w, x, Clock;
    input [1:0] Op;
    input [3:0] R;
    output reg [3:0] Q;
```

always @ (posedge
begin
if (w)

all incorrect 0



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Extra answer space for any question on the test, if needed:

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Extra answer space for any question on the test, if needed:

Page 21

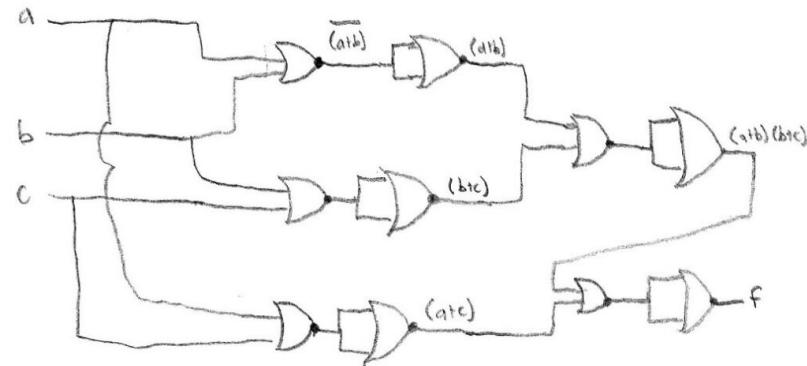


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Extra answer space for any question on the test, if needed:

$$f = (a+c)(\bar{a}+b)(b+c)$$



$$\begin{aligned} & \overline{(\bar{a}+b) + (\bar{b}+c)} \\ &= \overline{(\bar{a}b)} \cdot \overline{(\bar{b}c)} \end{aligned}$$

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Extra answer space for any question on the test, if needed:

$$\begin{array}{r} 98 \\ \times 2 \\ \hline 196 \end{array}$$

AB R I

$$\begin{array}{r} 102 \\ \times 2 \\ \hline 204 \end{array}$$

1000101

$$\begin{array}{r} 49 \\ \times 2 \\ \hline 98 \end{array}$$

49 R O

$$\begin{array}{r} 128 \\ 64 \\ \hline 192 \\ -192 \\ \hline 0 \end{array}$$

$2^8 + 1$

$$\begin{array}{r} 24 \\ \times 2 \\ \hline 49 \end{array}$$

24 R I

$$\begin{array}{r} 28 + 1 \\ = 2^1 + 2^0 \end{array}$$

$$\begin{array}{r} 12 \\ \times 2 \\ \hline 24 \end{array}$$

12 R O

$$1011\ 0010\ 1100$$

$$\begin{array}{r} 24 \\ \times 2 \\ \hline 48 \end{array}$$

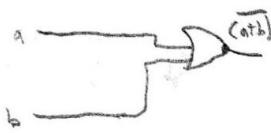
$$\begin{array}{r} 6 \\ \times 2 \\ \hline 12 \end{array}$$

6 R O

$$f = (a+c)(a+b)(b+c)$$

$$\begin{array}{r} 3 \\ \times 2 \\ \hline 6 \end{array}$$

3 R O



$$\begin{array}{r} 1 \\ \times 2 \\ \hline 2 \end{array}$$

1 R I

$$\begin{array}{r} 0 \\ \times 2 \\ \hline 0 \end{array}$$

0 R I

$$C \text{ ---}$$

$$\begin{array}{r} 0101 \\ 1001 \\ \hline 1010 \end{array}$$

5 9 7

2 ⁴	2 ³	2 ²	2 ¹	2 ⁰
0000	0			
0001	1			
0010	2			
0011	3			
0100	4			
0101	5			
0110	6			
0111	7			
1000	8			
1001	9			
1010	10			
1011	11			
1100	12			
1101	13			
1110	14			
1111	15			



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Aid Sheet

Boolean Algebra Axioms

- | | | | |
|-----|---------------------------------|-----|---------------------------------|
| 1a. | $0 \cdot 0 = 0$ | 1b. | $1 + 1 = 1$ |
| 2a. | $1 \cdot 1 = 1$ | 2b. | $0 + 0 = 0$ |
| 3a. | $0 \cdot 1 = 1 \cdot 0 = 0$ | 3b. | $1 + 0 = 0 + 1 = 1$ |
| 4a. | If $x = 0$, then $\bar{x} = 1$ | 4b. | If $x = 1$, then $\bar{x} = 0$ |

Boolean Algebra Rules

- | | | | |
|-----|-----------------------|-----|-------------------|
| 5a. | $x \cdot 0 = 0$ | 5b. | $x + 1 = 1$ |
| 6a. | $x \cdot 1 = x$ | 6b. | $x + 0 = x$ |
| 7a. | $x \cdot x = x$ | 7b. | $x + x = x$ |
| 8a. | $x \cdot \bar{x} = 0$ | 8b. | $x + \bar{x} = 1$ |
| 9. | $\bar{\bar{x}} = x$ | | |

Boolean Algebra Identities

- | | | | |
|------|---|------|---|
| 10a. | $x \cdot y = y \cdot x$ | 10b. | $x + y = y + x$ |
| 11a. | $x \cdot (y \cdot z) = (x \cdot y) \cdot z$ | 11b. | $x + (y + z) = (x + y) + z$ |
| 12a. | $x \cdot (y + z) = x \cdot y + x \cdot z$ | 12b. | $x + y \cdot z = (x + y) \cdot (x + z)$ |
| 13a. | $x + x \cdot y = x$ | 13b. | $x \cdot (x + y) = x$ |
| 14a. | $x \cdot y + x \cdot \bar{y} = x$ | 14b. | $(x + y) \cdot (x + \bar{y}) = x$ |
| 15a. | $\bar{x} \cdot \bar{y} = \bar{x} + \bar{y}$ | 15b. | $\bar{x} + \bar{y} = \bar{x} \cdot \bar{y}$ |
| 16a. | $x + \bar{x} \cdot y = x + y$ | 16b. | $x \cdot (\bar{x} + y) = x \cdot y$ |
| 17a. | $x \cdot y + y \cdot z + \bar{x} \cdot z = x \cdot y + \bar{x} \cdot z$ | 17b. | $(x + y) \cdot (y + z) \cdot (\bar{x} + z) = (x + y) \cdot (\bar{x} + z)$ |

